DLP® Digital Controller for the DLP4500 DMD

Check for Samples: DLPC350

FEATURES

- Supports Reliable Operation of the DLP4500 DMD
- Two Types of Input Interfaces
  - YUV, YCrCb, or RGB data format
    - 8, 9, or 10 bits per color
    - Pixel Clock support up to 150 MHz
  - Single channel, LVDS Flat-Panel Display (FPD-Link) compatible Input Interface
    - Supports sources up to a 90 MHz effective pixel clock rate
    - Four demodulated pixel mapped modes supported for 8, 9, 10 YUV, YCrCb, or RGB formatted input
- Two Modes of Operation
  - Structured Light Mode
    - Pixel Accurate Mode with no video processing
    - One-to-One Mapping of Input Data to Micromirrors
    - 1-Bit Binary Pattern Rates up to 4225 Hz
    - 8-Bit Gray Pattern Rates up to 120 Hz
  - Video Projection Mode
    - Programmable color coordinate adjustment
    - Programmable color space conversion
    - Programmable Degamma
    - Spatial-Temporal Multiplexing (Dithering)
- Dynamic and Anamorphic Scaling
- Splash Screen Display support
- Supports 10 Hz to 120 Hz frame rates
- High Speed, Double-Data-Rate DMD Interface
- Microprocessor Peripherals
  - Programmable PWM and Capture timers
  - Two I^2C Ports
  - One USB 1.1 Slave Port
  - 32 kB of internal RAM
  - Dedicated LED PWM generators
- Integrated Clock Generation Circuitry
  - Operates on a single 32 MHz Crystal
  - Integrated spread spectrum clocking
  - Parallel Flash for microprocessor
- System Control:
  - Integrated DMD Power and Reset Driver Control
  - DMD Horizontal and Vertical Image Flip
- JTAG Boundary Scan Test support
- 419 Pin Plastic Ball Grid Array package

APPLICATIONS

- Machine Vision
- Industrial Inspection
- 3D Scanning
- 3D Optical Metrology
- Automated Fingerprint Identification
- Face Recognition
- Augmented Reality
- Interactive Display
- Information Overlay
- Spectroscopy
- Chemical Analyzers
- Medical Instruments
- Photo-Stimulation
- Virtual Gauges

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The DLPC350 digital controller, part of the DLP 0.45 WXGA chip set, supports reliable operation of the DLP4500 DMD, or Digital Micromirror Device. The DLPC350 controller provides a convenient, multi-functional interface between user electronics and the DMD, enabling high-speed pattern rates, providing LED control and data formatting for multiple input resolutions. The DLPC350 also outputs a trigger signal for synchronizing displayed patterns with a camera, sensor, or other peripherals.

The DLPC350 controller enables integration of the DLP 0.45 WXGA chip set into small-form-factor and low-cost light steering applications. Example applications for the 0.45 WXGA chip set include 3D scanning or metrology systems with structured light, interactive displays, chemical analyzers, medical instruments, and other end equipment requiring spatial light modulation (light steering and patterning).

The DLPC350 is one of the two devices in the 0.45 WXGA chip set (see Figure 1). The other device is the DLP4500 DMD. Search the TI Website for 'DLPR350' for additional information, and see the *0.45 WXGA Chip-Set* data sheet DLPU009 for further details.

BLOCK DIAGRAM

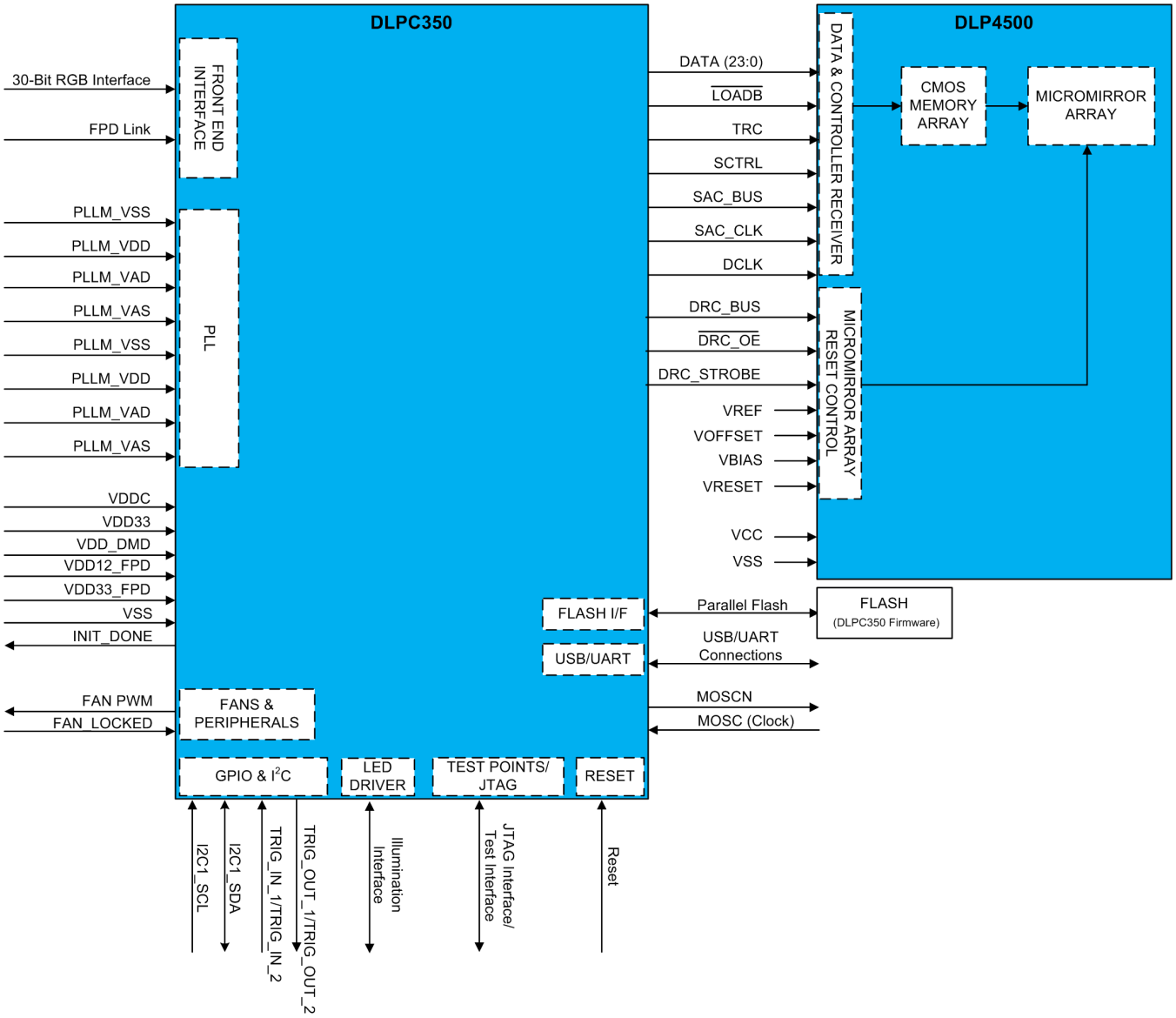


Figure 1. Chip Set Block Diagram

In DLP-based solutions, image data is 100% digital from the DLPC350 input port to the image on the DMD. The image stays in digital form and is not converted into an analog signal. The DLPC350 processes the digital input image and converts the data into a format needed by the DLP4500. The DLP4500 steers light by using binary pulse-width-modulation (PWM) for each micromirror. Refer to DLP4500 Data Sheet (TI literature number DLPS028) for further details.

Figure 2 is the DLPC350 functional block diagram. As part of the pixel processing functions, the DLPC350 offers format conversion functions: chroma interpolation and color-space conversion. The DLPC350 also offers several image-enhancement functions. The DLPC350 also supports the necessary functions to format the input data to the DMD. The pixel processing functions allow the DLPC350 and DLP4500 to support a wide variety of resolutions including NTSC, PAL, XGA, and WXGA. The pixel processing functions can be optionally bypassed with the native 912 × 1140 pixel resolution to support direct one-to-one pixel mapping.

When accurate pattern display is needed, the native 912 x 1140 input resolution pattern has a one-to-one association with the corresponding micromirror on the DLP4500. The DLPC350 enables high-speed display of these patterns. This functionality is well-suited for techniques such as structured light, additive manufacturing, or digital exposure.

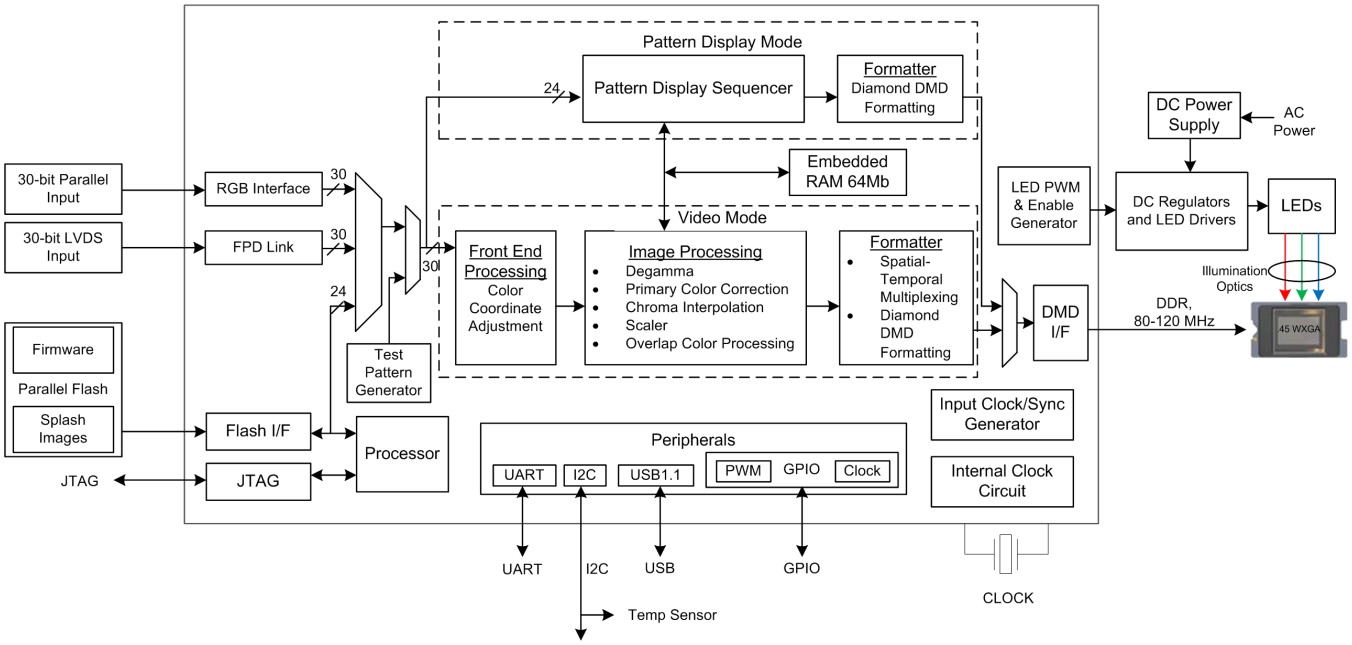


Figure 2. DLPC350 Functional Block Diagram

Commands can be input to the DLPC350 over an I^2C interface.

The DLPC350 takes as input 24-, 27- or 30-bit RGB data at up to 120-Hz frame rate. This frame rate is composed of three colors (red, green, and blue) with each color equally divided in the 120-Hz frame rate. Thus, each color has a 2.78 ms time slot allocated. Because each color has an 8-, 9-, or 10-bit depth, each color time slot is further divided into bit-planes. A bit-plane is the 2-dimensional arrangement of one-bit extracted from all the pixels in the full color 2D image to implement dynamic depth. See Figure 3.

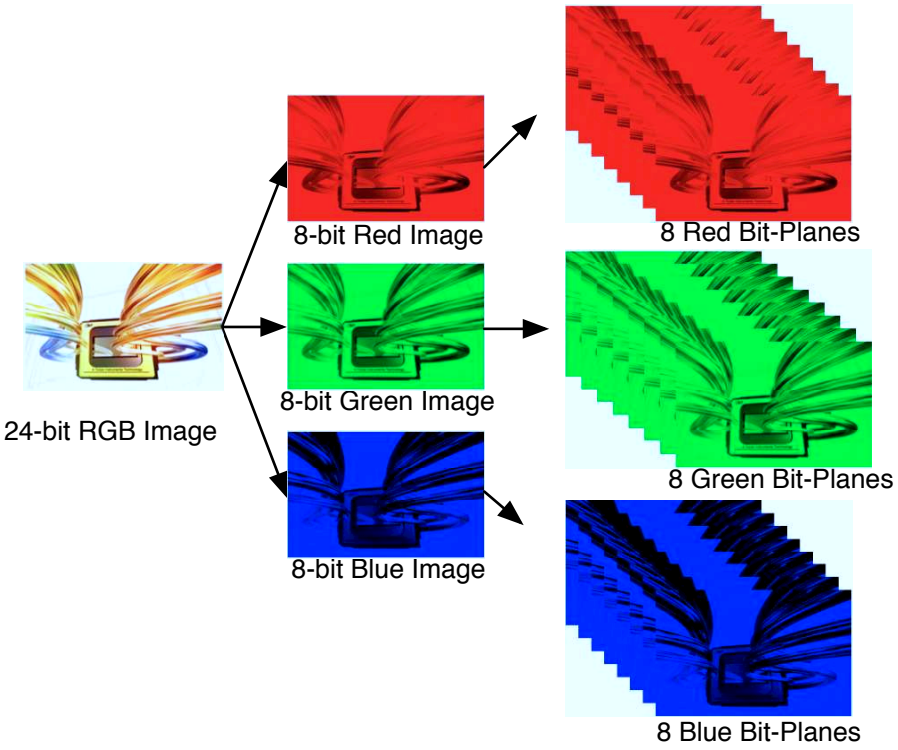


Figure 3. Bit Slices

The length of each bit-plane in the time slot is weighted by the corresponding power of two of its binary representation. This provides a binary pulse-width modulation of the image. For example, a 24-bit RGB input has three colors with 8-bit depth each. Each color time slot is divided into eight bit-planes, with the sum of the weight of all bit planes in the time slot equal to 256. See Figure 4 for an illustration of this partition of the bits in a frame.

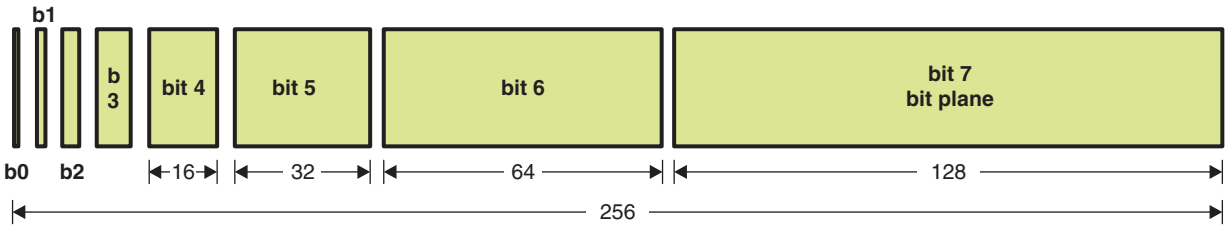


Figure 4. Bit Partition in a Frame for an 8-Bit Color

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane. With binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame image inputted to the DLPC350, the DLPC350 creates 24 bit planes, stores them in a double-buffered eDRAM embedded in the chip, and sends them to the DLP4500 DMD, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC350 controls the time this bit-plane is illuminated, controlling the intensity of the bit-plane. To improve image quality in video frames, these bit-planes, time slots, and color frames are shuffled and interleaved with spatial-temporal algorithms by the DLPC350.

Structured Light Applications

For other applications where this video enhancement is not desired, the video processing algorithms can be bypassed and replaced with a specific set of bit-planes. The bit-depth of the pattern is then allocated into the corresponding time slots. Furthermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed. For structured light applications, this mechanism provides the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object.

The DLPC350 stores two 24-bit frames in its internal memory buffer. This 48 bit-plane display buffer allows the DLPC350 to send one 24-bit buffer to the DMD array while the second buffer is filled from Flash or streamed in through the 24-bit RGB interface. In streaming mode, the DMD array displays the previous 24-bit frame while the current frame fills the second 24-bit frame of the display buffer. Once a 24-bit frame is displayed, the buffer rotates accessing the next 24-bit frame to the DMD. Thus, the displayed image is a 24-bit frame behind the data streamed through the 24-bit RGB parallel interface.

In structured light mode, the 48 bit-planes can be pre-loaded from Flash memory and then sequenced with a combination of patterns with different bit depths. To synchronize a camera to the displayed patterns, the DLPC350 supports three trigger modes: mode 0, mode 1, and mode 2.

In mode 0, the vertical sync is used as trigger input. In mode 1, a TRIG_IN_1 pulse indicates to the DLPC350 to advance to the next pattern, while TRIG_IN_2 starts and stops the pattern sequence. In both modes 0 and 1, TRIG_OUT_1 frames the exposure time of the pattern, while TRIG_OUT_2 indicates the start of the pattern sequence or internal buffer boundary of 24-bit planes. In mode 2, the TRIG_IN_1 signal toggles between two consecutive patterns, while a TRIG_IN_2 pulse advances to the next pair of patterns.

In trigger mode 0, shown in Figure 5, the VSYNC starts the pattern sequence display. The pattern sequence consists of a series of three consecutive patterns. The first pattern sequence consists of P1, P2, and P3. Since P3 is an RGB pattern, it is shown with its time sequential representation of P3.1, P3.2, and P3.3. The second pattern sequence consists of three patterns: P4, P5, and P6. The third sequence consists of P7, P8, and P9. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each of the three pattern sequences.

An example of trigger mode 1 is shown in Figure 6. Pattern sequences of four are displayed. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each four-pattern sequence. TRIG_IN_1 pulses advance the pattern.

Another example for mode 1 is shown in Figure 7, where pattern sequences of three are displayed. TRIG_OUT_1 frames each pattern displayed, while TRIG_OUT_2 indicates the start of each three-pattern sequence. TRIG_IN_2 serves as a start/stop signal. When high, the pattern sequence starts or continues. Note that in the middle of displaying the P4 pattern, TRIG_IN_2 is low, so the sequence stops displaying P4. When TRIG_IN_2 is raised, the pattern sequence continues where it stopped by re-displaying P4.

For trigger mode 2, shown in Figure 8, TRIG-IN_1 alternates between two patterns, while TRIG_IN_2 advances to the next pair of patterns. Table 1 shows the allowed pattern combinations in relation to the bit depth of the pattern.

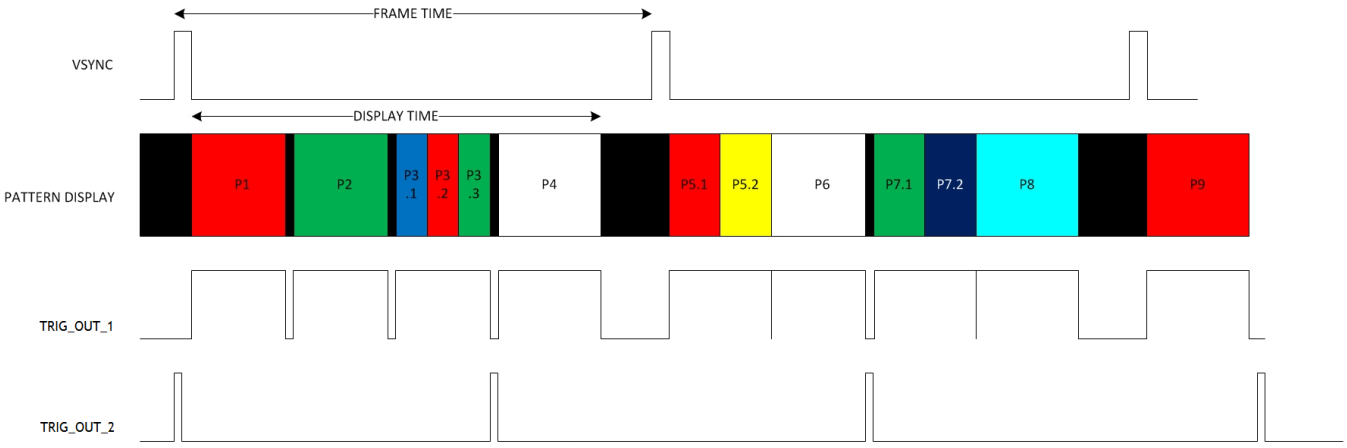


Figure 5. Mode 0 Trigger Timing Diagram

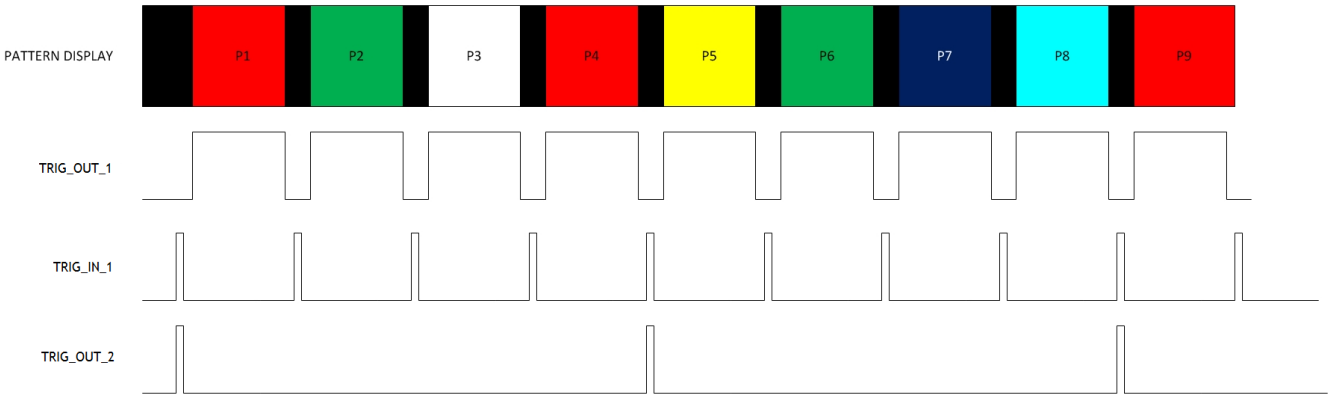


Figure 6. Mode 1 Triggers Timing Diagram for 6-Bit Patterns

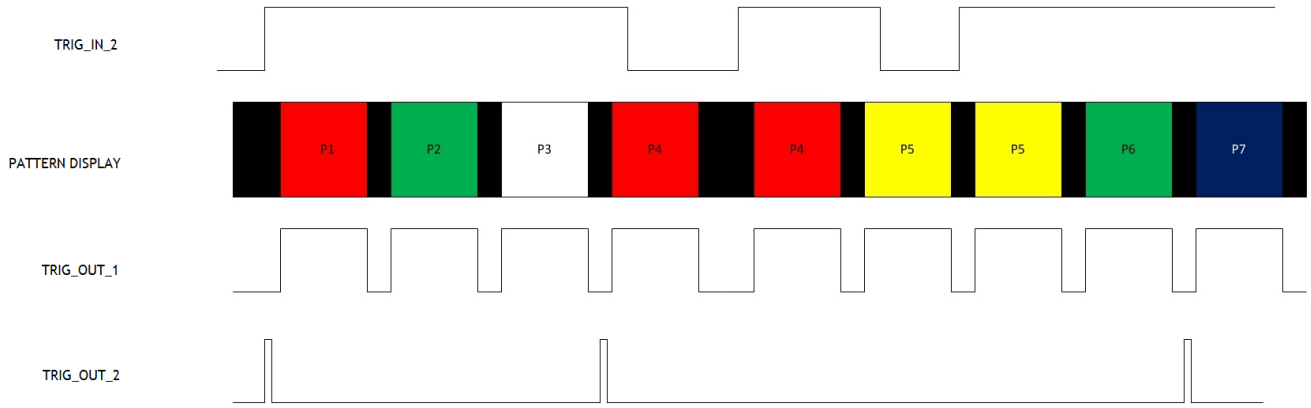


Figure 7. Mode 1 Trigger Timing Diagram

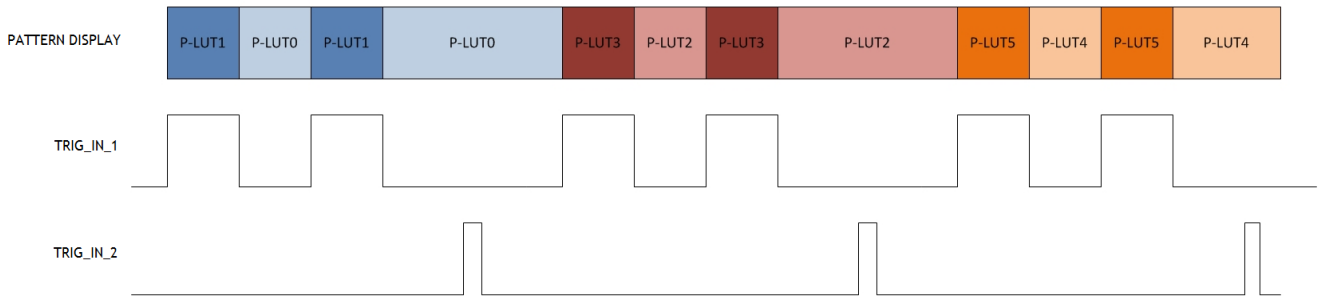


Figure 8. Mode 2 Trigger Timing Diagram

Table 1. Allowed Pattern Combinations

BIT DEPTH	EXTERNAL RGB INPUT PATTERN RATE (Hz)	PRE-LOADED PATTERN RATE (Hz)	MAXIMUM NUMBER OF PATTERNS (PRE-LOADED)
1	2880	4225	48
2	1428	1428	24
3	636	636	16
4	588	588	12
5	480	500	8
6	400	400	8
7	222	222	6
8	120	120	6

Typical System Application

A typical embedded system application using the DLPC350 is shown in Figure 9. In this configuration, the DLPC350 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. This system supports both still and motion video sources. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for *still images* by maintaining periodic syncs and only sending a new frame of data when needed. The *still image* must be fully contained within a single video frame and meet the frame timing constraints. The DLPC350 refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

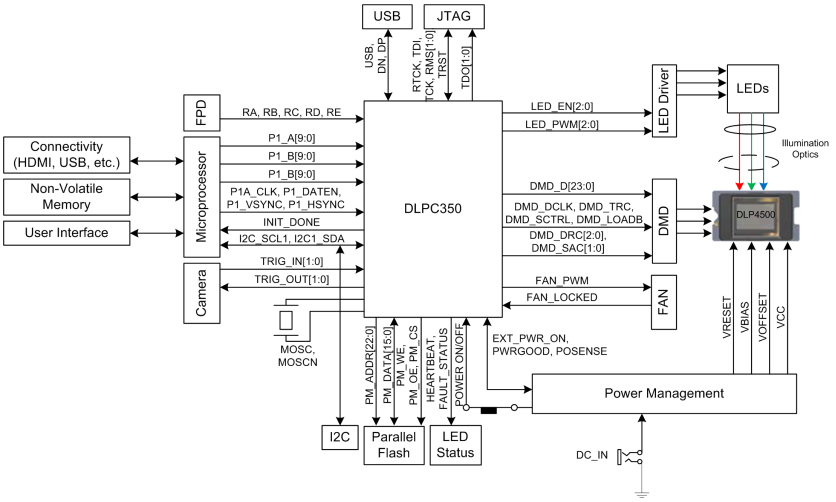


Figure 9. Typical Embedded System Block Diagram

Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP4500 0.45 WXGA DMD Data Sheet	DLPS028
DLP® 0.45 WXGA Chip Set Data Manual	DLPU009
DLPC350 Programmer's Guide	DLPU010

Device Nomenclature

Figure 10 provides a legend for reading the complete device name for any DLP device.

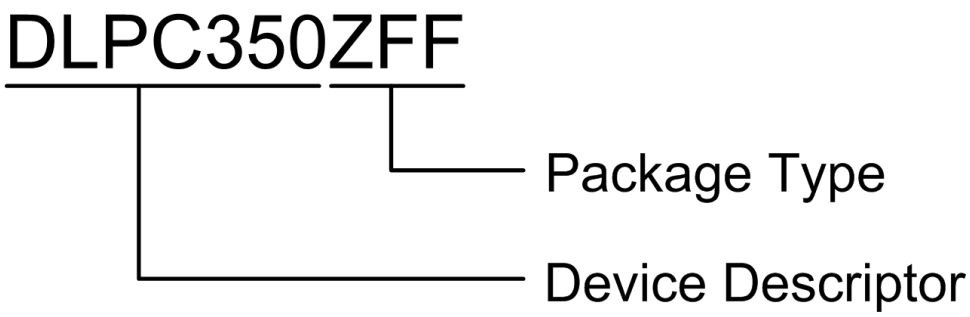


Figure 10. Device Nomenclature

Device Marking

The device marking consists of the fields shown in Figure 11.

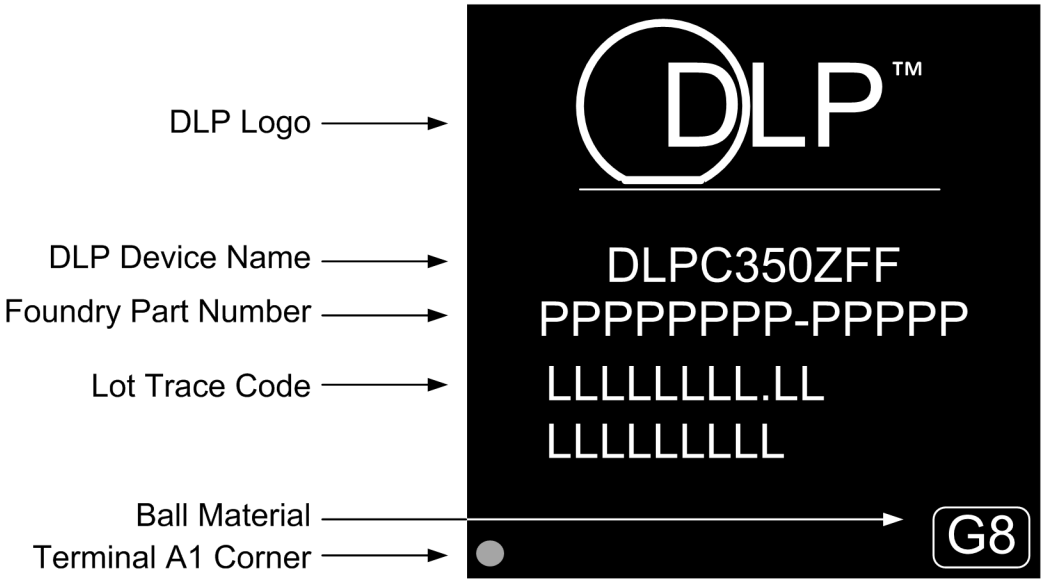


Figure 11. Device Marking

SIGNAL FUNCTIONAL DESCRIPTIONS

This section describes the input/output characteristics of signals that interface to the DLPC350 by functional groups. includes I/O power and type characteristic references which are further described in subsequent sections.

Table 2. Functional Pin Descriptions (1)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
CONTROL						
PWRGOOD	H19	VDDC	I_4 H		Async	Power Good is an active high signal with hysteresis that is generated by an external power supply or voltage monitor. A high value indicates all power is within operating voltage specs and the system is safe to exit its reset state. A transition from high to low should indicate that the controller or DMD supply voltage will drop below their rated minimum level within the next 0.5ms (POSENSE must remain active high during this interval). This is an early warning of an imminent power loss condition. This warning is required to enhance long term DMD reliability. A DMD park sequence, followed by a full controller reset, is performed by the DLPC350 when PWRGOOD goes low for a minimum of 4us protecting the DMD. This minimum de-assertion time is used to protect the input from glitches. Following this the DLPC350 will be held in its reset state as long as PWRGOOD is low. PWRGOOD must be driven high for normal operation. The DLPC350 will acknowledge PWRGOOD as active once it's been driven high for a minimum of 625ns. Utilizes hysteresis.
POSENSE	G21		I_4 H		Async	Power-On Sense is an active high input signal with hysteresis that is generated by an external voltage monitor circuit. POSENSE must be driven inactive (low) when any of the controller supply voltages are below minimum operating voltage specs. POSENSE must be active (high) when all controller supply voltages remain above minimum specs.
POWER_ON_OFF	N21	VDD33	B_2		Async	Power On/Off is an active high signal that indicates the power of the system. Power On/Off is high when the system is in power-up state, and low when the system is in standby. Power On/Off can also be used to power on/off an external power supply.
EXT_PWR_ON	D21	VDD33	B_2		Async	Signal to host processor or power supply to indicate that the DLPC350 is powered on. Asserted just before INIT_DONE.
HOLD_IN_BOOT	D18	VDD33	B_2	External pull-up required	N/A	
INIT_DONE	F19	VDD33	B_2		Async	Prior to transferring part of code from parallel flash content to internal memory, the internal memory is initialized and a memory test is performed. The result of this test (pass/fail) is recorded in the system status. If memory test fails, the initialization process is halted. INIT_DONE is asserted twice to indicate an error situation. See Figure 25 and note that GPIO26 is the INIT_DONE signal.
I2C_ADDR_SEL	F21	VDD33	B_2		Async	This signal is sampled during power-up. If the signal is low, the I^2C addresses are 0x34 and 0x35. If the signal is low, the I^2C are 0x3A and 0x3B. Once the system has been initialized, this signal is available as a GPIO.

(1) I/O Type: I indicates input, O indicates output, B indicates bi-directional, and H indicates hysteresis. See Table 6 for subscript explanation.

Table 2. Functional Pin Descriptions (continued)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
I2C1_SCL	J3	VDD33	B_2	Requires an external pull-up to 3.3V. The minimum acceptable pull-up value is 1 KΩ.	N/A	I^2C clock. Bi-directional, open-drain signal. I^2C slave clock input from the external processor. This bus supports 400 KHz.
I2C1_SDA	J4	VDD33	B_2	Requires an external pull-up to 3.3V. The minimum acceptable pull-up value is 1 KΩ.	I2C1_SCL	I^2C data. Bi-directional, open drain signal. I^2C slave to accept command or transfer data to and from the external processor. This bus supports 400 KHz.
I2C0_SCL	M2	VDD33	B_8	Requires an external pull-up to 3.3V. The minimum acceptable pull-up value is 1 KΩ. This input is NOT 5V tolerant.	N/A	I^2C Bus 0, Clock; I^2C master for on-board peripherals such as Temperature Sensor. This bus supports 400KHz, Fast Mode operation.
I2C0_SDA	M3	VDD33	B_8	Requires an external pull-up to 3.3V. The minimum acceptable pull-up value is 1 KΩ. This input is NOT 5V tolerant.	I2C0_SCL	I^2C Bus 0, Data; I^2C master for on-board peripherals such as Temperature Sensor. This bus supports 400KHz, Fast Mode operation.
SYSTEM CLOCK						
MOSC	A14	VDD33	I_{10}		N/A	System clock oscillator input (3.3V LVCMOS). Note that the MOSC must be stable a maximum of 25 ms after POSENSE transitions from high to low.
MOSCN	A15	VDD33	O_{10}		N/A	MOSC Crystal return
PORT 1: PARALLEL VIDEO/GRAPHICS INPUT (2)(3)(4)						
P1A_CLK	W15	VDD33	I_4	Includes an internal pull-down	N/A	Port 1 Input Data Pixel Write Clock 'A'
P1B_CLK	AB17	VDD33	I_4	Includes an internal pull-down	N/A	Port 1 Input Data Pixel Write Clock 'B'
P1C_CLK	Y16	VDD33	I_4	Includes an internal pull-down	N/A	Port 1 Input Data Pixel Write Clock 'C'
P1_VSYNC	Y15	VDD33	B_1 H	Includes an internal pull-down	P1A_CLK	Port 1 Vertical Sync. Utilizes hysteresis.
P1_HSYNC	AB16	VDD33	B_1 H	Includes an internal pull-down	P1A_CLK	Port 1 Horizontal Sync. Utilizes hysteresis.
P1_DATEN	AA16	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 Data Enable
P1_FIELD	W14	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 Field Sync. Required for interlaced sources only (and not progressive).
P1_A_9	AB20	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 128).
P1_A_8	AA19	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 64).
P1_A_7	Y18	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 32).
P1_A_6	W17	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 16).
P1_A_5	AB19	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 8).
P1_A_4	AA18	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 4).
P1_A_3	Y17	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 2).
P1_A_2	AB18	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 1).

(2) Port 1 can be used to support multiple source options for a given product (that is. HDMI, BT656). To do so, the data bus from both source components must be connected to the same port 1 pins and control given to the DLPC350 to tri-state the "inactive" source. Tying them together like this will cause some signal degradation due to reflections on the tri-stated path.
(3) The A, B, and C input data channels of Port 1 can be internally swapped for optimum board layout.
(4) Sources feeding less than the full 10-bits per color component channel should be MSB justified when connected to the DLPC350 and LSBs tied off to zero. For example, an 8-bit per color input should be connected to bits 9:2 of the corresponding A, B, or C input channel. BT656 are 8 or 10 bits in width. If a BT656 type input is utilized, the data bits must be MSB justified as with the other types of input sources on either of the A, B, or C data input channels.

Table 2. Functional Pin Descriptions (continued)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
P1_A_1	W16	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 0.5).
P1_A_0	AA17	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 A Channel Input Pixel Data (bit weight 0.25).
P1_B_9	U21	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 128).
P1_B_8	U20	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 64).
P1_B_7	V22	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 32).
P1_B_6	U19	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 16).
P1_B_5	V21	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 8).
P1_B_4	W22	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 4).
P1_B_3	W21	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 2).
P1_B_2	AA20	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 1).
P1_B_1	Y19	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 0.5).
P1_B_0	W18	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 B Channel Input Pixel Data (bit weight 0.25).
P1_C_9	P21	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 128).
P1_C_8	P22	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 64).
P1_C_7	R19	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 32).
P1_C_6	R20	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 16).
P1_C_5	R21	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 8).
P1_C_4	R22	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 4).
P1_C_3	T21	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 2).
P1_C_2	T20	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 1).
P1_C_1	T19	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 0.5).
P1_C_0	U22	VDD33	I_4	Includes an internal pull-down	P1A_CLK	Port 1 C Channel Input Pixel Data (bit weight 0.25).
PORT 2: FPD-LINK COMPATIBLE VIDEO/GRAPHICS INPUT(5)						
RCK_IN_P	Y9	VDD33_FPD	I_5	Includes weak internal pull-down.	N/A	Positive differential input signal for Clock, FPD-Link receiver.
RCK_IN_N	W9	VDD33_FPD	I_5	Includes weak internal pull-down.	N/A	Negative differential input signal for Clock, FPD-Link receiver.
RA_IN_P	AB10	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Positive differential input signal for data channel A, FPD-Link receiver.
RA_IN_N	AA10	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Negative differential input signal for data channel A, FPD-Link receiver.
RB_IN_P	Y11	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Positive differential input signal for data channel B, FPD-Link receiver.

(5) Port 2 is a single-channel FPD-Link compatible input interface. FPD-Link is a de-facto industry standard Flat-Panel Display Interface which utilizes the high bandwidth capabilities of LVDS signaling to serialize Video/Graphics data down to a couple wires to provide a low wire count and low EMI interface. Port 2 supports sources rates up to a maximum effective clock of 90 MHz. The Port 2 input pixel data must adhere to one of four supported data mapping formats (See Table 10). Given that Port 2 inputs contain weak pull-down resistors, they can be left floating when not used.

Table 2. Functional Pin Descriptions (continued)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
RB_IN_N	W11	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Negative differential input signal for data channel B, FPD-Link receiver.
RC_IN_P	AB12	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Positive differential input signal for data channel C, FPD-Link receiver.
RC_IN_N	AA12	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Negative differential input signal for data channel C, FPD-Link receiver.
RD_IN_P	Y13	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Positive differential input signal for data channel D, FPD-Link receiver.
RD_IN_N	W13	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Negative differential input signal for data channel D, FPD-Link receiver.
RE_IN_P	AB14	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Positive differential input signal for data channel E, FPD-Link receiver.
RE_IN_N	AA14	VDD33_FPD	I_5	Includes weak internal pull-down.	RCK_IN	Negative differential input signal for data channel E, FPD-Link receiver.
DMD INTERFACE						
DMD_D0	A8	VDD_DMD	O_7		DMD_DCLK	DMD data pins. DMD data pins are double data rate (DDR) signals that are clocked on both edges of DMD_DCLK. All 24 DMD data signals are use to interface to the DLP4500.
DMD_D1	B8					
DMD_D2	C8					
DMD_D3	D8					
DMD_D4	B11					
DMD_D5	C11					
DMD_D6	D11					
DMD_D7	E11					
DMD_D8	C7					
DMD_D9	B10					
DMD_D10	E7					
DMD_D11	D10					
DMD_D12	A6					
DMD_D13	A12					
DMD_D14	B12					
DMD_D15	C12					
DMD_D16	D12					
DMD_D17	B7					
DMD_D18	A10					
DMD_D19	D7					
DMD_D20	B6					
DMD_D21	E9					
DMD_D22	C10					
DMD_D23	C6					
DMD_DCLK	A9	VDD_DMD	O_7		N/A	DMD data clock (DDR)
$\overline{\text{DMD\_LOADB}}$	B9	VDD_DMD	O_7		DMD_DCLK	DMD data load signal (active-low).
DMD_SCTRL	C9	VDD_DMD	O_7		DMD_DCLK	DMD data serial control signal
DMD_TRC	D9	VDD_DMD	O_7		DMD_DCLK	DMD data toggle rate control
DMD_DRC_BUS	D5	VDD_DMD	O_7		DMD_SAC_CLK	DMD reset control bus data
DMD_DRC_STRB	C5	VDD_DMD	O_7		DMD_SAC_CLK	DMD reset control bus strobe
$\overline{\text{DMD\_DRC\_OE}}$	B5	VDD_DMD	O_7	Requires a 30kΩ to 51kΩ external pull-up resistor to VDD_DMD.	Async	DMD reset control enable (active-low).
DMD_SAC_BUS	D6	VDD_DMD	O7		DMD_SAC_CLK	DMD stepped-address control bus data
DMD_SAC_CLK	A5	VDD_DMD	O_7		N/A	DMD stepped-address control bus clock

Table 2. Functional Pin Descriptions (continued)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
DMD_PWR_EN	G20	VDD_DMD	O_2		Async	DMD Power Enable control. This signal indicates to an external regulator that the DMD is powered.
$\overline{\text{EXRES}}$	A3		O		Async	DMD drive strength adjustment precision reference. A ± 1% external precision resistor should be connected to this pin.
FLASH INTERFACE						
$\overline{\text{PM\_CS\_1}}$	U2	VDD33	O_2		Async	Boot Flash (active low). Required for Boot Memory
$\overline{\text{PM\_CS\_2}}$	U1	VDD33	O_2		Async	Optional for Additional Flash (up to 128 Mb)
PM_ADDR_22	V3	VDD33	B_2		Async	Flash memory address bit
PM_ADDR_21	W1					
PM_ADDR_20	W2		O_2			
PM_ADDR_19	Y1					
PM_ADDR_18	AB2					
PM_ADDR_17	AA3					
PM_ADDR_16	Y4					
PM_ADDR_15	W5					
PM_ADDR_14	AB3					
PM_ADDR_13	AA4					
PM_ADDR_12	Y5					
PM_ADDR_11	W6					
PM_ADDR_10	AB4					
PM_ADDR_9	AA5					
PM_ADDR_8	Y6					
PM_ADDR_7	W7					
PM_ADDR_6	AB5					
PM_ADDR_5	AA6					
PM_ADDR_4	Y7					
PM_ADDR_3	AB6					
PM_ADDR_2	W8					
PM_ADDR_1	AA7					
PM_ADDR_0	AB7					
$\overline{\text{PM\_WE}}$	V2	VDD33	O_2		Async	Write Enable (active low)
$\overline{\text{PM\_OE}}$	U4	VDD33	O_2		Async	Output Enable (active low)
$\overline{\text{PM\_BLS\_1}}$	AA8	VDD33	O_2		Async	Upper Byte(15:8) Enable
$\overline{\text{PM\_BLS\_0}}$	AB8	VDD33	O_2		Async	Lower Byte(7:0) Enable
PM_DATA_15	M1	VDD33	B_2		Async	Data bits, upper byte
PM_DATA_14	N1					
PM_DATA_13	N2					
PM_DATA_12	N3					
PM_DATA_11	N4					
PM_DATA_10	P1					
PM_DATA_9	P2					
PM_DATA_8	P3					

Table 2. Functional Pin Descriptions (continued)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
PM_DATA_7	P4	VDD33	B_2		Async	Data bits, lower byte
PM_DATA_6	R2					
PM_DATA_5	R3					
PM_DATA_4	R4					
PM_DATA_3	T1					
PM_DATA_2	T2					
PM_DATA_1	T3					
PM_DATA_0	T4					
LED DRIVER INTERFACE						
HEARTBEAT	C16	VDD33	B_2		Async	LED blinks continuously (heartbeat) to indicate the system is running fine. Period of 1 second; 50% high and low.
FAULT_STATUS	B16	VDD33	B_2		Async	LED off indicates any system fault
LEDR_PWM	K2	VDD33	O_2		Async	LED Red PWM Output Enable Control
LEDG_PWM	K3					LED Green PWM Output Enable Control
LEDB_PWM	K4					LED Blue PWM Output Enable Control
LEDR_EN	L3	VDD33	O_2		Async	LED Red PWM Output
LEDG_EN	L4					LED Green PWM Output
LEDB_EN	K1					LED Blue PWM Output
TRIGGER CONTROL						
TRIG_IN_1	G19	VDD33	B_2		Async	In trigger mode 1, this signal will be used to advance the pattern display. In trigger mode 2, the rising edge will display the pattern and the falling edge will display the next indexed pattern.
TRIG_IN_2	F22	VDD33	B_2		Async	In trigger mode 1, this signal will be used to start (rising edge)/stop (falling edge) the pattern display. It will work along with the software start/stop command. In trigger mode 2, this signal will be used to advance the pattern by two indexes.
TRIG_OUT_1	C17	VDD33	B_2		Async	Active high trigger output signal during pattern exposure
TRIG_OUT_2	K21	VDD33	B_2		Async	Active high trigger output to indicate first pattern display
PERIPHERAL INTERFACE						
USB_DAT_N	E3	VDD33	B_9		Async	USB D- I/O for USB command interface. A 5.0 Watt external series resistance (of 22Ω) is strongly recommended to limit the potential impact of a continuous short circuit between USB_DAT_N and either V_{BUS}, GND, the other data line, or the cable. For additional protection, an optional 200 mA Shottky diode from USB_DAT_N to VDD33 can also be added.
USB_DAT_P	E2					USB D+ I/O for USB command interface. A 5.0 Watt external series resistance (of 22Ω) is strongly recommended to limit the potential impact of a continuous short circuit between USB_DAT_P and either V_{BUS}, GND, the other data line, or the cable. For additional protection, an optional 200 mA Shottky diode from USB_DAT_P to VDD33 can also be added.
$\overline{\text{USB\_EN}}$	C18	VDD33	B_2		Async	USB Enable
UART_TXD	L19	VDD33	O_2		Async	Transmit Data Output. Reserved for debug messages
UART_RXD	L21	VDD33	I_4		Async	Receive Data Input. Reserved for debug messages
$\overline{\text{UART\_RTS}}$	M19	VDD33	O_2		Async	Ready to Send hardware flow control output. Reserved for debug messages

Table 2. Functional Pin Descriptions (continued)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
$\overline{\text{UART\_CTS}}$	L20	VDD33	I_4		Async	Clear to Send hardware flow control input. Reserved for debug messages
GPIOS (6)						**ALTERNATIVE MODE**
GPIO_36	G1	VDD33	B_2		Async	None
GPIO_35	H4	VDD33	B_2		Async	None
GPIO_34	H3	VDD33	B_2		Async	None
GPIO_33	H2	VDD33	B_2		Async	None
GPIO_29	F20	VDD33	B_2		Async	None
GPIO_28	E22	VDD33	B_2		Async	None
GPIO_27	E21	VDD33	B_2		Async	None
GPIO_25	D22	VDD33	B_2		Async	None
GPIO_24	E20	VDD33	B_2		Async	None
GPIO_21	N20	VDD33	B_2		Async	None
GPIO_20	N19	VDD33	B_2		Async	None
GPIO_15	B19	VDD33	B_2		Async	None
GPIO_14	B18	VDD33	B_2		Async	None
GPIO_13	L2	VDD33	B_2		Async	None
GPIO_12	M4	VDD33	B_2		Async	OCLKD (Output)
GPIO_11	A19	VDD33	B_2		Async	OCLKC (Output)
GPIO_06	A18	VDD33	B_2		Async	PWM_IN_1 (Input)
GPIO_05	D16	VDD33	B_2		Async	PWM_IN_0 (Input)
GPIO_02	A17	VDD33	B_2		Async	PWM_STD_2 (Output)
GPIO_00	C15	VDD33	B_2		Async	PWM_STD_0 (Output)
OTHER INTERFACES						
FAN_LOCKED	B17	VDD33	B_2		Async	Feedback from Fan to indicate Fan is connected and running
FAN_PWM	D15	VDD33	B_2		Async	Fan PWM speed control
CONTROLLER MANUFACTURER TEST SUPPORT						
HW_TEST_EN	V7	VDD33	I_4 H	Includes internal pull-down.	N/A	Reserved for test. Should be connected directly to ground on the PCB for normal operation
BOARD LEVEL TEST AND DEBUG						
TDI	P18	VDD33	I_4	Includes internal pull-up	TCK	JTAG serial data in. (7)
TCK	R18	VDD33	I_4	Includes internal pull-up	N/A	JTAG serial data clock. (7)
TMS1	V15	VDD33	I_4	Includes internal pull-up	TCK	JTAG test mode select. (7)
TDO1	L18	VDD33	O_1		TCK	JTAG serial data out. (7)
$\overline{\text{TRST}}$	V17	VDD33	I_4 H	Includes internal pull-up	Async	JTAG, RESET (active-low). This pin should be pulled high (or left unconnected) when the JTAG interface is in use for boundary scan. Connect this pin to ground otherwise. Failure to tie this pin low during normal operation will cause startup and initialization problems. (7)
RTCK	G18	VDD33	O_2		N/A	JTAG return clock. (8)
ICTSEN	V6	VDD33	I_4 H	Includes internal pull down. External pull-down recommended for added protection.	Async	IC 3-State Enable (active high). Asserting high will 3-state all outputs except the JTAG interface.

(6) GPIO signals must be configured via software for input, output, bi-directional, or open-drain. Some GPIOs have one or more "alternative use" modes which are also software configurable. The reset default for all optional GPIOs is as an input signal. However, any alternate function connected to these GPIO pins with the exception of General Purpose Clocks and PWM Generation, will be reset. An external pull-up to the 3.3V supply is required for each signal configured as open-drain. External pull-up or pull-down resistors may be required to ensure stable operation before software is able to configure these ports.
(7) All JTAG signals are LVCMOS compatible.
(8) See General Handling Guidelines for Unused CMOS-type Pins in General PCB Recommendations for instructions on handling unused pins.

Table 2. Functional Pin Descriptions (continued)

PIN		I/O POWER	I/O TYPE	INTERNAL TERMINATION	CLK SYSTEM	DESCRIPTION
NAME	NO.					
RESERVED PINS						
RESERVED	N22, M22, P19, P20	VDD33	I_4	Includes an internal pull-down	N/A	Reserved.(8)
RESERVED	V16	VDD33	I_4	Includes an internal pull-up	N/A	
RESERVED	D1, J2	VDD33	I_4		N/A	
RESERVED	F1, F2, G2, G3, G4	VDD33	O_2	Includes internal pull-down	N/A	Leave these pins unconnected.(8)
RESERVED	F3, J1, M21, $\overline{\text{PM\_CS\_0}}$, U3	VDD33	O_2		N/A	
RESERVED	H20, M18, M20	VDD33	O_1		N/A	
RESERVED	H21, H22, J19, J20, J21, J22, K19, K20	VDD33	B_2	Includes internal pull-down	N/A	Reserved(8)
RESERVED	C1, D2, F4	VDD33	B_2		N/A	

Power and Ground Pins

Power and ground connections to the DLPC350 are made up of the groupings shown in Table 3.

Table 3. Power and Ground Pin Descriptions

POWER GROUP	PIN NUMBER(S)	DESCRIPTION
PLLM_VSS	B15	Master clock generator PLL ground return
PLLM_VDD	E14	1.2V Master clock generator PLL Digital Power(1)
PLLM_VAD	D14	1.8V Master clock generator PLL Analog Power(1)
PLLM_VAS	C14	Master clock generator PLL ground return
PLLD_VSS	B14	DDR clock generator PLL ground return
PLLD_VDD	E13	1.2V DDR clock generator PLL Digital Power
PLLD_VAD	D13	1.8V DDR clock generator PLL Analog Power(1)
PLLD_VAS	C13	DDR clock generator PLL ground return
VSS	E5, D4, C3, B2, A2, N6, F11, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, H1, B1, C2, D3, E4, V5, W4, Y3, AA1, AA2, U8, U15, A21, A22, B21, B22, C20, D19, E18, V18, W19, Y20, AA21, AB22, M17, C22, C21, D20, E19, K22, L22, V19, V20, W20, Y21, R1, Y2, W3, V4, F9, A7, B3, B4, C4, A13, B13, B20, C19, Y14, Y12, W12, W10, Y10, AA13, AB13, AA11, AB11, Y8, AA9, F14, V14, V8	Common Ground (105)
VDDC	F12, F7, F6, G6, M6, F5, G5, M5, U6, U7, F17, G17, U16, U17, F18, N17, U18, U5, F16, E6, E12, E17, K6, L6, P6, R6, K17, L17, P17, R17	Core 1.2V Power
VDD33	AB1, F15, T5, T6, AA22, H6, J6, L1, E1, H5, J5, K5, L5, N5, P5, U9, U14, H17, J17, T17, Y22, T22, G22, H18, J18, N18, R5, V1, A20, A16, E15, V9, AA15, AB15, AB21, AB9, T18, K18, F13	LVCMOS I/O 3.3V Power
VDD_DMD	F10, F8, A4, A11, E8, E10	1.9V DMD Interface Voltage
VDD12_FPD	U11, U12, V12, V11	FPD-Link LVDS Interface 1.2V Power(1)
VDD33_FPD	U10, U13, V13, V10	FPD-Link LVDS Interface 3.3V Power(1)
Spare	E16	It is recommended that this signal be tied to ground via an external pull-down resistor
VPGM	D17	Fuse Programming Pin (for manufacturing use only). This signal should be tied directly to ground for normal operation.

(1) Special Filter is required for proper operation. See PLL .

ABSOLUTE MAXIMUM RATING

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
Electrical					
Supply Voltage (1) (2)	VDDC (Core 1.2V Power)		–0.5	1.7	V
	VDD33		–0.5	3.8	V
	VDD_DMD		-0.5	2.3	V
	VDD12_FPD		-0.5	1.7	V
	VDD33_FPD		-0.5	3.8	V
	VDD12_PLLD		-0.5	1.7	V
	VDD12_PLLM		-0.5	1.7	V
	VDD_18_PLLD		-0.5	2.3	V
	VDD_18_PLLM		-0.5	2.3	V
Input Voltage (V_I) (3)	USB		-1.00	5.25	V
	OSC		-0.3	3.6	V
	LVCMOS		-0.5	3.6	V
	I^2C		-0.5	3.6	V
	LVDS		-0.5	3.6	V
Output Voltage (V_O)	USB		-1.00	5.25	V
	DMD LPDDR		-0.3	2.0	V
	LVCMOS		-0.5	3.6	V
	I^2C		-0.5	3.6	V
Environmental					
T_J	Junction temperature		0	105	ºC
T_{stg}	Storage temperature		-40	125	ºC
ESD (4)	Electrostatic discharge immunity	Human Body Model (V_{ESDHBM})		±2000	V
		Charged Device Model (V_{ESDCDM})		±500	
		Machine Model ($V_{ESD\ MM}$)		±150	

(1) All voltages referenced to VSS (ground).
(2) All of the 3.3V, 1.9V, 1.8V, and 1.2V power should be applied and removed per the procedure defined in System Power and Reset.
(3) Applies to external input and bidirectional buffers.
(4) Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Electrical						
VDD33	3.3V Supply voltage, I/O		3.135	3.300	3.465	V
VDD_DMD	1.9V Supply voltage, I/O		1.8	1.9	2.0	V
VDD_18_PLLD	1.8V Supply voltage, PLL Analog		1.71	1.80	1.89	V
VDD_18_PLLM	1.8V Supply voltage, PLL Analog		1.71	1.80	1.89	V
VDD12	1.2V Supply voltage, Core logic		1.116	1.200	1.26	V
VDD12_PLLD	1.2V Supply voltage, PLL Digital		1.116	1.200	1.26	V
VDD12_PLLM	1.2V Supply voltage, PLL Digital		1.116	1.200	1.26	V
V_I	USB		0		VDD33	V
	OSC		0		VDD33	
	3.3V LVCMOS		0		VDD33	
	3.3V I^2C		0		VDD33	
	3.3V LVDS		0.6		2.2	
V_O	USB		0		VDD33	V
	3.3V LVCMOS		0		VDD33	
	3.3V I^2C		0		VDD33	
	1.9V LPDDR		0		VDD_DMD	
Environmental						
T_J	Operating junction temperature		0		85	ºC

POWER CONSUMPTION

Table 4 lists the typical current and power consumption of the individual supplies.

Normal mode refers to operation during full functionality, active product operation. Typical values correspond to power dissipated on nominal process devices operating at nominal voltage and 70°C junction temperature (approximately 25°C ambient) displaying typical video-graphics content from a high frequency source. Maximum values correspond to power dissipated on fast process devices operating at high voltage and 105°C junction temperature (approximately 55°C ambient) displaying typical video-graphics content from a high frequency source. The increased power dissipation observed on fast process devices operated at maximum recommended temperatures is primarily a result of increased leakage current. Maximum power values are estimates and may not reflect the actual final power consumption of the device.

Table 4. Power Consumption

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
I_{CC12}	Supply Voltage, 1.2V core power	Normal Mode		600	1020	mA
I_{CC19_DMD}	Supply Voltage, 1.9V I/O power (DMD LPDDR)	Normal Mode		30	50	mA
I_{CC33}	Supply Voltage, 3.3V (I/O) power	Normal Mode		40	70	mA
I_{CC12_FPD}	FPD-Link LVDS Interface Supply Voltage, 1.2V power	Normal Mode		60	100	mA
I_{CC33_FPD}	FPD-Link LVDS Interface Supply Voltage, 3.3V power	Normal Mode		50	85	mA
I_{CC12_PLLD}	Supply Voltage, PLL Digital Power (1.2V)	Normal Mode		9	15	mA
I_{CC12_PLLM}	Supply Voltage, Master Clock Generator PLL Digital power (1.2V)	Normal Mode		9	15	mA
I_{CC18_PLLD}	Supply Voltage, PLL Analog power (1.8V)	Normal Mode		10	15	mA
I_{CC18_PLLM}	Supply Voltage, Master Clock Generator PLL Analog power (1.8V)	Normal Mode		10	15	mA
Total Power		Normal Mode		1225	2200	mW

I/O Characteristics

Voltage and current characteristics for each I/O type signal. All inputs and outputs are LVCMOS.

Table 5. I/O Characteristics(1)

PARAMETER			CONDITIONS	MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	USB (9)		2.0			V
		OSC (10)		2.0			
		3.3V LVCMOS (1, 2, 3, 4)		2.0			
		3.3V I^2C (8)		2.4			
V_{IL}	Low-level input voltage	USB (9)				0.8	V
		OSC (10)				0.8	
		3.3V LVCMOS (1, 2, 3, 4)				0.8	
		3.3V I^2C				1.0	
V_{OH}	High-level output voltage	USB (9)		2.8			V
		3.3V LVCMOS (1, 2, 3)	I_{OH} = Max Rated	2.8			
		1.9V DMD LPDDR (7)	I_{OH} = -0.1 mA	0.9 × VDD_DMD			
V_{OL}	Low-level output voltage	USB (9)				0.3	V
		3.3V LVCMOS (1, 2, 3)	I_{OL} = Max Rated			0.4	
		1.9V DMD LPDDR (7)	I_{OL} = +0.1 mA			0.1 × VDD_DMD	
		3.3V I^2C (8)	I_{OL} = 3 mA sink			0.4	
V_{IDTH}	Input differential threshold	3.3V LVDS (5)		-200		200	mV
$\|V_{ID}\|$	Absolute input differential voltage	USB (9)		200			mV
		3.3V LVDS (5)		200		600	
V_{ICM}	Input Common Mode Voltage Range	USB (9)		0.8		2.5	V
		3.3V LVDS (5)	at MIN absolute input differential voltage	0.7		2.1	
		3.3V LVDS (5)	at MAX absolute input differential voltage	0.9		1.9	
V_{HYS}	Hysteresis (V_{T+} - V_{T-})	3.3V LVCMOS (1, 2, 3, 4)			400		mV
		3.3V I^2C (8)			550		
		USB (9)			320		
R_I	Receiver input impedance	3.3V LVDS (5)	VDDH = 3.3V	90	110	132	Ω
I_{IH}	High-level input current (IPD = internal pull-down)	USB (9)				10	µA
		OSC (10)				10	
		3.3V LVCMOS (1, 2, 3, 4) without IPD	V_{IH} = VDD33			10	
		3.3V LVCMOS (1, 2, 3, 4) with IPD	V_{IH} = VDD33			200	
		3.3V I^2C (8)	V_{IH} = VDD33			10	
I_{IL}	Low-level input current(IPU = internal pull-up)	USB (9)				-10	µA
		OSC (10)				-10	
		3.3V LVCMOS (1, 2, 3, 4) without IPU	V_{OH} = VDD33			-10	
		3.3V LVCMOS (1, 2, 3, 4) with IPU	V_{OH} = VDD33			-200	
		3.3V I^2C (8)	V_{OH} = VDD33			-10	
I_{OH}	High-level output current	USB (9)		17.08			mA
		1.9V DMD LPDDR (7)	V_O = 1.5V	-4.0			
		3.3V LVCMOS (1)	V_O = 2.4V	-4.0			
		3.3V LVCMOS (2)	V_O = 2.4V	-8.0			
		3.3V LVCMOS (3)	V_O = 2.4V	-12.0			

(1) Numbers in parentheses correspond with Table 6.

Table 5. I/O Characteristics(1) (continued)

PARAMETER			CONDITIONS	MIN	NOM	MAX	UNIT
I_{OL}	Low-level output current	USB (9)		-17.08			mA
		1.9V DMD LPDDR (7)	V_O = 0.4V	4.0			
		3.3V LVCMOS (1)	V_O = 0.4V	4.0			
		3.3V LVCMOS (2)	V_O = 0.4V	8.0			
		3.3V LVCMOS (3)	V_O = 0.4V	12.0			
		3.3V I^2C (8)		3.0			
I_{OZ}	High-impedance leakage current	USB (9)		-10		10	µA
		3.3V LVCMOS (1, 2, 3)		-10		10	
		3.3V I^2C (8)		-10		10	
C_I	Input capacitance (including package)	USB (9)		11.3	12.8	14.7	pF
		3.3V LVCMOS (2)		2.8	3.3	4.0	
		3.3V LVCMOS 4)		2.7	3.4	4.2	
		3.3V I^2C (8)		3.0	3.2	3.5	

Table 6. I/O Type Subscript Definition

I/O	
SUBSCRIPT	DEFINITION
1	3.3V LVCMOS I/O Buffer, with 4 mA Drive
2	3.3V LVCMOS I/O Buffer, with 8 mA Drive
3	3.3V LVCMOS I/O Buffer, with 12 mA Drive
4	3.3V LVCMOS Receiver
5	3.3V LVDS Receiver (FPD-Link Interface)
6	N/A
7	1.9V LPDDR Output Buffer (DMD Interface)
8	3.3V I^2C with 12 mA Sink
9	USB Compatible (3.3 Volts)
10	OSC 3.3V I/O Compatible LVCMOS

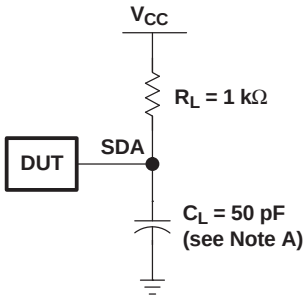
Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC350 Controller.

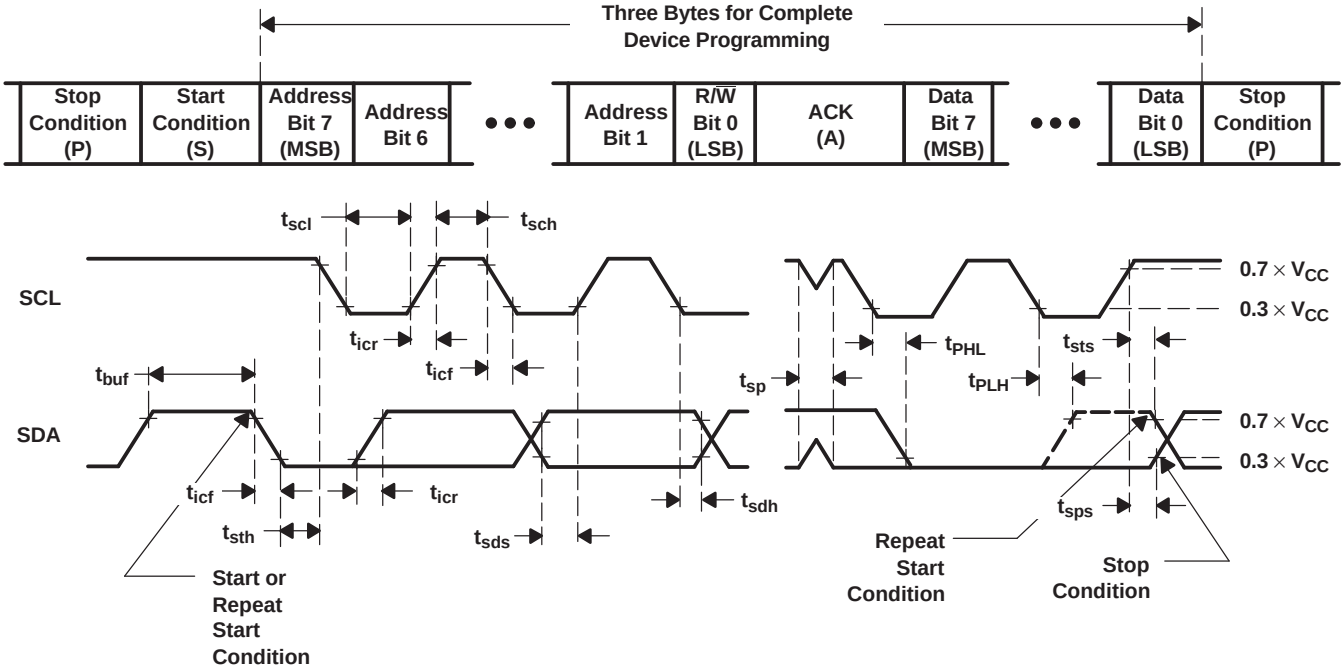
I^2C Electrical Data/Timing

Table 7. I^2C0 and I^2C1 INTERFACE TIMING REQUIREMENTS

PARAMETER			MIN	MAX	UNIT
f_{scl}	I^2C clock frequency		0	400	kHz
t_{sch}	I^2C clock high time		1		µs
t_{scl}	I^2C clock low time		1		µs
t_{sp}	I^2C spike time			20	ns
t_{sds}	I^2C serial-data setup time		100		ns
t_{sdh}	I^2C serial-data hold time		100		ns
t_{icr}	I^2C input rise time		100		ns
t_{ocf}	I^2C output fall time	50 pF	30	200	ns
t_{buf}	I^2C bus free time between stop and start conditions		1.3		µs
t_{sts}	I^2C start or repeat start condition setup		1		µs
t_{sth}	I^2C start or repeat start condition hold		1		µs
t_{sph}	I^2C stop condition setup		1		µs
t_{vd}	Valid-data time	SCL low to SDA output valid		1	µs
	Valid-data time of ACK condition	ACK signal from SCL low to SDA (out) low		1	µs
t_{sch}	I^2C bus capacitive load		0	100	pF



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

Figure 12. I^2C Interface Load Circuit and Voltage Waveforms

Port 1 Input Pixel Interface

Table 8. Port 1 Input Pixel Interface Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, P1A_CLK		12	150	MHz
t_c	Cycle time, P1A_CLK		6.666	83.330	ns
t_{jp}	Clock jitter, P1A_CLK (Deviation in period from ideal)(1)	Maximum f_{clock}			
$t_{w(L)}$	Pulse duration low, P1A_CLK	50% reference points	2.3		ns
$t_{w(H)}$	Pulse duration high, P1A_CLK	50% reference points	2.3		ns
t_{su}	Setup time – P1_(A-C)(9-0), P1_VSYNC, P1_HSYNC, P1_FIELD, P1_DATEN; Valid before P1A_CLK↑↓	50% reference points	3		ns
t_h	Hold time – P1_(A-C)(9-0), P1_VSYNC, P1_HSYNC, P1_FIELD, P1_DATEN; Valid after P1A_CLK↑↓	50% reference points	3		ns
t_t	Transition time -- P1A_CLK	20% to 80% reference points	0.6	2.0	ns
t_t	Transition time -- P1_A(9-0), P1_B(9-0), P1_C(9-0), P1_HSYNC, P1_VSYNC, P1_DATEN	20% to 80% reference points	0.6	3.0	ns

(1) For frequencies (f_{clock}) less than 150 MHz, clock jitter (in ns) should be calculated using this formula: Max Clock Jitter = ±[1/ f_{clock} – 5414 ps].

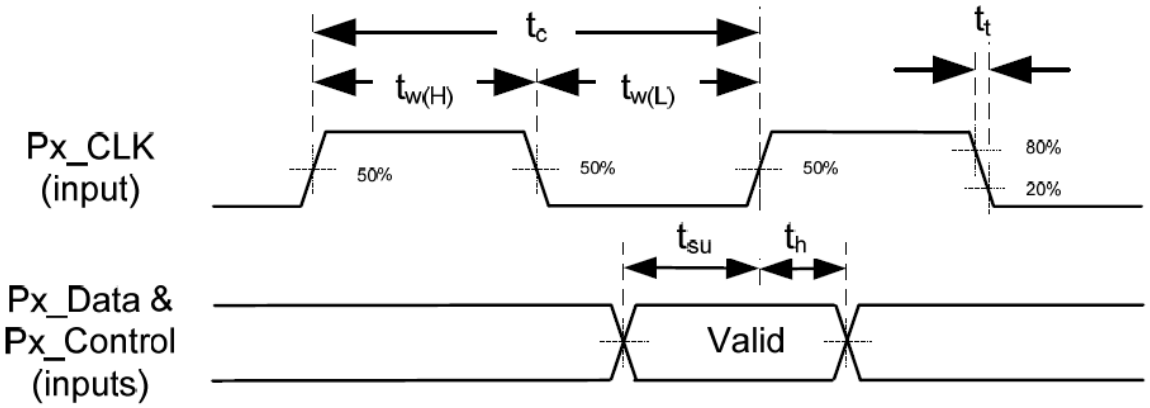


Figure 13. Port 1 Input Pixel Timing

Port 2 Input Pixel Interface (FPD-Link Compatible LVDS Input)

Table 9. Port 2 Input Pixel Interface (FPD-Link Compatible LVDS Input) Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, P2_CLK (LVDS input clock)		20	90	MHz
t_c	Cycle time, P2_CLK (LVDS input clock)		11.1	50.0	ns
t_{slew}	Clock or data slew rate	f_{pxck} < 90 MHz	0.3		V/ns
		f_{pxck} > 90 MHz	0.5		
$t_{startup}$	Link startup time (internal)			1	ms

Extra Notes:

Minimize cross-talk and match traces on PCB as close as possible.

It is recommended to keep the Common Mode Voltage as close to 1.2V as possible.

It is recommended to keep the Absolute Input Differential Voltage as high as possible.

The LVDS open input detection is only related to a low common mode voltage; it is not related to a low differential swing.

LVDS power 3.3V supply (VDD33_FPD) noise level should be below 100 mV_{p-p}.

LVDS power 1.2V supply (VDD12_FPD) noise level should be below 60 mV_{p-p}.

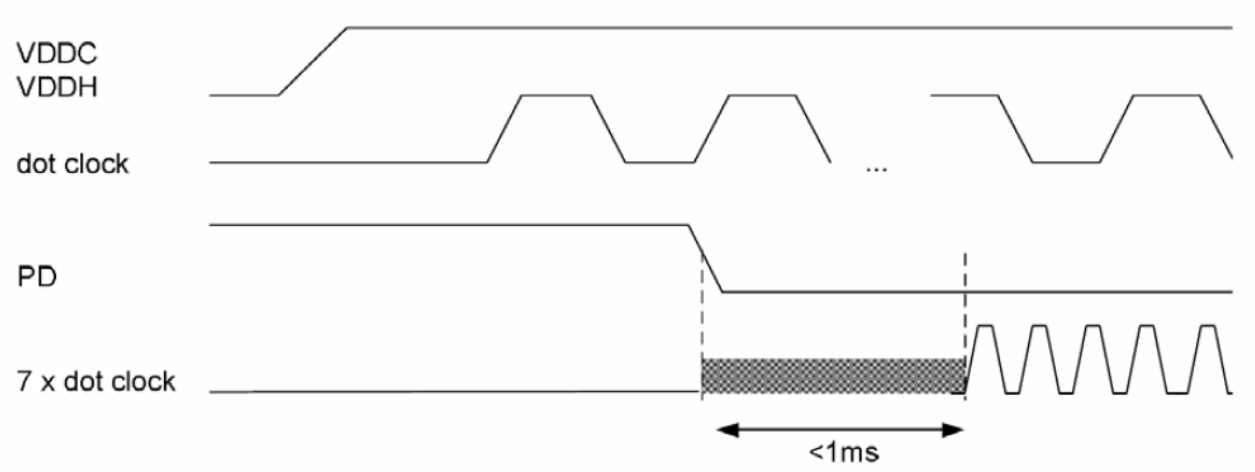


Figure 14. LVDS Timing Diagram

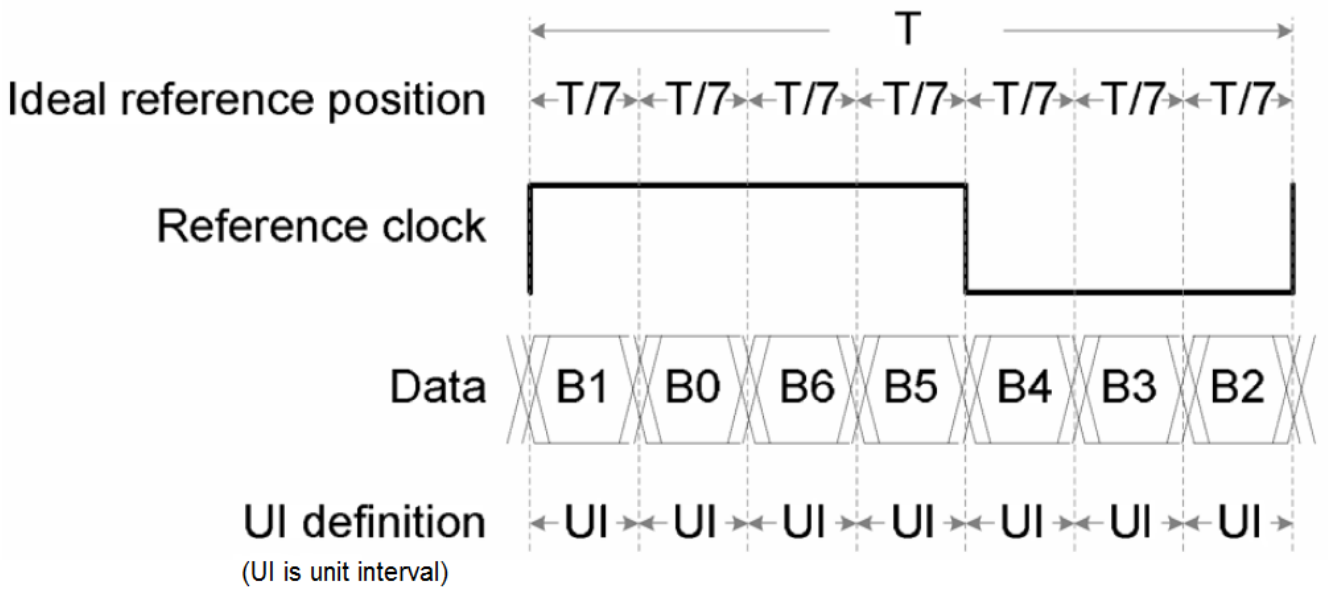


Figure 15. (LVDS) Link Start-Up Timing

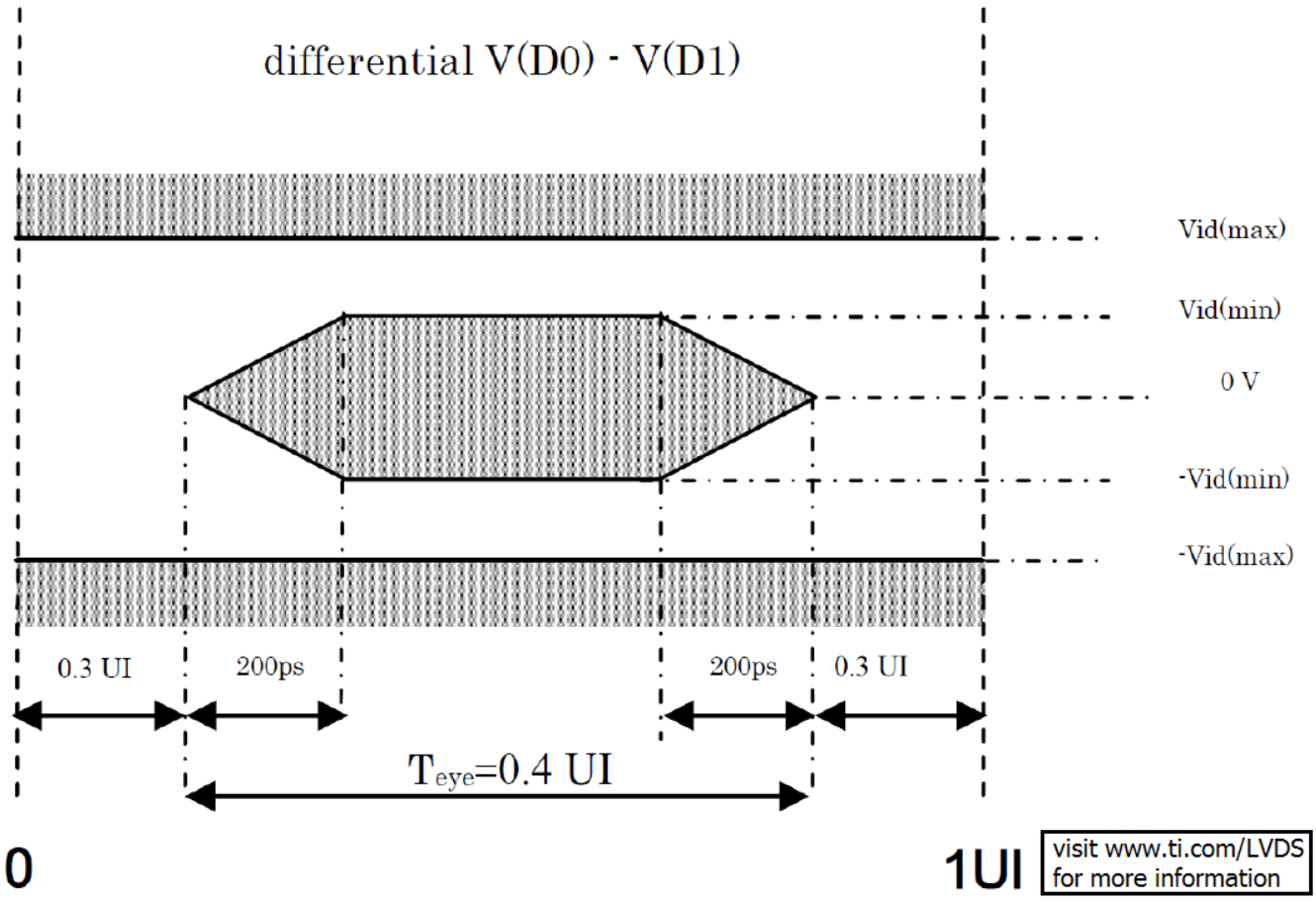


Figure 16. (LVDS) Clock: Data Skew Definition

Table 10. (LVDS) Receiver Supported Pixel Mapping Modes

LVDS Receiver Input	Mapping Selection 1	Mapping Selection 2	Mapping Selection 3	Mapping Selection 4 (18-bit Mode)
RA Input Channel				
RDA(6)	map to GRN(4)	map to GRN(2)	map to GRN(0)	map to GRN(4)
RDA(5)	map to RED(9)	map to RED(7)	map to RED(5)	map to RED(9)
RDA(4)	map to RED(8)	map to RED(6)	map to RED(4)	map to RED(8)
RDA(3)	map to RED(7)	map to RED(5)	map to RED(3)	map to RED(7)
RDA(2)	map to RED(6)	map to RED(4)	map to RED(2)	map to RED(6)
RDA(1)	map to RED(5)	map to RED(3)	map to RED(1)	map to RED(5)
RDA(0)	map to RED(4)	map to RED(2)	map to RED(0)	map to RED(4)
RB Input Channel				
RDB(6)	map to BLU(5)	map to BLU(3)	map to BLU(1)	map to BLU(5)
RDB(5)	map to BLU(4)	map to BLU(2)	map to BLU(0)	map to BLU(4)
RDB(4)	map to GRN(9)	map to GRN(7)	map to GRN(5)	map to GRN(9)
RDB(3)	map to GRN(8)	map to GRN(6)	map to GRN(4)	map to GRN(8)
RDB(2)	map to GRN(7)	map to GRN(5)	map to GRN(3)	map to GRN(7)
RDB(1)	map to GRN(6)	map to GRN(4)	map to GRN(2)	map to GRN(6)
RDB(0)	map to GRN(5)	map to GRN(3)	map to GRN(1)	map to GRN(5)
RC Input Channel				
RDC(6)	map to DEN			
RDC(5)	map to VSYNC			
RDC(4)	map to HSYNC			
RDC(3)	map to BLU(9)	map to BLU(7)	map to BLU(5)	map to BLU(9)
RDC(2)	map to BLU(8)	map to BLU(6)	map to BLU(4)	map to BLU(8)
RDC(1)	map to BLU(7)	map to BLU(5)	map to BLU(3)	map to BLU(7)
RDC(0)	map to BLU(6)	map to BLU(4)	map to BLU(2)	map to BLU(6)
RD Input Channel				
RDD(6)	map to Field (option 1 if available)			
RDD(5)	map to BLU(3)	map to BLU(9)	map to BLU(7)	NO MAPPING
RDD(4)	map to BLU(2)	map to BLU(8)	map to BLU(6)	NO MAPPING
RDD(3)	map to GRN(3)	map to GRN(9)	map to GRN(7)	NO MAPPING
RDD(2)	map to GRN(2)	map to GRN(8)	map to GRN(6)	NO MAPPING
RDD(1)	map to RED(3)	map to RED(9)	map to RED(7)	NO MAPPING
RDD(0)	map to RED(2)	map to RED(8)	map to RED(6)	NO MAPPING
RE Input Channel				
RDE(6)	map to Field (option 2 if available)			
RDE(5)	map to BLU(1)		map to BLU(9)	NO MAPPING
RDE(4)	map to BLU(0)		map to BLU(8)	NO MAPPING
RDE(3)	map to GRN(1)		map to GRN(9)	NO MAPPING
RDE(2)	map to GRN(0)		map to GRN(8)	NO MAPPING
RDE(1)	map to RED(1)		map to RED(9)	NO MAPPING
RDE(0)	map to RED(0)		map to RED(8)	NO MAPPING

Mapping options are selected via software. If Mapping Option #4 above is the only mapping mode needed, and if and only if a "Field 1" or "Field 2" input is not needed, then the board layout can leave the LVDS inputs for RD and RE channels only.

Video Timing Input Blanking Specification

The DLPC350 requires a minimum horizontal and vertical blanking for both Port 1 and Port 2. These parameters indicate the time allocated to retrace the signal at the end of each line and field of a display. This section defines the related parameters

Video Timing Parameter Definitions

VS Vertical Sync

Timing reference point that indicates the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. This active edge is the reference from which all Vertical Blanking parameters are measured

HS Horizontal Sync

Timing reference point that indicates the start of the horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. This active edge is the reference from which all Horizontal Blanking parameters are measured

TLPF Total Lines (active and inactive) Per Frame

Defines the Vertical Period (or frame time) in lines

ALPF Active Lines Per Frame

Number of lines in a frame containing displayable data. This is a subset of the TLPF

TPPL Total Pixel Per Line

Horizontal Line Period in pixel clocks. Total number of active and inactive pixel clocks per line

APPL Active Pixels Per Line

Number of pixel clocks in a line containing displayable data. This is a subset of the TPPL

VBP Vertical Back Porch blanking

Number of blank lines after Vertical Sync but before the first active line

VFP Vertical Front Porch blanking

Number of blank lines after the last active line but before Vertical Sync

HBP Horizontal Back Porch blanking

Number of blank pixel clocks after Horizontal Sync but before the first active pixel. HBP times are in reference to the leading (active) edge of the respective sync signal

HFP Horizontal Front Porch blanking

Number of blank pixel clocks after the last active pixel but before Horizontal Sync

Source Input Blanking

The Vertical and Horizontal Blanking requirements for both input ports are defined below. Reference the Video Timing Parameter Definitions listed above.

Table 11. Source Input Blanking Requirements

PORT	PARAMETER	MINIMUM BLANKING
Port 1 Vertical Blanking	VBP	370 µs
	VFP	2 lines
	Total Vertical Blanking	370 µs + 3 lines
Port 2 Vertical Blanking	VBP	370 µs
	VFP	0 lines
	Total Vertical Blanking	370 µs + 3 lines
Port 1 and 2 Horizontal Blanking	HBP	10 pixels
	HFP	0 pixels
	Total Horizontal Blanking for 0.45 WXGA DMD	154,286 ÷ Source APPL pixels (round up)

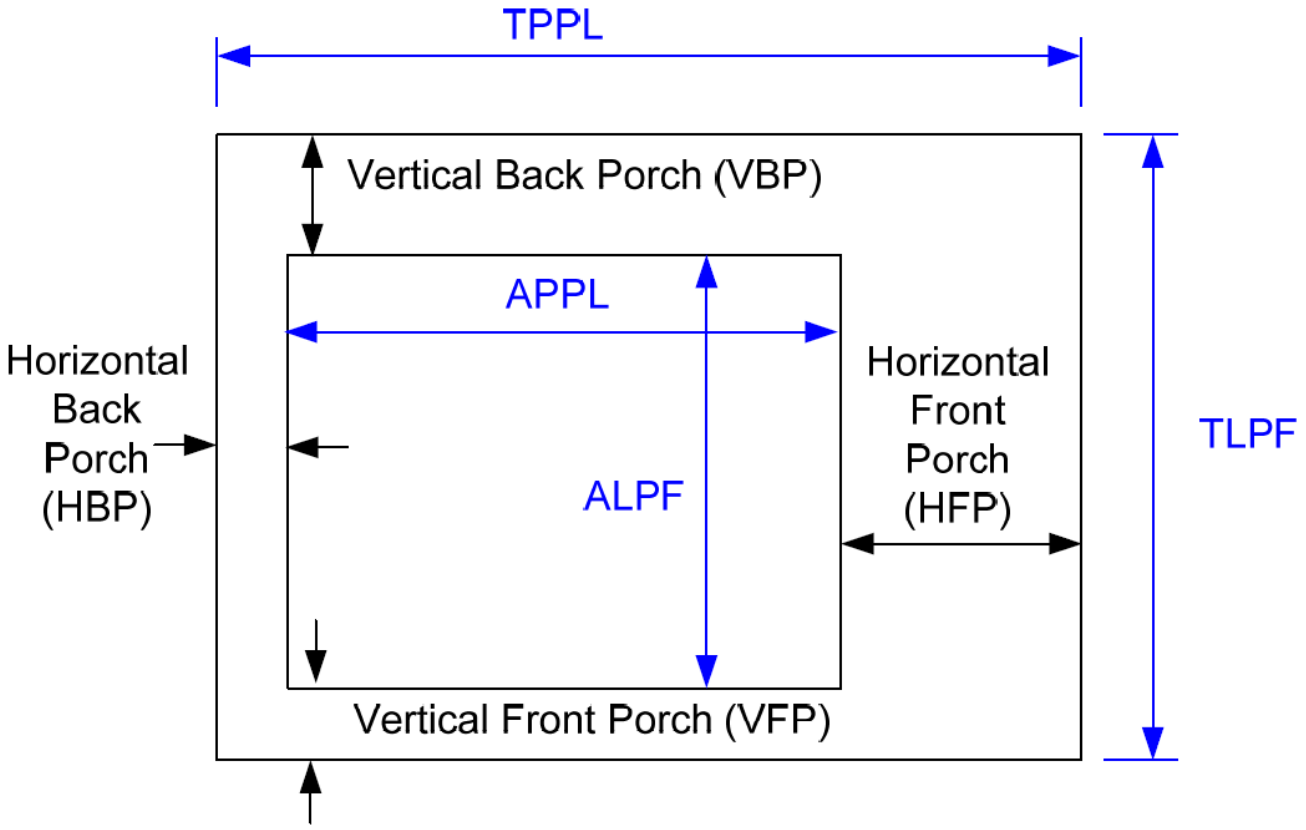


Figure 17. Horizontal and Vertical Blanking Diagram

Programmable Output Clocks

Table 12. Programmable Output Clocks Timing

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, OCLKC	N/A	OCLKC	0.7759	48	MHz
t_c	Cycle time, OCLKC	N/A	OCLKC	20.83	1288.80	ns
$t_{w(L)}$	Pulse duration low (50% reference points)	N/A	OCLKC	$(t_c/2)-2$		ns
$t_{w(H)}$	Pulse duration high (50% reference points)	N/A	OCLKC	$(t_c/2)-2$		ns
f_{clock}	Clock frequency, OCLKD	N/A	OCLKD	0.7759	48	MHz
t_c	Cycle time, OCLKD	N/A	OCLKD	20.83	1288.80	ns
$t_{w(L)}$	Pulse duration low (50% reference points)	N/A	OCLKD	$(t_c/2)-2$		ns
$t_{w(H)}$	Pulse duration high (50% reference points)	N/A	OCLKD	$(t_c/2)-2$		ns

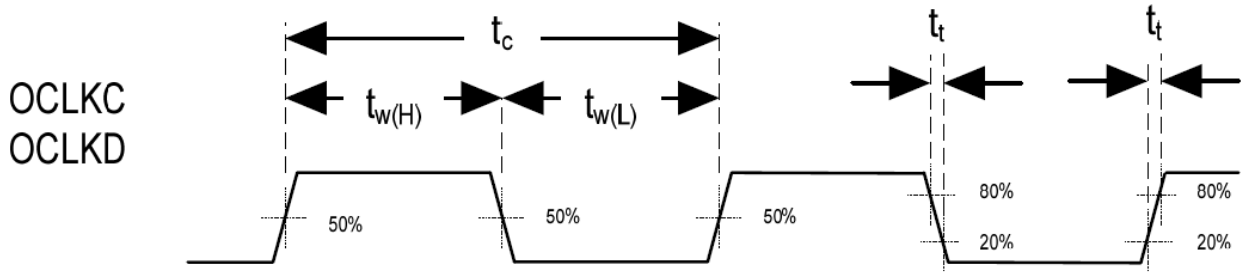


Figure 18. Programmable Output Clocks Timing Diagram

DMD Interface

The DLPC350 controller DMD interface is comprised of a combination of both single (SDR) and double data rate (DDR), and output signals using LPDDR (as defined by JESD209A). SDR signals are referenced to DMD_SAC_CLK and DDR signals are referenced to DMD_DCLK.

Switching characteristics over recommended operating conditions, C_L (minimum timing) = 5 pF, C_L (maximum timing) = 25 pF (unless otherwise noted).

Table 13. DMD Interface Timing Requirements

PARAMETER		TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock1}	Clock frequency(1)(2)		n/a	DMD_DCLK	79.992	120.012	MHz
t_{p1_clkper}	Clock period	50% reference points	n/a	DMD_DCLK	8.332	12.502	ns
t_{p1_cwh}	Clock pulse width low	50% reference points	n/a	DMD_DCLK	3.75		ns
t_{p1_cwl}	Clock pulse width high	50% reference points	n/a	DMD_DCLK	3.75		ns
f_{clock2}	Clock frequency(2)		n/a	DMD_SAC_CLK	74.659	74.675	MHz
t_{p2_clkper}	Clock period	50% reference points	n/a	DMD_SAC_CLK	13.391	13.394	ns
t_{p2_cwh}	Clock pulse width low	50% reference points	n/a	DMD_SAC_CLK	6		ns
t_{p2_cwl}	Clock pulse width high	50% reference points	n/a	DMD_SAC_CLK	6		ns
t_{slew}	Slew rate(3)(4)(5)		n/a	All	0.7		V/ns
t_{p1_su}	Output setup time(6)	50% reference points	both rising and falling edges of DMD_DCLK	DMD_D(23:0), DMD_SCTRL, DMD_LOADB, DMD_TRC		1.1	ns
t_{p1_h}	Output hold time(6)	50% reference points	both rising and falling edges of DMD_DCLK	DMD_D(23:0), DMD_SCTRL, DMD_LOADB, DMD_TRC		1.1	ns
t_{p1_skew}	DMD data skew	50% reference points	relative to each other	DMD_D(23:0), DMD_SCTRL, DMD_LOADB, DMD_TRC, DMD_DCLK		0.2	ns
t_{p2_su}	Output setup time(6)	50% reference points	rising edge of DMD_SAC_CLK	DMD_SAC_BUS, DMD_DRC_OE, DMD_DRC_BUS, DMD_DRC_STRB		2.35	ns
t_{p2_h}	Output hold time(6)	50% reference points	rising edge of DMD_SAC_CLK	DMD_SAC_BUS, DMD_DRC_OE, DMD_DRC_BUS, DMD_DRC_STRB		2.35	
t_{p2_skew}	DRC/SAC data skew	50% reference points	relative to each other	DMD_SAC_BUS, DMD_DRC_OE, DMD_DRC_BUS, DMD_DRC_STRB, DMD_SAC_CLK		0.2	ns

(1) The controller supports a fixed number of programmable clock rates with the min and max values as shown. The performance may be further limited by interface voltage and PCB routing.
(2) Note that these vales do not include any tolerance variation of the external crystal/oscillator, nor do they include any associated jitter.
(3) LPDDR Slew rate for the rising edge is measured between VILD(DC) to VIHD(AC) where VILD(DC) = 0.3*VDDQ and VILD(AC) = 0.8*VDDQ.
(4) LPDDR Slew rate for the rising edge is measured between VILD(DC) to VIHD(AC) where VILD(DC) = 0.7*VDDQ and VILD(AC) = 0.2*VDDQ.
(5) The DMD setup and hold time window must be de-rated by 300 ps for each 0.1 V/ns reduction in slew rate below 1V/ns. Thus a 0.7 V/ns slew rate increases this window by 900 ps from 1400 ps to 2300 ps.
(6) Output setup and hold values already include clock jitter, DCD, SSO, ISI noise and PCB variation. Only routing skew and DMD setup/hold need to be considered in system timing analysis.

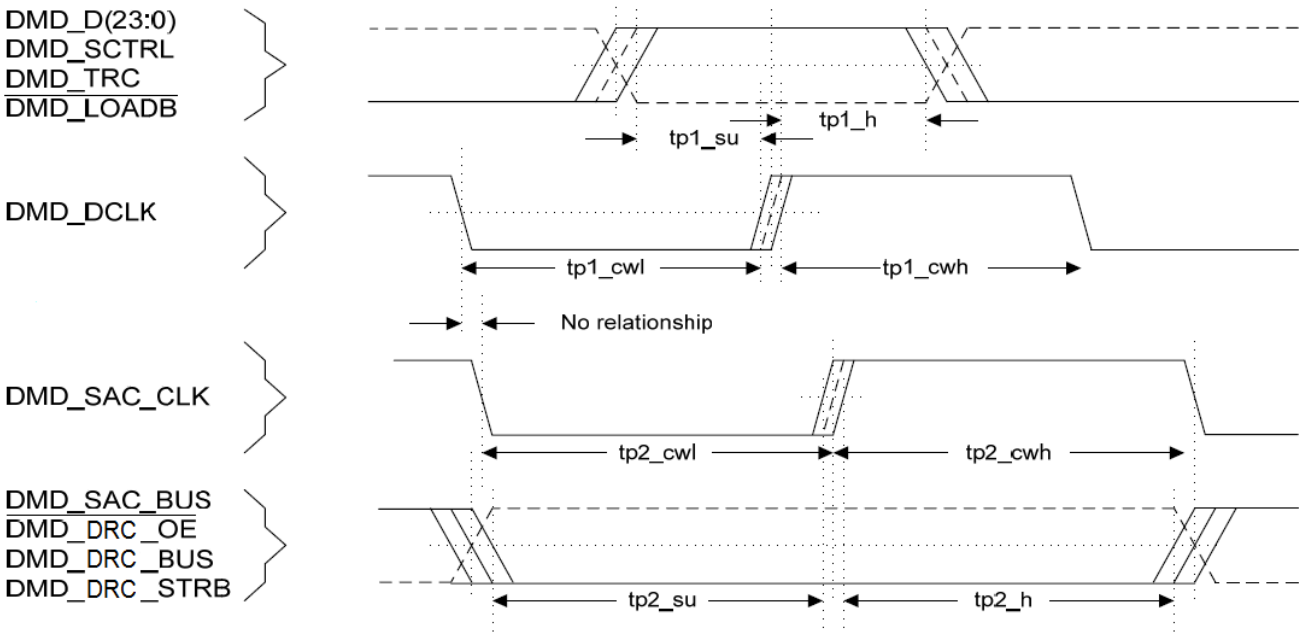


Figure 19. DMD Interface Timing

System Oscillator and JTAG Interfaces

Table 14. System Oscillator Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, MOSC (7)		31.9968	32.0032	MHz
t_c	Cycle time, MOSC (7)		31.188	31.256	ns
$t_{w(H)}$	Pulse duration (high), MOSC (8)	50% reference points	12.5		ns
$t_{w(L)}$	Pulse duration (low), MOSC (8)		12.5		ns
t_t	Transition time, MOSC (8)	20% to 80% reference points		7.5	ns
t_{jp}	Period jitter, MOSC (8) (Deviation in period from ideal period solely due to high frequency jitter and not spectrum clocking)		-100	+100	ps

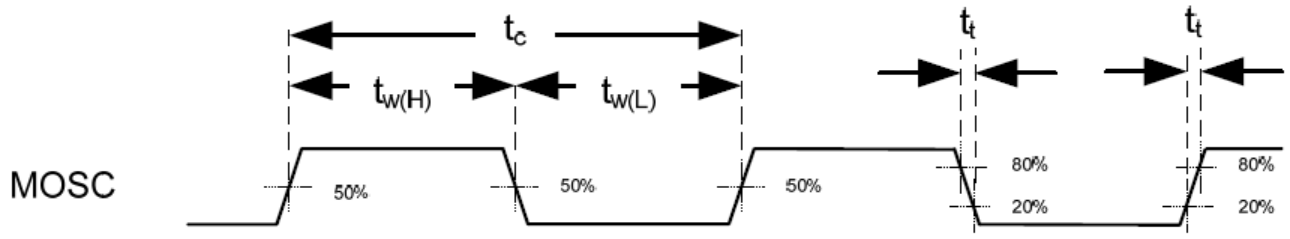


Figure 20. System Oscillators Timing

(7) The frequency range for MOSC is 32 MHz with ±100 PPM accuracy. This shall include impact to accuracy due to aging, temperature and trim sensitivity. The MOSC input cannot support spread spectrum clock spreading.
(8) Applies only when driven via an external digital oscillator.

Table 15. JTAG Interface: I/O Boundary Scan Application Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK			10	MHz
t_c	Cycle time, TCK		100		ns
$t_{w(L)}$	Pulse duration low, PCLK	50% reference points	40		ns
$t_{w(H)}$	Pulse duration high, PCLK	50% reference points	40		ns
t_{su}	Setup time – TDI, TMS1; Valid before TCK↑↓	20% to 80% reference points	8		ns
t_h	Hold time – TDI, TMS1; Valid after TCK↑↓		2		ns
t_t	Transition time			5	ns
t_{pd} (1)	Output propagation, Clock to Q	From (Input) TCK↓ to (Output) TDO1	3	12	ns

(1) Switching characteristics over recommended operating conditions, C_L (minimum timing) = 5 pF, C_L (maximum timing) = 85 pF (unless otherwise noted).

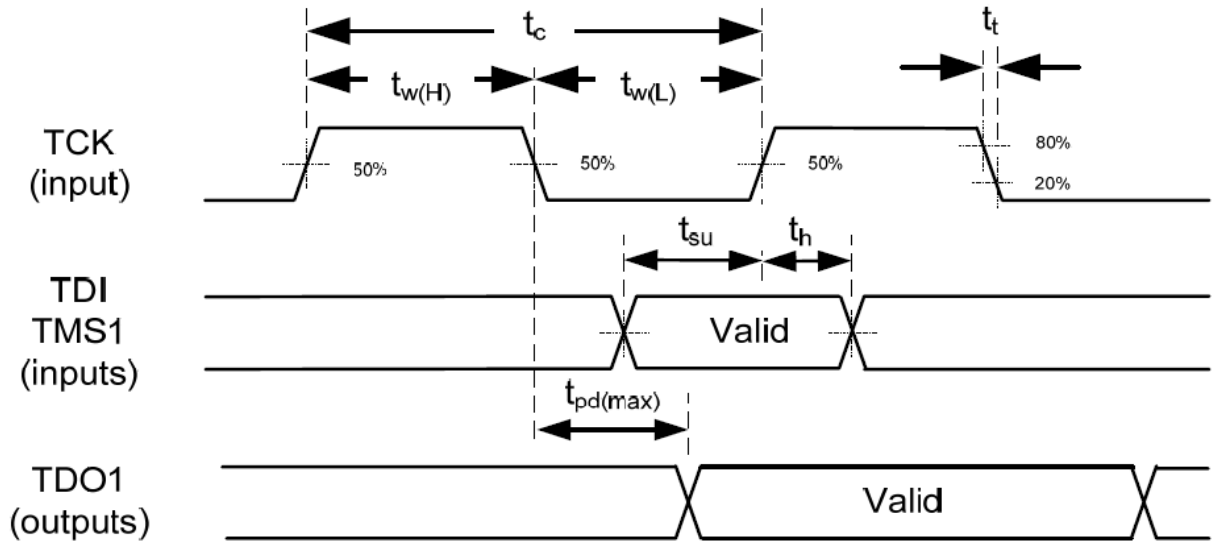


Figure 21. Boundary Scan Timing

System Power and Reset

There are several factors related to System Power and Reset which affect the DC error (offset) and AC noise at the DLPC350 power pins.

Default Conditions

At system power-up, the DLPC350 performs a power-up initialization routine that will default the controller to its normal power mode, related clocks will be enabled at their full rate, and associated resets will be released. Most other clocks will default to "disabled" with associated resets asserted until released by the processor. These same defaults will also be applied as part of all system reset events that occur without removing or recycling power.

Following power-up or system reset initialization, the system will boot from an external flash memory after which it will enable the rest of the controller clocks. Once system initialization is complete, application software will determine if and when to enter standby mode.

1.2V System Power

The controller supports a low cost power delivery system with a single 1.2V power source derived from a switching regulator. The main core should receive 1.2V power directly from the regulator output, and the internal DLPC350 PLLs (VDD_12_PLLM, VDD_12_PLLD) should receive individually filtered versions of this 1.2V power. See PLL for specific filter recommendations.

1.8V System Power

A single 1.8V power source should be used to supply both internal PLLs (VDD_18_PLLM, VDD_18_PLLD). In order to keep the power as clean as possible, it is recommended that this power be sourced via a linear regulator that is individually filtered for each PLL. See PLL for specific filter recommendations.

1.9V System Power

In order to maximize signal integrity, it is recommended that an independent linear regulator be used to source the 1.9V supply that supports the DMD interface (VDD_DMD). To achieve maximum performance, this supply must be tightly regulated to operating within a 1.9V ±0.1V range.

3.3V System Power

The DLPC350 supports a low cost power delivery system with a single 3.3V power source derived from a switching regulator. This 3.3V power will supply all LVCMOS I/O. 3.3V power (VDD33) should remain active in all power modes for which the 1.2V core power is applied.

FPD-Link Input LVDS System Power

The controller supports an FPD-Link compatible LVDS input for an additional method of inputting video/graphics data for display. This interface has some special controller power considerations that are separate from the other controller 1.2V or 3.3V power rails. An FPD-Link 1.2V power pin configuration example is shown in below.

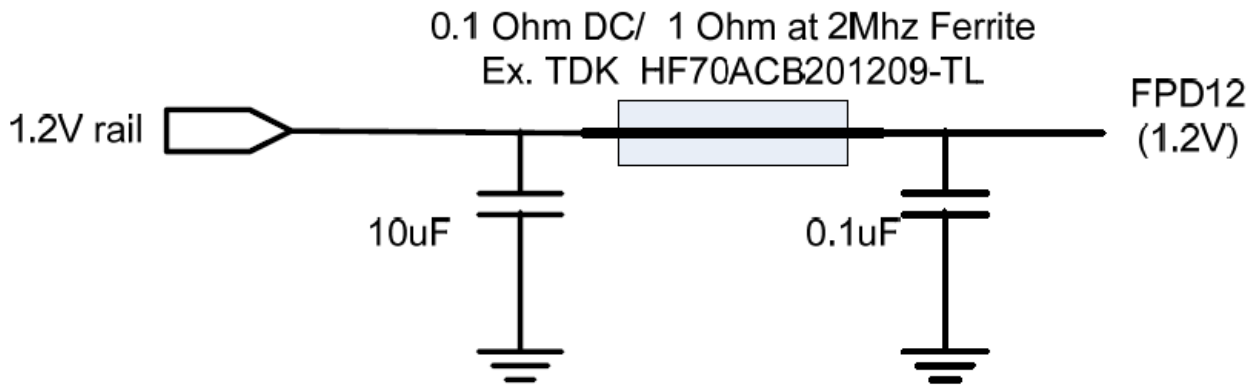


Figure 22. FPD-Link 1.2V Power Pin Configuration

In addition, it is recommended to place the 0.1µF low ESR (equivalent series resistance capacitors to ground as close to the FPD-Link power pins of the DLPC350 as possible. FPD-Link 3.3V power pins should also use external capacitors in the same manner as the 1.2V pins. When FPD-Link is not utilized, the filtering can be omitted. The corresponding voltages, however, MUST still be provided in order to avoid potential long-term reliability issues.

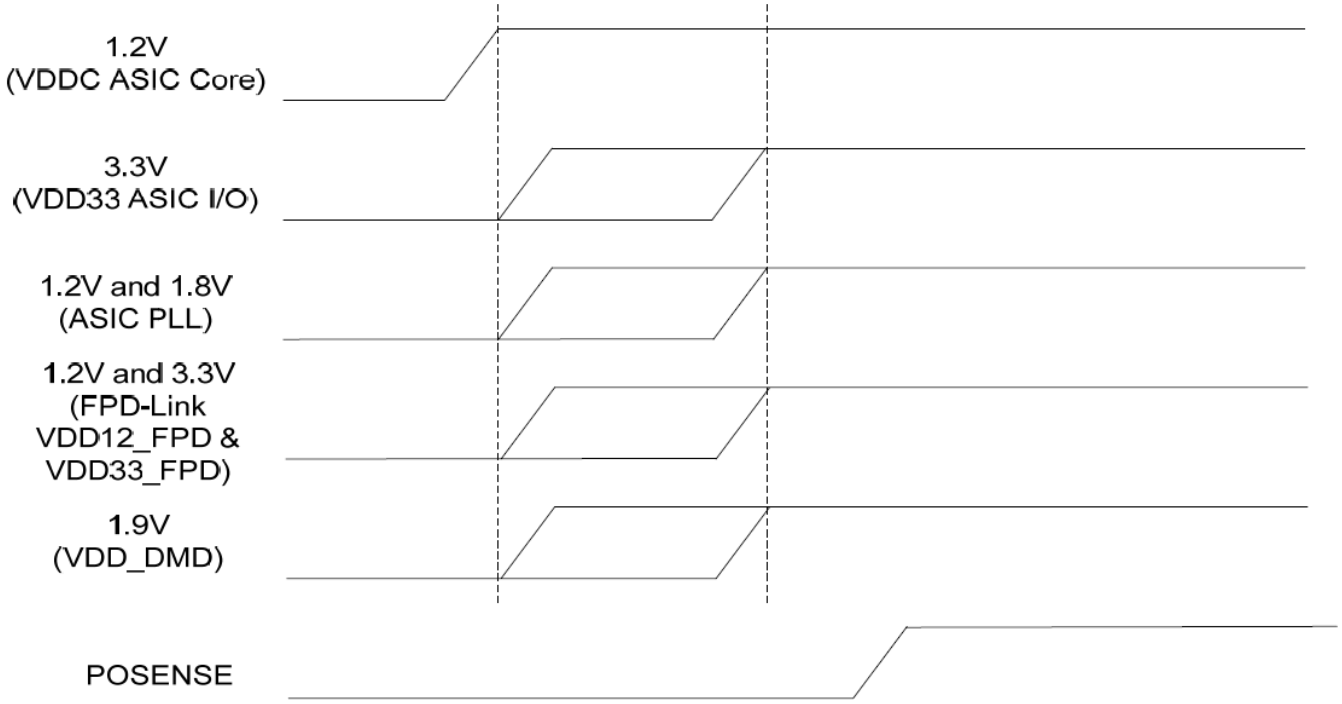


Figure 23. Initialization Timeline

System Power-Up/Down Sequence

Although the DLPC350 requires an array of power supply voltages, (e.g., VDDC, VDD_1X_PLLX, VCC_18, VCC_DMD, VCCXX_FPD), there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC350. This is true for both power-up and power-down. Similarly, there is no minimum time between powering up or powering down the different supplies of the DLPC350. Note, however, that it is not uncommon for there to be power-sequencing requirements for other devices that share power supplies with the DLPC350.

Although there is no risk of damaging the DLPC350 as a result of a given power sequence, from a functional standpoint there are a few specific power-sequencing recommendations to ensure proper operation.

- 1.2V Core power should be applied whenever any I/O power is applied. This ensures that the powered I/O pins are set to a known state. Thus, it is recommended that core power be applied first. Other supplies should be applied only after the 1.2V DLPC350 core has ramped up.
- All controller power should be applied before POSENSE is asserted to ensure proper power-up initialization is performed. 1.8V PLL power, 1.9V I/O power and 3.3V I/O power should remain applied as long as 1.2V core power is applied and POSENSE is asserted.

It is assumed that all DLPC350 power-up sequencing is handled by external hardware. It is also assumed that an external power monitor will hold the DLPC350 in system reset during power-up (itaht is, POSENSE = 0). It should continue to assert system reset until ALL DLPC350 voltages have reached minimum specified voltage levels. During this time, all controller I/O will either be tri-stated or driven low. The master PLL (PLLM) will be released from reset upon the low to high transition of POSENSE but the DLPC350 will keep the rest of the controller in reset for an additional 100 ms to allow the PLL to lock and stabilize its outputs. After this 100 ms delay, internal resets will be de-asserted causing the microprocessor to begin its boot-up routine.

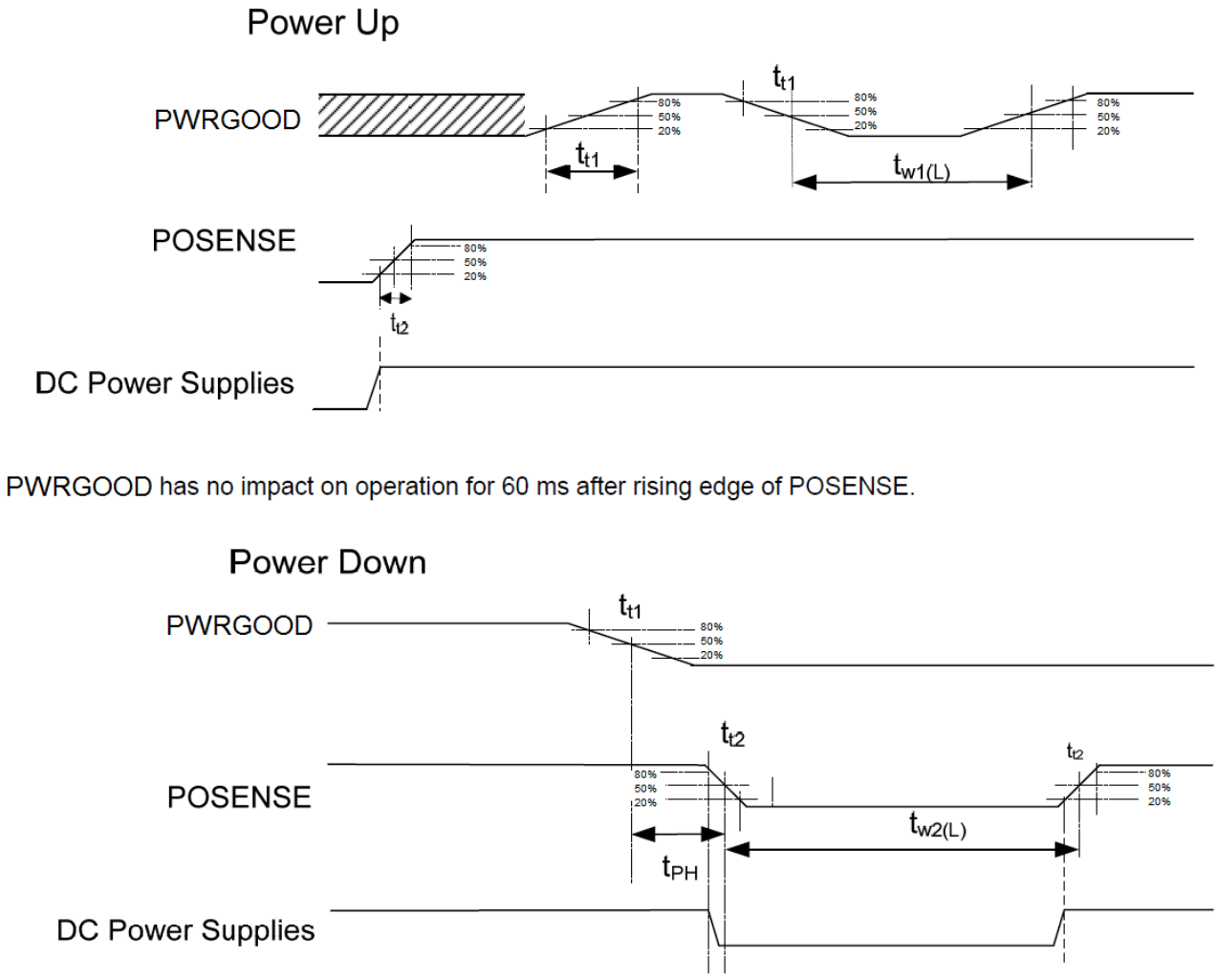


Figure 24. Power-Up/Down Timing

Power-On Sense (POSENSE) Support

It is difficult to set up a power monitor to trip exactly on the DLPC350 minimum supply voltages specifications. Thus, it is recommended that the external power monitor generating POSENSE target its threshold to 90% of the minimum supply voltages and ensure that POSENSE remain low for a sufficient amount of time to allow all supply voltages to reach minimum controller requirements and stabilize. Note that the trip voltage for detecting the loss of power is not critical for POSENSE and thus may be as low as 50% of rated supply voltages. In addition, the reaction time to respond to a low voltage condition is not critical for POSENSE. INIT_DONE has much more critical requirements in these areas.

Power-Good (PWRGOOD) Support

The PWRGOOD signal is defined to be an early warning signal that should alert the controller 500 µs before DC supply voltages have dropped below specifications. This allows the controller time to park the DMD, ensuring the integrity of future operation. It is recommended that monitor sensing PWRGOOD be on the input side of the supply regulators.

5V Tolerant Support

With the exception of USB_DAT, the DLPC350 does not support any other 5V tolerant I/O.

Power Reset Operation

Immediately following a power-up event, the DLPC350 hardware will automatically bring up the Master PLL and place the controller in NORMAL power mode. It will then follow the standard System Reset procedure (see next section).

System Reset Operation

Immediately following any type of system reset (power-up reset, PWRGOOD reset, etc.), the DLPC350 will automatically return to NORMAL power mode and return to the following state:

- All GPIO will tri-state and as a result all GPIO controlled voltage switches will default to enabling power to all the DLPC350 supply lines (assuming that these outputs are externally pulled-high).
- The Master PLL will remain active (it is only reset on a power-up reset) and most of the derived clocks will be active. However, only those resets associated with the internal processor and its peripherals will be released.
- The internal processor associated clocks will default to their full clock rates, as boot-up occurs at full speed).
- The PLL feeding the DDR DMD Interface (PLLD) will default to its Power Down mode, and all derived clocks will be inactive with the corresponding resets asserted.
- The DMD interface (except $\overline{\text{DMD\_DRC\_OE}}$) will default its outputs to a logic low state. $\overline{\text{DMD\_DRC\_OE}}$ will default to tri-state, but should be pulled high via an external 30KΩ to 51KΩ pull-up resistor on the PCB.
- All resets outputted by the DLPC350 will remain asserted until released by the internal processor (after boot-up).
- The DLPC350 will boot-up from external Flash. After the DLPC350 boots, it will:
  - Configure the programmable DDR Clock Generator (DCG) clock rates (i.e. the DMD LPDDR interface rate).
  - Enable the DCG PLL (PLLD) while holding the divider logic in reset.
  - Once the DCG PLL locks, the firmware will set the DMD clock rates.
  - The DLPC350 firmware will then release the DCG divider logic resets, which in turn, will enable all derived DCG clocks.
- After the clocks are configured, an Internal Memory Test is performed. See Figure 25 and note that GPIO26 is the INIT_DONE signal.

Application software should wait for a wake-up command from the user. Once the controller is requested to "wake-up," the software should place the controller back in NORMAL mode and re-initialize clocks and resets as required.

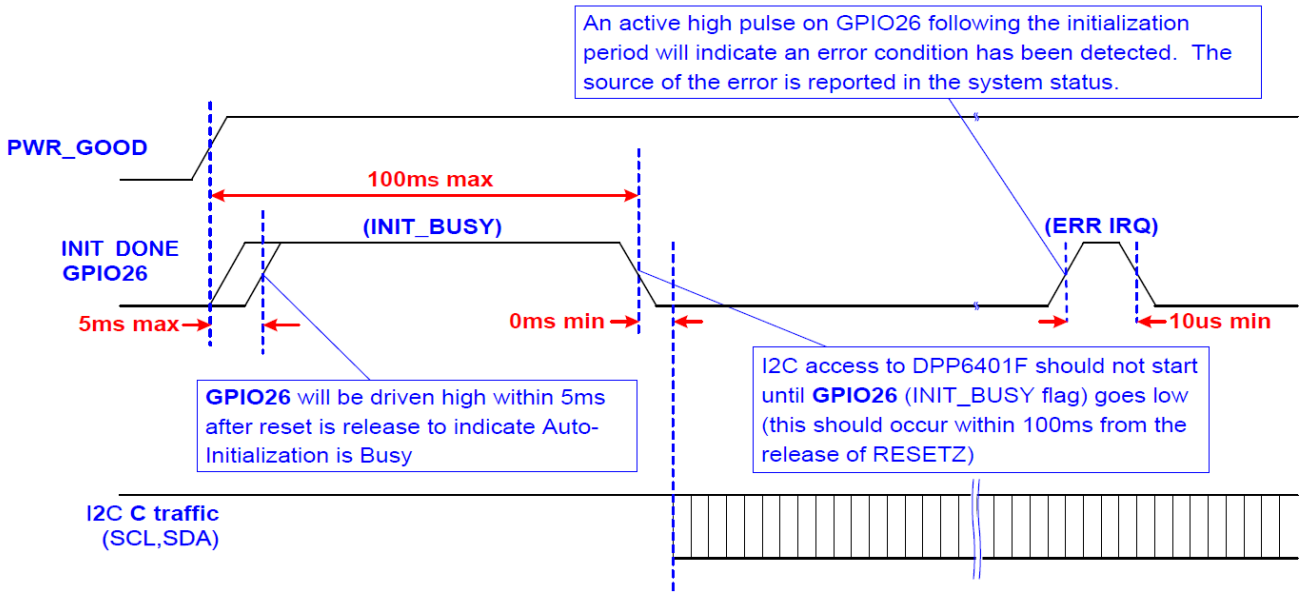


Figure 25. Internal Memory Test Diagram

Table 16. Reset Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w1(L)}$	Pulse duration, inactive low, PWRGOOD	50% reference points	4		µs
t_{t1}	Transition time, PWRGOOD	20% to 80% reference points		625	µs
$t_{w2(L)}$	Pulse duration, inactive low, POSENSE	50% reference points	500		µs
t_{t2}	Transition time, POSENSE	20% to 80% reference points		1	µs
t_{PH}	Power hold time, POSENSE remains active after PWRGOOD is de-asserted	20% to 80% reference points	500		µs

General PCB Recommendations

General Handling Guidelines for CMOS-type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended that unused input pins be tied through a pull-up resistor to its associated power supply, or a pull-down to ground. For inputs with internal pull-up or pull-down resistors, it is unnecessary to add an external pull-up or pull-down unless specifically recommended. Note that internal pull-up and pull-down resistors are weak and should not be expected to drive the external line.

Bi-directional pins are configured as inputs as a reset default.

Unless specifically specified, pull-up and pull-down resistors can be 10 kΩ.

Unused output-only pins can be left open.

Program Memory Flash Interface

The DLPC350 provides two external program memory chip selects.

- $\overline{\text{PM\_CS\_1}}$ - mandatory CS for Boot Flash device (Standard "NOR" Flash ≤ 128 Mb)
- $\overline{\text{PM\_CS\_2}}$ - available for optional Flash device (≤ 128 Mb)

The Flash access timing is software programmable up to 31 wait states. Wait state resolution is 6.7 nanoseconds in normal mode, and 53.57 nanoseconds in low power modes. To calculate the wait state values:

Wait State Value = Device Access Time ÷ Wait State Resolution

where the Wait State Value is rounded up. This equation assume a maximum single direction trace length of 75 mm. When another device such as an additional Flash is used in conjunction with the Boot Flash, stub lengths must be kept short and located as close as possible to the Flash end of the route.

The DLPC350 provides enough Program Memory address pins to support a flash device up to 128 Mb. There are two bi-directional pins (PM_ADDR_22 and PM_ADDR_21) that can be programmed as additional address pins once the software configures them. Enabling PM_ADDR_21 increases the Flash size from 32 Mb to 64 Mb. Enabling PM_ADDR_22 as well as PM_ADDR_21 increases the Flash size to 128 Mb. If these pins are used, then they require board-level pull-down resistors to prevent the Flash address bits from floating.

Thermal Considerations

The underlying thermal limitation for the DLPC350 is that the maximum operating junction temperature (T_J) must not be exceeded (see Recommended Operating Conditions). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC350, and power dissipation of surrounding components. The DLPC350 package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

Table 17. Thermal Characteristics

PARAMETER		MAXIMUM VALUE	UNITS
$R_{\theta JC}$ (1)	Thermal Resistance, Junction to Case	6.6	°C/W
$R_{\theta JA}$ at 0 m/s of forced airflow (2)	Thermal Resistance, Junction to Air	19.4	°C/W
$R_{\theta JA}$ at 1 m/s of forced airflow (2)	Thermal Resistance, Junction to Air	16.7	°C/W
$R_{\theta JA}$ at 2 m/s of forced airflow (2)	Thermal Resistance, Junction to Air	15.8	°C/W
Psi-jt (3)	Temperature variance from junction to package top center temperature, per unit power dissipation.	0.33	°C/W

(1) $R_{\theta JC}$ analysis assumptions: The heat generated in the chip flows both into over-mold (top side) and into the package laminate (bottom side) and then into the PCB via package solder balls. This should be used for heat sink analysis only.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC350 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different , it is the best information available during the design phase to estimate thermal performance.
(3) Example: (3 W) x (0.33 °C/W) = approximately a 1.00°C temperature rise.

Recommended MOSC Crystal Oscillator Configuration

The DLPC350 requires an external reference clock to feed its internal PLL. This reference may be supplied via a crystal or oscillator. The DLPC350 accepts a reference clock of 32 MHz with a maximum frequency variation of 100 ppm (including aging, temperature and trim component variation). When a crystal is used, several discrete components are also required as shown in Figure 26.

C_L = Crystal load capacitance (Farads)
$C_{L1} = 2 * (C_L - C_{Stray\text{-}MOSC})$
$C_{L2} = 2 * (C_L - C_{Stray\text{-}MOSCN})$
$C_{Stray\text{-}MOSC}$ = Sum of Package & PCB capacitance at the crystal pin associated with ASIC signal MOSC.
$C_{Stray\text{-}MOSCN}$ = Sum of Package & PCB capacitance at the crystal pin associated with ASIC signal MOSCN.

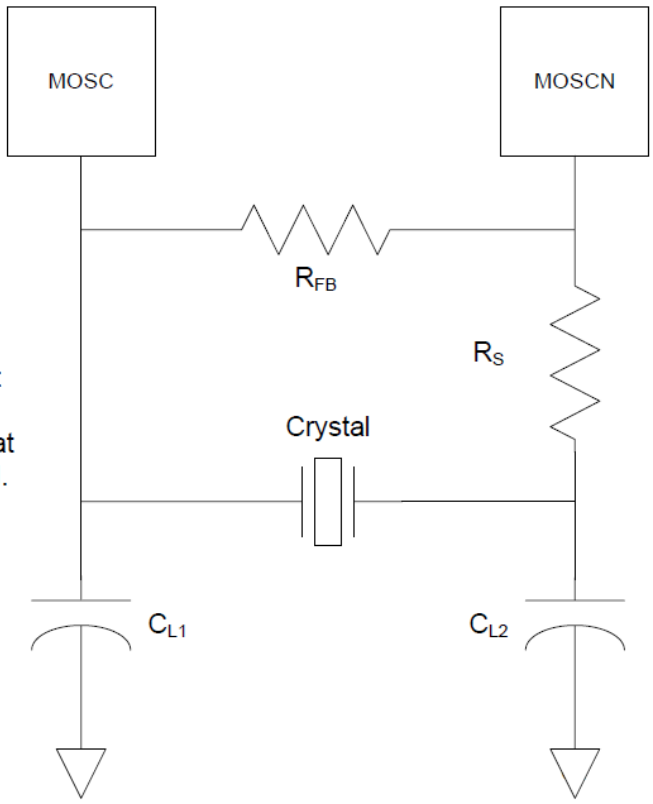


Figure 26. Recommended Crystal Oscillator Configuration

Table 18. Crystal Port Electrical Characteristics

PARAMETER	NOM	UNIT
MOSC TO GND capacitance	3.9	pF
MOSCN TO GND capacitance	3.8	pF

Table 19. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	32	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±100	PPM
Crystal equivalent series resistance (ESR)	50 max	Ω
Crystal load	10	pF
Crystal shunt load	7 max	pF
Crystal frequency temperature stability	±30	PPM
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor (MOSC)	Typical Drive Level with TCX9C3207001 crystal (ESRmax = 30Ω) = 160 µW. See Figure 26	pF
C_{L2} external crystal load capacitor (MOSCN)	Typical Drive Level with TCX9C3207001 crystal (ESRmax = 30Ω) = 160 µW. See Figure 26	pF
PCB layout	A ground isolation ring around the crystal is recommended	

If an external oscillator is used, then the oscillator output must drive the MOSC pin on the DLPC350 controller, and the MOSCN pin should be left unconnected. The benefit of an oscillator is that it can be made to provide a spread-spectrum clock that reduces EMI. Note, however, that the DLPC350 can only accept 0%, ±0.5%, and ±1.0% (center-spread modulation), and a triangular waveform.

Similar to the crystal option, the oscillator input frequency is limited to 32 MHz.

It is assumed that the external crystal or oscillator stabilizes within 50 ms after stable power is applied.

PLL

The following guidelines are recommended to achieve desired controller performance relative to the internal PLLs.

The DLPC350 contains two PLLs (PLLM and PLLD), each of which have dedicated 1.2V digital and 1.8V analog supply. These 1.2V PLL pins should be individually isolated from the main 1.2V system supply via a ferrite bead. The impedance of the ferrite bead should be much greater than the capacitor at frequencies where noise is expected. The impedance of the ferrite bead must also be less than 0.5Ω in the frequency range of 100-300KHz and greater than 10Ω at frequencies greater than 100MHz.

As a minimum, the 1.8V analog PLL power and ground pins should be isolated using an LC filter with a ferrite bead serving as the inductor and a 0.1µF capacitor on the DLPC350 side of the ferrite bead. It is recommended that this 1.8V PLL power be supplied from a dedicated linear regulator and each PLL should be individually isolated from the regulator. The same ferried recommendations described for the 1.8V analog PLL supply apply to the 1.2V digital PLL supply.

When describing the overall supply filter network, care must be taken to ensure that no resonances occur. Particular care must be taken in the 1-2MHz band, as this coincides with the PLL natural loop frequency.

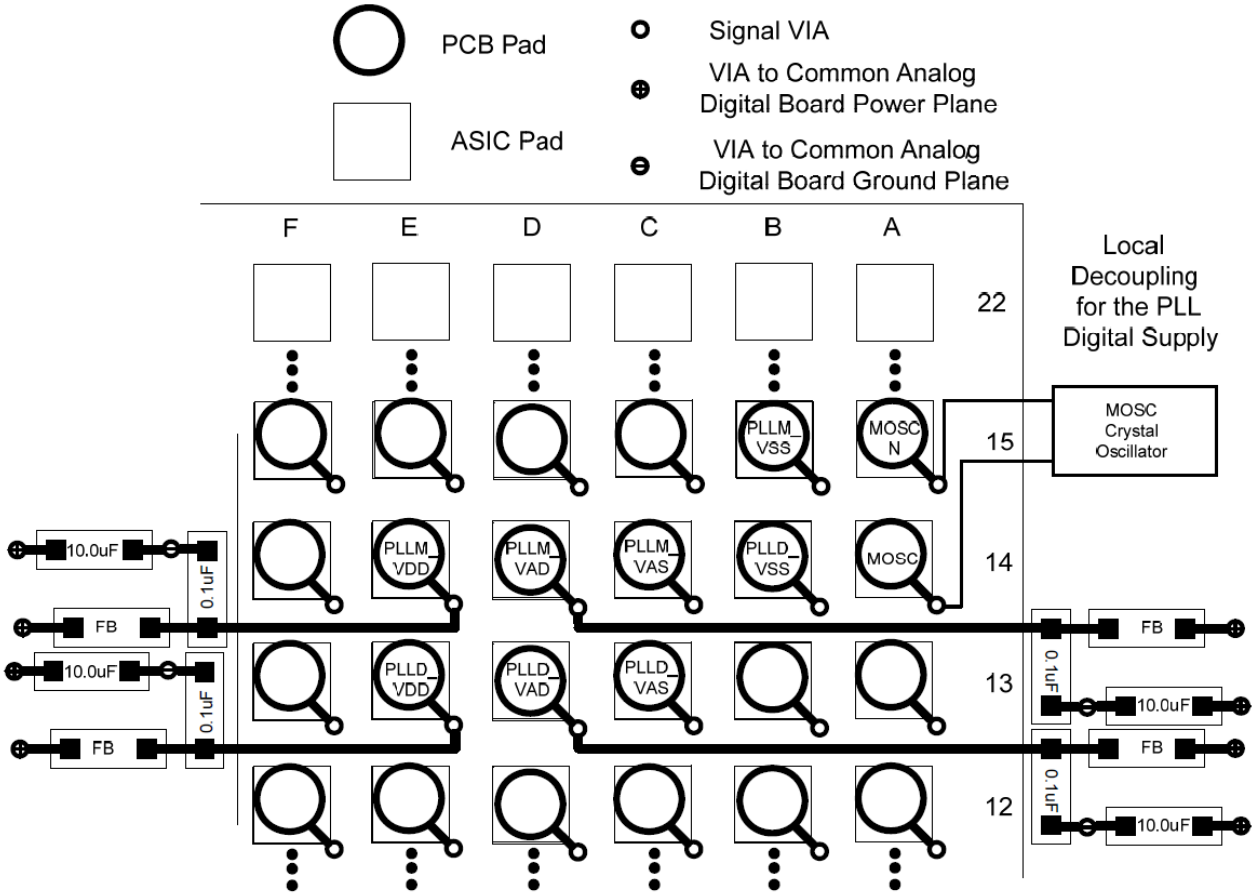


Figure 27. PLL Filter Layout

High frequency decoupling is required for both 1.2V and 1.8V PLL supplies and should be provided as close as possible to each of the PLL supply package pins. It is recommended that decoupling capacitors be placed under the package on the opposite side of the board. High quality, low-ESR, monolithic, surface mount capacitors should be used. Typically 0.1 µF for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting and thus, where possible, there should be no trace, allowing the via to butt up against the land itself. Additionally the connecting trance should be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design. Typically a good ceramic capacitor in the 10 µF range is adequate.

Board Level Test Support

The In-Circuit Tri-State Enable signal (ICTSEN) is a board level test control signal. By driving ICTSEN to a logic high state, all controller outputs (except TDO1) will be 3-stated.

The DLPC350 also provides JTAG boundary scan support on all I/O signals, non-digital I/O and a few special signals. The table below defines these exceptions.

Table 20. Signals Not Covered by JTAG

Signal Name	PKG Ball
USB_DAT_N	E3
USB_DAT_P	E2
HW_TEST_EN	V7
VPGM	D17
EXRES	A3
MOSC	A14
MOSCN	A15
RA_IN_P	AB10
RA_IN_N	AA10
RB_IN_P	Y11
RB_IN_N	W11
RC_IN_P	AB12
RC_IN_N	AA12
RD_IN_P	Y13
RD_IN_N	W13
RE_IN_P	AB14
RE_IN_N	AA14
RCK_IN_P	Y9
RCK_IN_N	W9

REVISION HISTORY

Changes from Original (April 2013) to Revision A — **Page**

- Changed the device From: Preview To: Production 1

Changes from Revision A (May 2013) to Revision B — **Page**

- Added PIB_CLK and P1C_CLK to Table 2 12
- Deleted $\overline{\text{PM\_CS\_0}}$ from FLASH INTERFACE in Table 2 15
- Deleted Y16 and AB17 from the RESERVED PINS list in Table 2 18
- Added $\overline{\text{PM\_CS\_0}}$ to the RESERVED PINS LIST in Table 2 18
- Deleted "PM_CS_0 - available for optional Flash device (≤ 128 Mb)" From the Program Memory Flash Interface section 43

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC350ZFF	ACTIVE	BGA	ZFF	419	5	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

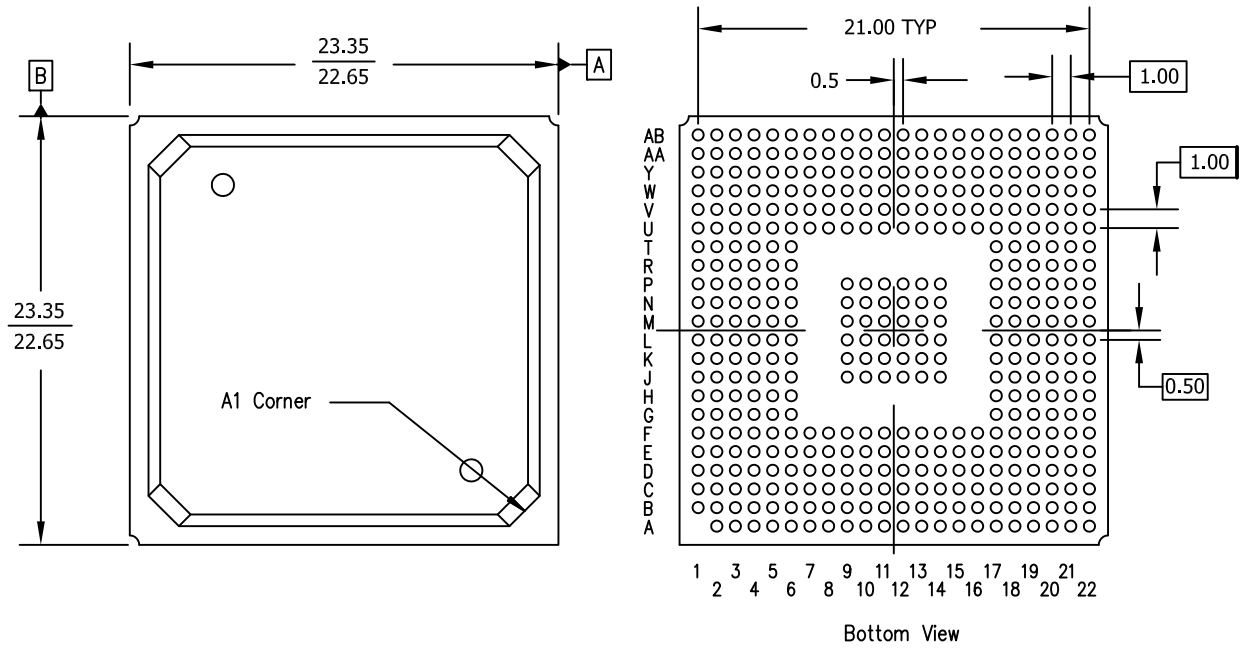
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

ZFF (S–PBGA–N419) PLASTIC BALL GRID ARRAY



4218205/A 11/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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