DLPC350
DLP4500
DLP® 0.45 WXGA Chip Set

Data Manual

Literature Number: DLPU009A
April 2013–Revised May 2013

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DLP® 0.45 WXGA Chip Set

Check for Samples: DLPC350, DLP4500

1 Introduction

1.1 Features

- Enables High-Performance Optical Imaging With DMD
  - 0.45-Inch (11.43-mm) Micromirror Diagonal Array
  - 1140 × 912 Array of Aluminum Micromirrors, 7.6-µm Pitch
  - ±12° Micromirror Tilt Angle
  - Side Illumination for Optimized Efficiency
  - Highly Efficient in Visible Light (420 nm–700 nm):
    - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
    - Micromirror Reflectivity, 89.4%
    - Array Diffraction Efficiency, 86%
    - Array Fill Factor, 92%
- Multi-Mode, 30-Bit Input Port:
  - Supports Parallel RGB With Pixel Clock up to 150 MHz
  - Four demodulated pixel mapped modes supported for 8, 9, 10 YUV, YCrCb, or RGB formatted input
- Pattern Input Mode
  - One-to-One Mapping of Input Data to Micromirrors
  - 1-Bit Binary Pattern Rates up to 4225-Hz
  - 8-Bit Grayscale Pattern Rates up to 120-Hz
- Video Input Mode with Pixel Data Processing
  - Supports 10Hz to 120Hz Frame Rates
  - Programmable Degamma
  - Spatial-Temporal Multiplexing (Dithering)
  - Programmable Color Coordinate Adjustment
  - Programmable Color Space Conversion
- Two Input/Output Trigger Signals each for Synchronizing with Camera, Sensor, or Other Peripherals
- External Memory Support:
  - Parallel Flash with access time of 70 ns
- Solid-State Illumination Interface (LED):
  - Supports Three Independent Channels, that is, Red, Green, and Blue LEDs
- System Control:
  - I^2C Interface for Device Control
  - Programmable Splash Screens
  - Programmable LED Current and Sync Control
  - Integrated DMD Reset Driver Circuitry to Simplify System Design

1.2 Applications

- Machine Vision
- Industrial Inspection
- 3D Scanning
- 3D Optical Metrology
- Automated Fingerprint Identification
- Facial Recognition
- Augmented Reality
- Interactive Display
- Information Overlay
- Spectroscopy
- Chemical Analyzers
- Medical Instruments
- Photo-Stimulation
- Virtual Gauges

1.3 Purpose

This document provides a description of the 0.45 WXGA chip set components and function, interconnect information for the individual chip set components, and system-level design guidelines to ensure proper function of the 0.45 WXGA chip set components.

1.4 Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP4500 0.45 WXGA DMD Data Sheet	DLPS028
DLPC350 Digital Controller for the DLP4500 Data Sheet	DLPS029
DLPC350 Programmer's Guide	DLPU010

2 Glossary

DDR	Double data rate
LVDS	Low-voltage differential signaling
DLP®	Digital light processing
DMD	Digital micromirror device
DVI	Digital video interface
WXGA	Wide XGA (extended graphics array)
PWM	Pulse width modulation
USB	Universal serial bus
I^2C	Inter-Integrated circuit bus, multi-master serial communication bus invented by Philips
RGB	Red, green, and blue
PCB	Printed circuit board

3 Device Description

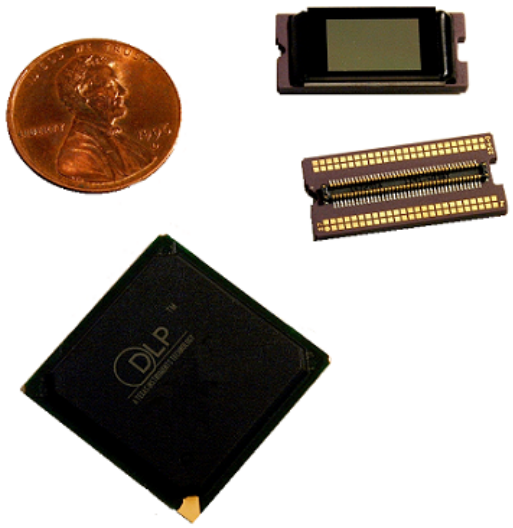

Figure 3-1. Chip Set Relative Size

The DLP 0.45 WXGA chip set consists of two individual components:

- DLP4500 – 0.45 WXGA FQE, FQD DMD
- DLPC350 – DLP4500 controller

Plus an additional component:

- Parallel configuration flash loaded with the DLPC350 Configuration and Support Firmware

Detailed specifications for the components can be found in the individual component data sheets.

Figure 3-2 illustrates the connectivity between the individual components in the chip set, which include the following internal chip set interfaces:

- DLPC350 to DLP4500 data and control interface (DMD pattern data)
- DLPC350 to DLP4500 micromirror array reset control interface
- DLPC350 to Parallel flash

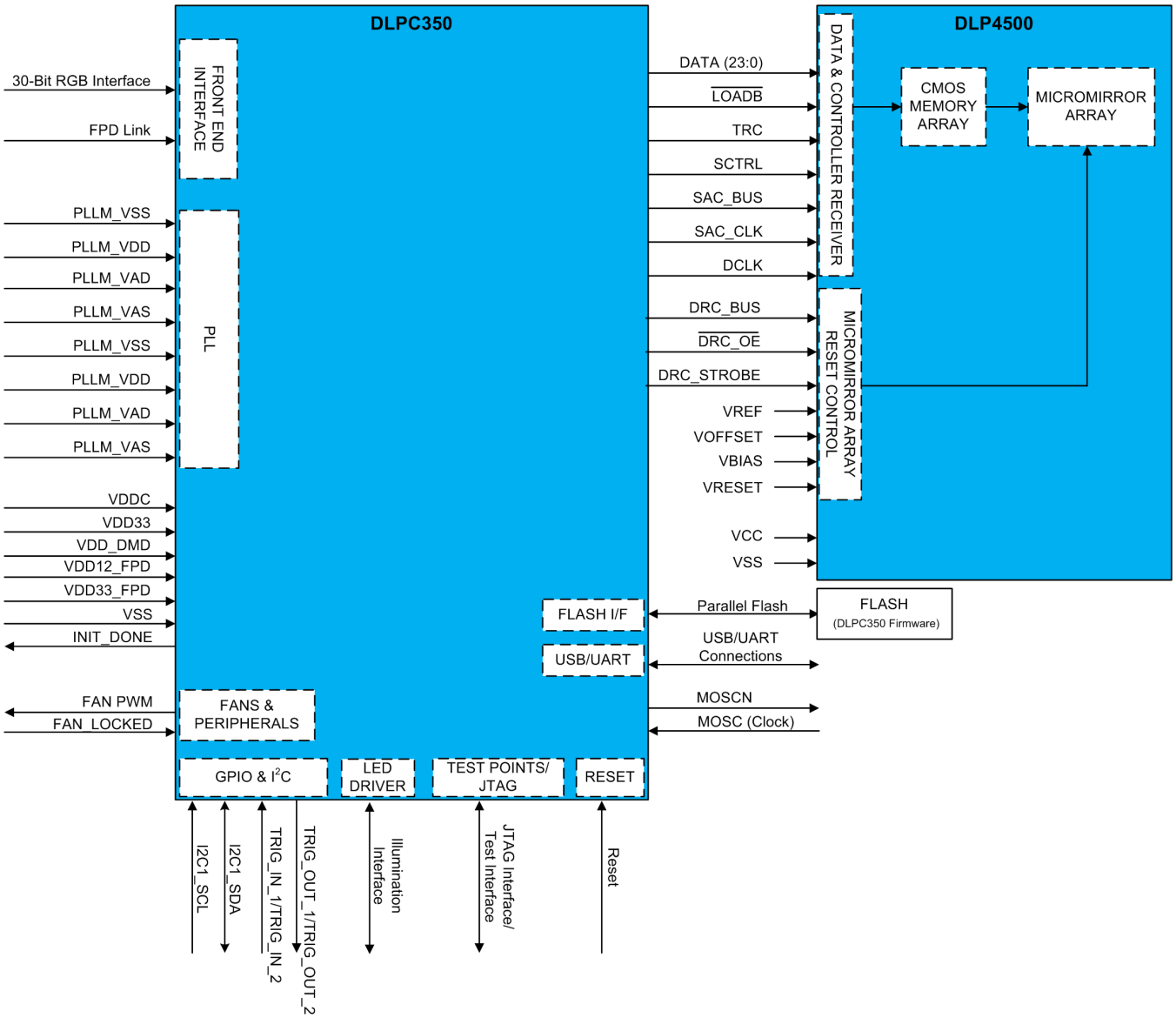

Figure 3-2. Chip Set Block Diagram

Figure 3-3 illustrates the connectivity between the chip set and other key system-level components, which include the following external chip set interfaces:

- System Input Interface, consisting of:
  - 30-bit data bus (P1_[A, B, C]_[9:0])
  - Vertical sync signal (P1_VSYNC)
  - Horizontal sync signal (P1_HSYNC)
  - Data valid signal (P1_DATAEN)
  - Data clock signal (P1A_CLK)

- Control Interface, consisting of:
  - I^2C signals (I2C1_SCL and I2C1_SDA)
  - USB 1.1 signals (USB_DAT_N, USB_DAT_P. USB_ENZ)
  - Power Good signal (PWRGOOD)
  - Power-On Sense signal (POSENSE)
  - Power On/Off signal (POWER_ON_OFF)
  - External Power On signal (EXT_PWR_ON)
  - Oscillator signals (MOSC, MOSCN)
- Parallel configuration flash interface
- Illumination driver control interface

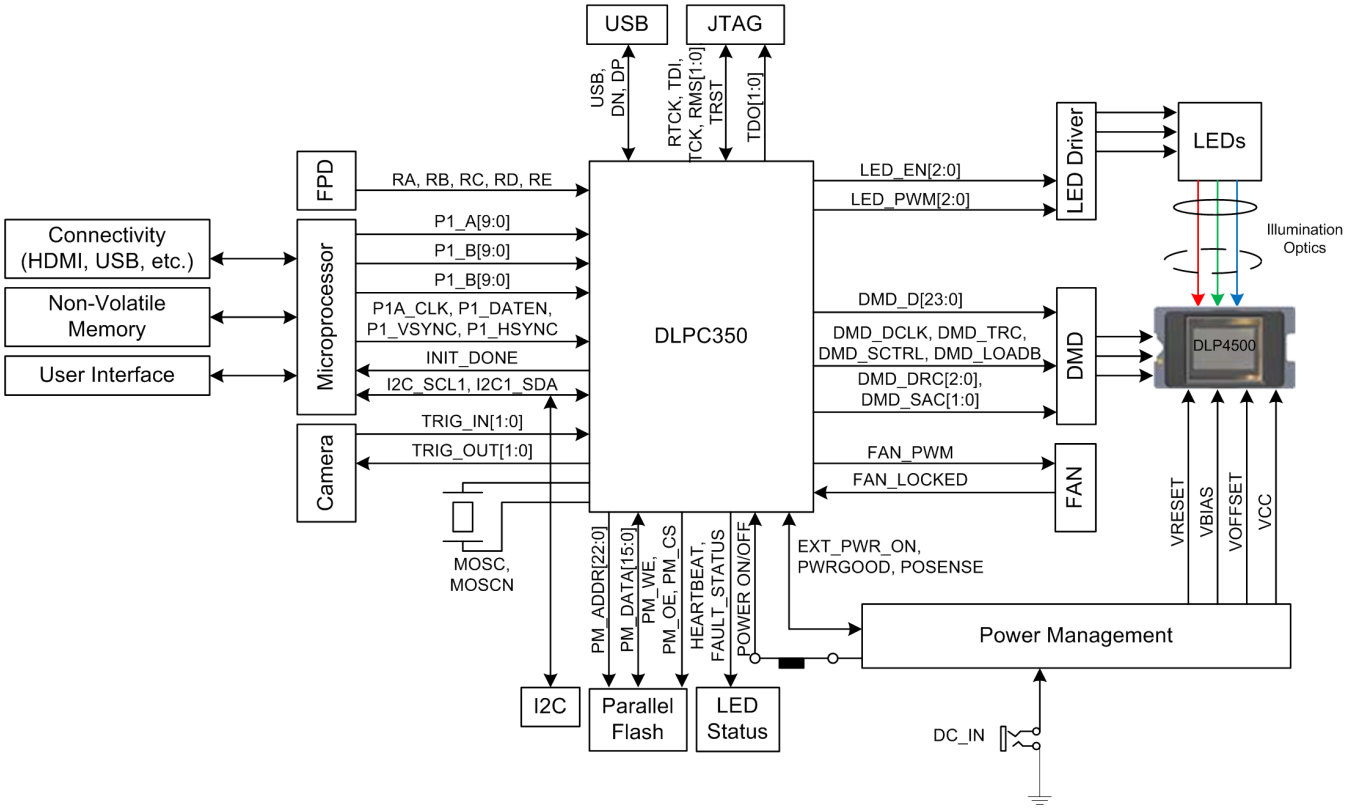

Figure 3-3. System Block Diagram

4 Control Interface

The 0.45 WXGA chip set is supported by a set of I^2C or USB commands to control its operation. The I^2C or USB commands allow users to control in real-time or configure the 0.45 WXGA chip set. For example, the I^2C or USB commands have functions to set the LED drive current or display splash screens stored in the external flash memory.

For more details about the specific functions and features, see the *DLPC350 Programmers Guide*, TI literature number DLPU010. Other related documents are listed in Section 1.4.

5 System Input Interfaces

The 0.45 WXGA chip set supports a 30-bit parallel RGB interface for image data transfers from another device and a 30-bit interface for video data transfers. The system input also requires proper generation of the PWRGOOD and POSENSE inputs to ensure reliable operation.

See the DLPC350 data sheet (TI literature number DLPS029) for detailed specifications for each of the following interfaces.

5.1 Data Interface

The data interface has two components: a Parallel RGB input port and an FPD-Link LVDS input port. Both components can support up to 30 bits and have a nominal I/O voltage of 3.3V. Maximum and minimum input timing specifications for both components are provided in the Interface Timing Requirements of the DLPC350 data sheet.

The parallel RGB port can support up to 30 bits in video mode. In pattern mode, the upper 8-bits of each color are used to convert the 30-bit input into a 24-bit RGB input.

The FPD-Link input port can be configured to connect to a video decoder device or an external processor through a 24- 27- or 30-bit interface. The mapping of the red-, green-, and blue-channel data bits is shown in Table 5-2.

Table 5-1 provides a description of the signals associated with the data interface.

Table 5-1. Active Signals – Data Interface

SIGNAL NAME	DESCRIPTION
RGB Parallel Interface	
P1_(A, B, C)_[0:9]	30-bit data inputs 10 bits for each of the red, green, and blue channels). If interfacing to a system with less than 10-bits per color, connect the bus of the red, green, and blue channels to the upper bits of the DLPC350 10-bit bus.
P1A_CLK	Pixel clock; all input signals on data interface are synchronized with this clock.
P1_VSYNC	Vertical sync
P1_HSYNC	Horizontal sync
P1_DATAEN	Input data valid
FPD-Link LVDS Input	
RCK	Differential input signal for Clock
RA_IN	Differential input signal for data channel A
RB_IN	Differential input signal for data channel B
RC_IN	Differential input signal for data channel C
RD_IN	Differential input signal for data channel D
RE_IN	Differential input signal for data channel E

The A, B, and C input data channels of Port 1 can also be internally swapped for optimum board layout. The mapping for Port 2 (FPD-Link) is shown in Table 5-2.

Table 5-2. (LVDS) Receiver Supported Pixel Mapping Modes

LVDS Receiver Input	Mapping Selection 1	Mapping Selection 2	Mapping Selection 3	Mapping Selection 4 (18-bit Mode)
RA Input Channel				
RDA(6)	map to GRN(4)	map to GRN(2)	map to GRN(0)	map to GRN(4)
RDA(5)	map to RED(9)	map to RED(7)	map to RED(5)	map to RED(9)
RDA(4)	map to RED(8)	map to RED(6)	map to RED(4)	map to RED(8)
RDA(3)	map to RED(7)	map to RED(5)	map to RED(3)	map to RED(7)
RDA(2)	map to RED(6)	map to RED(4)	map to RED(2)	map to RED(6)
RDA(1)	map to RED(5)	map to RED(3)	map to RED(1)	map to RED(5)
RDA(0)	map to RED(4)	map to RED(2)	map to RED(0)	map to RED(4)
RB Input Channel				
RDB(6)	map to BLU(5)	map to BLU(3)	map to BLU(1)	map to BLU(5)
RDB(5)	map to BLU(4)	map to BLU(2)	map to BLU(0)	map to BLU(4)
RDB(4)	map to GRN(9)	map to GRN(7)	map to GRN(5)	map to GRN(9)
RDB(3)	map to GRN(8)	map to GRN(6)	map to GRN(4)	map to GRN(8)
RDB(2)	map to GRN(7)	map to GRN(5)	map to GRN(3)	map to GRN(7)
RDB(1)	map to GRN(6)	map to GRN(4)	map to GRN(2)	map to GRN(6)
RDB(0)	map to GRN(5)	map to GRN(3)	map to GRN(1)	map to GRN(5)
RC Input Channel				
RDC(6)	map to DEN			
RDC(5)	map to VSYNC			
RDC(4)	map to HSYNC			
RDC(3)	map to BLU(9)	map to BLU(7)	map to BLU(5)	map to BLU(9)
RDC(2)	map to BLU(8)	map to BLU(6)	map to BLU(4)	map to BLU(8)
RDC(1)	map to BLU(7)	map to BLU(5)	map to BLU(3)	map to BLU(7)
RDC(0)	map to BLU(6)	map to BLU(4)	map to BLU(2)	map to BLU(6)
RD Input Channel				
RDD(6)	map to Field (option 1 if available)			
RDD(5)	map to BLU(3)	map to BLU(9)	map to BLU(7)	NO MAPPING
RDD(4)	map to BLU(2)	map to BLU(8)	map to BLU(6)	NO MAPPING
RDD(3)	map to GRN(3)	map to GRN(9)	map to GRN(7)	NO MAPPING
RDD(2)	map to GRN(2)	map to GRN(8)	map to GRN(6)	NO MAPPING
RDD(1)	map to RED(3)	map to RED(9)	map to RED(7)	NO MAPPING
RDD(0)	map to RED(2)	map to RED(8)	map to RED(6)	NO MAPPING
RE Input Channel				
RDE(6)	map to Field (option 2 if available)			
RDE(5)	map to BLU(1)		map to BLU(9)	NO MAPPING
RDE(4)	map to BLU(0)		map to BLU(8)	NO MAPPING
RDE(3)	map to GRN(1)		map to GRN(9)	NO MAPPING
RDE(2)	map to GRN(0)		map to GRN(8)	NO MAPPING
RDE(1)	map to RED(1)		map to RED(9)	NO MAPPING
RDE(0)	map to RED(0)		map to RED(8)	NO MAPPING

5.2 Control Interface

The 0.45 WXGA chip set supports I^2C or USB commands through the control interface. The control interface allows another master processor to send commands to the 0.45 WXGA chip set to query system status or perform real-time operations, such as, LED driver current settings. The DLPC350 offers two different sets of slave addresses. The I2C_ADDR_SEL pin provides the ability to select an alternate set of 7-bit I^2C slave address only during power-up. If I2C_ADDR_SEL is low, then the DLPC350 slave addresses are 0x34 and 0x35. If I2C-ADDR_SEL is high, then the DLPC350 slave address is 0x3A and 0x3B. This signal will also change the serial number for the USB device so that two DLPC350s can be connected to one computer via USB. Once the system initialization is complete, this pin will be available for as a GPIO. See the *DLPC350 Programmer's Guide* (TI literature number DLPU010) for detailed information about these operations.

Table 5-3 provides a description for active signals used by the DLPC350 to support the I^2C interface.

Table 5-3. Active Signals – I^2C Interface

SIGNAL NAME	DESCRIPTION
I2C1_SCL	I^2C clock. Bidirectional open-drain signal. I^2C slave clock input from the external processor.
I2C1_SDA	I^2C data. Bidirectional open-drain signal. I2C slave to accept command or transfer data to and from the external processor.
I2C0_SCL	I^2C Bus 0, Clock; I^2C master for on-board peripherals.
I2C0_SDA	I^2C Bus 0, Data; I^2C master for on-board peripherals.

6 System Output Interfaces

There are two primary output interfaces: illumination driver control interface and sync outputs.

6.1 Illumination Interface

An illumination interface is provided that supports up to a three (3) channel LED driver.

The illumination interface provides signals that support: LED driver enable, LED enable, LED enable select, and PWM signals to control the LED current. Table 6-1 describes the active signals for the illumination interface.

Table 6-1. Active Signals – Illumination Interface

SIGNAL NAME	DESCRIPTION
HEARTBEAT	LED blinks continuously to indicate system is running fine.
FAULT_STATUS	LED off indicates system fault
LEDR_EN	Red LED enable
LEDG_EN	Green LED enable
LEDB_EN	Blue LED enable
LEDR_PWM	Red LED PWM signal used to control the LED current
LEDG_PWM	Green LED PWM signal used to control the LED current
LEDB_PWM	Blue LED PWM signal used to control the LED current

6.2 Trigger Interface (Sync Outputs)

The DLPC350 outputs a trigger signal for synchronizing displayed patterns with a camera, sensor, or other peripherals.

The sync output supporting signals are: horizontal sync, vertical sync, two input triggers, and two output triggers. Depending on the application, these signals control how the pattern is displayed. More information about trigger modes and the corresponding signals can be found in the controller data sheet (TI literature number DLPS029).

Table 6-2. Active Signals – Sync Output

SIGNAL NAME	DESCRIPTION
P1_HSYNC	Horizontal Sync
P1_VSYNC	Vertical Sync
TRIG_IN_1	Advances the pattern display or displays two alternating patterns, depending on the mode
TRIG_IN_2	Pauses the pattern display or advances the pattern by two, depending on the mode
TRIG_OUT_1	Active high during pattern exposure
TRIG_OUT_2	Active high to indicate first pattern display

7 System Support Interfaces

There are two system support interfaces provided by the 0.45 WXGA chip set:

- System reference clock
- Parallel configuration non-volatile Flash

7.1 DLPC350 Reference Clock

The DLPC350 requires a 32-MHz 3.3-V external input from an oscillator. This signal serves as the 0.45 WXGA chip set reference clock from which the majority of the interfaces derive their timing. This includes DMD interfaces and serial interfaces.

See the DLPC350 data sheet (TI literature number DLPS029) for reference clock specifications.

7.2 Program Memory Flash Interface

The DLPC350 provides three external program memory chip selects.

- $\overline{\text{PM\_CS\_0}}$ - available for optional Flash device (≤ 128 Mb)
- $\overline{\text{PM\_CS\_1}}$ - mandatory CS for Boot Flash device (Standard "NOR" Flash ≤ 128 Mb)
- $\overline{\text{PM\_CS\_2}}$ - available for optional Flash device (≤ 128 Mb)

The Flash access timing is software programmable up to 31 wait states. Wait state resolution is 6.7 nanoseconds in normal mode, and 53.57 nanoseconds in the standby mode. (The modes are controlled by Power Control register 07h.) To calculate the wait state values:

Wait State Value = Device Access Time ÷ Wait State Resolution

where the Wait State Value is rounded up. This equation assumes a maximum single direction trace length of 75 mm. When an additional Flash is used in conjunction with the Boot Flash, stub lengths must be kept short and located as close as possible to the Flash end of the route.

The DLPC350 provides enough Program Memory address pins to support a Flash device up to 128 Mb. PM_ADDR_22 and PM_ADDR_21 are GPIO pins on reset, so they require board-level pull-down resistors to prevent the Flash address bits from floating during initial bootload.

8 DMD Interfaces

8.1 DLPC350 to DLP4500 Digital Data

The DLPC350 provides the pattern data to the DMD over a double data rate (DDR) interface.

Table 8-1 describes the signals used for this interface.

Table 8-1. Active Signals – DLPC350-to-DLP4500 Digital Data Interface

DLPC350 SIGNAL NAME	DLP4500 SIGNAL NAME
DMD_D(23:0)	DATA(23:0)
DMD_DCLK	DCLK

8.2 DLPC350-to-DLP4500 Control Interface

The DLPC350 provides the control data to the DMD over a serial bus.

Table 8-2 describes the signals used for this interface.

Table 8-2. Active Signals – DLPC350 to DLP4500 Control Interface

DLPC350 SIGNAL NAME	DLP4500 SIGNAL NAME	DESCRIPTION
DMD_SAC_BUS	SAC_BUS	DMD stepped-address control (SAC) bus data
DMD_SAC_CLK	SAC_CLK	DMD stepped-address control (SAC) bus clock
$\overline{\text{DMD\_LOADB}}$	$\overline{\text{LOADB}}$	DMD data load signal
DMD_SCTRL	SCTRL	DMD data serial control signal
DMD_TRC	TRC	DMD data toggle rate control

8.3 DLPC350-to-DLP4500 Micromirror Reset Control Interface

The DLPC350 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

Table 8-3 describes the signals used for this interface.

Table 8-3. Active Signals – DLPC350-to-DLP4500 Micromirror Reset Control Interface

DLPC350 SIGNAL NAME	DLP4500 SIGNAL NAME	DESCRIPTION
DMD_DRC_BUS	DRC_BUS	DMD reset control serial bus
$\overline{\text{DMD\_DRC\_OE}}$	$\overline{\text{DRC\_OE}}$	DMD reset control output enable
DMD_DRC_STRB	DRC_STRB	DMD reset control strobe

9 Printed Circuit Board (PCB) System Design Considerations for DMD Interface

The 0.45 WXGA chip set is a high-performance (high-frequency and high-bandwidth) set of components. This section provides PCB guidelines to help ensure proper operation of the 0.45 WXGA chip set.

The DLPC350 main board is a multi-layer PCB with primarily surface mount components on both sides. The majority of large surface mount components are placed on the top side of the PCB. Circuitry is primarily high speed digital logic. The high speed interfaces include:

- 120 MHz DDR interface from DLPC350 to DMD
- 150 MHz LVTTL interface from a video decoder to the DLPC350
- 150 MHz pixel clock supporting 30-bit Parallel RGB Interface
- LVTTL parallel memory interface between the DLPC350 controller and Flash with 70 ns access time
- LVDS Flat Panel Display port to DLPC350

The PCB should be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, Class 2.

9.1 Printed Circuit Board Design Guidelines

Table 9-1. PCB General Recommendations

DESCRIPTION	RECOMMENDATION
Configuration	Asymmetric dual stripline
Etch thickness (T)	1.0-oz. (1.2 mil thick) copper
Single-ended signal impedance	50 Ω (± 10%)
Differential signal impedance	100 Ω differential (± 10%)

9.2 Printed Circuit Board Layer Stackup Geometry

The PCB layer stack may vary depending on system design. However, careful attention is required in order to meet design considerations.

The DLPC350 PCB is targeted at six layers with layer stack up shown in Figure 9-1. Layers one and six should consist of the components layers. Low speed routing and power splits are allowed. Layer two should consist of a solid ground plane. Layer five should be a split voltage plane. Layers three and four should be used as the primary routing layers. Routing on external layers should be less than 0.25 inches for priority one and two signals. Refer to Table 9-7 for signal priority groups.

Board material should be FR-370HR or similar. PCB should be designed for lead-free assembly with the stackup geometry shown in Figure 9-1.

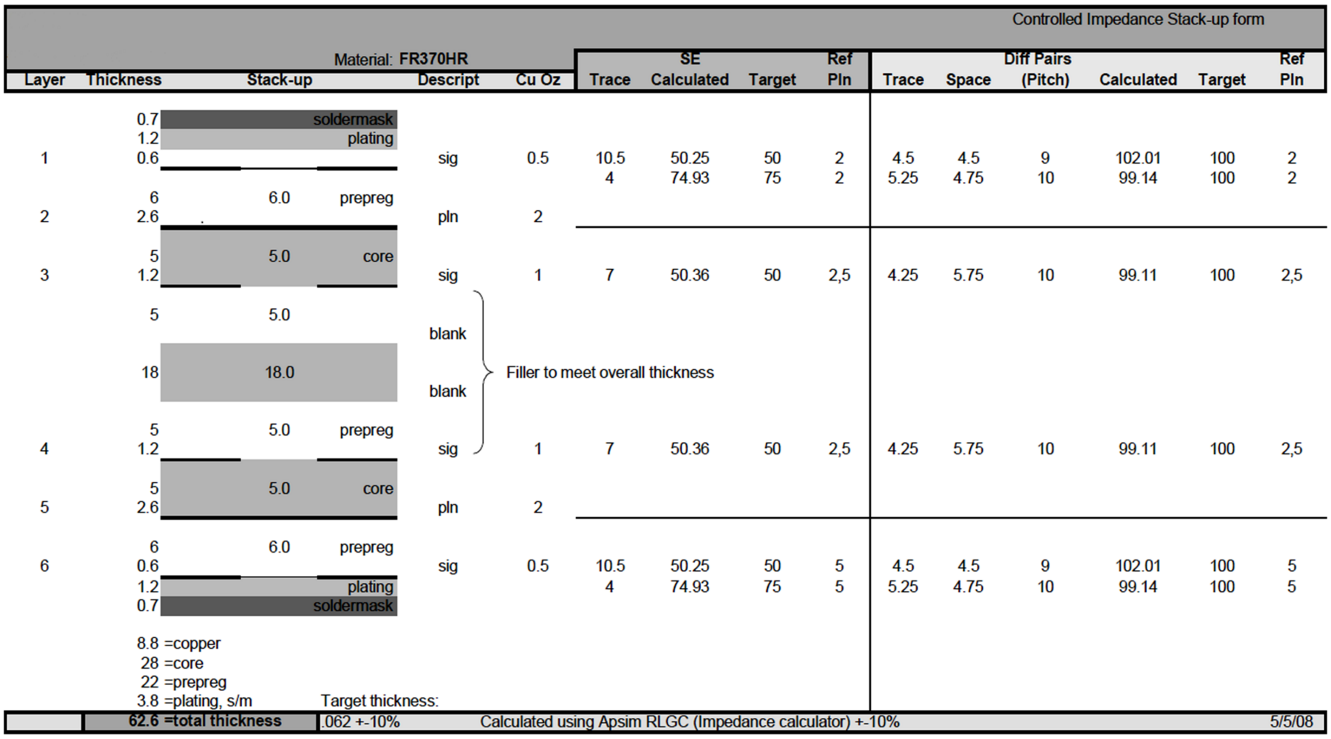

Figure 9-1. Layer Stackup

Table 9-2. PCB Layer Stackup Geometry

PARAMETER	DESCRIPTION	RECOMMENDATION
Reference plane 1	Ground plane for proper return	
Reference plane 2	1.9V DMD I/O power plane or ground	
Er	Dielectric FR4	4.3 at 1 GHz (nominal)
H1	Signal trace distance to reference plane 1	5 mil (0.127 mm)
H2	Signal trace distance to reference plane 2	30.4 mil

9.3 PCB Manufacturing

9.3.1 Power Planes

For best performance, TI recommends two power planes: one solid plane for ground (GND) and one split plane for other voltages with no signal routing on the power planes. Power and ground pins should be connected to these planes through a via for each pin. All device pin and via connections to these planes should use a thermal relief with a minimum of four spokes. Trace lengths for the component power and ground pins should be minimized to 0.03 inches or less. Vias should be spaced out to avoid forming slots on the power planes. High speed signals should not cross over a slot in the adjacent power planes. Prior to routing, vias connecting all the digital layers should be placed around the edge of the rigid PCB regions 0.03 inches from the board edges with 0.1 inch spacing. Placing extra vias is not required if there are sufficient ground vias due to normal ground connections of devices. All signal routing and signal vias should be inside the perimeter ring of ground vias.

9.3.2 Trace Widths and Minimum Spacings

For best performance, TI recommends the trace widths and minimum spacings shown in Table 9-3.

Table 9-3. Trace Widths and Minimum Spacings

SIGNAL NAME	TRACE WIDTH (inches)	MINIMUM TRACE SPACING (inches)
P1P2, P1P2V_PLLM, P1P2V_PLLD, P2P5V, P3P3V, P1P9V, A1P8V, A1P8V_PLLD, A1P8V_PLLM	0.02	0.010
VRST, VBIAS, VOFFSET	0.02	0.010
VSS (GND)	0.02	0.005
FANx_OUT	0.02	0.020
DMD_DCLK		0.030
P1A_CLK, P1B_CLK, P1C_CLK		0.030
MOSC, MOSCN		0.030

9.3.3 Decoupling Capacitors

The decoupling capacitors should be given placement priority. The supply voltage pin of the capacitor should be located close to the DLPC350 supply voltage pin(s). Decoupling capacitors should have two vias connecting the capacitor to ground and two vias connecting the capacitor to the voltage, but if the trace length is less than 0.05 inches, the device can be connected directly to the decoupling capacitor. The vias should be located on opposite sides of the long side of the capacitor, and those connections should be less than 0.05 inches as well.

9.4 Signal Layers

The PCB signal layers should follow typical good practice guidelines including:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first.

The PCB should have a solder mask on the top and bottom layers. The mask should not cover the vias.

- Except for fine pitch devices (pitch ≤ 0.032 inches), the copper pads and the solder mask cutout should be of the same size.
- Solder mask between pads of fine pitch devices should be removed.
- In the BGA package, the copper pads and the solder mask cutout should be of the same size.

9.5 Routing Constraints

In order to meet the specifications listed in the following tables, typically the PCB designer must route these signals manually (not using automated PCB routing software). In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Traces must be 0.1 inches from board edges when possible; otherwise they must be 0.05 inches minimum from the board edges. Avoid routing long traces all around the PCB. PCB layout assumes line spacing is twice the line width. However, three times the line width will reduce crosstalk and significantly help performance.

The maximum and minimum signal routing lengths include escape routing.

Table 9-4. Signal Length Routing Constraints for DMD Interface

SIGNALS	MINIMUM SIGNAL ROUTING LENGTH(1)	MAXIMUM SIGNAL ROUTING LENGTH(2)
DMD_D(23:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB,	2480 mil (63 mm)	2953 mil (75 mm)
DMD_OE, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	512 mil (13 mm)	5906 mil (150 mm)

(1) Signal lengths below the stated minimum will likely result in overshoot or undershoot.
(2) DMD-DDR maximum signal length is a function of the DMD_DCLK rate.

Each high-speed, single-ended signal should be routed in relation to its reference signal, such that a constant impedance is maintained throughout the routed trace. Avoid sharp turns and layer switching while keeping lengths to a minimum. The following signals should follow the signal matching requirements described in Table 9-5.

Table 9-5. High-Speed Signal Matching Requirements for DMD Interface

SIGNALS	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD_D(23:0), DMD_TRC, DMD_SCTRL, DMD_LOADB	DMD_DCLK	±200 (±5.08)	mil (mm)
DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_BUS, DMD_OE	DMD_SAC_CLK	±200 (±5.08)	mil (mm)

The above values apply to the PCB routing only. They do not include any internal package routing mismatch associated with the DLPC350 or the DLP4500. Additional margin can be attained if internal DLPC350 package skew is taken into account. Additionally, to minimize EMI radiation, serpentine routes added to facilitate matching should only be implemented on signal layers *between* reference planes.

Both the DLPC350 output timing parameters and the DMD input timing parameters include a timing budget to account for their respective internal package routing skew. Thus, additional system margin can be attained by comprehending the package variations and compensating for them in the PCB layout. To increase the system timing margin, it is recommended that the DLPC350 package variation be compensated for (by signal group) but it may not be desirable to compensate for DMD package skew. This is due to the fact that each DMD has a different skew profile, making the PCB layout DMD specific. To use a common PCB design for different DMDs, it is recommended that either the DMD package skew variation not be compensated for on the PCB, or the package lengths for all applicable DMDs be considered. The following table provides the DLPC350 package output delay at the package ball for each DMD interface signal.

The total length of all the traces in Table 9-6 should be matched to the DMD_DCLK trace length. Total length includes package skews, PCB length, and DMD flex cable length. Traces from the DMD to the controller should be no longer than six inches for all modes of operation.

Table 9-6. DLPC350 Package Skew and Routing Trace Length for the DMD Interface

SIGNAL	TOTAL DELAY (PACKAGE SKEWS) in ps	TOTAL DELAY (PACKAGE SKEWS) in mils	PACKAGE BALL
DMD_D0	25.9	152.35	A8
DMD_D1	19.6	115.29	B8
DMD_D2	13.4	78.82	C8
DMD_D3	7.4	43.53	D8
DMD_D4	18.1	106.47	B11
DMD_D5	11.1	65.29	C11
DMD_D6	4.4	25.88	D11
DMD_D7	0.0	0.00	E11
DMD_D8	14.8	87.06	C7
DMD_D9	18.4	108.24	B10
DMD_D10	6.4	37.65	E7
DMD_D11	4.8	28.24	D10
DMD_D12	29.8	175.29	A6
DMD_D13	25.7	151.18	A12
DMD_D14	19.0	111.76	B12
DMD_D15	11.7	68.82	C12
DMD_D16	4.7	27.65	D12
DMD_D17	21.5	126.47	B7
DMD_D18	24.8	145.88	A10
DMD_D19	8.3	48.82	D7
DMD_D20	23.9	140.59	B6
DMD_D21	1.6	9.41	E9
DMD_D22	10.7	62.94	C10
DMD_D23	16.7	98.24	C6
DMD_DCLK	24.8	145.88	A9
$\overline{\text{DMD\_LOADB}}$	18.0	105.88	B9
DMD_SCTRL	11.4	67.06	C9
DMD_TRC	4.6	27.06	D9

Table 9-7. Routing Priority

SIGNAL	ROUTING PRIORITY	ROUTING LAYER	MATCHING REFERENCE SIGNAL	TOLERANCE
DMD_DCLK(1)(2)(3)	1	3	--	--
DMD_D[23:0], DMD_SCTRL(1)(2)(3)(4)	1	3, 4	DMD_DCLK	±150 mils
P1_A[9:0], P1_B[9:0], P1_C[9:0], P1_HSYNC, P1_VSYNC, P1_DATAEN, P1X_CLK	1	3, 4	P1X_CLK	±0.1 inches
R[A-E]_IN_P, R[A-E]_IN_N, RCK_IN_P, RCK_IN_N	2	3, 4	RCK	±150 mils Differential Signals need to be matched within ±12mils

(1) Total signal length from the DLPC350 and the DMD, including flex cable traces and PCB signal trace lengths must be held less than 4 inches and less than 3 inches for 120 MHz operation.
(2) Switching routing layers is not permitted except at the beginning and end of a trace.
(3) Minimize vias on DMD traces.
(4) Matching includes PCB trace length plus the DLPC350 package length plus the DMD flex cable length.

9.6 Design Considerations for DMD Interface

The DMD interface is modeled after the Low Power DDR memory (LPDDR) interface. In order to minimize power dissipation, the LPDDR interface is defined to be un-terminated. As a result, PCB signal integrity management is imperative. Impedance control and crosstalk mitigation is critical to robust operation. LPDDR board design recommendations include trace spacing that is three times the trace width, impedance control within 10%, and signal routing directly over a neighboring reference plane (ground or 1.9V plane).

DMD Interface performance is also a function of trace length, so the length of the line will limit performance. The DLPC350 will only work over a narrow range of DMD signal routing lengths at 120 MHz. Ensuring positive timing margins requires attention to many factors.

As an example, the DMD Interface system timing margin can be calculated as follows.

Setup Margin = (DLPC350 Output Setup) - (DMD Input Setup) - (PCB Routing Mismatch) - (PCB SI degradation)

Hold-Time Margin = (DLPC350 Output Hold) - (DMD Input Hold) - (PCB Routing Mismatch) - (PCB SI degradation)

PCB SI degradation corresponds signal integrity degradation due to PCB affects, which includes Simultaneously Switching Output (SSO) noise, crosstalk, and Inter-Symbol Interface (ISI). Additionally, PCB Routing Mismatch can be budgeted via controlled PCB routing.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided. They describe an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB Routing Mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.

9.6.1 Fiducials

Fiducials for automatic component insertion should be 0.05 inches copper with a 0.1 inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

9.6.2 Flex Considerations

Table 9-8 shows the general DMD flex design recommendations. Table 9-9 lists the minimum flex design requirements.

Table 9-8. Flex General Recommendations

DESCRIPTION	RECOMMENDATION
Configuration	2 Layer Micro Strip
Reference Plane 1	Ground plan for proper return
Vias	Maximum 2 per signal
Single trace width	4 mil minimum
Etch thickness (T)	0.5-oz. (0.6 mil thick) copper
Single-ended signal impedance	50 Ω (± 10%)

Table 9-9. Minimum Flex Design Requirements

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	UNIT
Line Width (W)(1)	Escape routing in ball field	4 (0.1)	mil (mm)
	PCB Etch Data/Control	5 (0.13)	mil (mm)
	PCB Etch Clocks	7 (0.18)	mil (mm)
Minimum Line Spacing to Other Signals (S)	Escape routing in ball field	4 (0.1)	mil (mm)
	PCB Etch Data/Control	2x the line width(2)	mil (mm)
	PCB Etch Clocks	3x the line width	mil (mm)

(1) Line width is expected to be adjusted to achieve impedance requirements.
(2) Three times the line spacing is recommended for all signals to help achieve the desired signal integrity.

9.6.3 DMD Termination Requirements

Table 9-10 lists the termination requirements for the DMD interface. These series resistors should be placed as close to the DLPC350 pins as possible while following all PCB guidelines.

Table 9-10. Termination Requirements for DMD Interface

SIGNALS	SYSTEM TERMINATION
DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	External 5Ω series termination at the transmitter
DMD_DCLK	External 5Ω series termination
$\overline{\text{DMD\_DRC\_OE}}$	External 0Ω series termination. This signal must be externally pulled-up to VDD_DMD via a 30kΩ to 51kΩ resistor

Series terminated clocks should be equal lengths, as shown below.

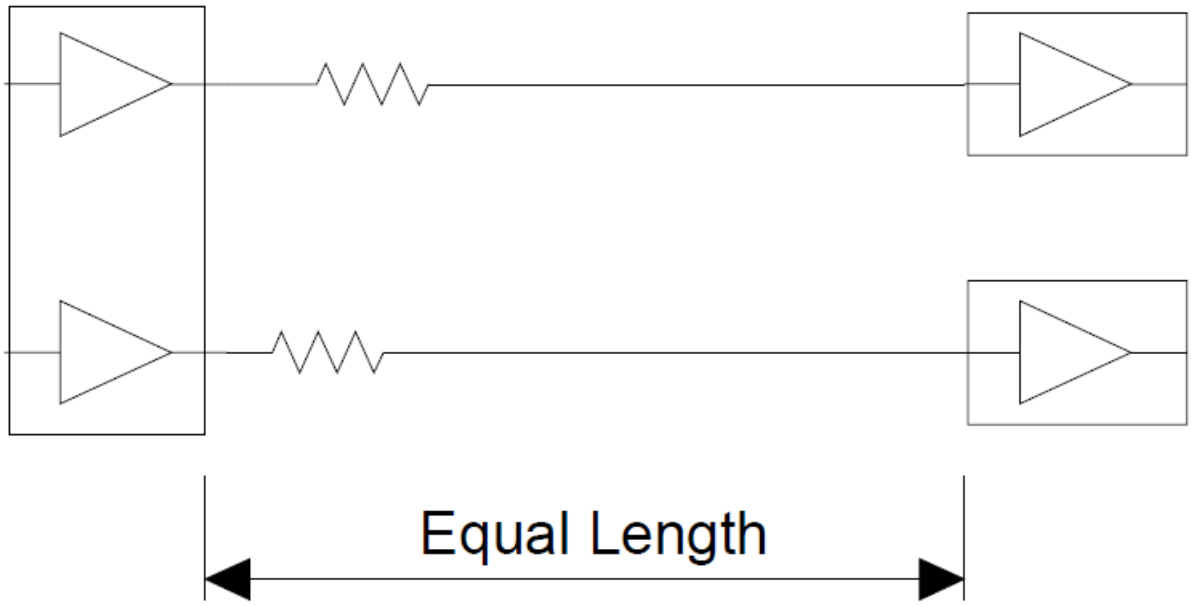

Figure 9-2. Series Terminated Clocks

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2013) to Revision A	Page
• Changed the devices From: Preview To: Production	5

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