5-V, THREE PHASE, SENSORLESS BLDC MOTOR DRIVER

Check for Samples: DRV10963

FEATURES

- **Proprietary Sensor-less Window-less 180° Sinusoidal Control Scheme**
- **Input Voltage Range 2.1 V to 5.5 V**
- **500-mA Output Current**
- **Low Quiescent Current 15 µA (typical) at Standby Mode**
- **Total Driver H+L Rdson Less than 1.5 Ω**
- **Current Limit and Short Circuit Current Protection**
- **Lock Detection**
- **Anti Voltage Surge (AVS)**
- **UVLO**
- **Thermal Shutdown**

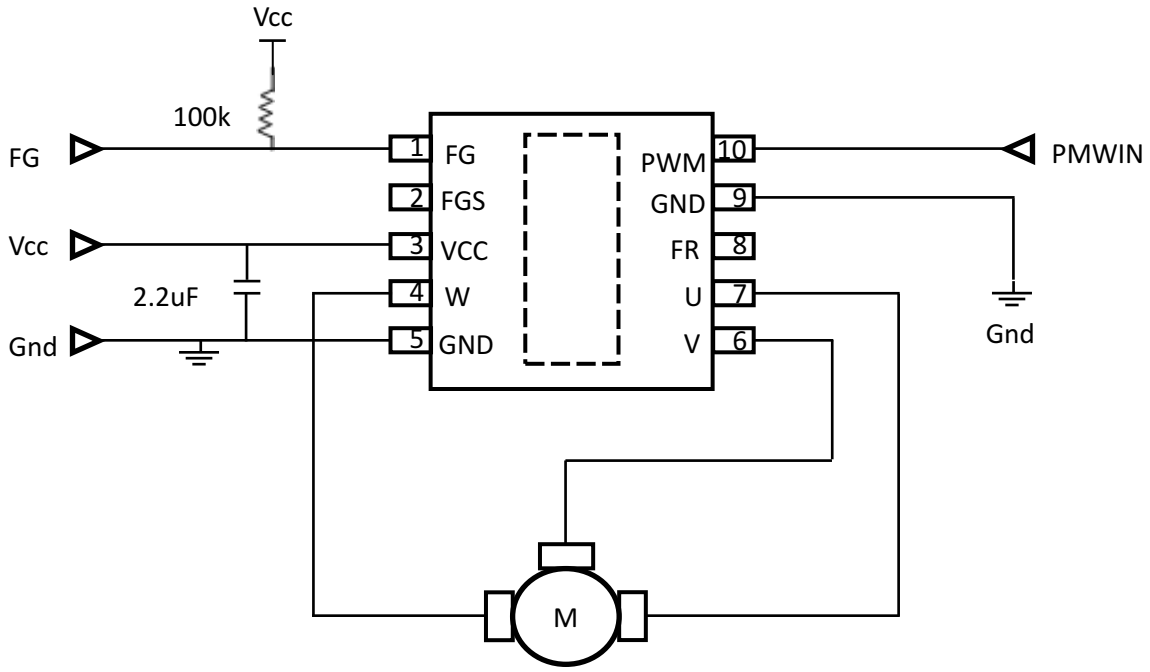
APPLICATIONS

- **Notebook CPU Fan**
- **Game Station CPU Fan**
- **ASIC Cooling Fan**

DESCRIPTION

The DRV10963 is a three phase sensor-less motor driver with integrated power MOSFETs. It is specifically designed for high efficiency, low noise and low external component count motor drive applications. The proprietary sensor-less window-less 180° sinusoidal control scheme satisfies the ultra-quiet requirement. The DRV10963 contains an intelligent lock detect function, which ensures safe operation in the event of a locked rotor. The DRV10963 is available in a thermally efficient 10-pin USON package with an exposed thermal pad.

TYPICAL APPLICATION



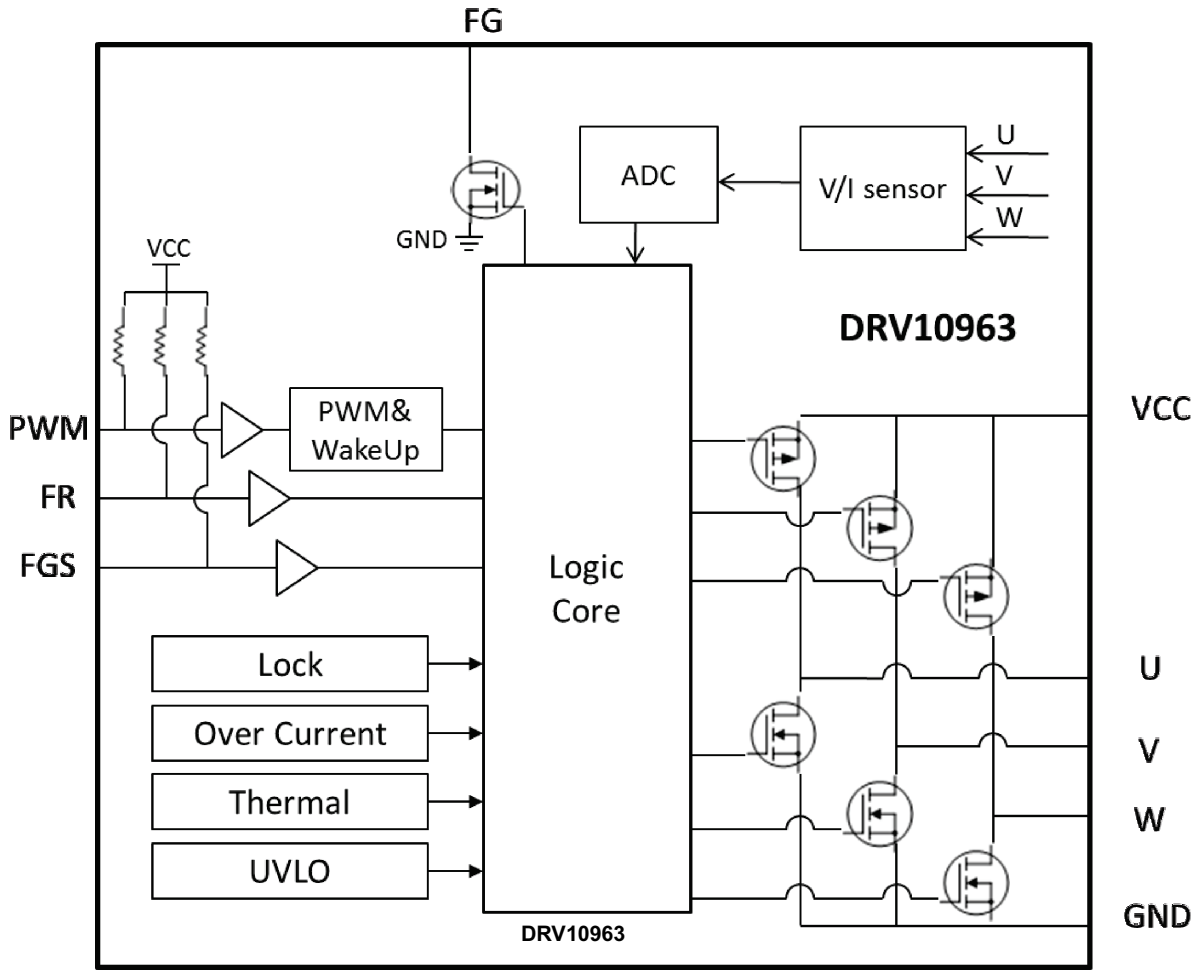
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)(2)

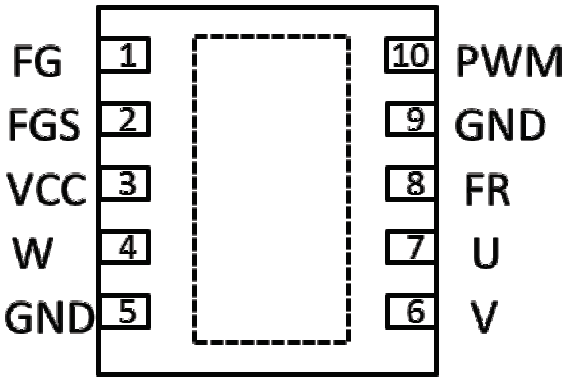
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DRV10963	USON-10	DSN	-40°C to 150°C	DRV10963B	DRV10963DSNR	Reel of 3000

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DRV10963 BLOCK DIAGRAM



DSN PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	FG	Output	Motor speed indicator output (open drain)
2	FGS	Input	Motor speed indicator selector. The state of this pin is latched on power-up and can not be changed dynamically.
3	VCC	Power	Input voltage for motor and chip supply
4	W	IO	Motor Phase W
5	GND	Ground	Ground
6	V	IO	Motor Phase V
7	U	IO	Motor Phase U
8	FR	Input	Motor direction selector. This pin can be dynamically changed after power-up.
9	GND	Ground	Ground
10	PWM	Input	Motor speed control input.
Thermal Pad	Thermal Pad		Connect to Ground for maximum thermal efficiency. Thermal pad is on the bottom of the package

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VCC	VCC Pin supply voltage	–0.3 to 6	V
U, V, W	Motor phase pins	–1.0 to 7.7	V
FR, FGS, PWM	Direction, speed indicator input, and speed input	–0.3 to 6	V
FG	Speed output	–0.3 to 7.7	V
T_J	Junction temperature	–40 to 150	°C
T_{STG}	Storage temperature	–55 to 150	°C
T_{SDR}	Maximum lead soldering temperature, 10 seconds	260	°C

(1) Stresses beyond those under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to ground.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV10963 DSN 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	40.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	46.6	
θ_{JB}	Junction-to-board thermal resistance(4)	15.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	16	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	VCC Pin supply voltage	2.1	5.5	V
U, V, W	Motor phase pins	–0.1	7	V
FR, FGS, PWM	Direction, speed indicator input, and speed input	–0.1	5.5	V
FG	Speed output	–0.1	7.5	V
T_J	Junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

(VCC = 5 V, T_A = 25°C unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating current	PWM = V_{CC}, no motor connected		5.5		mA
I_{VCC_STBY}	Standby current	PWM = 0 V		15	20	µA
UVLO						
V_{UVLO_H}	Undervoltage threshold high			2	2.1	V
V_{UVLO_L}	Undervoltage threshold low		1.7	1.8		V
V_{UVLO_HYS}	Undervoltage threshold hysteresis		100	200	300	mV
INTEGRATED MOSFET						
R_{DSON}	Series resistance (H+L)	V_{CC} = 5 V; I_{OUT} = 0.5 A		1	1.5	Ω
PWM						
V_{IH_PWM}	Input high threshold		2.3			V
V_{IL_PWM}	Input low threshold				0.8	V
F_{PWM}	PWM input frequency	Duty cycle >0% and <100%	15		100	kHz
$R_{PU\_PWM\_VCC}$	PWM pin pull up resistor	Active Mode		50		kΩ
		Standby Mode		2		MΩ
TSTBY	Standby entry time	PWM = 0 V		500		µs
FG						
I_{OL_FG}	FG sink current	V_{FG} = 0.3 V	5			mA
I_{SC_FG}	FG short circuit current	V_{FG} = 5 V		13	25	mA
FGS and FR						
V_{IH_FGS}	Input high threshold		2.3			V
V_{IL_FGS}	Input low threshold				0.8	V
V_{IH_FR}	Input high threshold		2.3			V
V_{IL_FR}	Input low threshold				0.8	V
$R_{PU\_FGS\_VCC}$	FGS pin pull up resistor	Active Mode		50		kΩ
		Standby Mode		2		MΩ
$R_{PU\_FR\_VCC}$	FR pin pull up resistor			500		kΩ
LOCK PROTECTION						
T_{ON_LOCK}	Lock detect time			0.3		s
T_{OFF_LOCK}	Lock release time			5		s
CURRENT LIMIT						
I_{LIM}	Current limit value			500		mA
SHORT CIRCUIT CURRENT PROTECTION						
I_{SHT}	Short circuit current protection			1.8		A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			160		°C
T_{SD_HYS}	Thermal shutdown hysteresis			10		°C

FUNCTIONAL DESCRIPTION

The DRV10963 is a three phase sensor-less motor driver with integrated power MOSFETs. It is specifically designed for high efficiency, low noise and low external component count motor drive applications. The proprietary sensor-less window-less 180° sinusoidal control scheme satisfies the ultra-quiet motor operation requirement.

Upon startup, the DRV10963 will spin the motor in the direction indicated by the FR input pin. The speed is determined by the duty cycle of the PWM pin. Using this input, the DRV10963 will operate a three phase BLDC motor using a sinusoidal control scheme. As the motor spins, the DRV10963 provides the speed information at the FG pin.

The DRV10963 contains an intelligent lock detect function. Once the motor is stalled by external force, system will be able to detect the lock condition within, T_{ON_LOCK}, and then release the output. It will attempt to restart the motor after T_{OFF_LOCK}.

The DRV10963 also contains several internal protection circuits, such as over current protection, over voltage protection, under voltage protection, and over temperature protection.

SPEED INPUT AND STANDBY MODE

The duty cycle of the PWM input is captured and converted into the corresponding duty cycle at the phase outputs. The phase outputs are driven by an internally generated frequency of approximately 25 kHz. This frequency is selected to reduce noise in the audible range and reduce the energy loss by the PWM switching.

In order to achieve reliable spin up and prevent a spike in the PWM signal, the transfer function is adjusted in the DRV10963. The output duty cycle will be proportional to input duty cycle after the input reaches 10% duty cycle. When the input is below a 10% duty cycle and above a 1.5% duty cycle, the output will be controlled at a 10% duty cycle. When the input duty cycle is lower than 1.5%, the DRV10963 will not drive the output, but will be in the active mode.

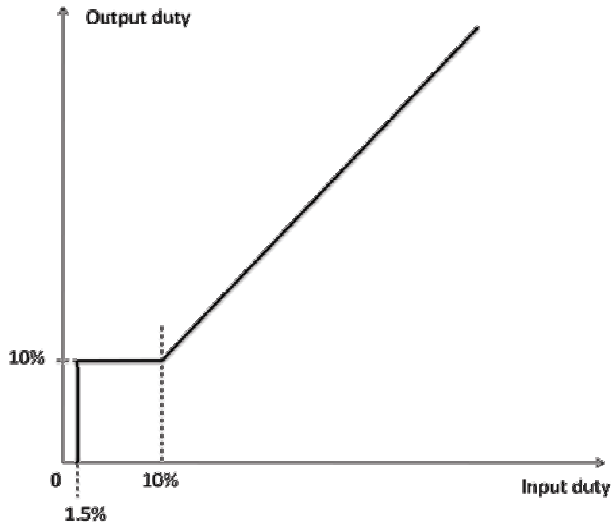


Figure 1. Duty Cycle Transfer Function

When the PWM input is driven low for at least TSTBY time, the DRV10963 will enter a low current standby mode. In standby mode, the phase outputs will no longer be driven and circuitry within the device will be disabled to minimize the system current in this state.

The device will remain in standby mode until either the PWM input is driven to a logic high (or a duty cycle of greater than 0% is applied) or the PWM input is allow to float. If the input is allowed to float an internal pull-up resistor will raise the voltage to a logic high level.

MOTOR DIRECTION CHANGE

FR (Forward Reverse) pin is used to change the direction of motor rotation as shown in Table 1.

Table 1. Motor Direction Phase Sequencing

	FR = 1	FR = 0
Motor direction	U→V→W	U→W→V

MOTOR STATUS INDICATOR (SPEED)

During operation of the DRV10963, the FG status pin indicates the speed of the motor. Using Table 2, the status of the motor can be determined.

Table 2. Motor Status Speed Indicator Configuration

Motor Condition	FG (FGS = 1)	FG (FGS = 0)
DRV10963DSNR Normal operation	Toggles once per electrical cycle	Toggles once every 2 electrical cycles
Locked Rotor	Remains at high level	Remains at high level

The FG pin is used to indicate the speed of the motor, and can be configured by use of the FGS pin to toggle either once per electrical cycle or twice per electrical cycle as described in the preceding figure. Using this information and the number of pole pairs are in the motor, the mechanical speed of the motor can be determined. The formula to determine the speed of the motor is:

If FGS = 1, $RPM = (FREQ_{FG} \times 60) / number\ of\ pole\ pairs$
If FGS = 0, RPM = $(FREQ_{FG} \times 120) / number\ of\ pole\ pairs$

The FG pin has built in short circuit protection, which limits the current in the event the pin is shorted to V_{CC}. The current will be limited to I_{SC_FG}.

SPIN UP SETTINGS

DRV10963 starts the motor using a procedure which is illustrated in Figure 2.

The motor start profile includes open loop to close loop transition threshold, align time and accelerate rate as described in Table 3.

Table 3. Motor Status Speed Indicator Configuration

	ALIGN TIME (t_{align}) (ms)	ACCELERATION RATE (R_{acc}) (Hz/S)	THRESHOLD (H_{offth}) (Hz)
DRV10963DSNR	350	80	100

In order to align the rotor to the motor acceleration profile the DRV10963 applies a 50% duty cycle on phases V and W while holding phase U at GND. This condition is maintained for t_{align} seconds. When the align phase completes the motor is accelerated by stepping through the commutation sequence at an increasing rate described by R_{acc} until the rate of commutation reaches H_{offth} Hz. When this threshold is reached the commutation drive sequence is determined by the internal control algorithm and the applied voltage is determined by the PWM input duty cycle.

The graphical illustration of the spin up procedure is shown in Figure 2:

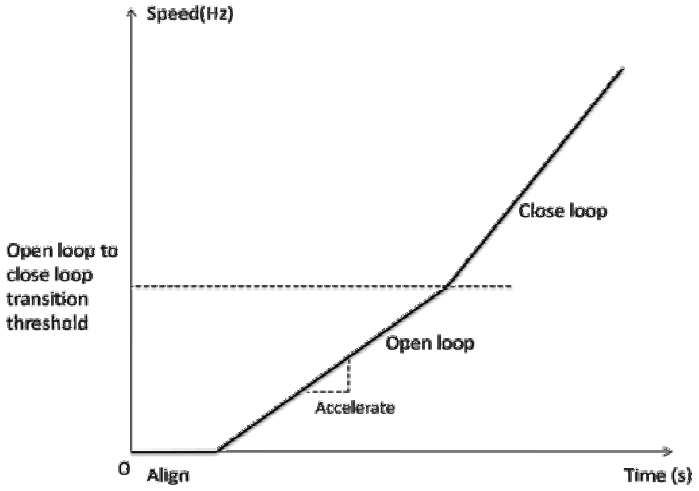


Figure 2. Motor Start Procedure

LOCK DETECTION

If the motor is stalled during running, the lock detection algorithm will be triggered after T_{ON_LOCK}. The DRV10963 will immediately stop driving the motor for T_{OFF_LOCK}. The DRV10963 will then attempt to drive the motor again.

If the motor is stalled from a stationary condition, the lock detection algorithm will be triggered after the system goes into close loop as illustrated in the Motor Start Procedure figure. After the part transitions into closed loop the lock condition will be detected and the DRV10963 will immediately stop driving the motor for T_{OFF_LOCK}. The DRV10963 will then attempt to drive the motor again. If the lock condition still exists, the DRV10963 will re-enter the next lock protection cycle until the lock condition is removed.

CURRENT LIMIT

The DRV10963 provides an internal current limit function. The output voltage (duty cycle) is limited such that the motor phase current does not exceed I_{LIM}. When the current limit function is active the duty cycle output will not be controlled by the PWM input duty cycle.

SHORT CIRCUIT CURRENT PROTECTION

The DRV10963 contains internal short circuit current protection circuitry. It is triggered when motor phase current exceeds I_{SHT}. The circuit will temporarily disable the output voltage. When the motor phase current drops below I_{SHT}, the DRV10963 will attempt to restart the motor.

ANTI VOLTAGE SURGE (AVS)

The DRV10963 includes circuitry to prevent the motor from transferring energy back into the power supply. This can typically happen when the PWM input duty cycle suddenly decreases or the motor is suddenly shut down due to lock protection or thermal protection.

OVER TEMPERATURE PROTECTION

The DRV10963 contains a thermal shut down function which disables motor operation upon detecting the device junction temperature has exceeded T_{SD}. After the junction temperature has lowered approximately T_{SD_HYS}°, motor operation will resume.

UNDER VOLTAGE PROTECTION

The DRV10963 contains an under voltage lockout feature, which prevents motor operation below a specified voltage. Upon power up, the DRV10963 will operate once V_{CC} rises above V_{UVLO_H}. The DRV10963 will continue to operate until V_{CC} falls below V_{UVLO_L}.

Table 4. Recommended Component Values

PIN	TO	FUNCTION	VALUE
VCC	GND	Decoupling Capacitor	2.2 µF, 10 V, X5R
FG	Voltage ≤ V_{CC}	Pull up resistor for Open Drain output	100 kΩ

PCB Thermal Layout Considerations

The package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV10963DSNR	ACTIVE	SON	DSN	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	10963B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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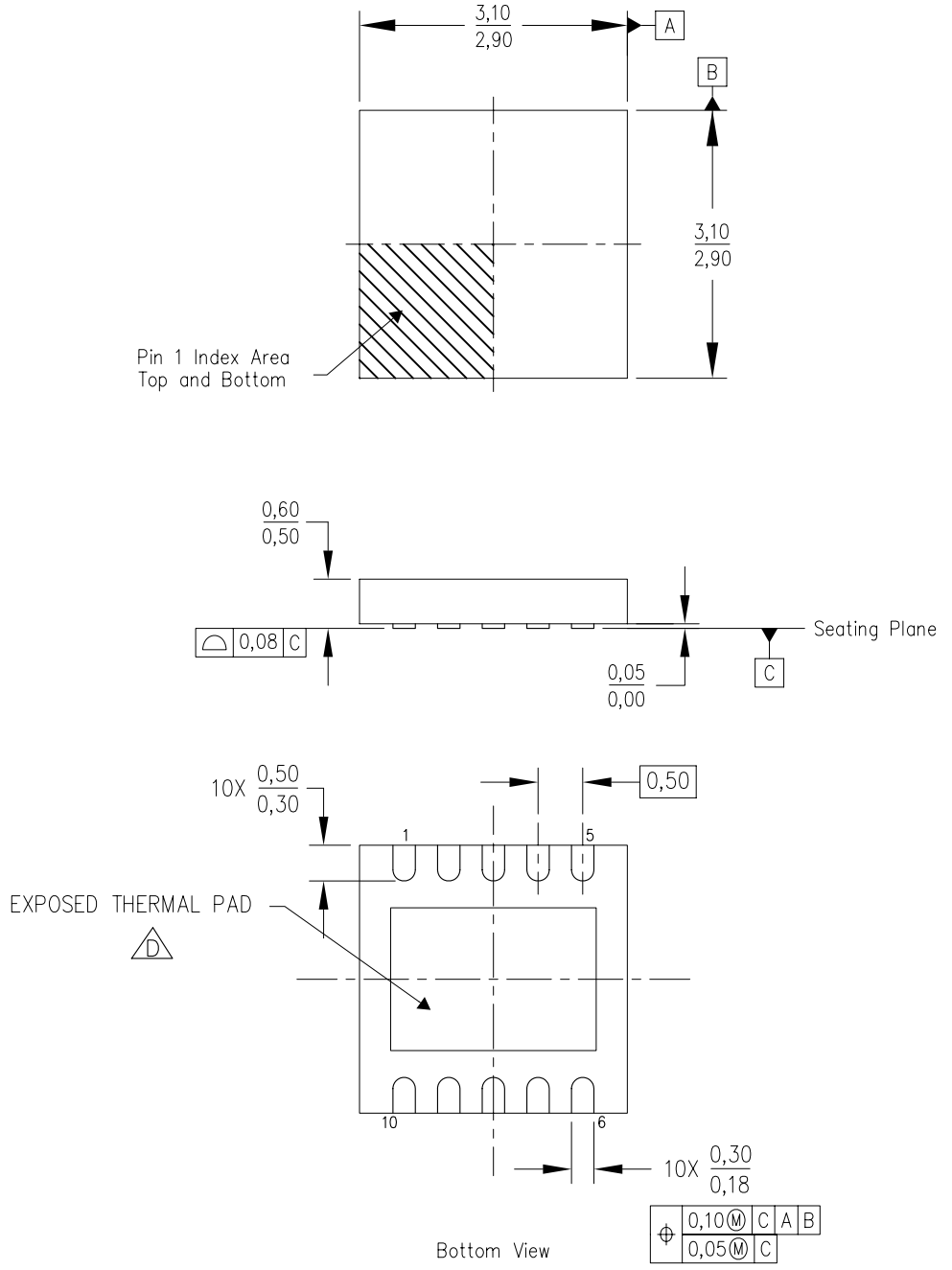
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

DSN (S–PUSON–N10) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

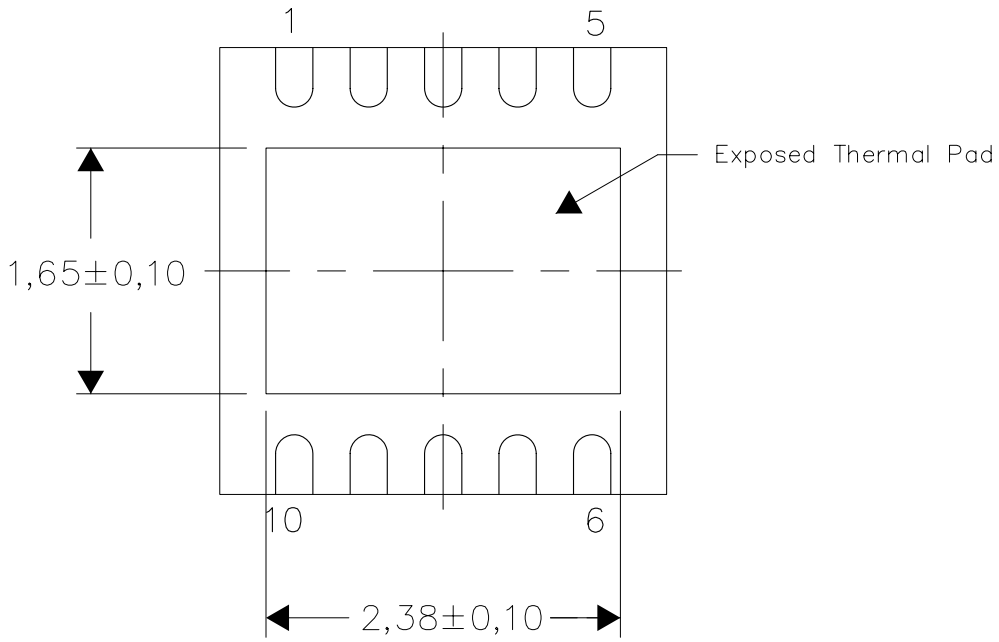
DSN (S–PDSO–N10) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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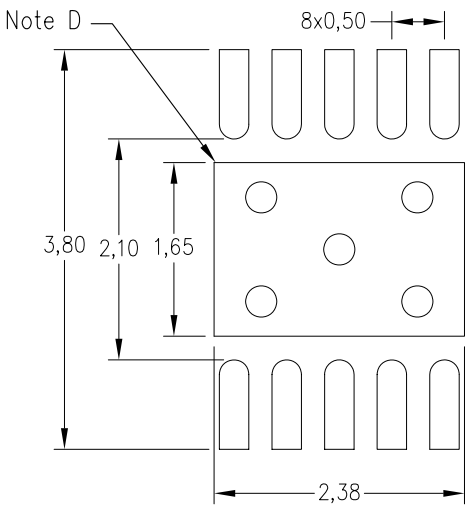
NOTES:

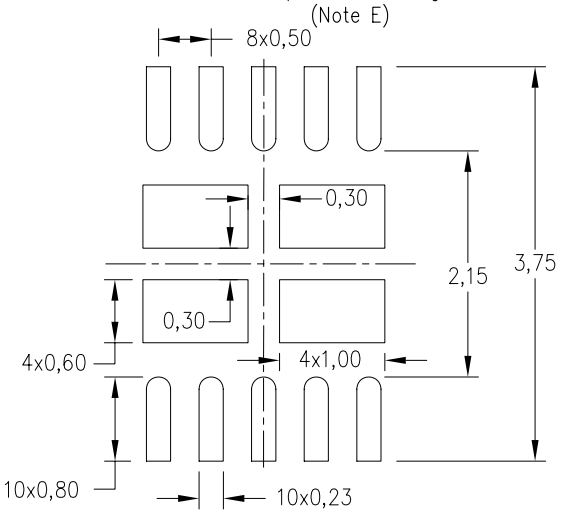
A. All linear dimensions are in millimeters

DSN (S–PUSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout

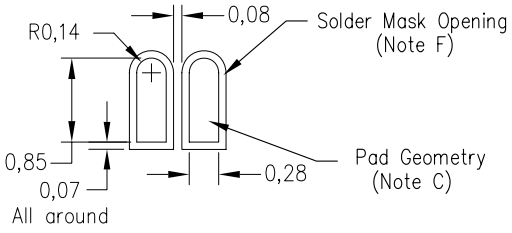


Example Stencil Design
(Note E)

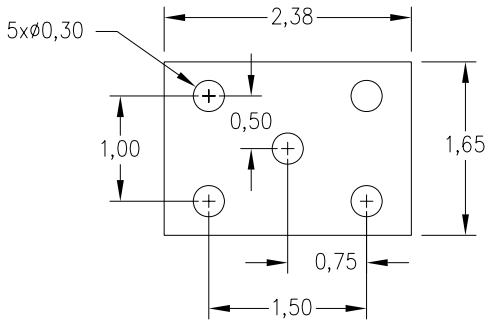


62% solder coverage on center pad

Non Solder Mask
Defined Pad



Exposed Pad Geometry



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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