DS100KR401 Ultra Low Power, 4 Lane (8-channel, bi-directional) Repeater for Data-rates up to 10.3 Gbps

Check for Samples: DS100KR401

FEATURES

- **Comprehensive Product Family:**
  - **DS100KR800: 8-channel, Uni-directional Repeater**
  - **DS100KR401: 4x Lane, Bi-directional Repeater**
  - **DS100BR210: 2-channel, Uni-directional Repeater**
  - **DS100BR111: 1x Lane, Bi-directional Repeater**
- **4 Lane (8-channel, Bi-directional) Repeater for 4x 10G-KR and Other Serial Standards up to 10.3 Gbps**
- **Transparent Management of 10G-KR (802.3ap) Link Training Protocol**
- **Low 65 mW/channel (Typ) Power Consumption, with Option to Power Down Unused Channels**
- **Advanced Signal Conditioning Features**
  - **Receive Equalization up to 36 dB at 5 GHz**
  - **Transmit De-emphasis up to -12 dB**
  - **Transmit Output Voltage Control: 700 mV to 1300 mV**
- **Programmable via Pin Selection, EEPROM or SMBus Interface**
- **Single Supply Operation Selectable: 2.5V or 3.3V**
- **–40°C to +85°C Operating Temperature Range**
- **3 kV HBM ESD Rating**
- **Flow-thru Pinout in 10mm×5.5mm 54-pin Leadless WQFN Package**

DESCRIPTION

The DS100KR401 is an extremely low power, high performance repeater designed to support 4 lane (bi-directional) 10G-KR and other high speed interface serial protocols up to 10.3 Gbps. The receiver's continuous time linear equalizer (CTLE) provides a boost of up to +36 dB at 5 GHz (10.3125 Gbps) in each of its eight channels and is capable of opening an input eye that is completely closed due to inter symbol interference (ISI) induced by interconnect medium such as long backplanes or cables, hence enabling host controllers to ensure an error free end-to-end link. The transmitter provides a de-emphasis boost of up to -12 dB and output voltage amplitude control from 700 mV to 1300 mV to allow maximum flexibility in the physical placement within the interconnect channel.

When operating in 10G-KR mode, the DS100KR401 transparently allows the host controller and the end point to optimize the full link and negotiate transmit equalizer coefficients as defined in the 802.3ap standard. This seamless management of the link training protocol ensures guaranteed system level interoperability with minimum latency.

With a low power consumption of 65 mW/channel (typ) and option to turn-off unused channels, the DS100KR401 enables energy efficient system design. A single supply of 3.3v or 2.5v is required to power the device.

The programmable settings can be applied via pin settings, SMBus (I2C) protocol or an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up. This eliminates the need for an external microprocessor or software driver.

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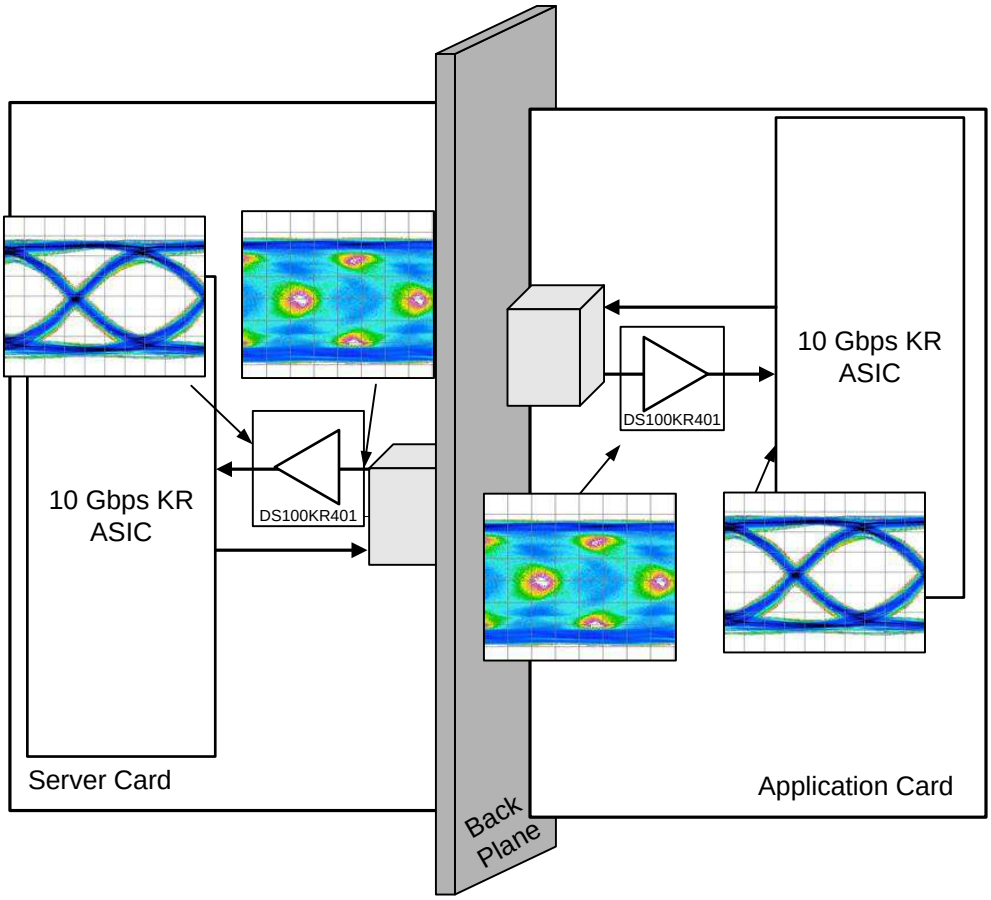
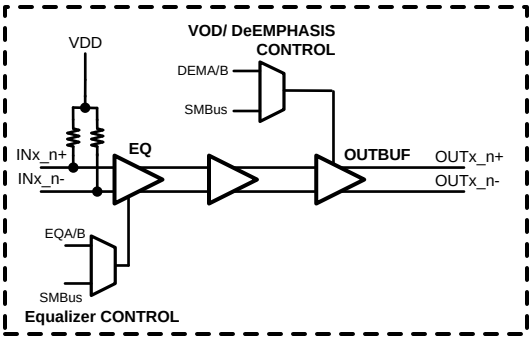
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION



BLOCK DIAGRAM - DETAIL VIEW OF CHANNEL (1 of 8)



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PIN DIAGRAM

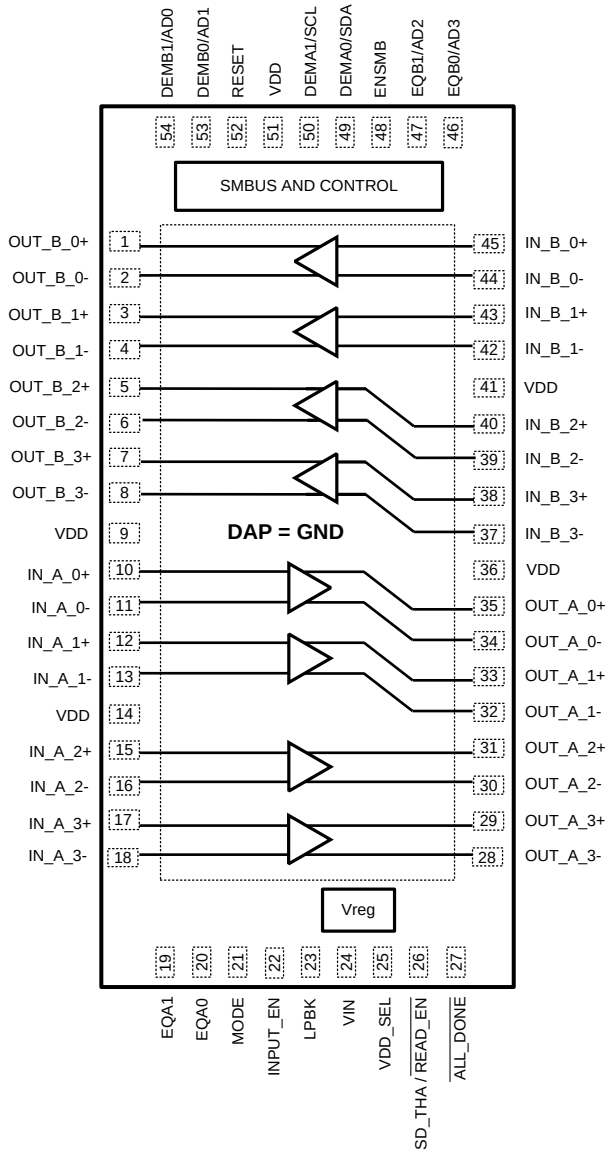

Figure 1. DS100KR401 Pin Diagram 54 lead

PIN DESCRIPTIONS(1)

Pin Name	Pin Number	I/O, Type	Pin Description
Differential High Speed I/O's			
OUT_B_0+, OUT_B_0-, OUT_B_1+, OUT_B_1-, OUT_B_2+, OUT_B_2-, OUT_B_3+, OUT_B_3-	1, 2, 3, 4, 5, 6, 7, 8	O	Inverting and non-inverting 50Ω driver bank B outputs with de-emphasis. Compatible with AC coupled CML inputs.
IN_A_0+, IN_A_0-, IN_A_1+, IN_A_1-, IN_A_2+, IN_A_2-, IN_A_3+, IN_A_3-	10, 11, 12, 13, 15, 16, 17, 18	I	Inverting and non-inverting differential inputs to bank A equalizer. A gated on-chip 50Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD when enabled.
IN_B_0+, IN_B_0-, IN_B_1+, IN_B_1-, IN_B_2+, IN_B_2-, IN_B_3+, IN_B_3-	45, 44, 43, 42, 40, 39, 38, 37	I	Inverting and non-inverting differential inputs to bank B equalizer. A gated on-chip 50Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD when enabled.
OUT_A_0+, OUT_A_0-, OUT_A_1+, OUT_A_1-, OUT_A_2+, OUT_A_2-, OUT_A_3+, OUT_A_3-	35, 34, 33, 32, 31, 30, 29, 28	O	Inverting and non-inverting 50Ω driver bank A outputs with de-emphasis. Compatible with AC coupled CML inputs.
Control Pins — Shared (LVCMOS)			
ENSMB	48	I, LVCMOS	System Management Bus (SMBus) enable pin Tie 1kΩ to VDD = Register Access SMBus Slave mode FLOAT = Read External EEPROM (Master SMBUS Mode) Tie 1kΩ to GND = Pin Mode
ENSMB = 1 (SMBUS MODE)			
SCL	50	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode SMBUS clock input pin is enabled. Clock output when loading EEPROM configuration (master mode).
SDA	49	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode The SMBus bi-directional SDA pin is enabled. Data input or open drain (pull-down only) output.
AD0-AD3	54, 53, 47, 46	I, LVCMOS	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.
$\overline{\text{READ\_EN}}$	26	I, 4-LEVEL, LVCMOS	When using an External EEPROM, a transition from high to low starts the load from the external EEPROM
ENSMB = 0 (PIN MODE)			
EQA0, EQA1, EQB0, EQB1	20, 19, 46, 47	I, 4-LEVEL, LVCMOS	EQA[1:0] and EQB[1:0] control the level of equalization on the input pins. The pins are active only when ENSMB is deasserted (low). The 8 channels are organized into two banks. Bank A is controlled with the EQA[1:0] pins and bank B is controlled with the EQB[1:0] pins. When ENSMB is high the SMBus registers provide independent control of each channel. The EQB[1:0] pins are converted to SMBUS AD2/ AD3 inputs. See Table 2
DEMA0, DEMA1, DEMB0, DEMB1	49, 50, 53, 54	I, 4-LEVEL, LVCMOS	DEMA[1:0] and DEMB[1:0] control the level of de-emphasis of the output driver when in Gen1/2 mode. The pins are only active when ENSMB is de-asserted (low). The 8 channels are organized into two banks. Bank A is controlled with the DEMA [1:0] pins and bank B is controlled with the DEMB[1:0] pins. When ENSMB is high the SMBus registers provide independent control of each channel. The DEMA[1:0] pins are converted to SMBUS SCL/SDA and DEMB[1:0] pins are converted to AD0, AD1 inputs. See Table 3

(1) Notes:
LVCMOS inputs without the “Float” conditions must be driven to a logic low or high at all times or operation is not guaranteed.
Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.
For 3.3V mode operation, VIN pin = 3.3V and the "VDD" for the 4-level input is 3.3V.
For 2.5V mode operation, VDD pin = 2.5V and the "VDD" for the 4-level input is 2.5V.

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PIN DESCRIPTIONS(1) (continued)

Pin Name	Pin Number	I/O, Type	Pin Description
MODE	21	I, 4-LEVEL, LVCMOS	Tie 1kΩ to VDD = 10G-KR Mode Operation Tie 1kΩ to GND = 10G Mode Operation
SD_TH	26	I, 4-LEVEL, LVCMOS	Controls the internal Signal Detect Threshold See Table 4
Control Pins — Both Pin and SMBus Modes (LVCMOS)			
INPUT_EN	22	I, 4-LEVEL, LVCMOS	Tie 1kΩ to VDD = Normal Operation
LPBK	23	I, 4-LEVEL, LVCMOS	Controls the loopback function Tie 1kΩ to GND = INA_n to OUTB_n loopback Float = Normal Operation (loopback is disabled) Tie 1kΩ to VDD = INB_n to OUTA_n loopback
VDD_SEL	25	I, FLOAT	Controls the internal regulator Float = 2.5V mode Tie GND = 3.3V mode
RESET	52	I, LVCMOS	LOW = Device is enabled (Normal Operation) HIGH = Low Power Mode
Outputs			
$\overline{\text{ALL\_DONE}}$	27	O, LVCMOS	Valid Register Load Status Output HIGH = External EEPROM load failed LOW = External EEPROM load passed
Power			
VIN	24	Power	In 3.3V mode, feed 3.3V to VIN In 2.5V mode, leave floating.
VDD	9, 14, 36, 41, 51	Power	Power supply pins CML/analog 2.5V mode, connect to 2.5V 3.3V mode, connect 0.1 uF cap to each VDD pin
GND	DAP	Power	Ground pad (DAP - die attach pad).

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (VDD = 2.5V mode)		-0.5V to +2.75V
Supply Voltage (VIN = 3.3V mode)		-0.5V to +4.0V
LVCMOS Input/Output Voltage		-0.5V to +4.0V
CML Input Voltage		-0.5V to (VDD+0.5)
CML Input Current		-30 to +30 mA
Junction Temperature		125°C
Storage Temperature		-40°C to +125°C
Lead Temperature Range Soldering (4 sec.)		+260°C
Derate NJY0054A Package		52.6mW/°C above +25°C
ESD Rating	HBM, STD - JESD22-A114F	5 kV
	MM, STD - JESD22-A115-A	150 V
	CDM, STD - JESD22-C101-D	1000 V
Thermal Resistance	θ_{JC}	11.5°C/W
	θ_{JA}, No Airflow, 4 layer JEDEC	19.1°C/W
For soldering specifications: see product folder at www.ti.com , and SNOA549		

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are specified for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

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RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units
Supply Voltage (2.5V mode)	2.375	2.5	2.625	V
Supply Voltage (3.3V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V
Supply Noise up to 50 MHz (1)			100	mVp-p

(1) Allowed supply noise (mVp-p sine wave) under typical conditions.

ELECTRICAL CHARACTERISTICS(1)

Symbol	Parameter	Conditions	Min	Typ(2)	Max	Units
Power						
PD	Power Dissipation	**VDD = 2.5 V supply**, EQ Enabled, VOD = 1.0 Vp-p, INPUT_EN = 1, RESET = 0		500	700	mW
		VIN = 3.3 V supply, EQ Enabled, VOD = 1.0 Vp-p, INPUT_EN = 1, RESET = 0		660	900	mW
LVCMOS / LVTTL DC Specifications						
V_{ih}	High Level Input Voltage	3.3V Mode Operation (VIN = 3.3V)	2.0		3.6	V
V_{il}	Low Level Input Voltage		0		0.8	V
V_{oh}	High Level Output Voltage (ALL_DONE pin)	I_{oh} = −4mA	2.0			V
V_{ol}	Low Level Output Voltage (ALL_DONE pin)	I_{ol} = 4mA			0.4	V
I_{ih}	Input High Current (RESET pin)	VIN = 3.6 V, LVCMOS = 3.6 V	-15		+15	uA
	Input High Current with internal resistors (4–level input pin)		+20		+150	uA
I_{il}	Input Low Current (RESET pin)	VIN = 3.6 V, LVCMOS = 0 V	-15		+15	uA
	Input Low Current with internal resistors (4–level input pin)		-160		-40	uA
CML Receiver Inputs (IN_n+, IN_n-)						
$RL_{rx\text{-}diff}$	RX package pins plus Si differential return loss	0.05 GHz - 7.5 GHz		-15		dB
		7.5 GHz - 15 GHz		-5		dB
RLrx-cm	Common mode RX return loss	0.05 GHz - 5 GHz		-10		dB
Zrx-dc	RX DC common mode impedance	Tested at VDD = 0	40	50	60	Ω
Zrx-diff-dc	RX DC differntial mode impedance	Tested at VDD = 0	80	100	120	Ω
Vrx-diff-dc	Differential RX peak to peak voltage	Tested at pins	0.6		1.2	V
Vrx-signal-det-diff-pp	Signal detect assert level for active data signal	SD_TH = F (float), 0101 pattern at 10.3 Gbps		180		mVp-p
Vrx-idle-det-diff-pp	Signal detect de-assert level for electrical idle	SD_TH = F (float), 0101 pattern at 10.3 Gbps		110		mVp-p
High Speed Outputs						
$V_{tx\text{-}diff\text{-}pp}$	Output Voltage Differential Swing	Differential measurement with Out_n+ and OUT_n-, terminated by 50Ω to GND, AC-Coupled, VID = 1.0 Vp-p, DEM0 = 1, DEM1 = 0	0.8	1.0	1.2	Vp-p
$V_{tx\text{-}de\text{-}ratio\_3.5}$	TXde-emphasis ratio	VOD = 1.0 Vp-p, DEM0 = 0, DEM1 = R		−3.5		dB
$V_{tx\text{-}de\text{-}ratio\_6}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM0 = R, DEM1= R		−6		dB
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	TX Dj > 1.5 MHz				0.15	UI
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	TX RMS jitter < 1.5 MHz				3.0	ps RMS

(1) The Electrical Characteristics tables list specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are **NOT** guaranteed.

(2) Typical values represent most likely parametric norms at VDD = 2.5V, TA = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are **NOT** guaranteed.

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ELECTRICAL CHARACTERISTICS[1] (continued)

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Units
$T_{TX-RISE-FALL}$	Transmitter rise/fall time	20% to 80% of differential output voltage	35	45		ps
$T_{RF-MISMATCH}$	Transmitter rise/fall mismatch	20% to 80% of differential output voltage		0.01	0.1	UI
$RL_{TX-DIFF}$	Differential return loss	0.05 GHz - 7.5 GHz		-15		dB
		7.5 GHz - 15 GHz		-5		dB
RL_{TX-CM}	Common mode return loss	0.05 GHz - 5 GHz		-10		dB
$Z_{TX-DIFF-DC}$	DC differential TX impedance			100		Ω
$V_{TX-CM-AC-PP}$	TX AC common mode voltage	VOD = 1.0 Vp-p, DEM0 = 1, DEM1 = 0			100	mVpp
$I_{TX-SHORT}$	Transmitter short circuit current limit	Total current the transmitter can supply when shorted to VDD or GND		20		mA
T_{PDEQ}	Differential propagation delay	EQ = 00, [3]		200		ps
T_{LSK}	Lane to lane skew	T = 25C, VDD = 2.5V		25		ps
T_{PPSK}	Part to part propagation delay skew	T = 25C, VDD = 2.5V		40		ps
Equalization						
DJE1	Residual deterministic jitter at 10.3 Gbps	35” 4 mil FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 1F'h,** DEM = 0 dB		0.3		UI
DJE2	Residual deterministic jitter at 10.3 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.3		UI
De-emphasis						
DJD1	Residual deterministic jitter at 10.3 Gbps	20” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1.0 Vp-p, **DEM = −9 dB**		0.1		UI

(3) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the shortest propagation delays.

ELECTRICAL CHARACTERISTICS — SERIAL MANAGEMENT BUS INTERFACE

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	See [1]	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	See [1] [2]			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3V, See [1] [2] [3]		2000		Ω
		Pullup V_{DD} = 2.5V, See [1] [2] [3]		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
TBUF	Bus Free Time Between Stop and Start Condition		1.3			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
TSU:STA	Repeated Start Condition Setup Time		0.6			µs

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.

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ELECTRICAL CHARACTERISTICS — SERIAL MANAGEMENT BUS INTERFACE (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TSU:STO	Stop Condition Setup Time		0.6			µs
THD:DAT	Data Hold Time		0			ns
TSU:DAT	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	See (4)	0.6		50	µs
t_F	Clock/Data Fall Time	See (4)			300	ns
t_R	Clock/Data Rise Time	See (4)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	See (4) (5)			500	ms

(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(5) Specified by Design. Parameter not tested in production.

TIMING DIAGRAMS

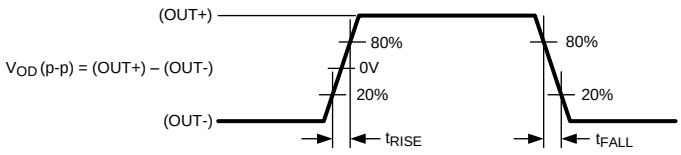

Figure 2. CML Output and Rise and FALL Transition Time

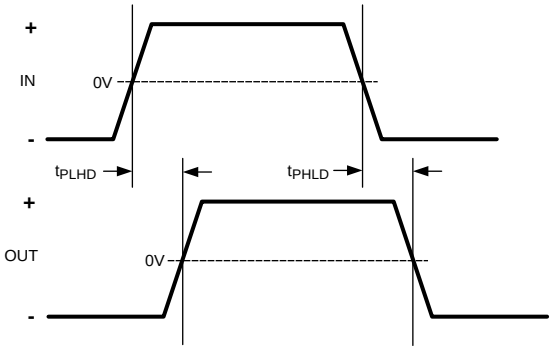

Figure 3. Propagation Delay Timing Diagram

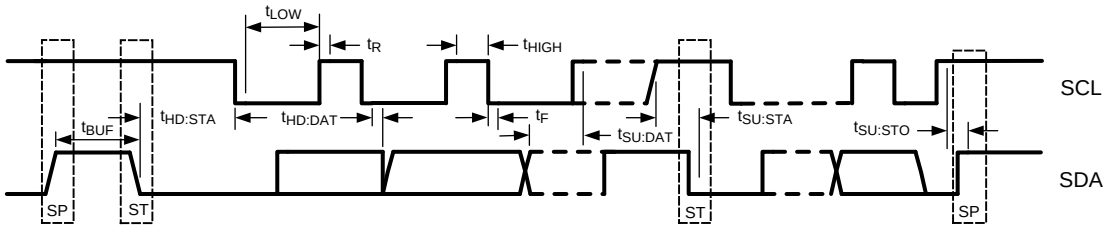

Figure 4. SMBus Timing Parameters

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FUNCTIONAL DESCRIPTIONS

The DS100KR401 is a low power media compensation 4 lane repeater optimized for 10G–KR. The DS100KR401 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS100KR401 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register informations from external EEPROM; please refer to SMBUS Master Mode for additional information.

Pin Control Mode:

When in pin mode (ENSMB = 0) , the repeater is configurable with external pins. Equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the De-Emphasis table below. The receiver electrical idle detect threshold is also adjustable via the SD_TH pin.

SMBUS Mode:

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB the MODE, EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If RESET is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-Emphasis levels are set by registers.

The input control pins have been enhanced to have 4 different levels and provide a wider range of control settings when ENSMB=0.

Table 1. 4–Level Control Pin Settings(1)

Pin Setting	Description	Voltage at Pin
0	Tie 1kΩ to GND	0.03 x VDD
R	Tie 20kΩ to GND	1/3 x VDD
Float	Float (leave pin open)	2/3 x VDD
1	Tie 1kΩ to VDD	0.98 x VDD

(1) The above required resistor value is for a single device. When there are multiple devices connected to the pull-up / pull-down resistor, the value must scale with the number of devices. If 4 devices are connected to a single pull-up or pull-down, the 1kΩ resistor value should be 250Ω. For the 20kΩ to GND, this should also scale to 5kΩ.

3.3V or 2.5V Supply Mode Operation

The DS100KR401 has an optional internal voltage regulator to provide the 2.5V supply to the device. In 3.3V mode, the VIN pin = 3.3V is used to supply power to the device and the VDD pins should be left open. The internal regulator will provide the 2.5V to the VDD pins of the device and a 0.1 µF cap is needed at each of 5 VDD pins for power supply de-coupling (total capacitance should be ≤0.5 µF). The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5V mode, the VIN pin should be left open and 2.5V supply must be applied to the VDD pins. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

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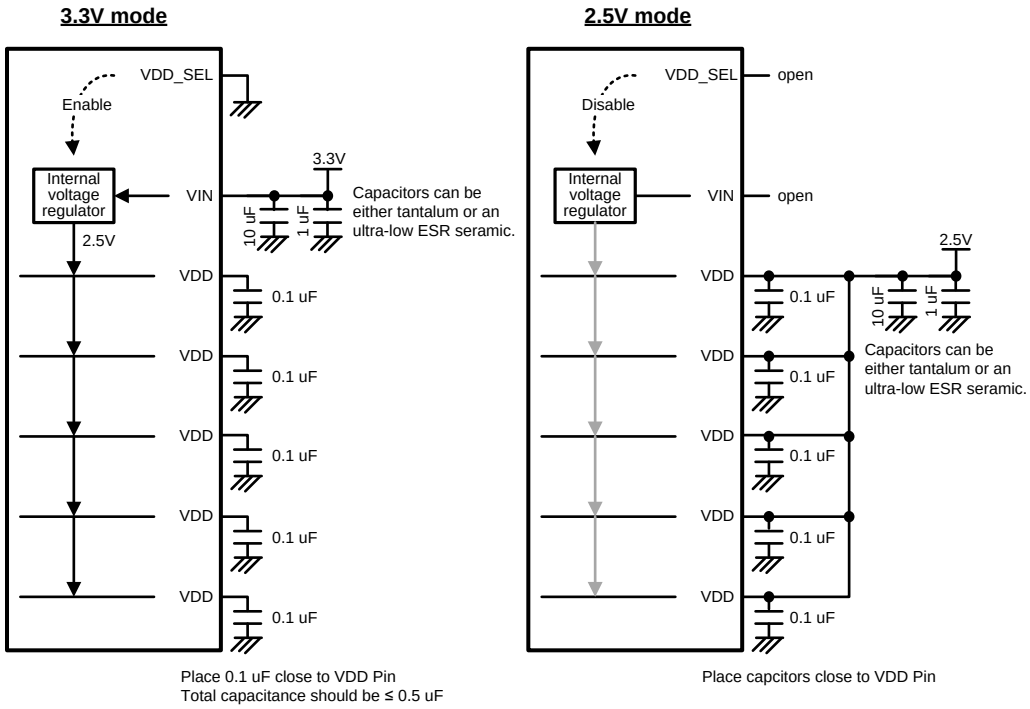

Figure 5. 3.3V or 2.5V Supply Connection Diagram

Table 2. Equalizer Settings

Level	EQA1 EQB1	EQA0 EQB0	EQ – 8 bits [7:0]	dB at 1.0 GHz	dB at 3.0 GHz	dB at 5.0 GHz	Suggested Use
1	0	0	0000 0000 = 0x00	1.7	4.2	5.3	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	2.8	6.6	8.7	FR4 5 inch 5–mil trace
3	0	Float	0000 0010 = 0x02	4.1	8.6	10.6	FR4 5 inch 4–mil trace
4	0	1	0000 0011 = 0x03	5.1	9.8	11.7	FR4 10 inch 5–mil trace
5	R	0	0000 0111 = 0x07	6.2	12.4	15.6	FR4 10 inch 4–mil trace
6	R	R	0001 0101 = 0x15	5.1	12.0	16.6	FR4 15 inch 4–mil trace
7	R	Float	0000 1011 = 0x0B	7.7	15.0	18.3	FR4 20 inch 4–mil trace
8	R	1	0000 1111 = 0x0F	8.8	16.5	19.7	FR4 25 to 30 inch 4–mil trace
9	Float	0	0101 0101 = 0x55	6.3	14.8	20.3	FR4 30 inch 4–mil trace
10	Float	R	0001 1111 = 0x1F	9.9	19.2	23.6	FR4 35 inch 4–mil trace
11	Float	Float	0010 1111 = 0x2F	11.3	21.7	25.8	10m, 30awg cable
12	Float	1	0011 1111 = 0x3F	12.4	23.2	27.0	10m – 12m cable
13	1	0	1010 1010 = 0xAA	11.9	24.1	29.1	
14	1	R	0111 1111 = 0x7F	13.6	26.0	30.7	
15	1	Float	1011 1111 = 0xBF	15.1	28.3	32.7	
16	1	1	1111 1111 = 0xFF	16.1	29.7	33.8	

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Table 3. De-emphasis and Output Voltage Settings

Level	DEMA1 DEMB1	DEMA0 DEMB0	VOD Vp-p	DEM dB	Inner Amplitude Vp-p	Suggested Use
1	0	0	0.8	0	0.8	FR4 <5 inch 4–mil trace
2	0	R	0.9	0	0.9	FR4 <5 inch 4–mil trace
3	0	Float	0.9	- 3.5	0.6	FR4 10 inch 4–mil trace
4	0	1	1.0	0	1.0	FR4 <5 inch 4–mil trace
5	R	0	1.0	- 3.5	0.7	FR4 10 inch 4–mil trace
6	R	R	1.0	- 6	0.5	FR4 15 inch 4–mil trace
7	R	Float	1.1	0	1.1	FR4 <5 inch 4–mil trace
8	R	1	1.1	- 3.5	0.7	FR4 10 inch 4–mil trace
9	Float	0	1.1	- 6	0.6	FR4 15 inch 4–mil trace
10	Float	R	1.2	0	1.2	FR4 <5 inch 4–mil trace
11	Float	Float	1.2	- 3.5	0.8	FR4 10 inch 4–mil trace
12	Float	1	1.2	- 6	0.6	FR4 15 inch 4–mil trace
13	1	0	1.3	0	1.3	FR4 <5 inch 4–mil trace
14	1	R	1.3	- 3.5	0.9	FR4 10 inch 4–mil trace
15	1	Float	1.3	- 6	0.7	FR4 15 inch 4–mil trace
16	1	1	1.3	- 9	0.5	FR4 20 inch 4–mil trace

Table 4. Signal Detect Threshold Level(1)

SD_TH	SMBus REG bit [3:2] and [1:0]	Assert Level (typ)	De-assert Level (typ)
0	10	210 mVp-p	150 mVp-p
R	01	160 mVp-p	100 mVp-p
F (default)	00	180 mVp-p	110 mVp-p
1	11	190 mVp-p	130 mVp-p

(1) VDD = 2.5V, 25°C and 0101 pattern at 10.3 Gbps

SMBUS Master Mode

The DS100KR401 devices support reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS100KR401 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Set ENSMB = Float — enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0'h and capable of 400 kHz operation at 2.5V and 3.3V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.

When tying multiple DS100KR401 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 device.
  - U1: AD[3:0] = 0000 = 0xB0'h,
  - U2: AD[3:0] = 0001 = 0xB2'h,
  - U3: AD[3:0] = 0010 = 0xB4'h,
  - U4: AD[3:0] = 0011 = 0xB6'h
- Use a pull-up resistor on SDA and SCL; value = 2k ohms
- Daisy-chain READEN# (pin 26) and ALL_DONE# (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  - 1. Tie READEN# of the 1st device in the chain (U1) to GND
  - 2. Tie ALL_DONE# of U1 to READEN# of U2

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– 3. Tie ALL_DONE# of U2 to READEN# of U3
– 4. Tie ALL_DONE# of U3 to READEN# of U4
– 5. Optional: Tie ALL_DONE# output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS100KR401 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS100KR401 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS100KR401 device.

:20000000**00001000000407002FAD4002FAD4002FAD4002FAD401805F5A8005F5A8005F5A**D8

:20002000**8005F5A800005454**00000000000000000000000000000000000000000000000F6

:20006000000000000000000000000000000000000000000000000000000000000000000080

:20008000000000000000000000000000000000000000000000000000000000000000000060

:2000A000000000000000000000000000000000000000000000000000000000000000000040

:2000C000000000000000000000000000000000000000000000000000000000000000000020

:2000E000000000000000000000000000000000000000000000000000000000000000000000

:20004000000000000000000000000000000000000000000000000000000000000000000A0

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Table 5. EEPROM Register Map - Single Device with Default Value

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	0	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	DEVICE COUNT[3]	DEVICE COUNT[2]	DEVICE COUNT[1]	DEVICE COUNT[0]
Value		0	0	0	0	0	0	0	0
Description	1	RES	RES	RES	RES	RES	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	2	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Value		0	0	0	0	0	0	0	0
Description	3	PWDN_ch7	PWDN_ch6	PWDN_ch5	PWDN_ch4	PWDN_ch3	PWDN_ch2	PWDN_ch1	PWDN_ch0
Value		0	0	0	0	0	0	0	0
Description	4	RES_1	RES_0	PWDN_INPUTS	PWDN_OSC	Ovrd_RESET	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	5	RES	RES	RES	RES	RES	RES_btb_en	Ovrd_RES	Ovrd_RES
Value		0	0	0	0	0	1	0	0
Description	6	Ovrd_RES	Ovrd_RES	Ovrd_RES	Ovrd_RES	Ovrd_RES	rx_delay_sel_2	rx_delay_sel_1	rx_delay_sel_0
Value		0	0	0	0	0	1	1	1
Description	7	RD_delay_sel_3	RD_delay_sel_2	RD_delay_sel_1	RD_delay_sel_0	ch0_Idle_auto	ch0_Idle_sel	ch0_RES_1	ch0_RES_0
Value		0	0	0	0	0	0	0	0
Description	8	ch0_BST_7	ch0_BST_6	ch0_BST_5	ch0_BST_4	ch0_BST_3	ch0_BST_2	ch0_BST_1	ch0_BST_0
Value		0	0	1	0	1	1	1	1
Description	9	ch0_Sel_scp	ch0_Sel_mode	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_VOD_2	ch0_VOD_1	ch0_VOD_0
Value		1	0	1	0	1	1	0	1
Description	10	ch0_DEM_2	ch0_DEM_1	ch0_DEM_0	ch0_Slow	ch0_idle_tha_1	ch0_idle_tha_0	ch0_idle_thd_1	ch0_idle_thd_0
Value		0	1	0	0	0	0	0	0
Description	11	ch1_Idle_auto	ch1_Idle_sel	ch1_RES_1	ch1_RES_0	ch1_BST_7	ch1_BST_6	ch1_BST_5	ch1_BST_4
Value		0	0	0	0	0	0	1	0
Description	12	ch1_BST_3	ch1_BST_2	ch1_BST_1	ch1_BST_0	ch1_Sel_scp	ch1_Sel_mode	ch1_RES_2	ch1_RES_1
Value		1	1	1	1	1	0	1	0
Description	13	ch1_RES_0	ch1_VOD_2	ch1_VOD_1	ch1_VOD_0	ch1_DEM_2	ch1_DEM_1	ch1_DEM_0	ch1_Slow
Value		1	1	0	1	0	1	0	0
Description	14	ch1_idle_tha_1	ch1_idle_tha_0	ch1_idle_thd_1	ch1_idle_thd_0	ch2_Idle_auto	ch2_Idle_sel	ch2_RES_1	ch2_RES_0
Value		0	0	0	0	0	0	0	0
Description	15	ch2_BST_7	ch2_BST_6	ch2_BST_5	ch2_BST_4	ch2_BST_3	ch2_BST_2	ch2_BST_1	ch2_BST_0
Value		0	0	1	0	1	1	1	1

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Table 5. EEPROM Register Map - Single Device with Default Value (continued)

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	16	ch2_Sel_scp	ch2_Sel_mode	ch2_RES_2	ch2_RES_1	ch2_RES_0	ch2_VOD_2	ch2_VOD_1	ch2_VOD_0
Value		1	0	1	0	1	1	0	1
Description	17	ch2_DEM_2	ch2_DEM_1	ch2_DEM_0	ch2_Slow	ch2_idle_tha_1	ch2_idle_tha_0	ch2_idle_thd_1	ch2_idle_thd_0
Value		0	1	0	0	0	0	0	0
Description	18	ch3_Idle_auto	ch3_Idle_sel	ch3_RES_1	ch3_RES_0	ch3_BST_7	ch3_BST_6	ch3_BST_5	ch3_BST_4
Value		0	0	0	0	0	0	1	0
Description	19	ch3_BST_3	ch3_BST_2	ch3_BST_1	ch3_BST_0	ch3_Sel_scp	ch3_Sel_mode	ch3_RES_2	ch3_RES_1
Value		1	1	1	1	1	0	1	0
Description	20	ch3_RES_0	ch3_VOD_2	ch3_VOD_1	ch3_VOD_0	ch3_DEM_2	ch3_DEM_1	ch3_DEM_0	ch3_Slow
Value		1	1	0	1	0	1	0	0
Description	21	ch3_idle_tha_1	ch3_idle_tha_0	ch3_idle_thd_1	ch3_idle_thd_0	ovrd_fast_idle	en_high_idle_th_n	en_high_idle_th_s	en_fast_idle_n
Value		0	0	0	0	0	0	0	1
Description	22	en_fast_idle_s	eqsd_mgain_n	eqsd_mgain_s	ch4_Idle_auto	ch4_Idle_sel	ch4_RXDET_1	ch4_RXDET_0	ch4_BST_7
Value		1	0	0	0	0	0	0	0
Description	23	ch4_BST_6	ch4_BST_5	ch4_BST_4	ch4_BST_3	ch4_BST_2	ch4_BST_1	ch4_BST_0	ch4_Sel_scp
Value		0	1	0	1	1	1	1	1
Description	24	ch4_Sel_mode	ch4_RES_2	ch4_RES_1	ch4_RES_0	ch4_VOD_2	ch4_VOD_1	ch4_VOD_0	ch4_DEM_2
Value		0	1	0	1	1	0	1	0
Description	25	ch4_DEM_1	ch4_DEM_0	ch4_Slow	ch4_idle_tha_1	ch4_idle_tha_0	ch4_idle_thd_1	ch4_idle_thd_0	ch5_Idle_auto
Value		1	0	0	0	0	0	0	0
Description	26	ch5_Idle_sel	ch5_RES_1	ch5_RES_0	ch5_BST_7	ch5_BST_6	ch5_BST_5	ch5_BST_4	ch5_BST_3
Value		0	0	0	0	0	1	0	1
Description	27	ch5_BST_2	ch5_BST_1	ch5_BST_0	ch5_Sel_scp	ch5_Sel_mode	ch5_RES_2	ch5_RES_1	ch5_RES_0
Value		1	1	1	1	0	1	0	1
Description	28	ch5_VOD_2	ch5_VOD_1	ch5_VOD_0	ch5_DEM_2	ch5_DEM_1	ch5_DEM_0	ch5_Slow	ch5_idle_tha_1
Value		1	0	1	0	1	0	0	0
Description	29	ch5_idle_tha_0	ch5_idle_thd_1	ch5_idle_thd_0	ch6_Idle_auto	ch6_Idle_sel	ch6_RES_1	ch6_RES_0	ch6_BST_7
Value		0	0	0	0	0	0	0	0
Description	30	ch6_BST_6	ch6_BST_5	ch6_BST_4	ch6_BST_3	ch6_BST_2	ch6_BST_1	ch6_BST_0	ch6_Sel_scp
Value		0	1	0	1	1	1	1	1
Description	31	ch6_Sel_mode	ch6_RES_2	ch6_RES_1	ch6_RES_0	ch6_VOD_2	ch6_VOD_1	ch6_VOD_0	ch6_DEM_2
Value		0	1	0	1	1	0	1	0

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Table 5. EEPROM Register Map - Single Device with Default Value (continued)

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	32	ch6_DEM_1	ch6_DEM_0	ch6_Slow	ch6_idle_tha_1	ch6_idle_tha_0	ch6_idle_thd_1	ch6_idle_thd_0	ch7_Idle_auto
Value		1	0	0	0	0	0	0	0
Description	33	ch7_Idle_sel	ch7_RES_1	ch7_RES_0	ch7_BST_7	ch7_BST_6	ch7_BST_5	ch7_BST_4	ch7_BST_3
Value		0	0	0	0	0	1	0	1
Description	34	ch7_BST_2	ch7_BST_1	ch7_BST_0	ch7_Sel_scp	ch7_Sel_mode	ch7_RES_2	ch7_RES_1	ch7_RES_0
Value		1	1	1	1	0	1	0	1
Description	35	ch7_VOD_2	ch7_VOD_1	ch7_VOD_0	ch7_DEM_2	ch7_DEM_1	ch7_DEM_0	ch7_Slow	ch7_idle_tha_1
Value		1	0	1	0	1	0	0	0
Description	36	ch7_idle_tha_0	ch7_idle_thd_1	ch7_idle_thd_0	iph_dac_ns_1	iph_dac_ns_0	ipp_dac_ns_1	ipp_dac_ns_0	ipp_dac_1
Value		0	0	0	0	0	0	0	0
Description	37	ipp_dac_0	RD23_67	RD01_45	RD_PD_ovrd	RD_Sel_test	RD_RESET_ovrd	PWDB_input_DC	DEM_VOD_ovrd
Value		0	0	0	0	0	0	0	0
Description	38	DEM_ovrd_N2	DEM_ovrd_N1	DEM_ovrd_N0	VOD_ovrd_N2	VOD_ovrd_N1	VOD_ovrd_N0	SPARE0	SPARE1
Value		0	1	0	1	0	1	0	0
Description	39	DEM__ovrd_S2	DEM__ovrd_S1	DEM_ovrd_S0	VOD_ovrd_S2	VOD_ovrd_S1	VOD_ovrd_S0	SPARE0	SPARE1
Value		0	1	0	1	0	1	0	0

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Table 6. Example of EEPROM for 4 Devices Using 2 Address Maps(1)

EEPROM Address	Address (Hex)	EEPROM Data	Comments
0	00	0x43	CRC_EN = 0, Address Map = 1, >256 bytes = 0, Device Count[3:0] = 3
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x0B	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x30	Device 3 Address Location
11	0B	0x00	Begin Device 0, 1 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x00	EQ CHB0 = 00
17	11	0xAB	VOD CHB0 = 1.0V
18	12	0x00	DEM CHB0 = 0 (0dB)
19	13	0x00	EQ CHB1 = 00
20	14	0x0A	VOD CHB1 = 1.0V
21	15	0xB0	DEM CHB1 = 0 (0dB)
22	16	0x00	
23	17	0x00	EQ CHB2 = 00
24	18	0xAB	VOD CHB2 = 1.0V
25	19	0x00	DEM CHB2 = 0 (0dB)
26	1A	0x00	EQ CHB3 = 00
27	1B	0x0A	VOD CHB3 = 1.0V
28	1C	0xB0	DEM CHB3 = 0 (0dB)
29	1D	0x01	
30	1E	0x80	
31	1F	0x01	EQ CHA0 = 00
32	20	0x56	VOD CHA0 = 1.0V
33	21	0x00	DEM CHA0 = 0 (0dB)
34	22	0x00	EQ CHA1 = 00
35	23	0x15	VOD CHA1 = 1.0V
36	24	0x60	DEM CHA1 = 0 (0dB)
37	25	0x00	
38	26	0x01	EQ CHA2 = 00
39	27	0x56	VOD CHA2 = 1.0V
40	28	0x00	DEM CHA2 = 0 (0dB)
41	29	0x00	EQ CHA3 = 00
42	2A	0x15	VOD CHA3 = 1.0V
43	2B	0x60	DEM CHA3 = 0 (0dB)
44	2C	0x00	
45	2D	0x00	

(1) CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. This example has all 8–channels set to EQ = 00 (min boost), VOD = 1.0V, DEM = 0 (0dB) and multiple device can point to the same address map.

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Table 6. Example of EEPROM for 4 Devices Using 2 Address Maps(1) (continued)

EEPROM Address	Address (Hex)	EEPROM Data	Comments
46	2E	0x54	
47	2F	0x54	End Device 0, 1 - Address Offset 39
48	30	0x00	Begin Device 2, 3 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x00	EQ CHB0 = 00
54	36	0xAB	VOD CHB0 = 1.0V
55	37	0x00	DEM CHB0 = 0 (0dB)
56	38	0x00	EQ CHB1 = 00
57	39	0x0A	VOD CHB1 = 1.0V
58	3A	0xB0	DEM CHB1 = 0 (0dB)
59	3B	0x00	
60	3C	0x00	EQ CHB2 = 00
61	3D	0xAB	VOD CHB2 = 1.0V
62	3E	0x00	DEM CHB2 = 0 (0dB)
63	3F	0x00	EQ CHB3 = 00
64	40	0x0A	VOD CHB3 = 1.0V
65	41	0xB0	DEM CHB3 = 0 (0dB)
66	42	0x01	
67	43	0x80	
68	44	0x01	EQ CHA0 = 00
69	45	0x56	VOD CHA0 = 1.0V
70	46	0x00	DEM CHA0 = 0 (0dB)
71	47	0x00	EQ CHA1 = 00
72	48	0x15	VOD CHA1 = 1.0V
73	49	0x60	DEM CHA1 = 0 (0dB)
74	4A	0x00	
75	4B	0x01	EQ CHA2 = 00
76	4C	0x56	VOD CHA2 = 1.0V
77	4D	0x00	DEM CHA2 = 0 (0dB)
78	4E	0x00	EQ CHA3 = 00
79	4F	0x15	VOD CHA3 = 1.0V
80	50	0x60	DEM CHA3 = 0 (0dB)
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 2, 3 - Address Offset 39

SYSTEM MANAGEMENT BUS (SMBus) and CONFIGURATION REGISTERS

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1kΩ to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS100KR401 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, the DS100KR401 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

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Table 7. Device Slave Address Bytes

AD[3:0] Settings	Address Bytes (HEX)
0000	B0
0001	B2
0010	B4
0011	B6
0100	B8
0101	BA
0110	BC
0111	BE
1000	C0
1001	C2
1010	C4
1011	C6
1100	C8
1101	CA
1110	CC
1111	CE

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

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WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see SMBus Register Map Table for more information.

Table 8. SMBUS Slave Mode Register Map

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x00	Observation, Reset	7	Reserved	R/W	0x00	Set bit to 0.
		6:3	Address Bit AD[3:0]	R		Observation of AD[3:0] bit [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0
		2	EEPROM Read Done	R		1: Device completed the read from external EEPROM.
		1	Block Reset	R/W		1: Block bit 0 from resettting the registers; self clearing.
		0	Reset	R/W		SMBus Reset 1: Reset registers to default value; self clearing.
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel [7]: CH7 – CHA_3 [6]: CH6 – CHA_2 [5]: CH5 – CHA_1 [4]: CH4 – CHA_0 [3]: CH3 – CHB_3 [2]: CH2 – CHB_2 [1]: CH1 – CHB_1 [0]: CH0 – CHB_0 00'h = all channels enabled FF'h = all channels disabled Note: override RESET pin.

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Table 8. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x02	Override RESET, LPBK Control	7:6	Reserved	R/W	0x00	Set bits to 0.
		5:4	LPBK Control			00: Use LPBK pin control 01: INA to OUTB loopback 10: INB to OUTA loopback 11: Disable loopback and ignore LPBK pin.
		3:1	Reserved			Set bits to 0.
		0	Override RESET			1: Block RESET pin control 0: Allow RESET pin control
0x05	Slave Mode CRC Bits	7:0	CRC bits	R/W	0x00	CRC bits [7:0]
0x06	Slave CRC Control	7:5	Reserved	R/W	0x10	Set bits to 0.
		4	Reserved			Set bit to 1.
		3	Slave CRC			1: Disables the slave CRC mode 0: Enables the slave CRC mode Note: In order to change VOD, DEM and EQ of the channels in slave mode, set bit to 1 to disable the CRC.
		2:0	Reserved			Set bits to 0.
0x08	Override Pin Control	7	Reserved	R/W	0x00	Set bit to 0.
		6	Override SD_TH			1: Block SD_TH pin control 0: Allow SD_TH pin control
		5:2	Reserved			Set bits to 0.
		1	Override DEM			1: Block DEM pin control 0: Allow DEM pin control
		0	Reserved			Set bit to 0.
0x0E	CH0 - CHB0 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x0F	CH0 - CHB0 EQ	7:0	EQ Control	R/W	0x2F	IB0 EQ Control - total of 256 levels. See Table 2.
0x10	CH0 - CHB0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x11	CH0 - CHB0 DEM	7	STATUS	R	0x02	Observation bit for CH0 - CHB0.
		6:5	STATUS	R		Observation bit for CH0 - CHB0.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB0 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB

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Table 8. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x12	CH0 - CHB0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x15	CH1 - CHB1 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x16	CH1 - CHB1 EQ	7:0	EQ Control	R/W	0x2F	IB1 EQ Control - total of 256 levels. See Table 2.
0x17	CH1 - CHB1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB1 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x18	CH1 - CHB1 DEM	7	STATUS	R	0x02	Observation bit for CH1 - CHB1.
		6:5	STATUS	R		Observation bit for CH1 - CHB1.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB1 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x19	CH1 - CHB1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x1C	CH2 - CHB2 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x1D	CH2 - CHB2 EQ	7:0	EQ Control	R/W	0x2F	IB2 EQ Control - total of 256 levels. See Table 2.

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Table 8. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x1E	CH2 - CHB2 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB2 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x1F	CH2 - CHB2 DEM	7	STATUS	R	0x02	Observation bit for CH2 - CHB2.
		6:5	STATUS	R		Observation bit for CH2 - CHB2.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB2 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x20	CH2 - CHB2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x23	CH3 - CHB3 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x24	CH3 - CHB3 EQ	7:0	EQ Control	R/W	0x2F	IB3 EQ Control - total of 256 levels. See Table 2.
0x25	CH3 - CHB3 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OB0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V

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Table 8. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x26	CH3 - CHB3 DEM	7	STATUS	R	0x02	Observation bit for CH3 - CHB3.
		6:5	STATUS	R		Observation bit for CH3 - CHB3.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OB3 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x27	CH3 - CHB3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x2B	CH4 - CHA0 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x2C	CH4 - CHA0 EQ	7:0	EQ Control	R/W	0x2F	IA0 EQ Control - total of 256 levels. See Table 2.
0x2D	CH4 - CHA0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA0 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x2E	CH4 - CHA0 DEM	7	STATUS	R	0x02	Observation bit for CH4 - CHA0.
		6:5	STATUS	R		Observation bit for CH4 - CHA0.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA0 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB

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Table 8. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x2F	CH4 - CHA0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x32	CH5 - CHA1 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x33	CH5 - CHA1 EQ	7:0	EQ Control	R/W	0x2F	IA1 EQ Control - total of 256 levels. See Table 2.
0x34	CH5 - CHA1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA1 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x35	CH5 - CHA1 DEM	7	STATUS	R	0x02	Observation bit for CH5 - CHA1.
		6:5	STATUS	R		Observation bit for CH5 - CHA1.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA1 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x36	CH5 - CHA1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x39	CH6 - CHA2 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x3A	CH6 - CHA2 EQ	7:0	EQ Control	R/W	0x2F	IA2 EQ Control - total of 256 levels. See Table 2.

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Table 8. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x3B	CH6 - CHA2 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA2 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V
0x3C	CH6 - CHA2 DEM	7	STATUS	R	0x02	Observation bit for CH6 - CHA2.
		6:5	STATUS	R		Observation bit for CH6 - CHA2.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA2 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x3D	CH6 - CHA2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x40	CH7 - CHA3 Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x41	CH7 - CHA3 EQ	7:0	EQ Control	R/W	0x2F	IA3 EQ Control - total of 256 levels. See Table 2.
0x42	CH7 - CHA3 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	Reserved			Set bit to 0.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			OA3 VOD Control 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V 100: 1.1 V 101: 1.2 V (default) 110: 1.3 V 111: 1.4 V

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Table 8. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit (s)	Field	Type	Default	Description
0x43	CH7 - CHA3 DEM	7	STATUS	R	0x02	Observation bit for CH7 - CHA3.
		6:5	STATUS	R		Observation bit for CH7 - CHA3.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		OA3 DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x44	CH7 - CHA3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	IDLE thd			De-assert threshold 00 = 110 mVp-p (default) 01 = 100 mVp-p 10 = 150 mVp-p 11 = 130 mVp-p Note: override the SD_TH pin.
		1:0	IDLE tha			Assert threshold 00 = 180 mVp-p (default) 01 = 160 mVp-p 10 = 210 mVp-p 11 = 190 mVp-p Note: override the SD_TH pin.
0x51	Device ID	7:5	VERSION	R	0x44	010'b
		4:0	ID			00100'b

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APPLICATIONS INFORMATION

GENERAL RECOMMENDATIONS

The DS100KR401 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 (SNOA401) for additional information on WQFN packages.

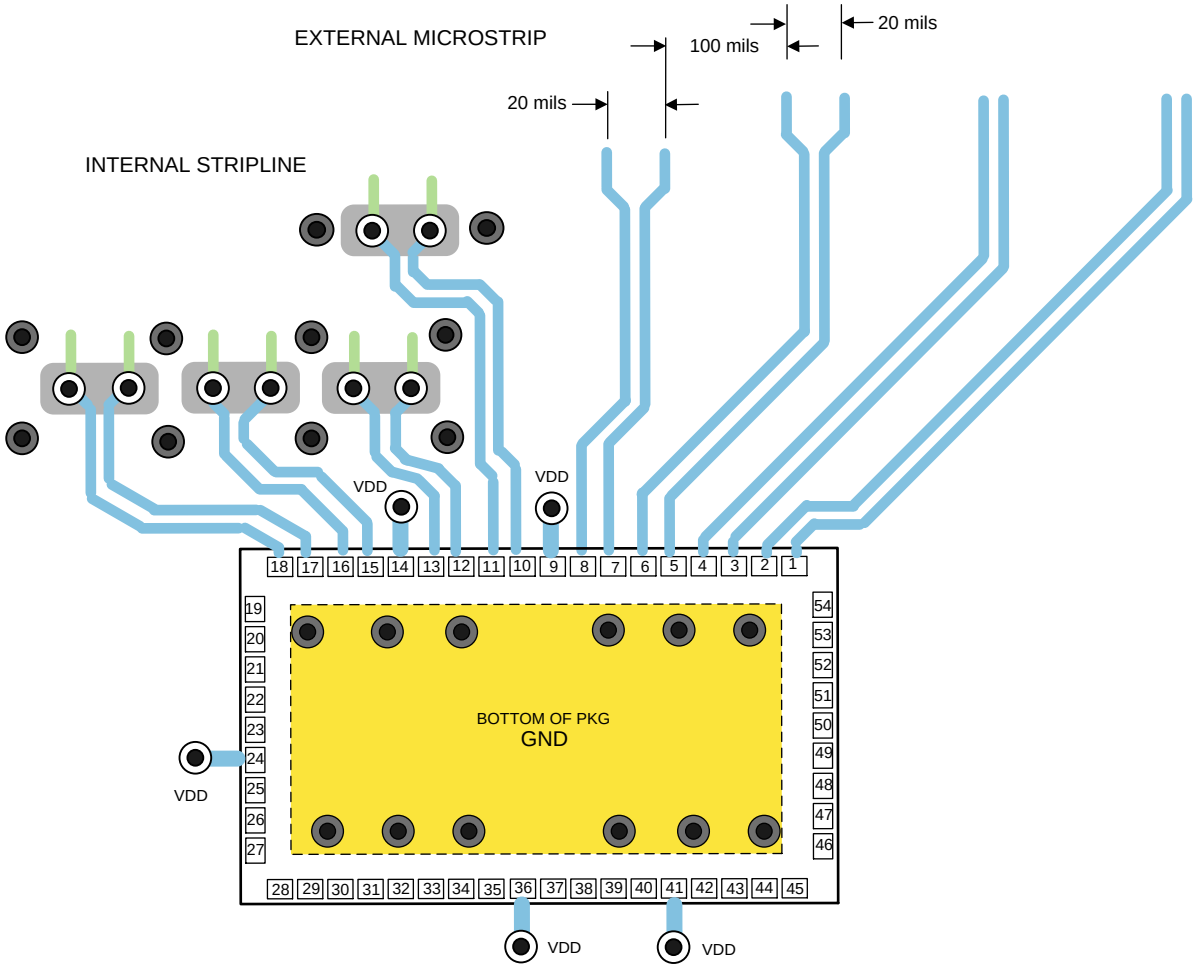

Figure 6. Typical Routing Options

The graphic shown above depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the deterimential high frequency effects of stubs on the signal path.

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POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS100KR401 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS100KR401. Smaller body size capacitors can help facilitate proper component placement. In the case of 3.3V mode operation with the internal LDO regulator, recommend using capacitors with capacitance in the range of 1.0 µF to 10 µF should be incorporated in the power supply bypassing design for the VIN pin. These capacitors should be ultra-low ESR ceramic.

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TYPICAL CHARACTERISTICS

Typical Performance Curves Characteristics

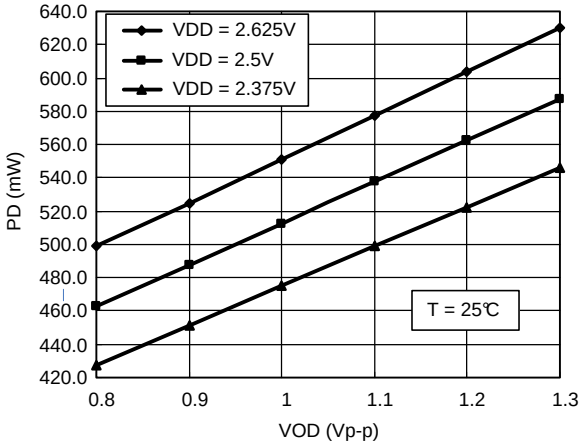

Figure 7. Power Dissipation (PD) vs. Output Differential Voltage (VOD)

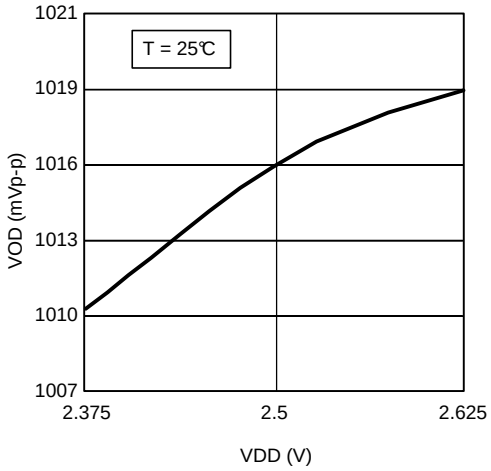

Figure 8. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Supply Voltage (VDD)

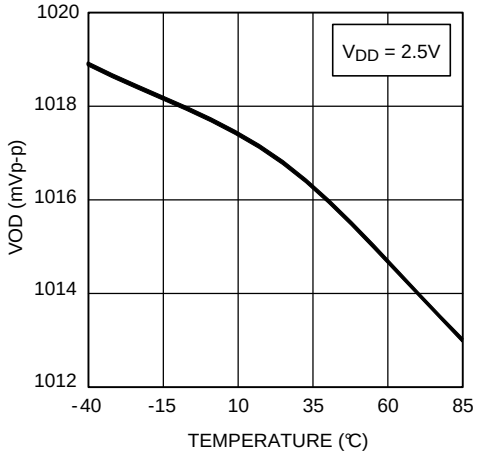

Figure 9. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

Typical Performance Eye Diagrams Characteristics

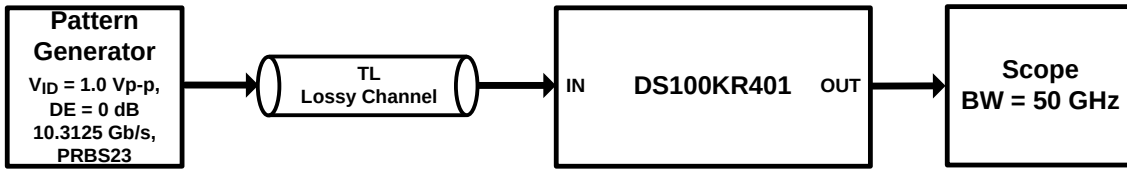

Figure 10. Test Setup Connections Diagram

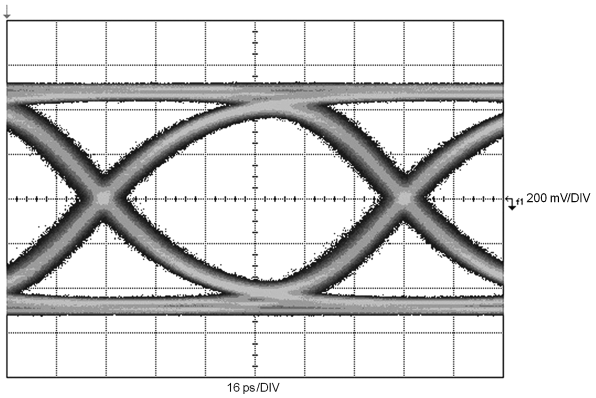

**Figure 11. TL = 20 inch 4–mil FR4 trace,
DS100KR401 settings: EQ[1:0] = R, R = 15'h, DEM[1:0] = float, float**

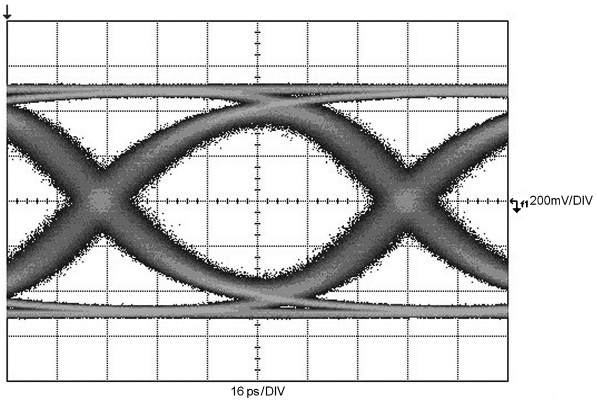

**Figure 12. TL = 30 inch 4–mil FR4 trace,
DS100KR401 settings: EQ[1:0] = float, R = 1F'h, DEM[1:0] = float, float**

Figure 13. Test Setup Connections Diagram

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TYPICAL CHARACTERISTICS (continued)

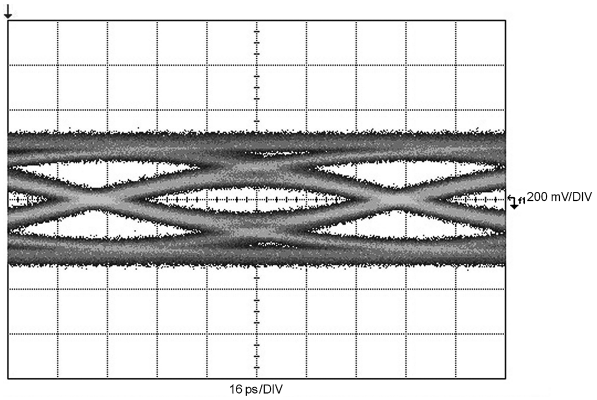

Figure 14. TL1 = 20 inch 4–mil FR4 trace, TL2 = 15 inch 4–mil FR4 trace, DS100KR401 settings: EQ[1:0] = R, R = 15'h, DEM[1:0] = float, float

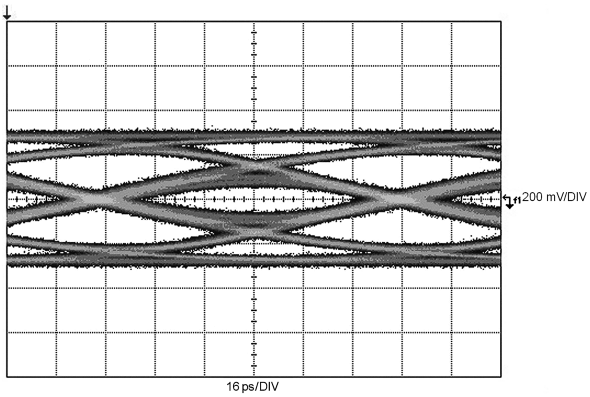

Figure 15. TL1 = 30 inch 4–mil FR4 trace, TL2 = 15 inch 4–mil FR4 trace, DS100KR401 settings: EQ[1:0] = float, R = 1F'h, DEM[1:0] = float, float

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS100KR401SQ/NOPB	ACTIVE	WQFN	NJY	54	2000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS100KR401SQ	Samples
DS100KR401SQE/NOPB	ACTIVE	WQFN	NJY	54	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS100KR401SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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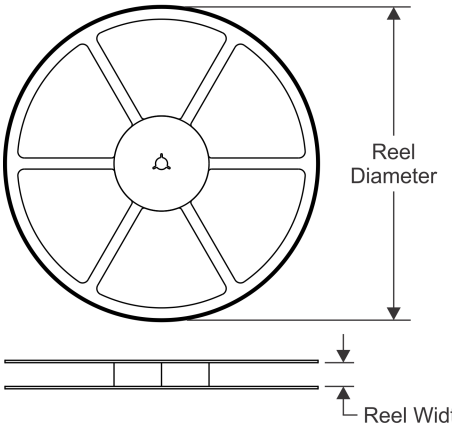
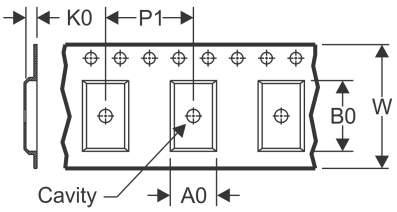
TAPE AND REEL INFORMATION

REEL DIMENSIONS

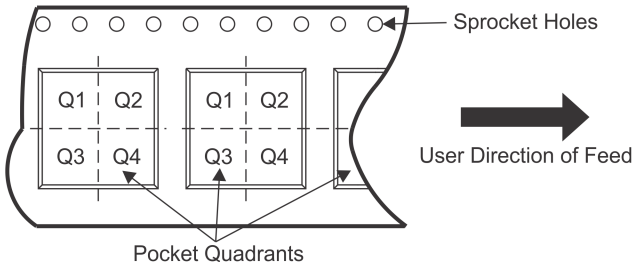


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

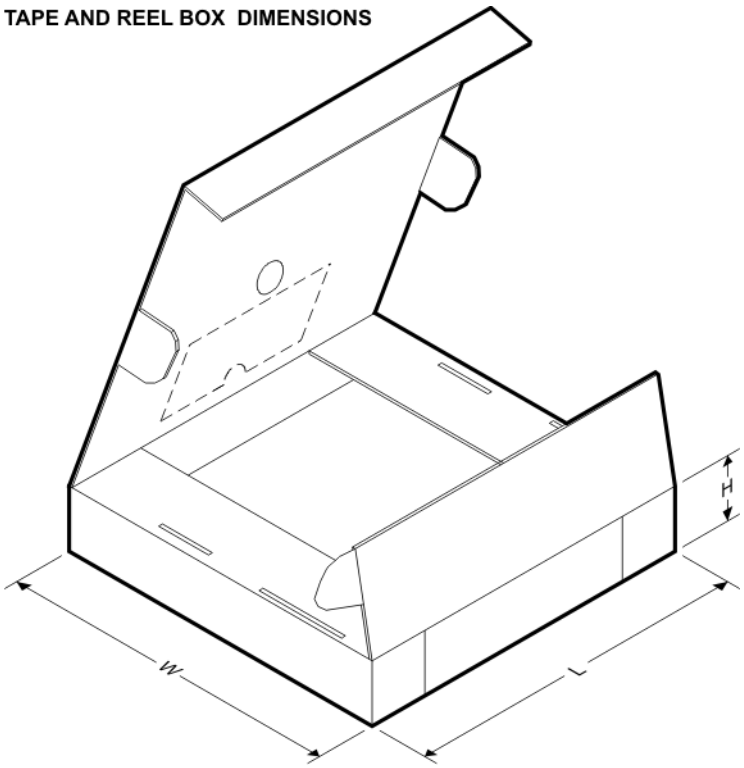
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

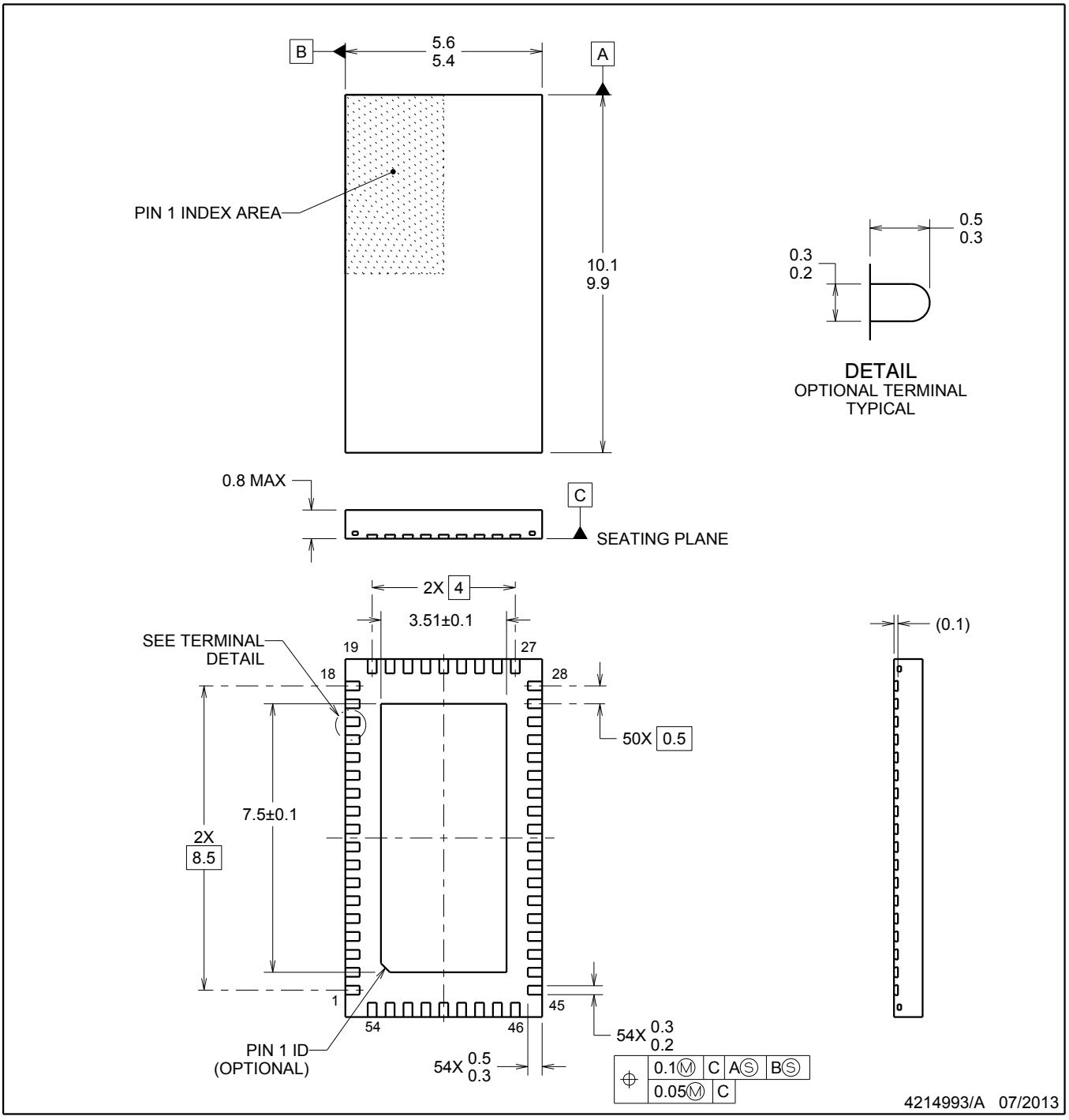
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS100KR401SQ/NOPB	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
DS100KR401SQE/NOPB	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



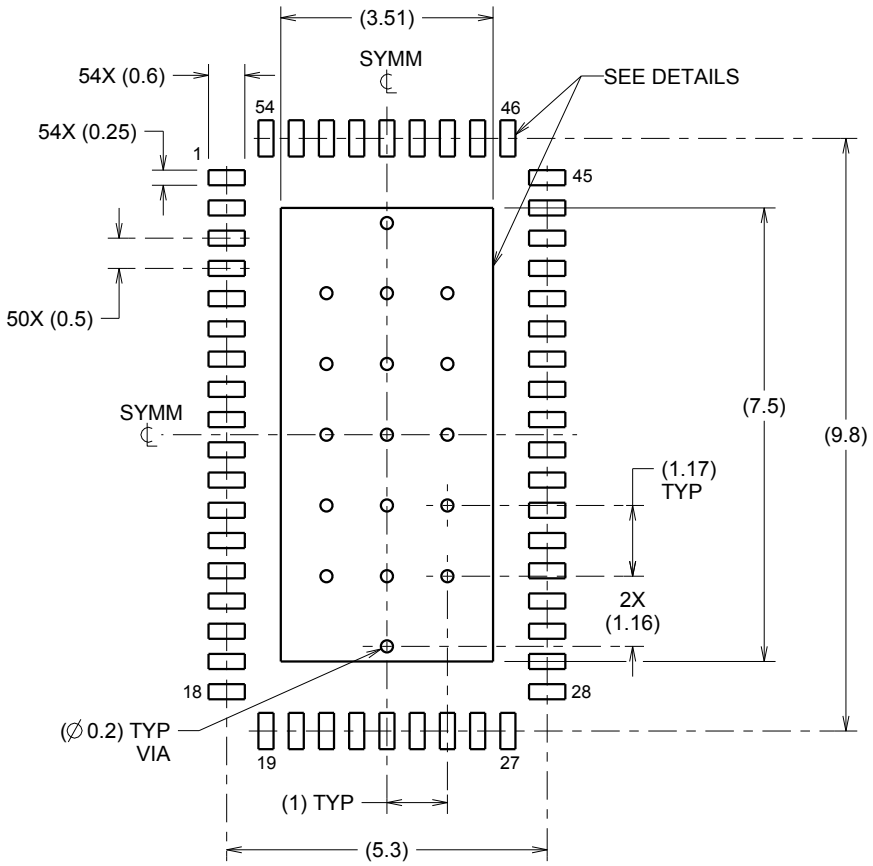
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS100KR401SQ/NOPB	WQFN	NJY	54	2000	367.0	367.0	38.0
DS100KR401SQE/NOPB	WQFN	NJY	54	250	213.0	191.0	55.0

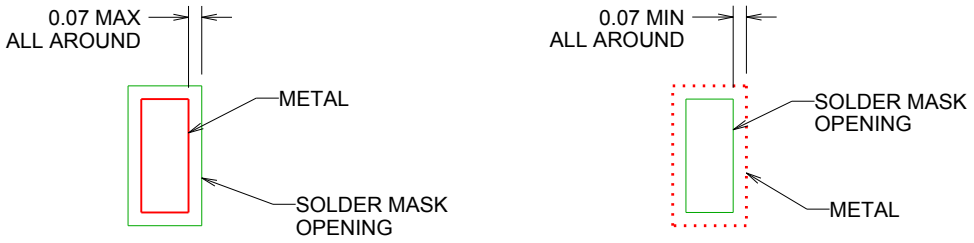


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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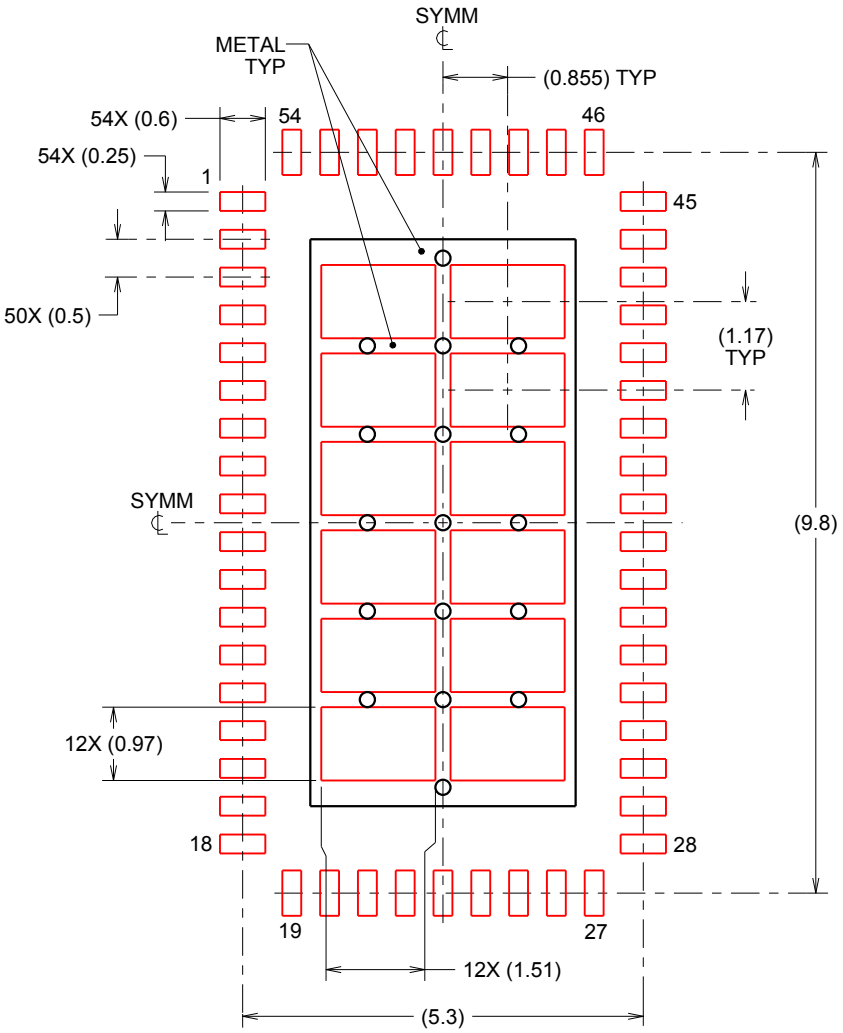
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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