DS8921/DS8921A/DS8921AT Differential Line Driver and Receiver Pair

Check for Samples: DS8921, DS8921A, DS8921AT

FEATURES

- **12 ns Typical Propagation Delay**
- **Output Skew - 0.5 ns Typical**
- **Meet the Requirements of EIA Standard RS-422**
- **Complementary Driver Outputs**
- **High Differential or Common-Mode Input Voltage Ranges of ±7V**
- **±0.2V Receiver Sensitivity over the Input Voltage Range**
- **Receiver Input Hysteresis-70 mV Typical**
- **DS8921AT Industrial Temperature Operation: (−40°C to +85°C)**

DESCRIPTION

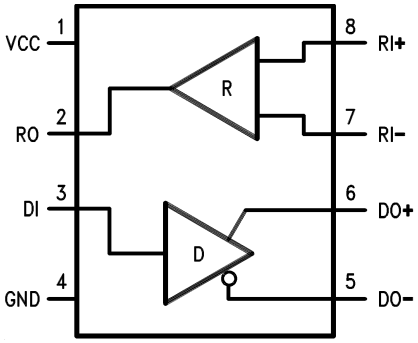
The DS8921, DS8921A are Differential Line Driver and Receiver pairs designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, these devices meet the requirements of the EIA Standard RS-422.

The DS8921, DS8921A receivers offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms.

The DS8921, DS8921A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

The DS8921, DS8921A are designed to be compatible with TTL and CMOS.

Connection Diagram



DS8921/DS8921A/DS8921AT
See Package Number D (R-PDSO-G8) or P (R-PDIP-T8)

Truth Table

Receiver		Driver		
Input	V_{OUT}	Input	V_{OUT}	$\overline{V_{OUT}}$
$V_{ID} \geq V_{TH}$ (MAX)	1	1	1	0
$V_{ID} \leq V_{TH}$ (MIN)	0	0	0	1
Open	1			

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage	7V
Driver Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Maximum Package Power Dissipation @ +25°C	
D Package	730 mW
P Package	1160 mW
Derate D Package	9.3 mW/°C above +25°C
Derate P Package	5.8 mW/°C above +25°C
Storage Temperature Range	−65°C to +165°C
Lead Temperature	+260°C
(Soldering, 4 sec.)	+260°C
Maximum Junction Temperature	+150°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The Table of Electrical Characteristics provides conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instrument Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)			
DS8921/DS8921A	0	70	°C
DS8921AT	−40	+85	°C

DS8921/DS8921A Electrical Characteristics (1)(2)(3)

Symbol	Conditions	Min	Typ	Max	Units
RECEIVER					
V_{TH}	−7V ≤ V_{CM} ≤ +7V	−200	±35	+200	mV
V_{HYST}	−7V ≤ V_{CM} ≤ +7V	15	70		mV
R_{IN}	V_{IN} = −7V, +7V (Other Input = GND)	4.0	6.0		kΩ
I_{IN}	V_{IN} = 10V			3.25	mA
	V_{IN} = −10V			−3.25	mA
V_{OH}	I_{OH} = −400 µA	2.5			V
V_{OL}	I_{OL} = 8 mA			0.5	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V	−15		−100	mA
DRIVER					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V		−40	−200	µA
I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V			20	µA
I_I	V_{CC} = MAX, V_{IN} = 7.0V			100	µA
V_{CL}	V_{CC} = MIN, I_{IN} = −18 mA			−1.5	V
V_{OH}	V_{CC} = MIN, I_{OH} = −20 mA	2.5			V
V_{OL}	V_{CC} = MIN, I_{OL} = +20 mA			0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5V			100	µA
$\lvert V_T \rvert - \lvert \overline{VT} \rvert$				0.4	V
V_T		2.0			V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$				0.4	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V	−30		−150	mA
DRIVER and RECEIVER					
I_{CC}	V_{CC} = MAX, V_{OUT} = Logic 0			35	mA

(1) All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.
(2) All typical values are V_{CC} = 5V, T_A = 25°C.
(3) Only one output at a time should be shorted.

Receiver Switching Characteristics

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF (Figure 1 and Figure 2)		14	22.5	20	20	ns
T_{pHL}	C_L = 30 pF (Figure 1 and Figure 2)		14	22.5	20	20	ns
$\lvert T_{pLH} - T_{pHL} \rvert$	C_L = 30 pF (Figure 1 and Figure 2)		0.5	5	3.5	5	ns

Driver Switching Characteristics

SINGLE ENDED CHARACTERISTICS

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF (Figure 3 and Figure 4)		10	15	15	15	ns
T_{pHL}	C_L = 30 pF		10	15	15	15	ns

Driver Switching Characteristics (continued)

SINGLE ENDED CHARACTERISTICS

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
	(Figure 3 and Figure 4)						
T_{TLH}	C_L = 30 pF (Figure 7 and Figure 8)		5	8	8	9.5	ns
T_{THL}	C_L = 30 pF (Figure 7 and Figure 8)		5	8	8	9.5	ns
Skew	CL = 30 pF(1) (Figure 3 and Figure 4)		1	5	3.5	3.5	ns

(1) Difference between complementary outputs at the 50% point.

Driver Switching Characteristics(1)

DIFFERENTIAL CHARACTERISTICS

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF		10	15	15	15	ns
	(Figure 3, Figure 5, and Figure 6)						
T_{pHL}	C_L = 30 pF		10	15	15	15	ns
	(Figure 3, Figure 5, and Figure 6)						
$\lvert T_{pLH} - T_{pHL} \rvert$	C_L = 30 pF		0.5	6	2.75	2.75	ns
	(Figure 3, Figure 5, and Figure 6)						

(1) Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE). The calculated ATE results assume a linear transition between measurement points and are a result of the following equations: $T_{cr} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$ Where: T_{cr} = Crossing Point T_{ra}, T_{rb}, T_{fa} and T_{fb} are time measurements with respect to the input. See Figure 6.

AC Test Circuits and Switching Diagrams

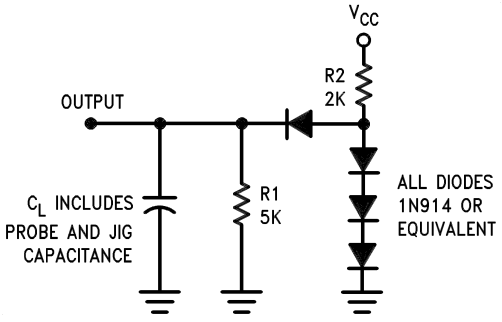


Figure 1.

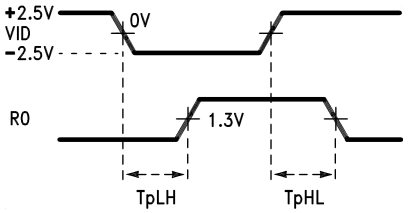


Figure 2.

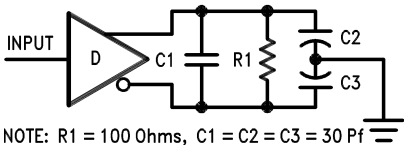


Figure 3.

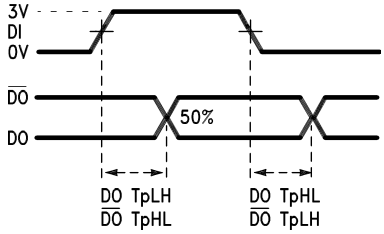


Figure 4.

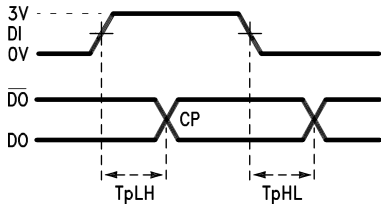


Figure 5.

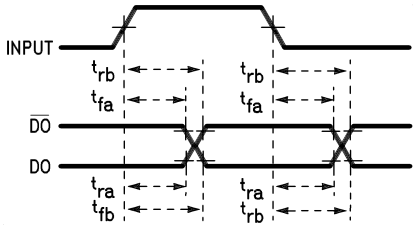


Figure 6.

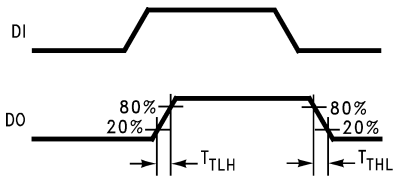


Figure 7.

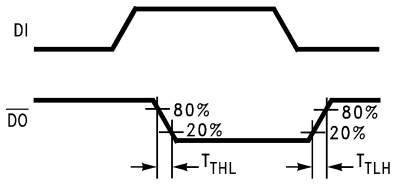


Figure 8.

TYPICAL APPLICATIONS

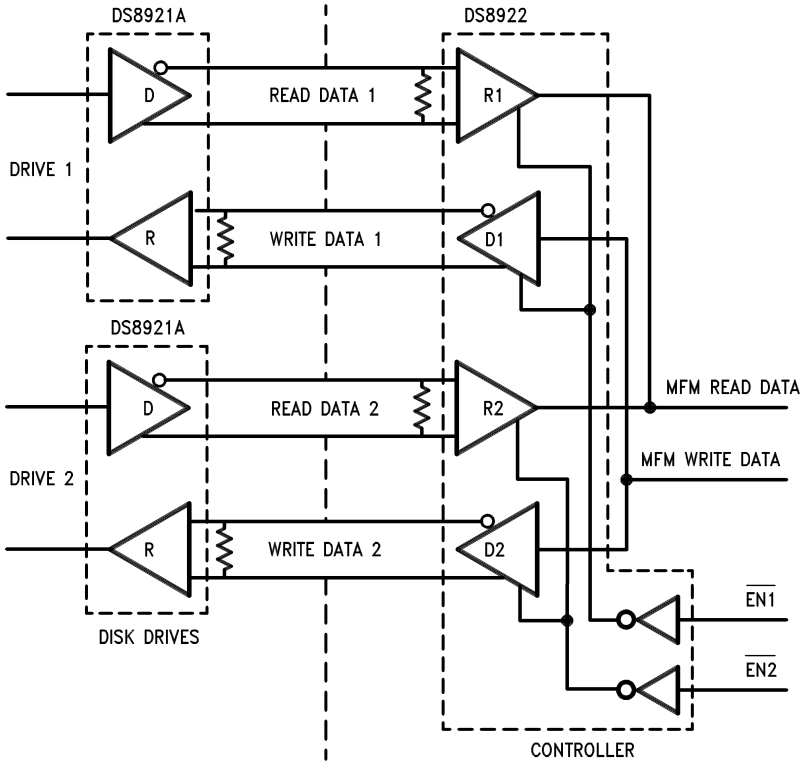


Figure 9. ST506 and ST412 Application

Figure 10.

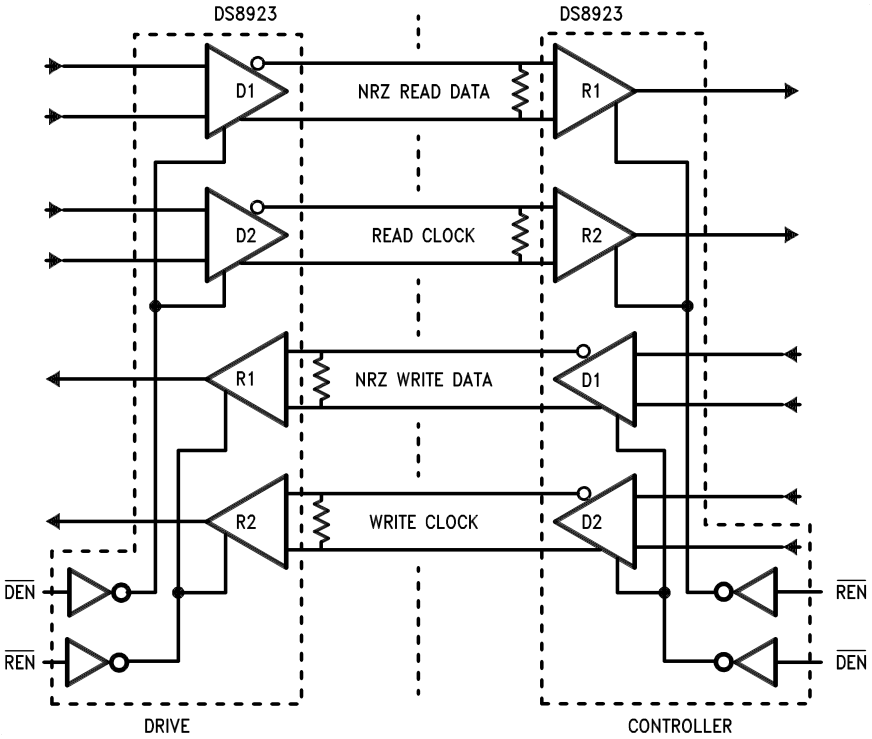


Figure 11. ESDI Application

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS8921AM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	DS89 21AM	
DS8921AM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS89 21AM	Samples
DS8921AMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	DS89 21AM	
DS8921AMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS89 21AM	Samples
DS8921ATM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	DS892 1ATM	
DS8921ATM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS892 1ATM	Samples
DS8921M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	DS892 1M	
DS8921M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS892 1M	Samples
DS8921MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS892 1M	Samples
DS8921N	NRND	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	DS8921N	
DS8921N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-1-NA-UNLIM	0 to 70	DS8921N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

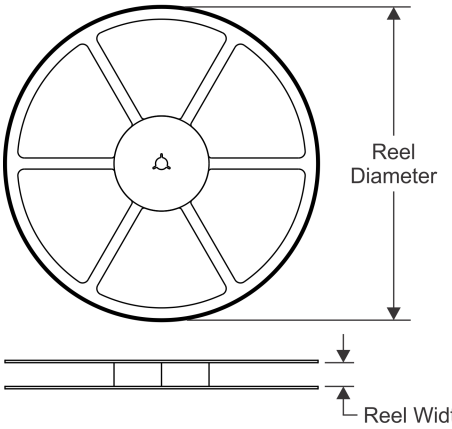
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

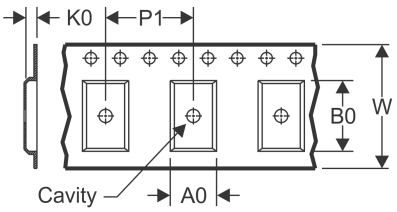
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

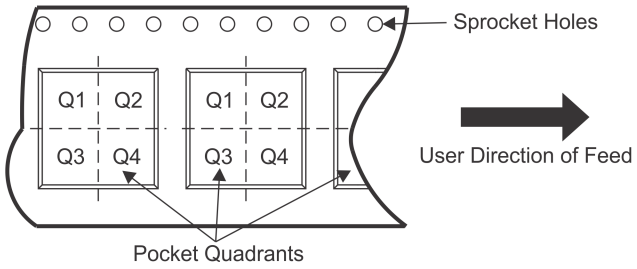


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

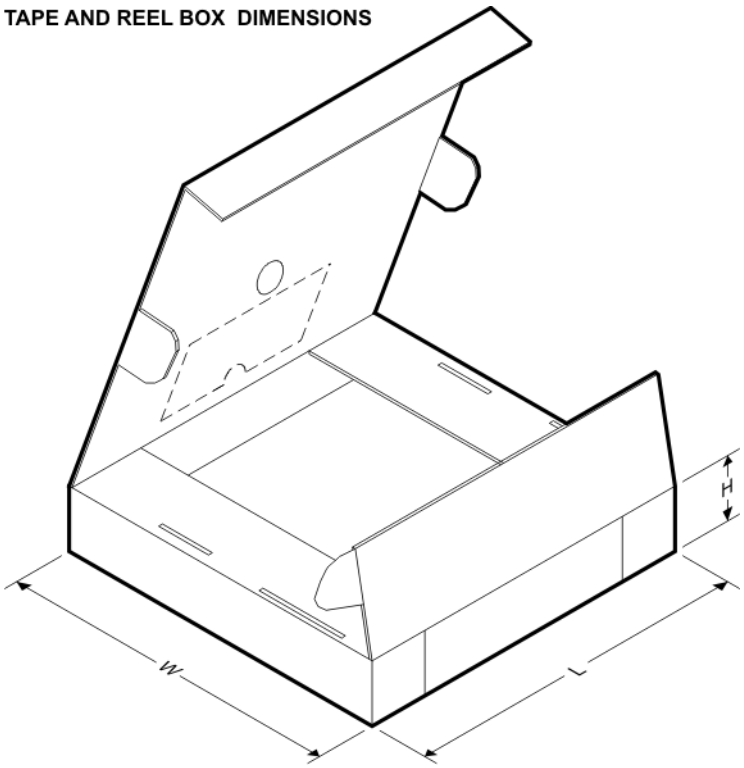
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS8921AMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS8921AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS8921MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

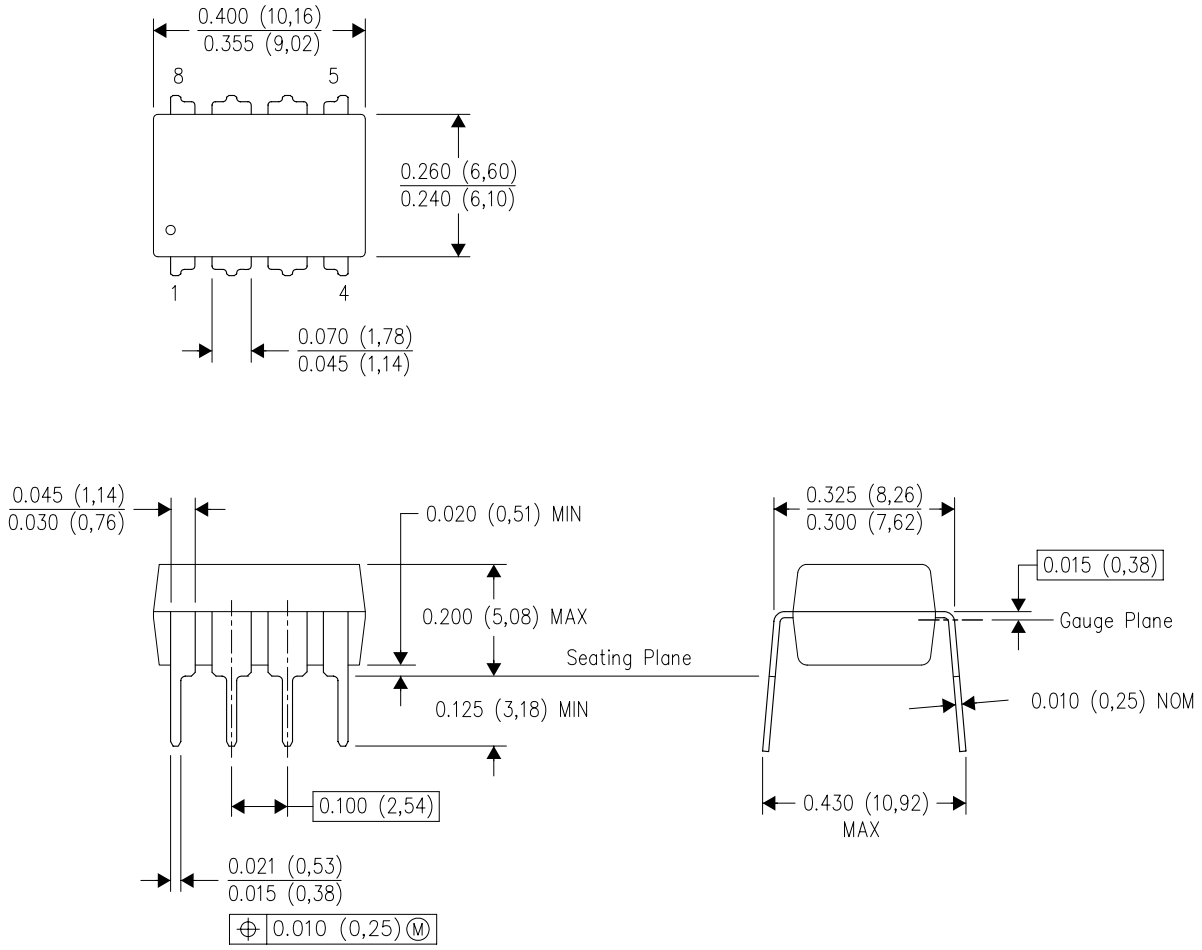
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

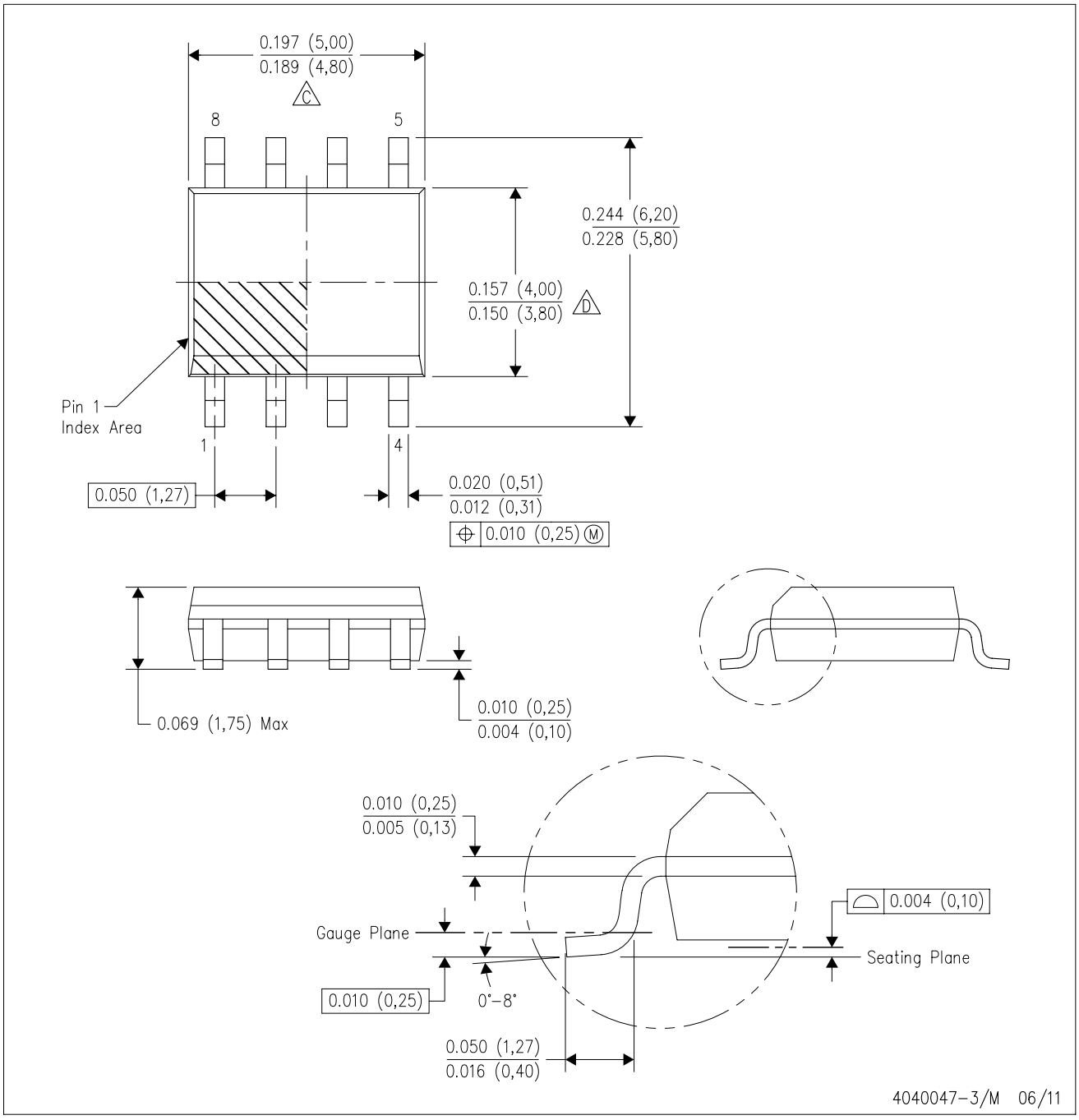
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS8921AMX	SOIC	D	8	2500	367.0	367.0	35.0
DS8921AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
DS8921MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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