DS90C401 Dual Low Voltage Differential Signaling (LVDS) Driver

Check for Samples: DS90C401

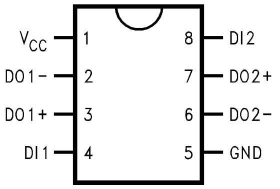
FEATURES

- **Ultra Low Power Dissipation**
- **Operates Above 155.5 Mbps**
- **Standard TIA/EIA-644**
- **8 Lead SOIC Package Saves Space**
- **Low Differential Output Swing typical 340 mV**

DESCRIPTION

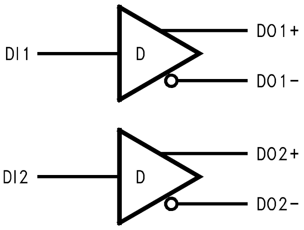
The DS90C401 is a dual driver device optimized for high data rate and low power applications. This device along with the DS90C402 provides a pair chip solution for a dual high speed point-to-point interface. The DS90C401 is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is in a 8 lead small outline package. The differential driver outputs provides low EMI with its low output swings typically 340 mV.

Connection Diagram



See Package Number D (SOIC)

Functional Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})		−0.3V to +6V
Input Voltage (D_{IN})		−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-})		−0.3V to (V_{CC} + 0.3V)
Short Circuit Duration (D_{OUT+}, D_{OUT-})		Continuous
Maximum Package Power Dissipation @ +25°C	D Package	1068 mW
	Derate D Package	8.5 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)		+260°C
Maximum Junction Temperature		+150°C
ESD Rating[3]	(HBM, 1.5 kΩ, 100 pF)	≥ 3,500V
	(EIAJ, 0 Ω, 200 pF)	≥ 250V

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) ESD Ratings:
HBM (1.5 kΩ, 100 pF) ≥ 3,500V
EIAJ (0Ω, 200 pF) ≥ 250V

Recommended OperatingConditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (Figure 1)	D_{OUT-}, D_{OUT+}	250	340	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High	R_L = 100Ω			1.41	1.60	V
V_{OL}	Output Voltage Low			0.90	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V[3]			−3.5	−5.0	mA
V_{IH}	Input Voltage High		D_{IN}	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_I	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V		−10	±1	+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{CC}	No Load Supply Current	D_{IN} = V_{CC} or GND	V_{CC}		1.7	3.0	mA
		D_{IN} = 2.5V or 0.4V			3.5	5.5	mA
I_{CCL}	Loaded Supply Current	R_L = 100Ω All Channels V_{IN} = V_{CC} or GND (all inputs)			8	14.0	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.
(2) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Switching Characteristics

V_{CC} = +5.0V ±10%, T_A = −40°C to +85°C (1)(2)(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (Figure 2 and Figure 3)	0.5	2.0	3.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.5	2.1	3.5	ns
t_{SKD}	Differential Skew $\|t_{PHLD} – t_{PLHD}\|$		0	80	900	ps
t_{SK1}	Channel-to-Channel Skew (2)		0	0.3	1.0	ns
t_{SK2}	Chip to Chip Skew (3)				3.0	ns
t_{TLH}	Rise Time			0.35	2.0	ns
t_{THL}	Fall Time			0.35	2.0	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(2) Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
(3) Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 6 ns, and t_f ≤ 6 ns.
(5) C_L includes probe and jig capacitance.

Parameter Measurement Information

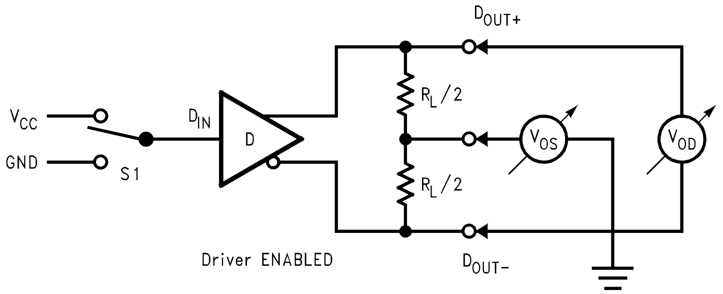


Figure 1. Driver V_{OD} and V_{OS} Test Circuit

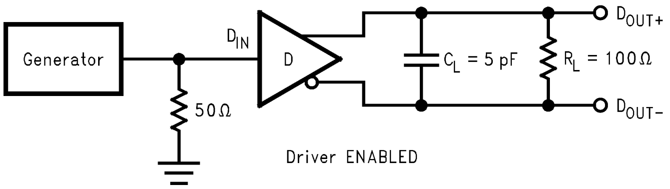


Figure 2. Driver Propagation Delay and Transition Time Test Circuit

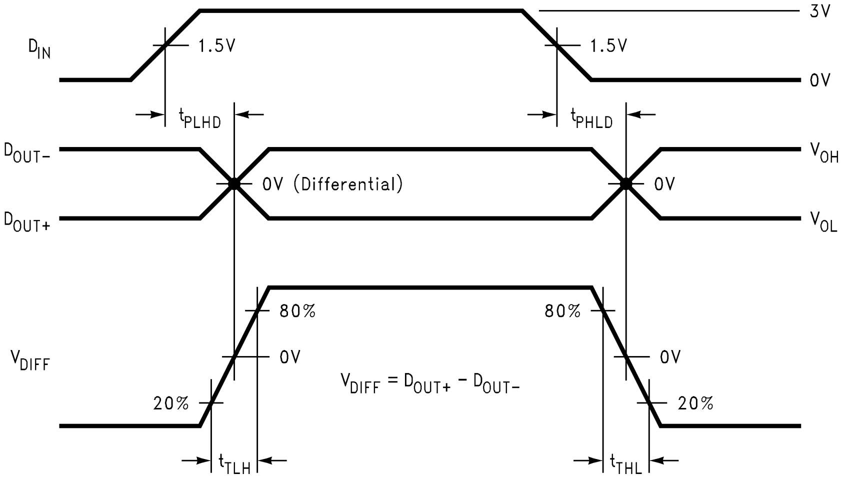


Figure 3. Driver Propagation Delay and Transition Time Waveforms

TYPICAL APPLICATION

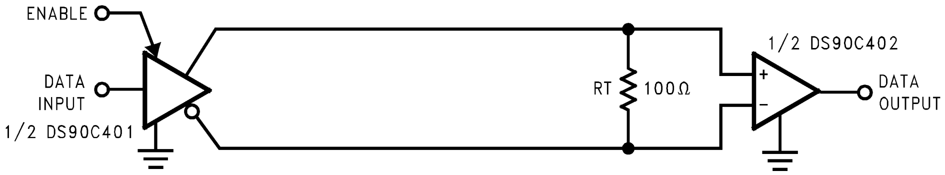


Figure 4. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 4. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C401 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is mere 3.4 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 4. AC or unterminated configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the 100Ω termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340 mV – 100 mV = 240 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 5. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

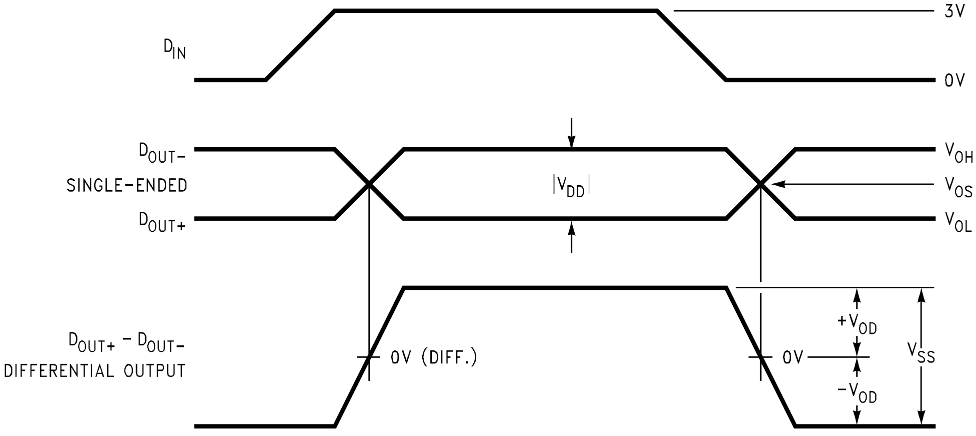


Figure 5. Driver Output Levels

PIN DESCRIPTIONS

Pin No.	Name	Description
4, 8	D_{IN}	TTL/CMOS driver input pins
3, 7	D_{OUT+}	Non-inverting driver output pin
2, 6	D_{OUT-}	Inverting driver output pin
5	GND	Ground pin
1	V_{CC}	Positive power supply pin, +5.0V ± 10%

Truth Table[1]

D_{IN}	D_{OUT+}	D_{OUT-}
L	L	H
H	H	L
D_{IN} > 0.8V and D_{IN} < 2.0V	X	X

[1] H = Logic high level
L = Logic low level
X = Indeterminant state

Typical Performance Characteristics

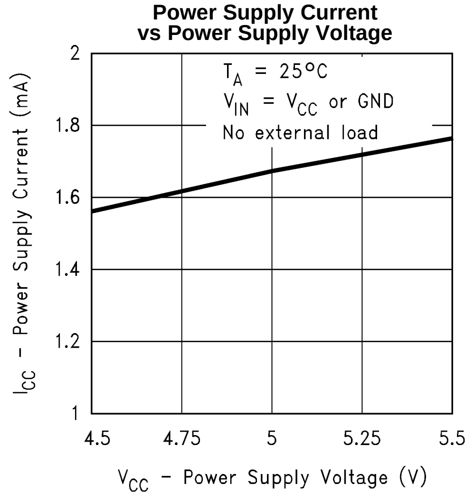

Power Supply Current vs Power Supply Voltage

Figure 6.

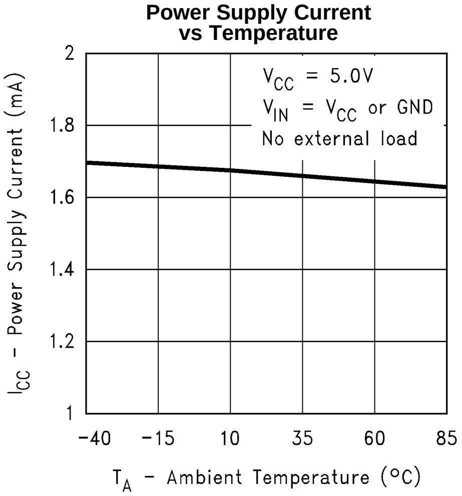

Power Supply Current vs Temperature

Figure 7.

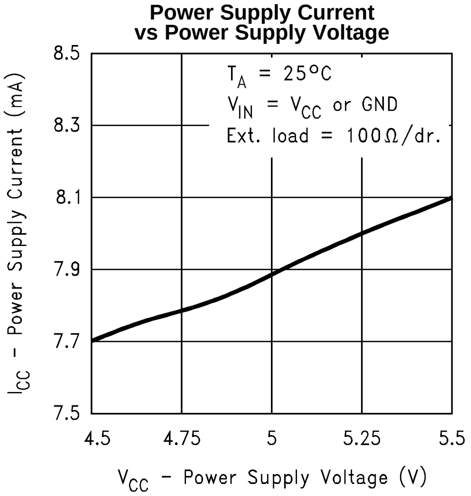

Power Supply Current vs Power Supply Voltage

Figure 8.

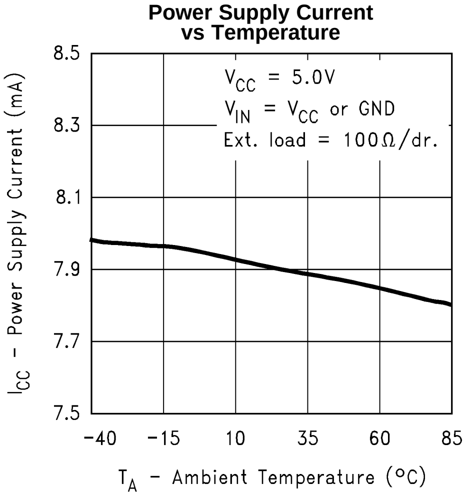

Power Supply Current vs Temperature

Figure 9.

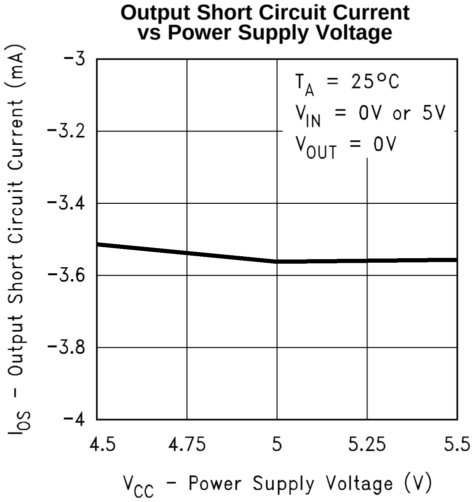

Output Short Circuit Current vs Power Supply Voltage

Figure 10.

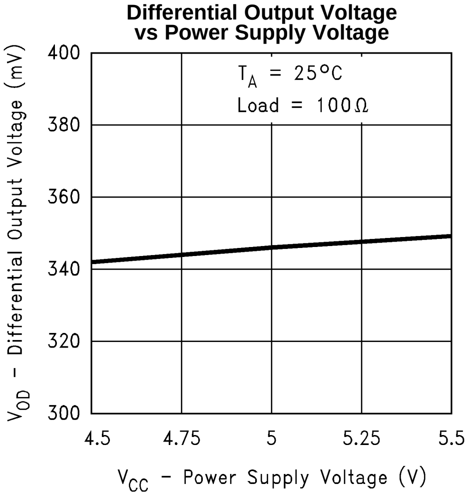

Differential Output Voltage vs Power Supply Voltage

Figure 11.

Typical Performance Characteristics (continued)

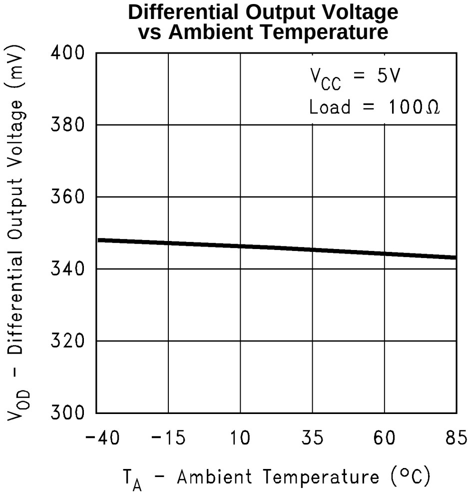


Figure 12.

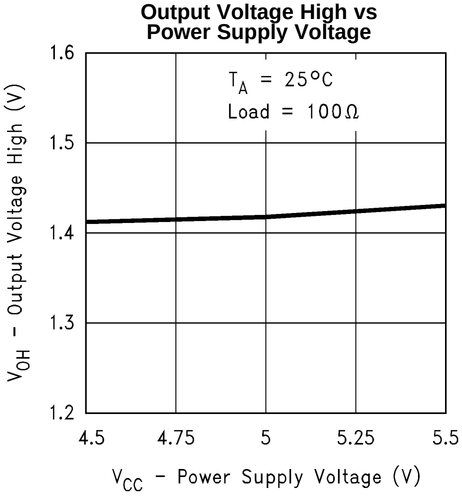


Figure 13.

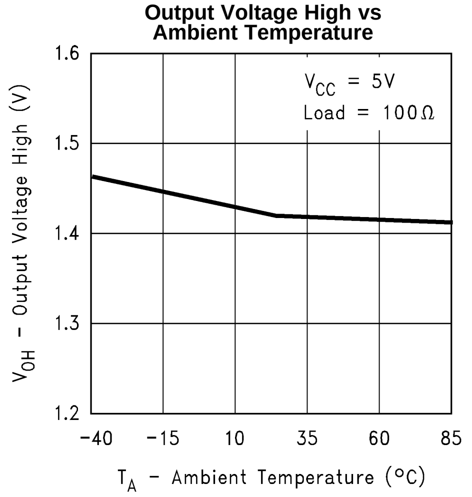


Figure 14.

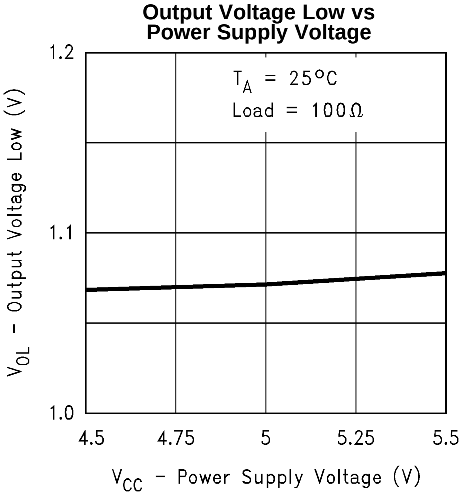


Figure 15.

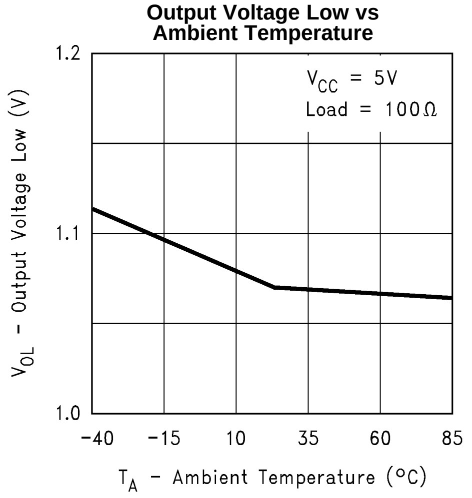


Figure 16.

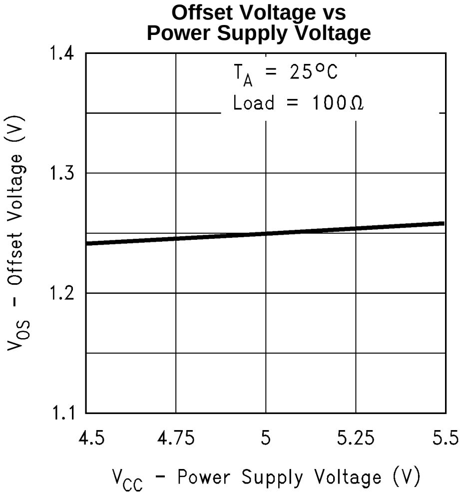
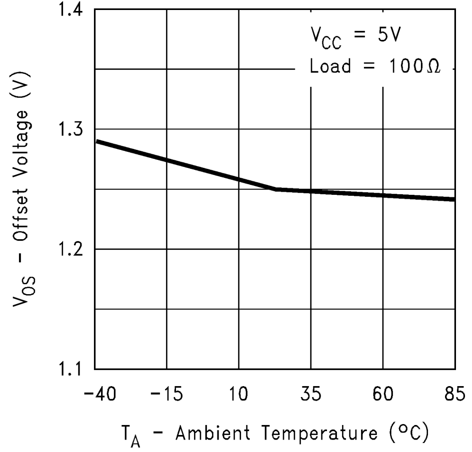


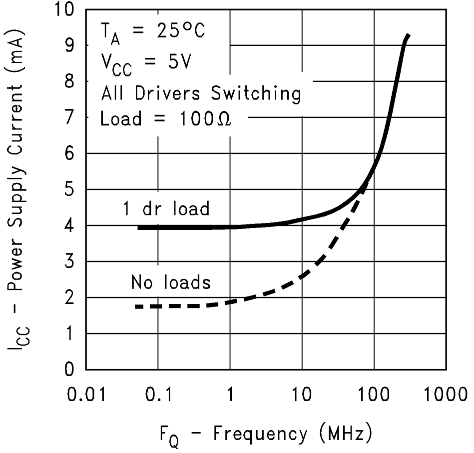
Figure 17.

Typical Performance Characteristics (continued)



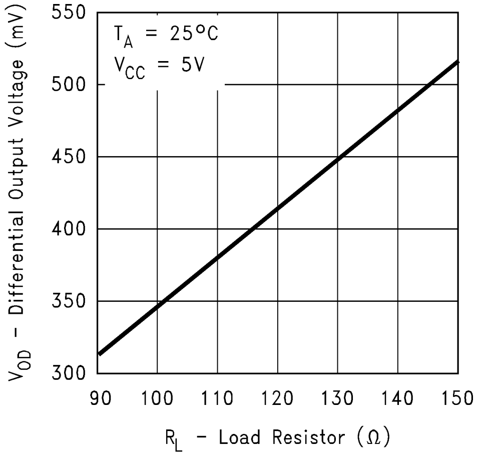
Offset Voltage vs Ambient Temperature

Figure 18.



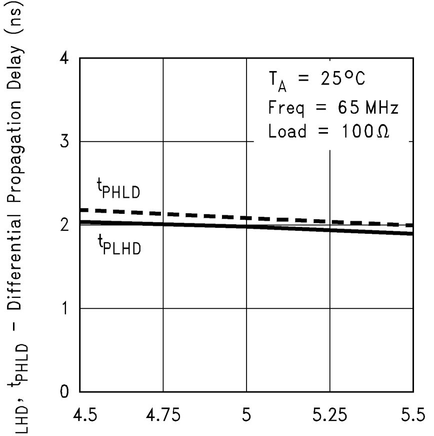
Power Supply Current vs Frequency

Figure 19.



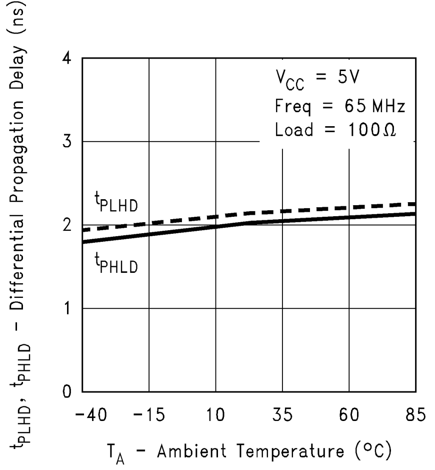
Differential Output Voltage vs Load Resistor

Figure 20.



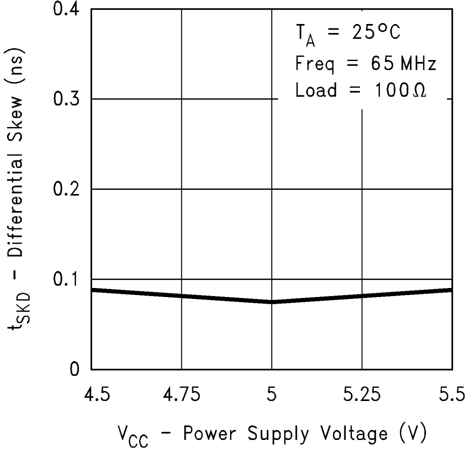
Differential Propagation Delay vs Power Supply Voltage

Figure 21.



Differential Propagation Delay vs Ambient Temperature

Figure 22.



Differential Skew vs Power Supply Voltage

Figure 23.

Typical Performance Characteristics (continued)

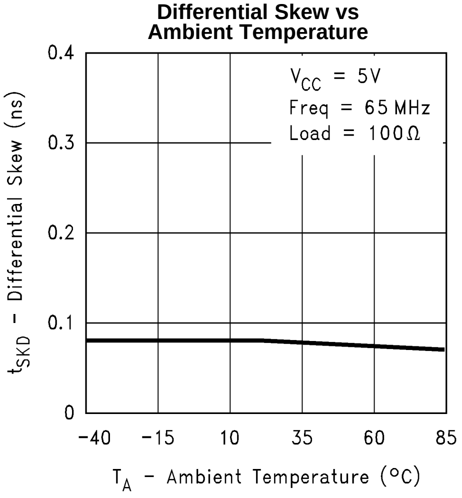


Figure 24.

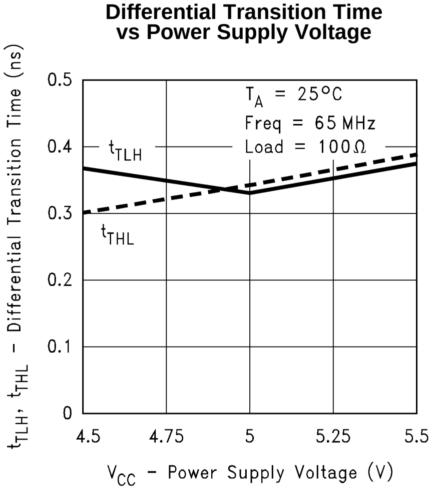


Figure 25.

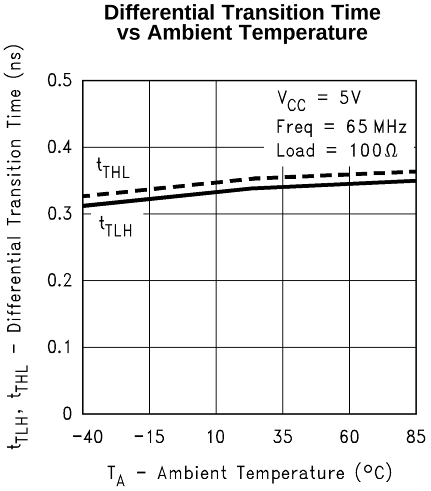


Figure 26.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	**Page**
• Changed layout of National Data Sheet to TI format	9

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C401M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI		DS90C 401M	
DS90C401M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		DS90C 401M	Samples
DS90C401MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI		DS90C 401M	
DS90C401MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		DS90C 401M	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

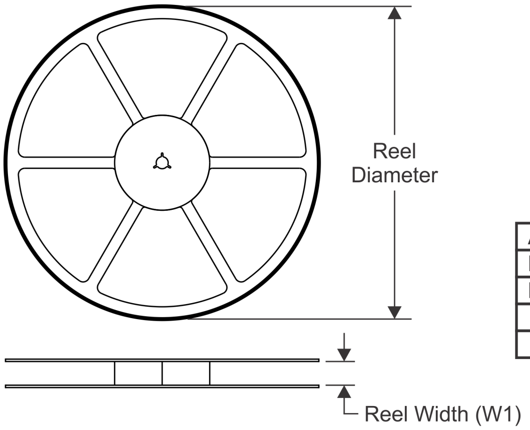
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

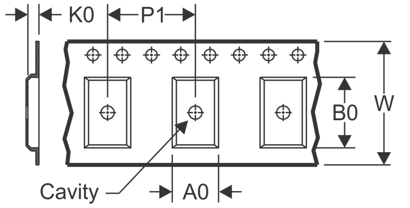
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

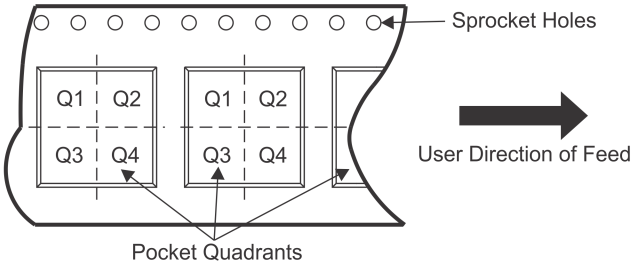


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

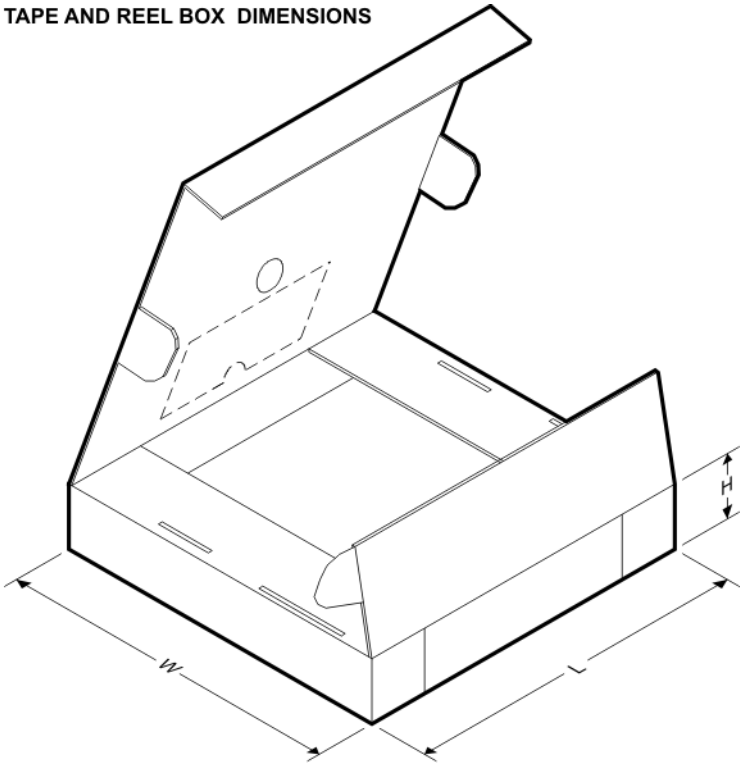
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C401MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS90C401MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

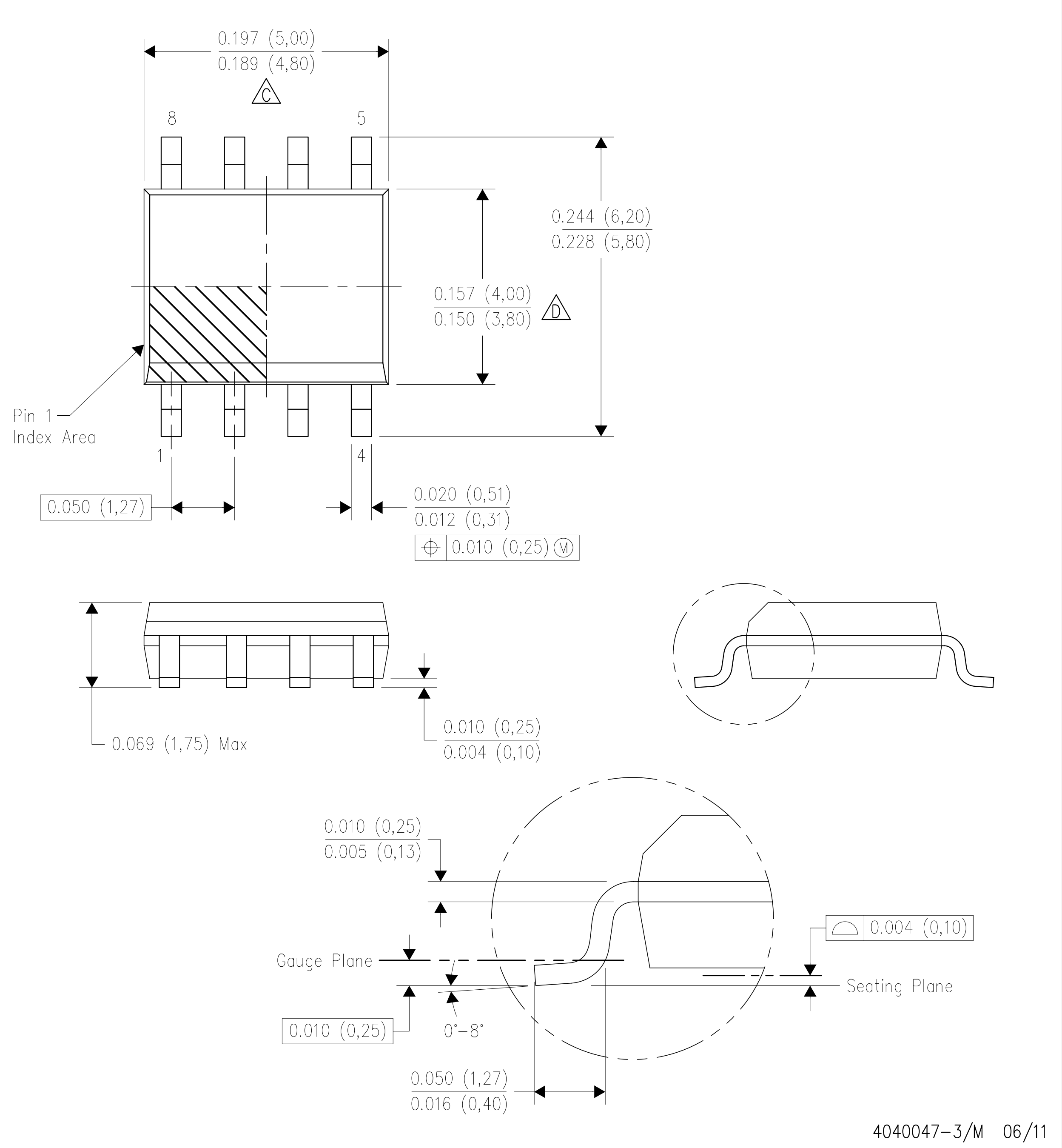
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C401MX	SOIC	D	8	2500	367.0	367.0	35.0
DS90C401MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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