DS90LV028AQ Automotive LVDS Dual Differential Line Receiver

Check for Samples: DS90LV028AQ, DS90LV028AQ-Q1

FEATURES

- **AECQ-100 Grade 1**
- **-40°C to +125°C Operating Temperature Range**
- **>400 Mbps (200 MHz) Switching Rates**
- **50 ps Differential Skew (Typical)**
- **0.1 ns Channel-to-Channel Skew (Typical)**
- **2.5 ns Maximum Propagation Delay**
- **3.3V Power Supply Design**
- **Flow-Through Pinout**
- **Power Down High Impedance on LVDS Inputs**
- **Low Power design (18mW @ 3.3V static)**
- **LVDS Inputs Accept LVDS/CML/LVPECL Signals**
- **Conforms to ANSI/TIA/EIA-644 Standard**
- **Available in SOIC Package**

DESCRIPTION

The DS90LV028AQ is a dual CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV028AQ accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The DS90LV028AQ has a flow-through design for easy PCB layout.
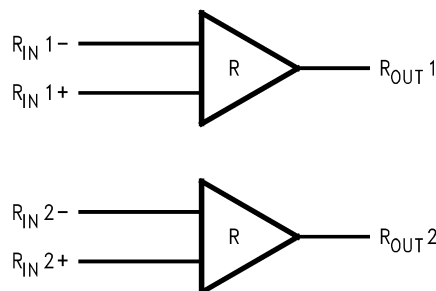
The DS90LV028AQ and companion LVDS line driver DS90LV027AQ provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Connection Diagram
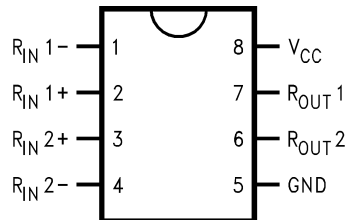
Figure 1. SOIC
See Package Number D0008A

Functional Diagram

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Truth Table

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	R_{OUT}
$V_{ID} \geq 0.1V$	H
$V_{ID} \leq -0.1V$	L

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2]

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage ($R_{IN}+$, $R_{IN}-$)	−0.3V to +3.9V
Output Voltage (R_{OUT})	−0.3V to V_{CC} + 0.3V
Maximum Package Power Dissipation @ +25°C	
D Package	1068 mW
Derate D Package	9.71 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	103.0°C/W
θ_{JC}	41.0°C/W
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering	
(4 sec.)	+260°C
Maximum Junction Temperature	+135°C
ESD Rating	
HBM [3]	≥ 8 kV
MM [4]	≥ 250 V
CDM [5]	≥ 1250 V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		3.0	V
Operating Free Air				
Temperature (T_A)	−40	25	+125	°C

Product Folder Links: *DS90LV028AQ DS90LV028AQ-Q1*

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. [1][2]

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V, 0V, 3V		R_{IN}+, R_{IN}−			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.8V	V_{CC} = 3.6V or 0V		−10	±1	+10	µA
		V_{IN} = 0V			−10	±1	+10	µA
		V_{IN} = +3.6V	V_{CC} = 0V		-20		+20	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	2.7	3.1		V
		I_{OH} = −0.4 mA, Inputs terminated			2.7	3.1		V
		I_{OH} = −0.4 mA, Inputs shorted			2.7	3.1		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.3	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V [3]			−15	−50	−100	mA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current	Inputs Open		V_{CC}		5.4	9	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).
(2) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. [1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 15 pF	1.0	1.6	2.5	ns
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200 mV	1.0	1.7	2.5	ns
t_{SKD1}	Differential Pulse Skew $|t_{PHLD} − t_{PLHD}|$ [4]	(Figure 2 and Figure 3)	0	50	650	ps
t_{SKD2}	Differential Channel-to-Channel Skew-same device [5]		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew [6]		0		1.0	ns
t_{SKD4}	Differential Part to Part Skew [7]		0		1.5	ns
t_{TLH}	Rise Time			325	800	ps
t_{THL}	Fall Time			225	800	ps
f_{MAX}	Maximum Operating Frequency [8]			250		MHz

(1) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(2) C_L includes probe and jig capacitance.
(3) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(4) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(5) t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(6) t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(7) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(8) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), load = 15 pF (stray plus probes).
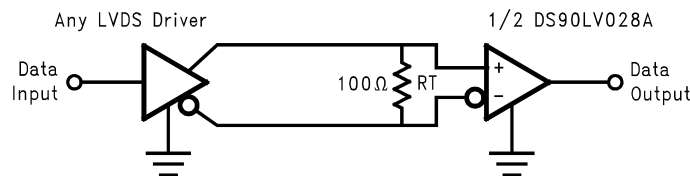
Parameter Measurement Information
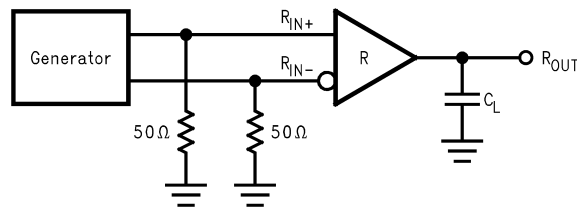
Figure 2. Receiver Propagation Delay and Transition Time Test Circuit
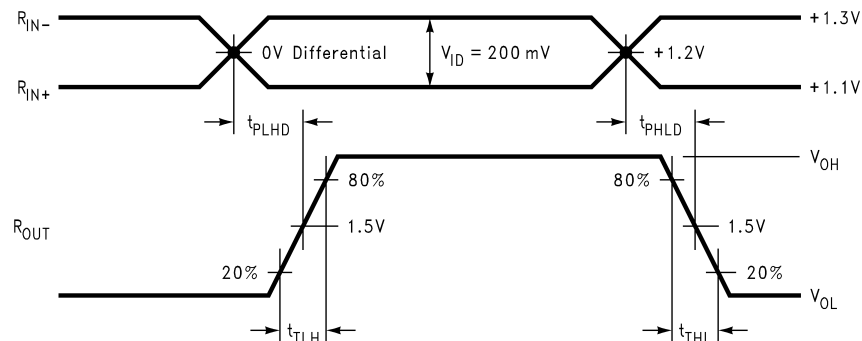
Figure 3. Receiver Propagation Delay and Transition Time Waveforms

Typical Application

**Figure 4. Balanced System
Point-to-Point Application**

APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual at www.ti.com.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 4. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV028AQ differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{CC}, but exceeding V_{CC} will turn on the ESD protection circuitry which will clamp the bus voltages.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1µF and 0.01µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194, "Failsafe Biasing of LVDS Interfaces" (SNLA051)for more information.

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.
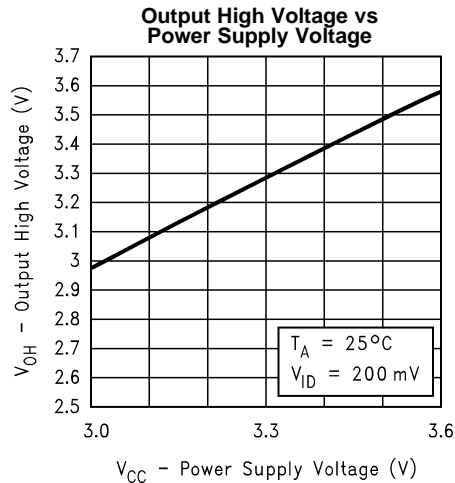
Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.
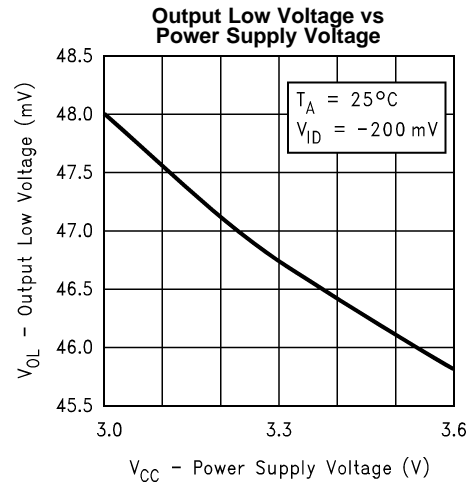
PIN DESCRIPTIONS

Pin Number	Name	Description
1, 4	R_{IN}-	Inverting receiver input pin
2, 3	R_{IN}+	Non-inverting receiver input pin
6, 7	R_{OUT}	Receiver output pin
8	V_{CC}	Power supply pin, +3.3V ± 0.3V
5	GND	Ground pin

Product Folder Links: *DS90LV028AQ DS90LV028AQ-Q1*

Typical Performance Curves

Figure 5. Output High Voltage vs Power Supply Voltage

Figure 6. Output Low Voltage vs Power Supply Voltage

Figure 7. Output Short Circuit Current vs Power Supply Voltage

Figure 8. Differential Transition Voltage vs Power Supply Voltage

Figure 9. Power Supply Current vs Frequency

Figure 10. Differential Propagation Delay vs Power Supply Voltage
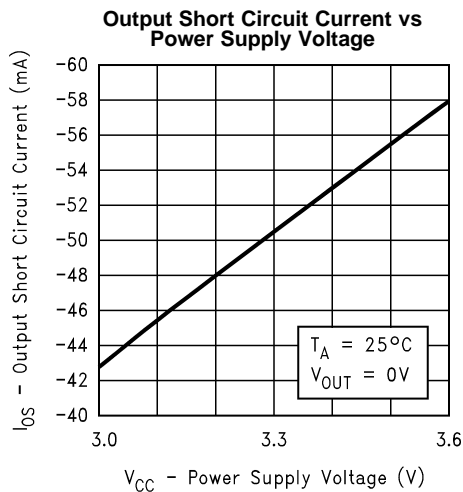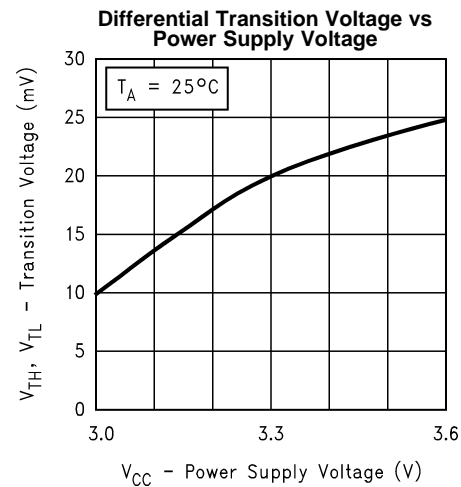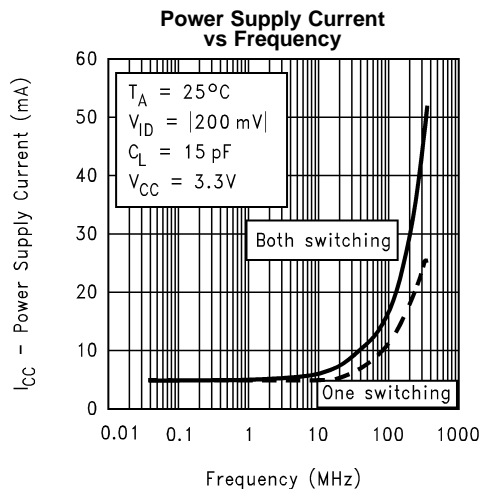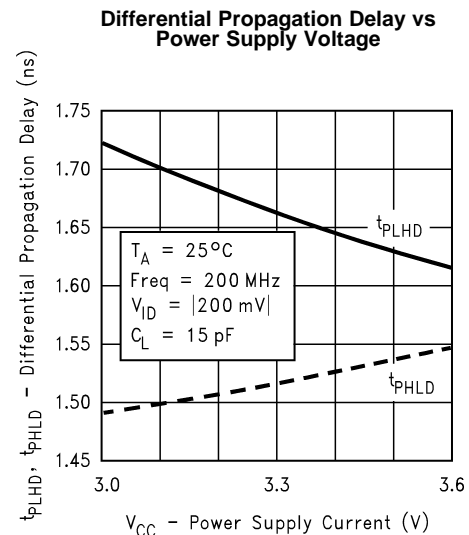
Typical Performance Curves (continued)

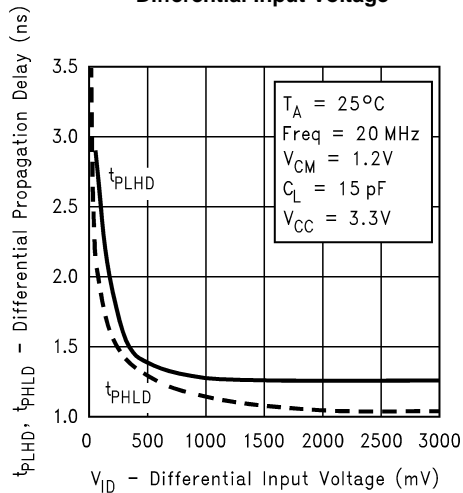**Differential Propagation Delay vs Differential Input Voltage**

Figure 11.

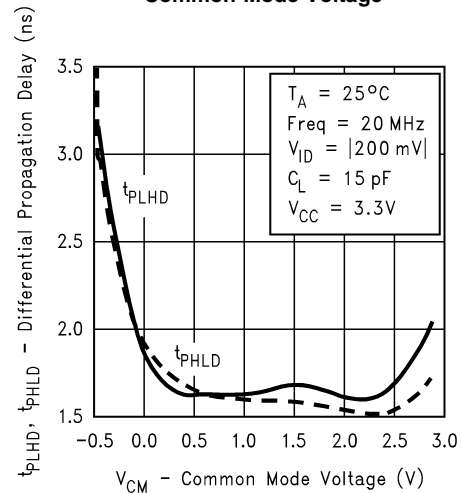**Differential Propagation Delay vs Common-Mode Voltage**

Figure 12.

Transition Time vs Power Supply Voltage
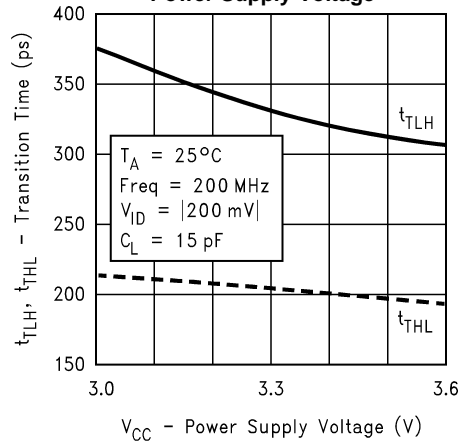
Figure 13.

Differential Skew vs Power Supply Voltage

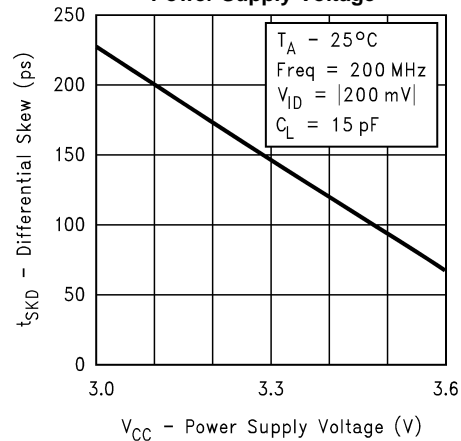

Figure 14.

Differential Propagation Delay vs Load
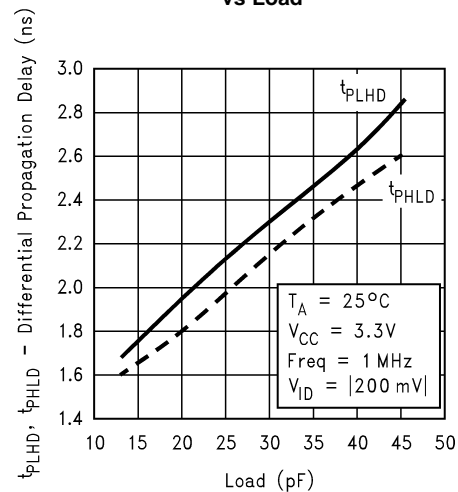
Figure 15.

Differential Propagation Delay vs Load
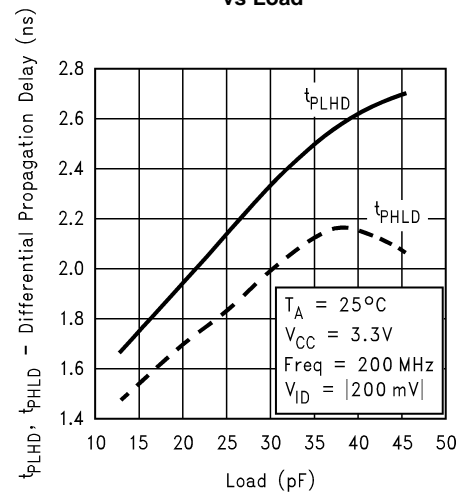
Figure 16.
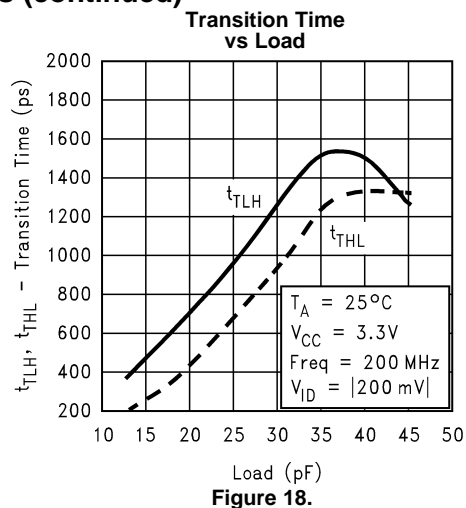
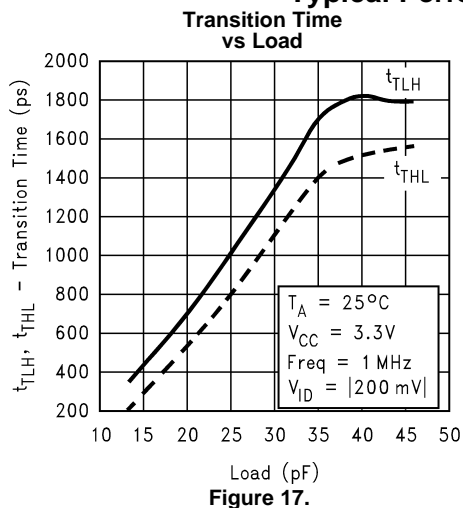Product Folder Links: DS90LV028AQ DS90LV028AQ-Q1

Typical Performance Curves (continued)

Figure 17.

Figure 18.

Product Folder Links: *DS90LV028AQ DS90LV028AQ-Q1*

REVISION HISTORY

Product Folder Links: *DS90LV028AQ DS90LV028AQ-Q1*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90LV028AQMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AQM	Samples
DS90LV028AQMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AQM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV028AQMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV028AQMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
⟨C⟩

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00) ⟨D⟩
0.150 (3,80)

Pin 1
Index Area

1   4

0.050 (1,27)   0.020 (0,51)
                            0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max   0.010 (0,25)
                            0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

⌂ 0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
     ⟨C⟩   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
           not exceed 0.006 (0,15) each side.
     ⟨D⟩   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.

TEXAS INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		