To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

3806 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3806 group is 8-bit microcomputer based on the 740 family core technology.

The 3806 group is designed for controlling systems that require analog signal processing and include two serial I/O functions, A-D converters, and D-A converters.

The various microcomputers in the 3806 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3806 group, refer to the section on group expansion.

FEATURES

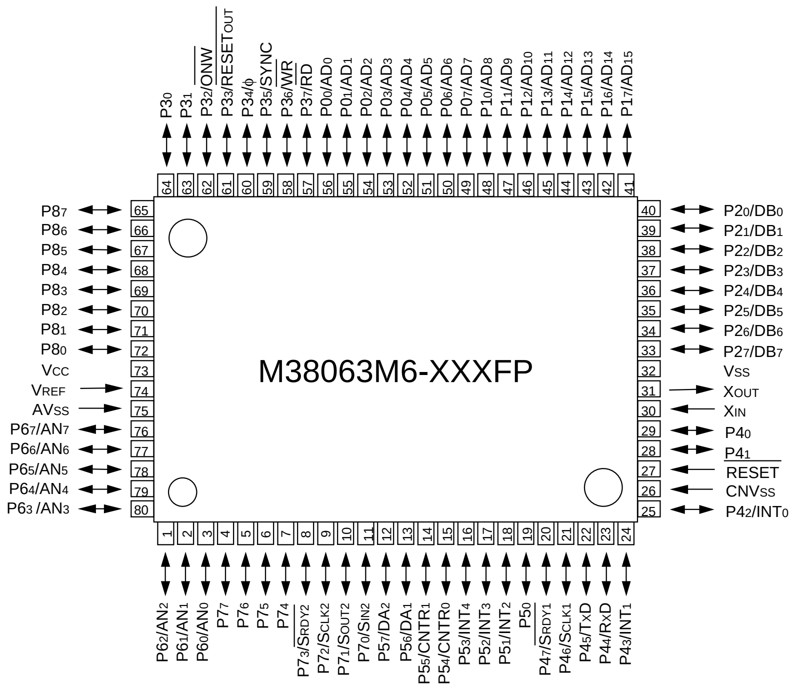
- Basic machine-language instructions 71
- Memory size
  - ROM .... 12 K to 48 K bytes
  - RAM .... 384 to 1024 bytes
- Programmable input/output ports 72
- Interrupts .... 16 sources, 16 vectors
- Timers .... 8 bit × 4
- Serial I/O1 .... 8-bit × 1 (UART or Clock-synchronized)
- Serial I/O2 ....8-bit × 1 (Clock-synchronized)
- A-D converter .... 8-bit × 8 channels
- D-A converter .... 8-bit × 2 channels
- Clock generating circuit .... Internal feedback resistor (connect to external ceramic resonator or quartz-crystal)
- Memory expansion possible

Specification (unit)	Standard	Extended operating temperature version	High-speed version
Minimum instruction execution time (µs)	0.5	0.5	0.4
Oscillation frequency (MHz)	8	8	10
Power source voltage (V)	3.0 to 5.5	4.0 to 5.5	2.7 to 5.5
Power dissipation (mW)	32	32	40
Operating temperature range (°C)	–20 to 85	–40 to 85	–20 to 85

APPLICATIONS

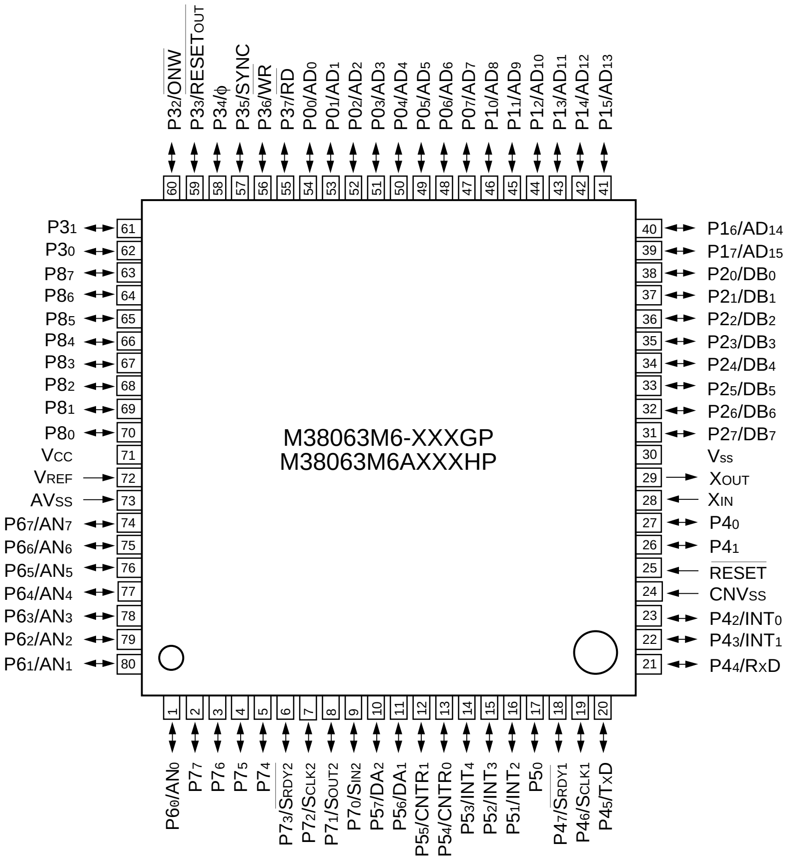
Office automation, VCRs, tuners, musical instruments, cameras, air conditioners, etc.

PIN CONFIGURATION (TOP VIEW)



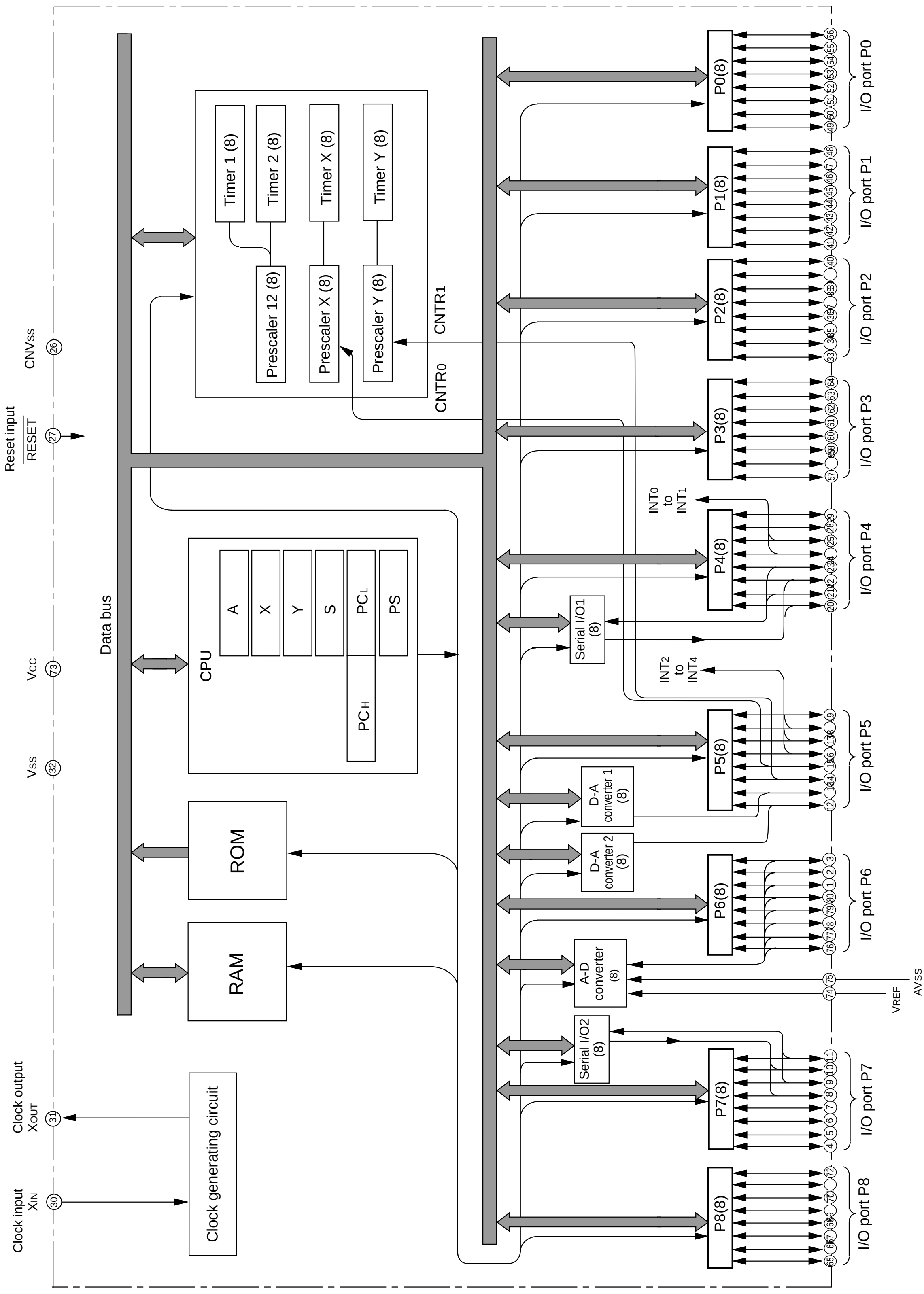
Package type : 80P6N-A
80-pin plastic-molded QFP

PIN CONFIGURATION (TOP VIEW)



Package type : 80P6S-A/80P6D-A
80-pin plastic-molded QFP

FUNCTIONAL BLOCK DIAGRAM (Package : 80P6N)



PIN DESCRIPTION

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 3.0 V to 5.5 V to V_{CC}, and 0 V to V_{SS}. (Extended operating temperature version : 4.0 V to 5.5 V) (High-speed version : 2.7 V to 5.5 V)	
CNV_{SS}	CNV_{SS}	• This pin controls the operation mode of the chip. • Normally connected to V_{SS}. • If this pin is connected to V_{CC}, the internal ROM is inhibited and external memory is accessed.	
V_{REF}	Analog reference voltage	• Reference voltage input pin for A-D and D-A converters	
AV_{SS}	Analog power source	• GND input pin for A-D and D-A converters • Connect to V_{SS}.	
$\overline{RESET}$	Reset input	• Reset input pin for active “L”	
X_{IN}	Clock input	• Input and output signals for the internal clock generating circuit. • Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. • The clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
$P0_0$ – $P0_7$	I/O port P0	• 8 bit CMOS I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • At reset this port is set to input mode. • In modes other than single-chip, these pins are used as address, data, and control bus I/O pins. • CMOS compatible input level • CMOS 3-state output structure	
$P1_0$ – $P1_7$	I/O port P1		
$P2_0$ – $P2_7$	I/O port P2		
$P3_0$ – $P3_7$	I/O port P3		
$P4_0$, $P4_1$	I/O port P4	• 8-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structure	
$P4_2/INT_0$, $P4_3/INT_1$			• External interrupt input pin
$P4_4/R_XD$, $P4_5/T_XD$, $P4_6/\overline{S_{CLK1}}$, $P4_7/\overline{S_{RDY1}}$			• Serial I/O1 I/O pins
$P5_0$	I/O port P5	• 8-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structure	
$P5_1/INT_2$ – $P5_3/INT_4$			• External interrupt input pin
$P5_4/CNTR_0$, $P5_5/CNTR_1$			• Timer X and Timer Y I/O pins
$P5_6/DA_1$, $P5_7/DA_2$			• D-A conversion output pins
$P6_0/AN_0$ – $P6_7/AN_7$	I/O port P6	• 8-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structure	• A-D conversion input pins

PIN DESCRIPTION (Continued)

Pin	Name	Function	Function except a port function
$P7_0/S_{IN2}$, $P7_1/S_{OUT2}$, $P7_2/S_{CLK2}$, $P7_3/\overline{S_{RDY2}}$	I/O port P7	• 8-bit I/O port with the same function as port P0 • CMOS compatible input level • N-channel open-drain output structure	• Serial I/O2 I/O pins
$P7_4$ – $P7_7$			
$P8_0$ – $P8_7$	I/O port P8	• 8-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structure	

PART NUMBERING

Product M3806 3 M 6 - XXX FP

Package type
FP : 80P6N-A package
GP : 80P6S-A package
FS : 80D0 package

ROM number
Omitted in some types.

Normally, using hyphen
When electrical characteristic, or division of quality identification code using alphanumeric character
– : standard
D : Extended operating temperature version
A : High-speed version

ROM/PROM size
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes
9 : 36864 bytes
A : 40960 bytes
B : 45056 bytes
C : 49152 bytes
D : 53248 bytes
E : 57344 bytes
F : 61440 bytes

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

Memory type
M : Mask ROM version
E : EPROM or One Time PROM version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes

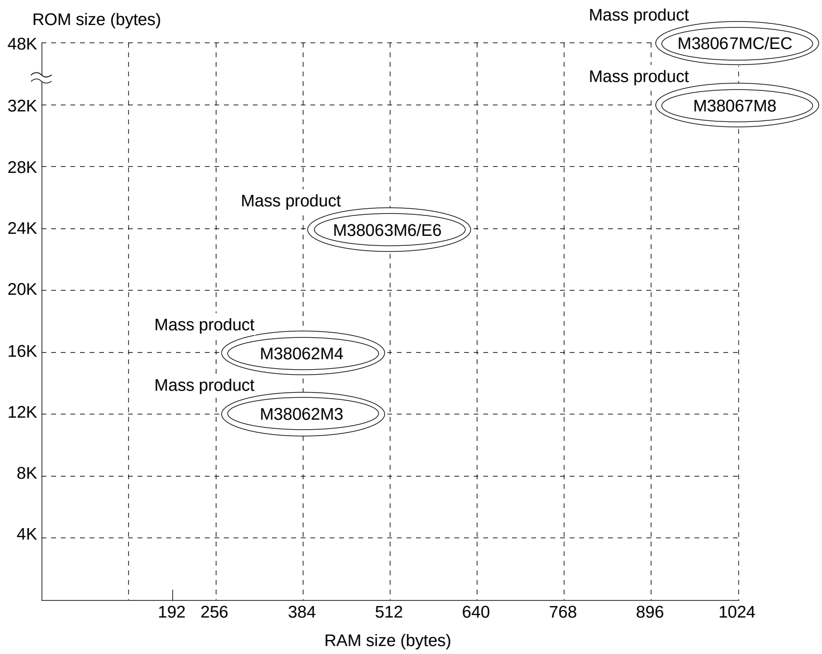
GROUP EXPANSION

Mitsubishi plans to expand the 3806 group as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions
ROM/PROM capacity .... 12 K to 48 K bytes
RAM capacity .... 384 to 1024 bytes

(2) Packages
80P6N-A .... 0.8 mm-pitch plastic molded QFP
80P6S-A .... 0.65 mm-pitch plastic molded QFP
80D0 .... 0.8 mm-pitch ceramic LCC (EPROM version)

Memory Expansion Plan



Products under development : the development schedule and specification may be revised without notice.

Currently supported products are listed below

As of May 1996

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38062M3-XXXFP	12288 (12158)	384	80P6N-A	Mask ROM version
M38062M3-XXXGP			80P6S-A	Mask ROM version
M38062M4-XXXFP	16384 (16254)	384	80P6N-A	Mask ROM version
M38062M4-XXXGP			80P6S-A	Mask ROM version
M38063M6-XXXFP	24576 (24446)	512	80P6N-A	Mask ROM version
M38063E6-XXXFP				One Time PROM version
M38063E6FP				One Time PROM version (blank)
M38063M6-XXXGP			80P6S-A	Mask ROM version
M38063E6-XXXGP				One Time PROM version
M38063E6GP				One Time PROM version (blank)
M38063E6FS			80D0	EPROM version
M38067M8-XXXFP	32768 (32638)	1024	80P6N-A	Mask ROM version
M38067M8-XXXGP			80P6S-A	Mask ROM version
M38067MC-XXXFP	49152 (49022)	1024	80P6N-A	Mask ROM version
M38067EC-XXXFP				One Time PROM version
M38067ECFP				One Time PROM version (blank)
M38067MC-XXXGP			80P6S-A	Mask ROM version
M38067EC-XXXGP				One Time PROM version
M38067ECGP				One Time PROM version (blank)

GROUP EXPANSION

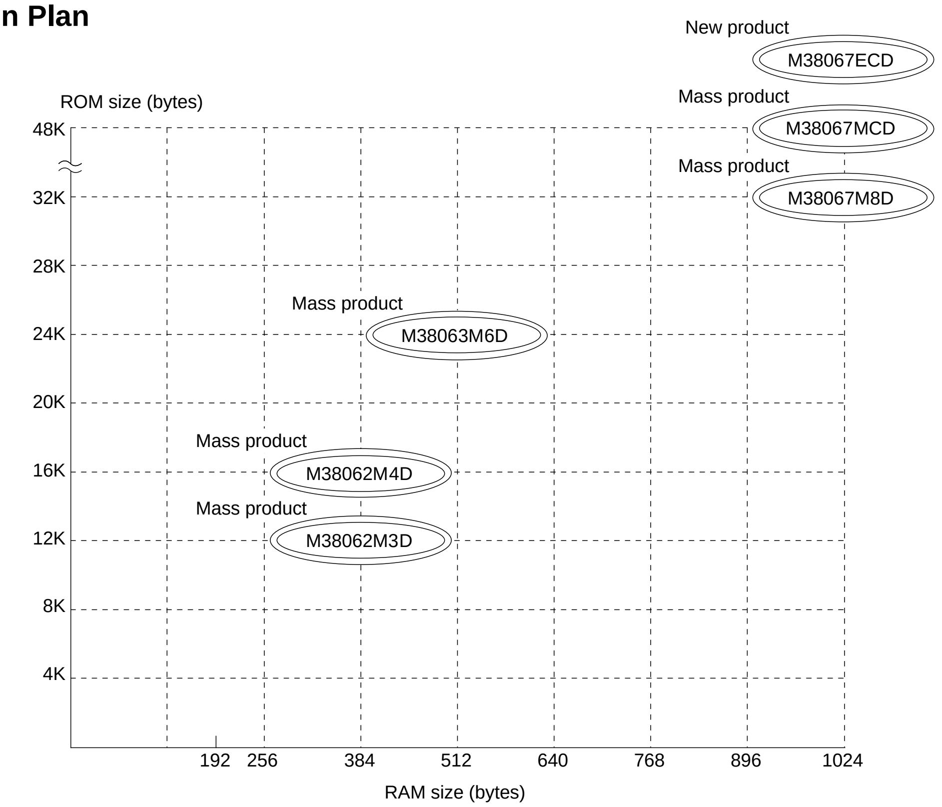
(EXTENDED OPERATING TEMPERATURE VERSION)

Mitsubishi plans to expand the 3806 group (extended operating temperature version) as follows:

(1) Support for mask ROM version
ROM/PROM capacity .... 12 K to 48 K bytes
RAM capacity .... 384 to 1024 bytes

(2) Packages
80P6N-A .... 0.8 mm-pitch plastic molded QFP

Memory Expansion Plan



Currently supported products are listed below. **As of May 1996**

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38062M3DXXXFP	12288(12158)	384	80P6N-A	Mask ROM version
M38062M4DXXXFP	16384(16254)	384		Mask ROM version
M38063M6DXXXFP	24576(24446)	512		Mask ROM version
M38067M8DXXXFP	32768(32638)	1024		Mask ROM version
M38067MCDXXXFP	49152(49022)	1024		Mask ROM version
M38067ECDXXXFP				One Time PROM version
M38067ECDFP				One Time PROM version (blank)

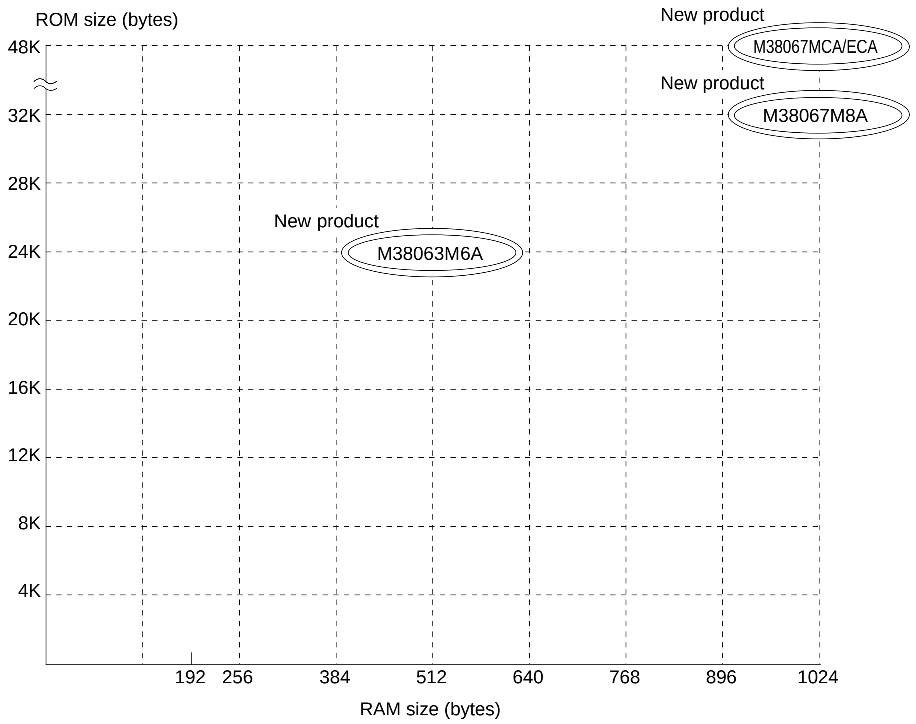
GROUP EXPANSION (HIGH-SPEED VERSION)

Mitsubishi plans to expand the 3806 group (high-speed version) as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions
ROM/PROM capacity .... 24 K to 48 K bytes
RAM capacity .... 512 to 1024 bytes

(2) Packages
80P6N-A .... 0.8 mm-pitch plastic molded QFP
80P6S-A .... 0.65 mm-pitch plastic molded QFP
80P6D-A .... 0.5 mm-pitch plastic molded QFP
80D0 .... 0.8 mm-pitch ceramic LCC (EPROM version)

Memory Expansion Plan



Products under development: the development schedule and specification may be revised without notice.

Currently supported products are listed below.

As of May 1996

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38063M6AXXXFP	24576 (24446)	512	80P6N-A	Mask ROM version
M38063M6AXXXGP			80P6S-A	Mask ROM version
M38063M6AXXXHP			80P6D-A	Mask ROM version
M38067M8AXXXFP	32768 (32638)	1024	80P6N-A	Mask ROM version
M38067M8AXXXGP			80P6S-A	Mask ROM version
M38067MCAXXXFP	49152 (49022)	1024	80P6N-A	Mask ROM version
M38067ECAXXXFP				One Time PROM version
M38067ECAFP				One Time PROM version (blank)
M38067MCAXXXGP			80P6S-A	Mask ROM version
M38067ECAXXXGP				One Time PROM version
M38067ECAGP				One Time PROM version (blank)
M38067ECAFS			80D0	EPROM version

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 3806 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

CPU mode register

The CPU mode register is allocated at address $003B_{16}$.

The CPU mode register contains the stack page selection bit.

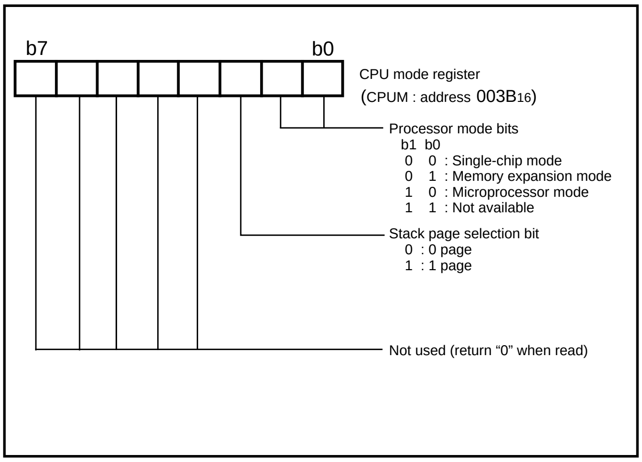


Fig. 1 Structure of CPU mode register

Memory

Special function register (SFR) area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM capacity (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}

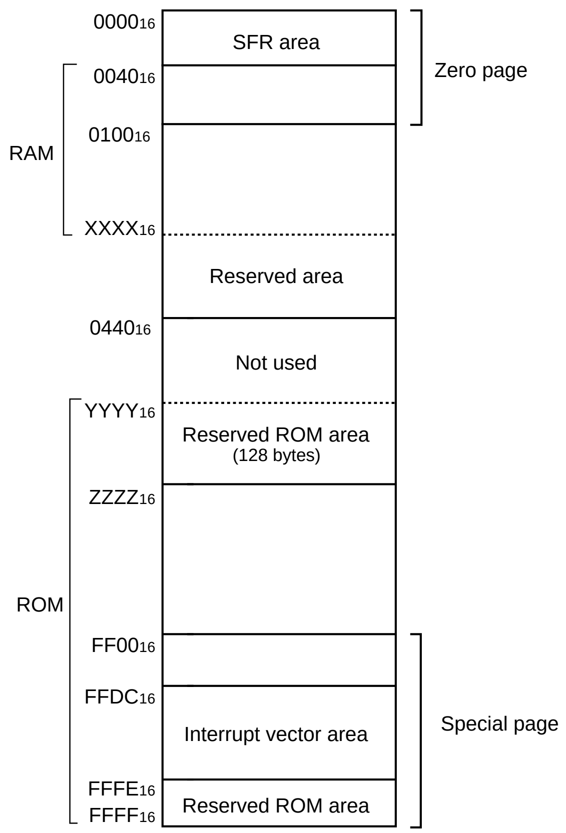


Fig. 2 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Prescaler 12 (PRE12)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer 1 (T1)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 2 (T2)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer XY mode register (TM)
0004_{16}	Port P2 (P2)	0024_{16}	Prescaler X (PREX)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer X (TX)
0006_{16}	Port P3 (P3)	0026_{16}	Prescaler Y (PREY)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer Y (TY)
0008_{16}	Port P4 (P4)	0028_{16}	
0009_{16}	Port P4 direction register (P4D)	0029_{16}	
$000A_{16}$	Port P5 (P5)	$002A_{16}$	
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	
$000C_{16}$	Port P6 (P6)	$002C_{16}$	
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}	Port P8 (P8)	0030_{16}	
0011_{16}	Port P8 direction register (P8D)	0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	AD/DA control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (AD)
0016_{16}		0036_{16}	D-A1 conversion register (DA1)
0017_{16}		0037_{16}	D-A2 conversion register (DA2)
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2(ICON2)

Fig. 3 Memory map of special function register (SFR)

I/O Ports

Direction registers

The 3806 group has 72 programmable I/O pins arranged in nine I/O ports (ports P0 to P8). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
$P0_0$ – $P0_7$	Port P0	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Address low-order byte output	CPU mode register	(1)
$P1_0$ – $P1_7$	Port P1	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Address high-order byte output	CPU mode register	
$P2_0$ – $P2_7$	Port P2	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Data bus I/O	CPU mode register	
$P3_0$ – $P3_7$	Port P3	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Control signal I/O	CPU mode register	
$P4_0$,$P4_1$	Port P4	Input/output, individual bits	CMOS 3-state output CMOS compatible input level			
$P4_2$/INT_0, $P4_3$/INT_1				External interrupt input	Interrupt edge selection register	(2)
$P4_4$/R_XD,				Serial I/O1 function I/O	Serial I/O1 control register UART control register	(3)
$P4_5$/T_XD,						(4)
$P4_6$/S_{CLK1},						(5)
$P4_7$/$\overline{S_{RDY1}}$						(6)
$P5_0$	Port P5	Input/output, individual bits	CMOS 3-state output CMOS compatible input level			(1)
$P5_1$/INT_2, $P5_2$/INT_3, $P5_3$/INT_4				External interrupt input	Interrupt edge selection register	(2)
$P5_4$/$CNTR_0$, $P5_5$/$CNTR_1$				Timer X and Timer Y function I/O	Timer XY mode register	(7)
$P5_6$/DA_1, $P5_7$/DA_2				D-A conversion output	AD/DA control register	(8)
$P6_0$/AN_0 – $P6_7$/AN_7	Port P6	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	A-D conversion input		(9)
$P7_0$/S_{IN2},	Port P7	Input/output, individual bits	N-channel open-drain output CMOS compatible input level	Serial I/O2 function I/O	Serial I/O2 control register	(10)
$P7_1$/S_{OUT2},						(11)
$P7_2$/S_{CLK2},						(12)
$P7_3$/$\overline{S_{RDY2}}$						(13)
$P7_4$ – $P7_7$						(14)
$P8_0$ – $P8_7$	Port P8	Input/output, individual bits	CMOS 3-state output CMOS compatible input level			(1)

Note 1: For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, refer to the applicable sections.

2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

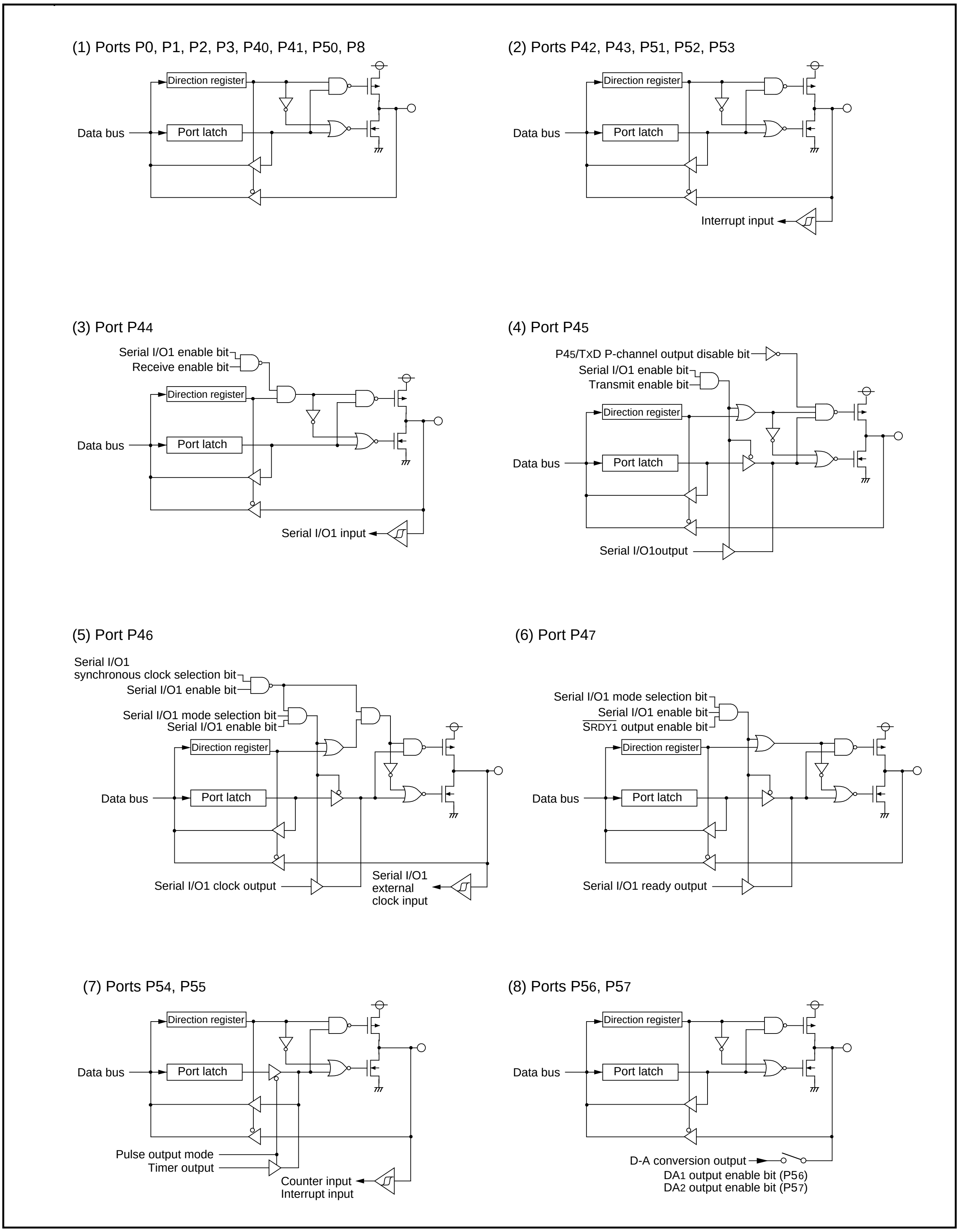


Fig. 4 Port block diagram (single-chip mode) (1)

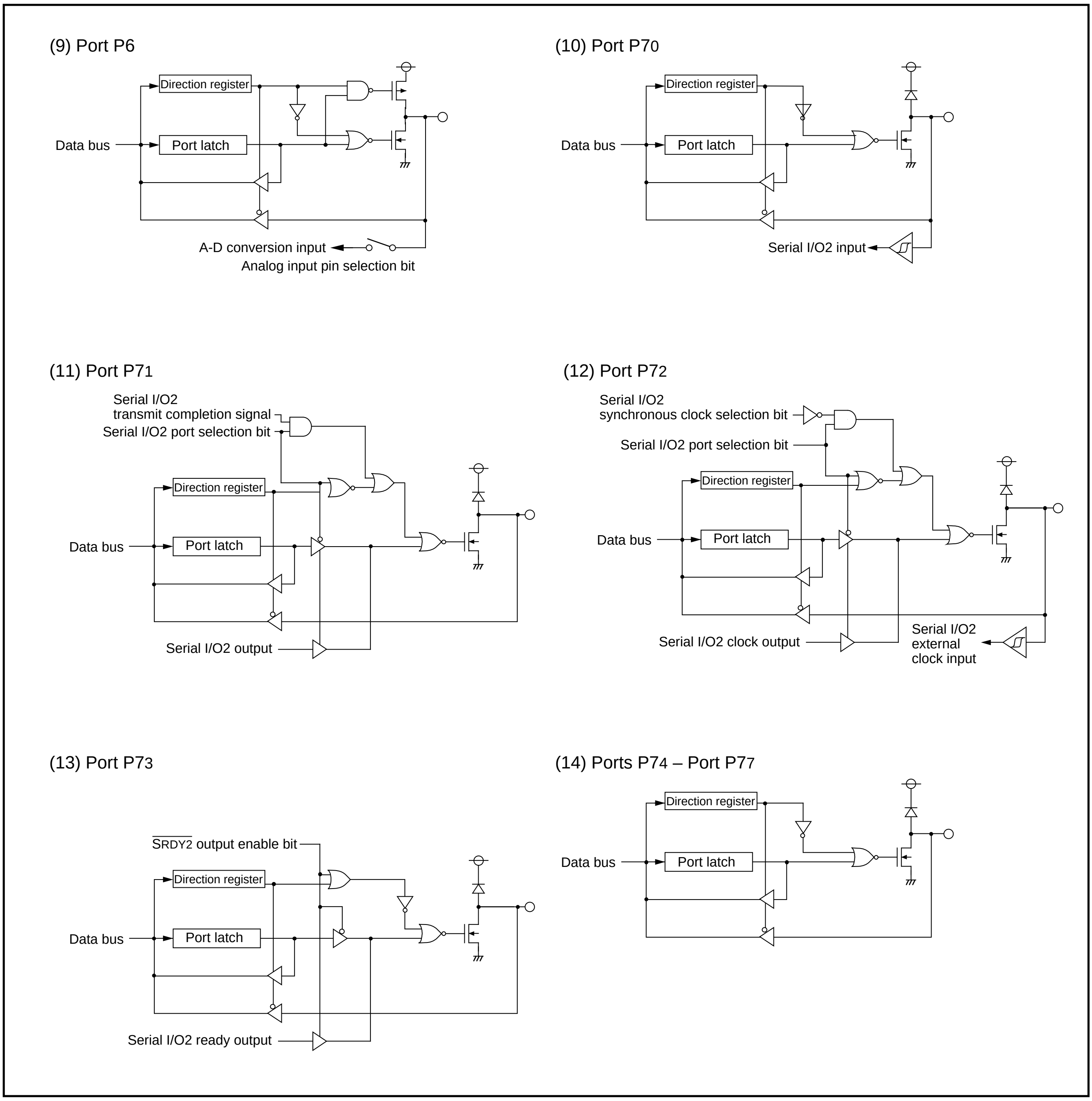


Fig. 5 Port block diagram (single-chip mode) (2)

INTERRUPTS

Interrupts occur by sixteen sources: seven external, eight internal, and one software.

Interrupt control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.
Interrupt enable bits can be set or cleared by software.
Interrupt request bits can be cleared by software, but cannot be set by software.
The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

Interrupt operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering.The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on use

When the active edge of an external interrupt (INT_0 to INT_4, $CNTR_0$, or $CNTR_1$) is changed, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;
(1) Disable the external interrupt which is selected.
(2) Change the active edge selection.
(3) Clear the interrupt request bit which is selected to “0”.
(4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O1 reception	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 underflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Serial I/O2	12	$FFE7_{16}$	$FFE6_{16}$	At completion of serial I/O2 data transfer	Valid when serial I/O2 is selected
INT_2	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_4 input	External interrupt (active edge selectable)
A-D converter	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion	
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

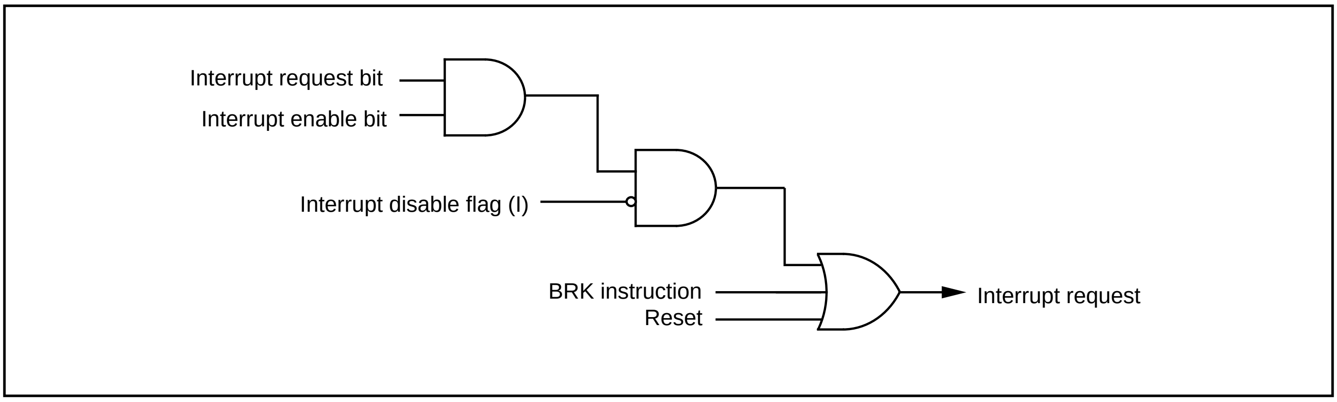


Fig. 6 Interrupt control

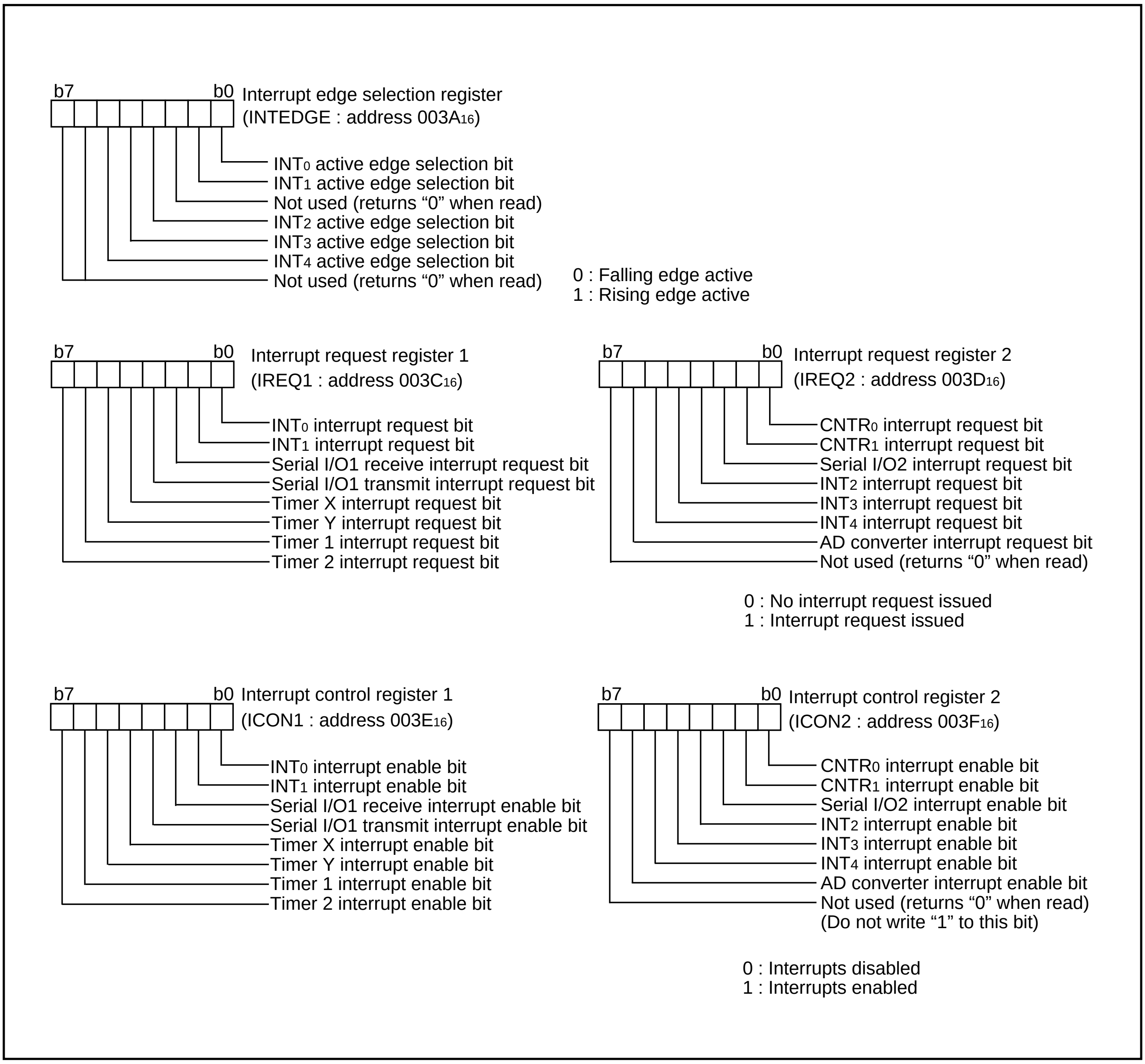


Fig. 7 Structure of interrupt-related registers

Timers

The 3806 group has four timers: timer X, timer Y, timer 1, and timer 2.
All timers are count down. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".
The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

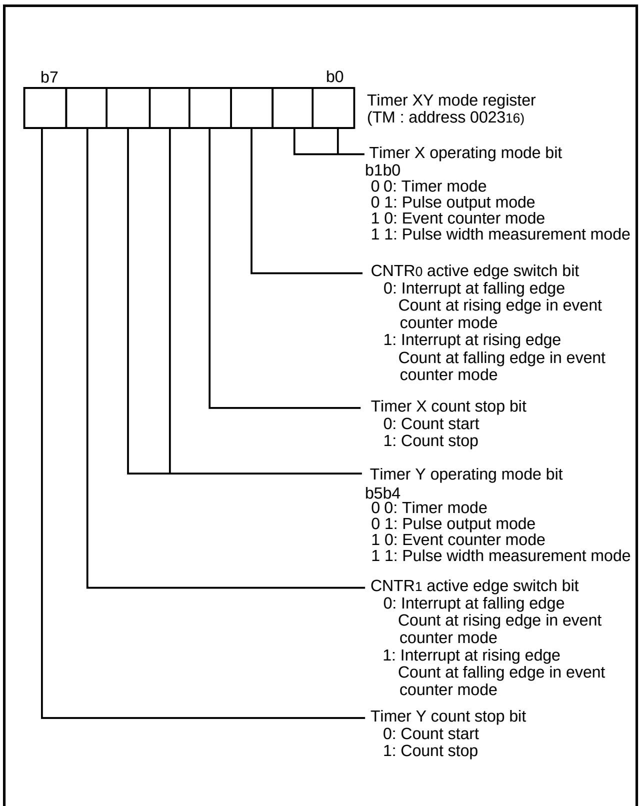


Fig. 8 Structure of timer XY register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each be selected in one of four operating modes by setting the timer XY mode register.

Timer Mode

The timer counts $f(X_{IN})/16$ in timer mode.

Pulse Output Mode

Timer X (or timer Y) counts $f(X_{IN})/16$. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge switch bit is "0", output begins at " H".
If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P5_4$ (or port $P5_5$) direction register to output mode.

Event Counter Mode

Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts at the oscillation frequency divided by 16 while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge switch bit is "1", the count continues during the time that the $CNTR_0$ (or $CNTR_1$) pin is at "L".

In all of these modes, the count can be stopped by setting the timer X (timer Y) count stop bit to "1". Every time a timer underflows, the corresponding interrupt request bit is set.

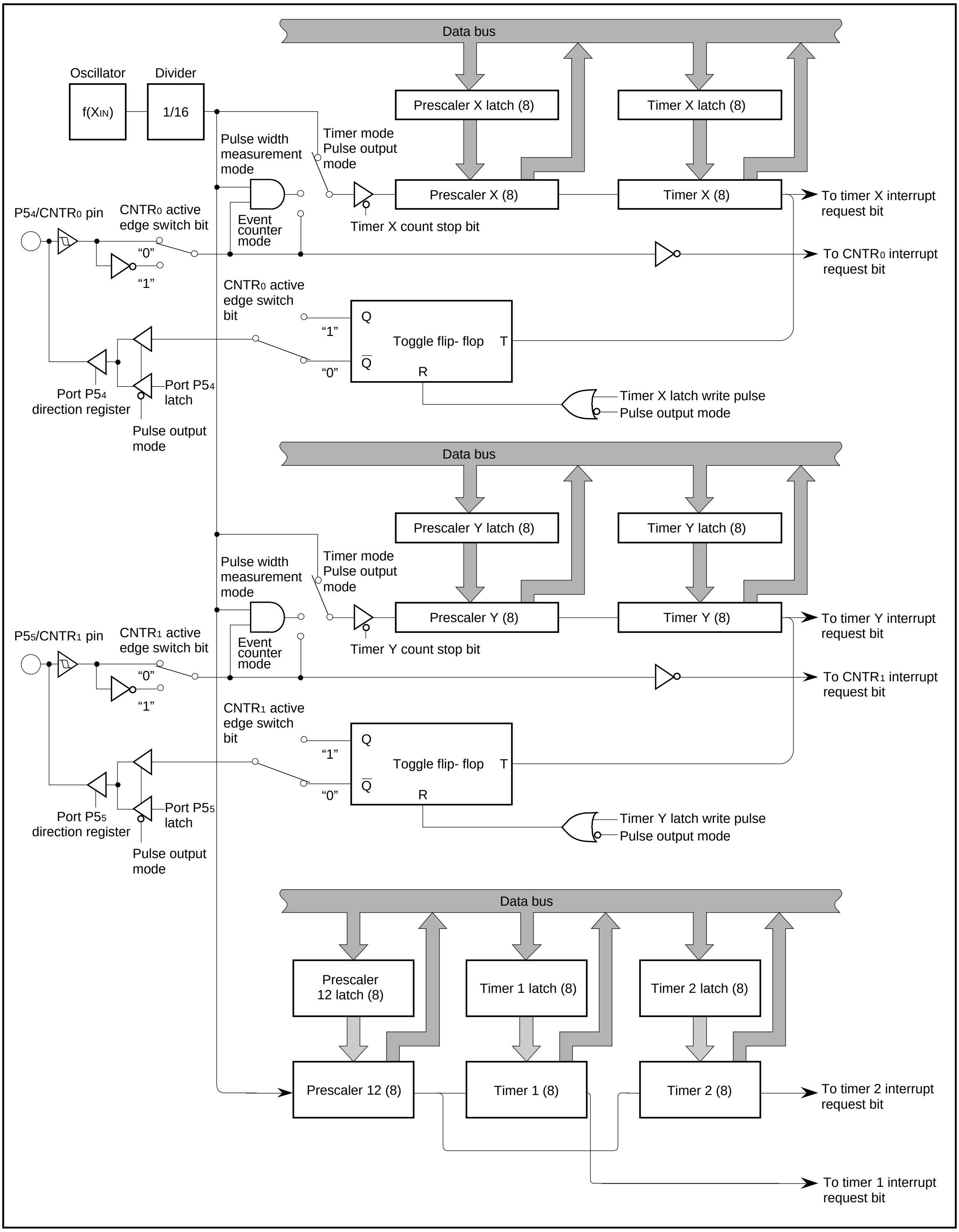


Fig. 9 Block diagram of timer X, timer Y, timer 1, and timer 2

Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

Clock synchronous serial I/O mode

Clock synchronous serial I/O1 mode can be selected by setting the mode selection bit of the serial I/O1 control register to “1”.
For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (address 0018_{16}).

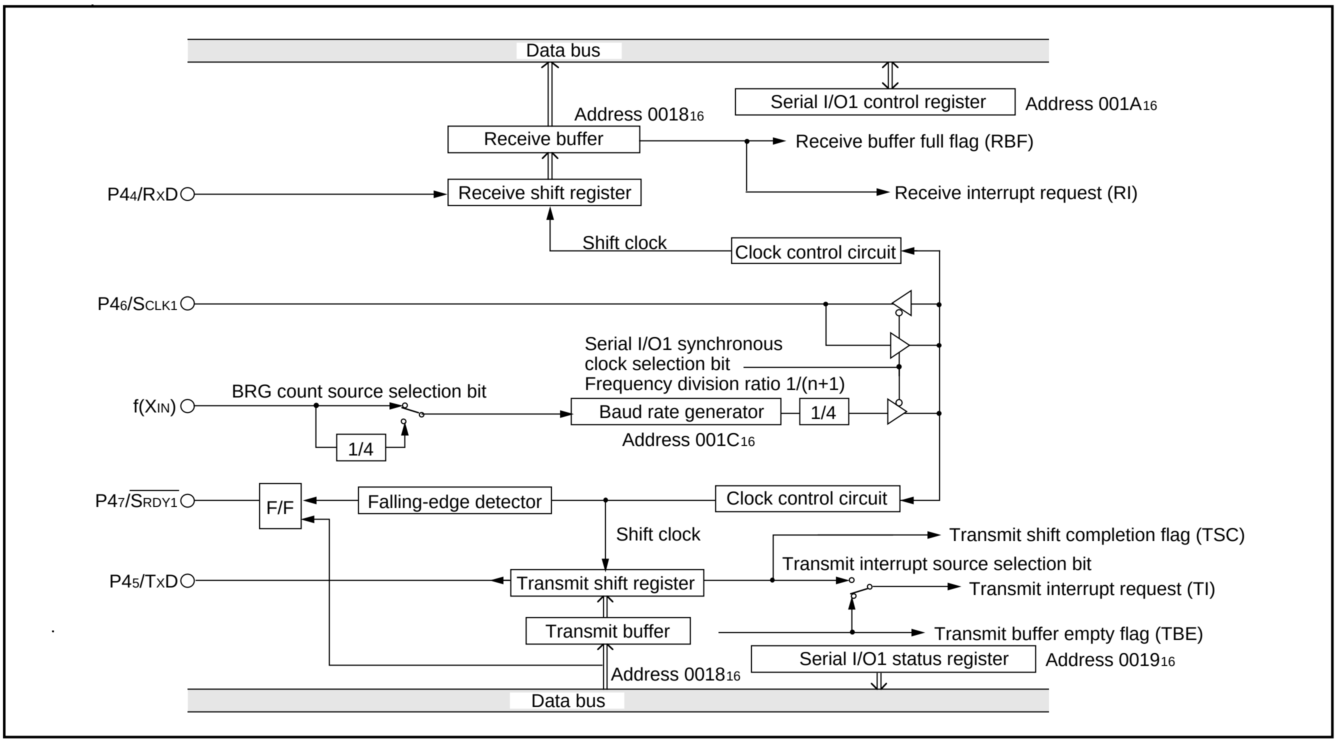
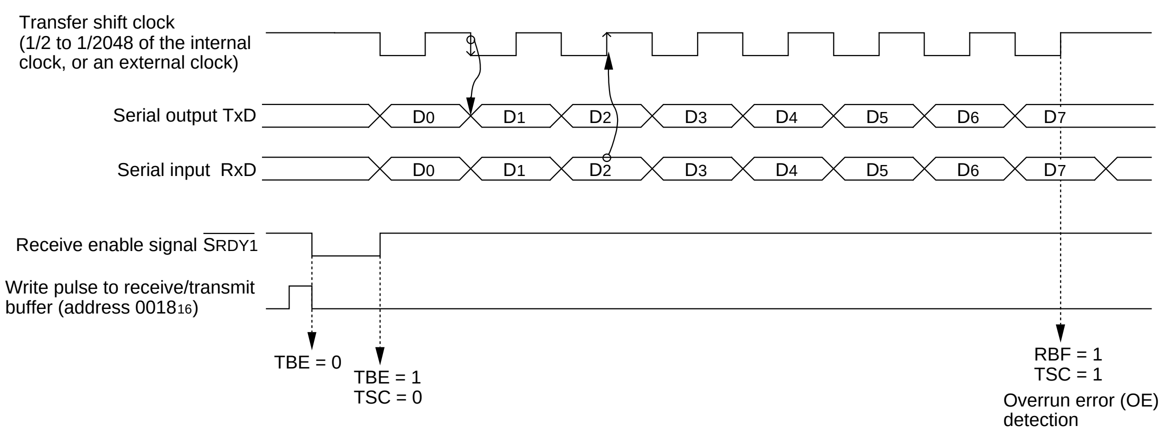


Fig. 10 Block diagram of clock synchronous serial I/O1



Notes 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2 : If data is written to the transmit buffer when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 11 Operation of clock synchronous serial I/O1 function

Asynchronous serial I/O (UART) mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to “0”.
Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.
The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.
The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

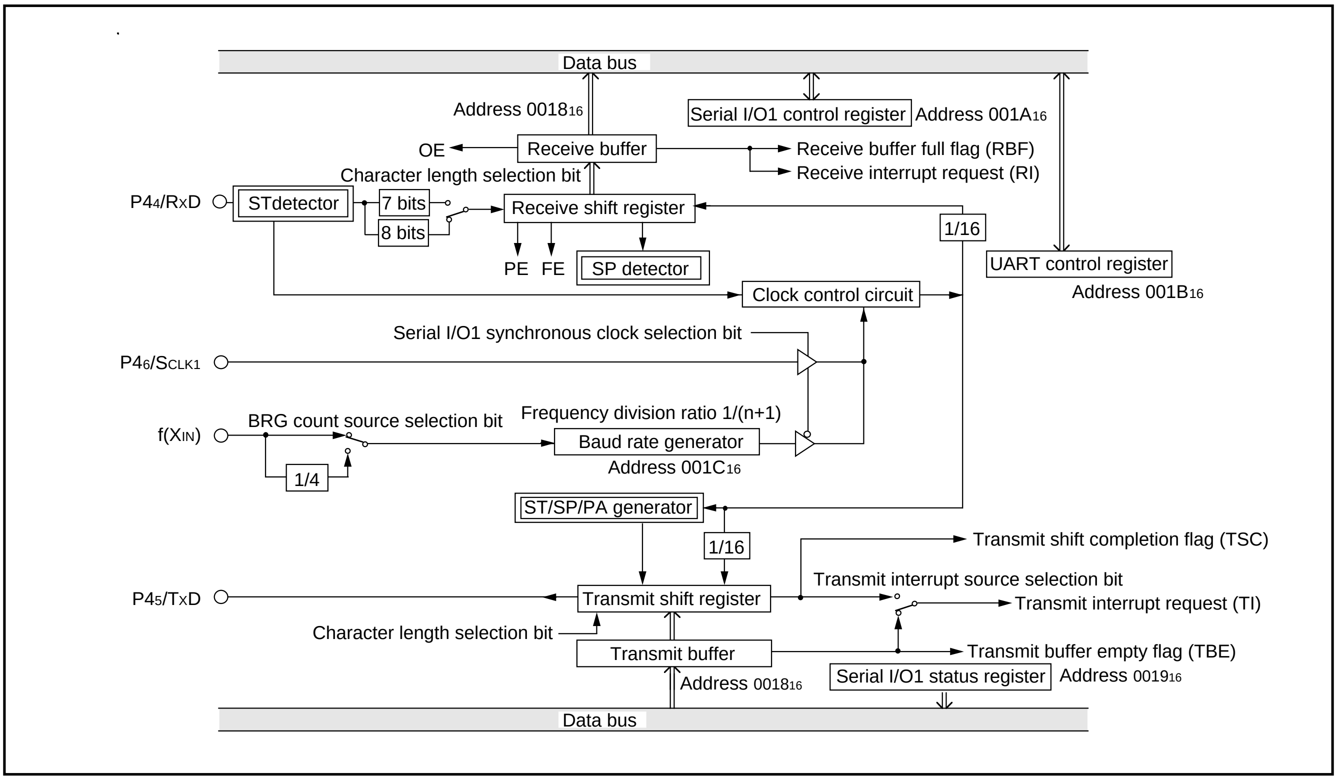
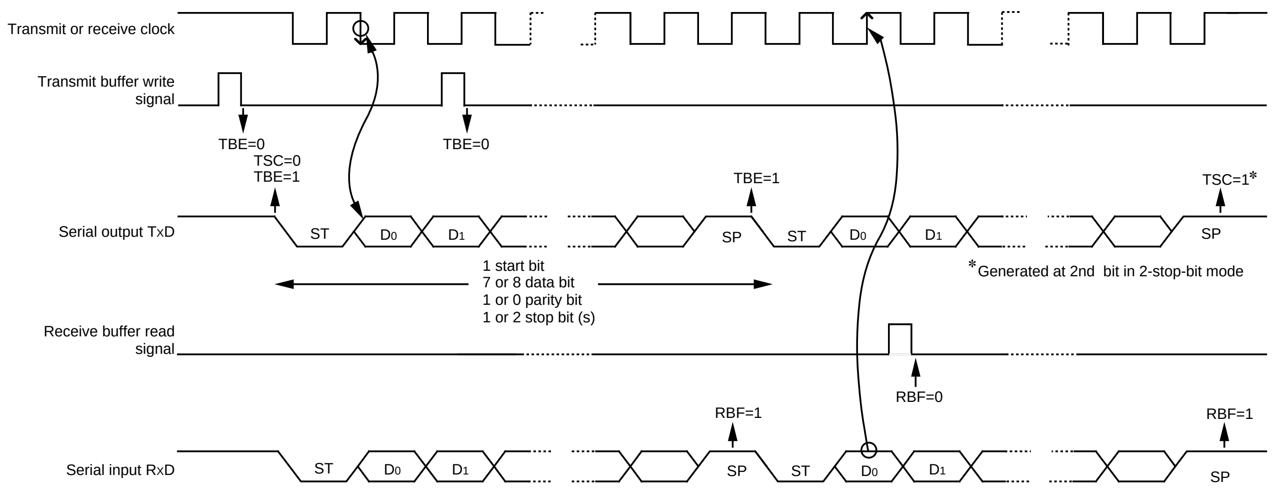


Fig. 12 Block diagram of UART serial I/O



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 13 Operation of UART serial I/O function

Serial I/O1 control register (SIO1CON) $001A_{16}$

The serial I/O control register consists of eight control bits for the serial I/O function.

UART control register (UARTCON) $001B_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the $P4_5$/TxD pin.

Serial I/O1 status register (SIO1STS) 0019_{16}

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.
All bits of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

Transmit buffer/Receive buffer register (TB/RB) 0018_{16}

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

Baud rate generator (BRG) $001C_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

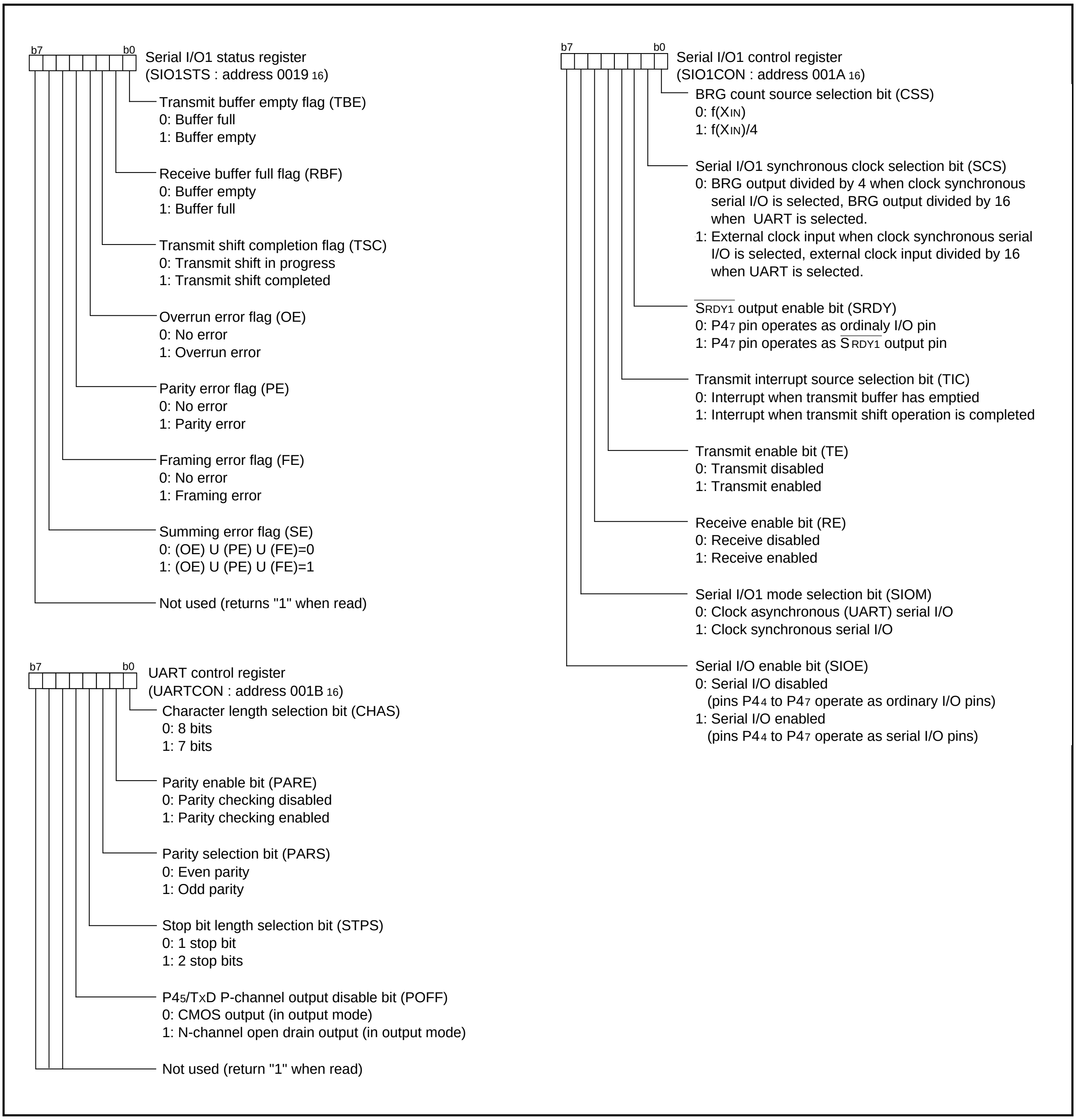


Fig. 14 Structure of serial I/O control registers

Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

Serial I/O2 control register (SIO2CON) $001D_{16}$

The serial I/O2 control register contains seven bits which control various serial I/O functions.

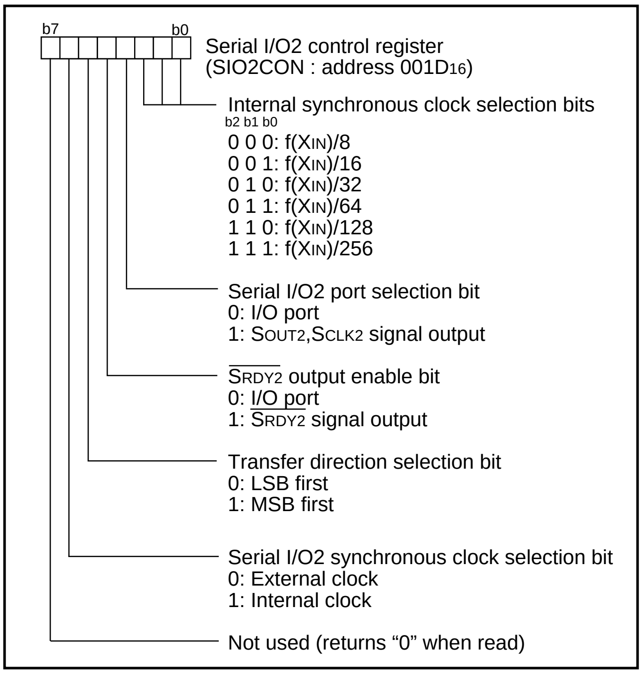


Fig. 15 Structure of serial I/O2 control register

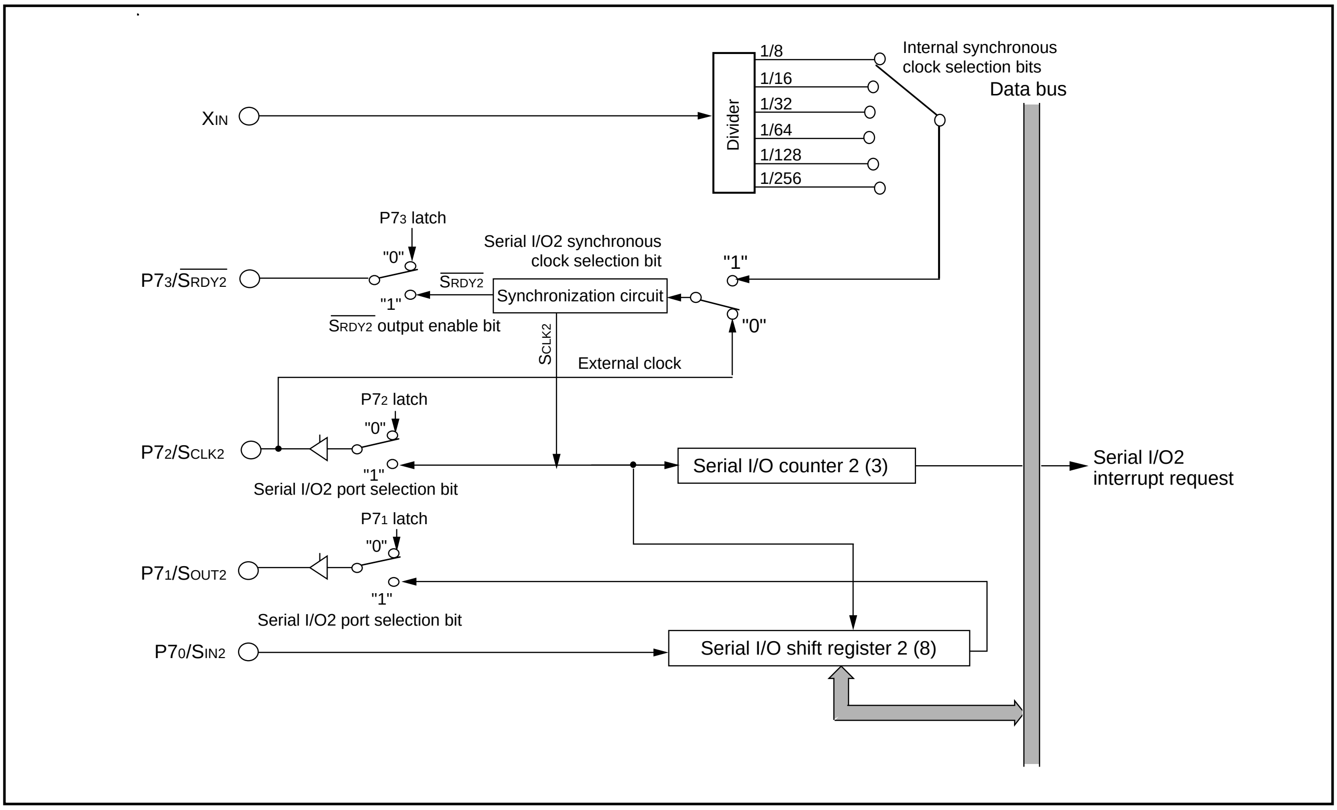
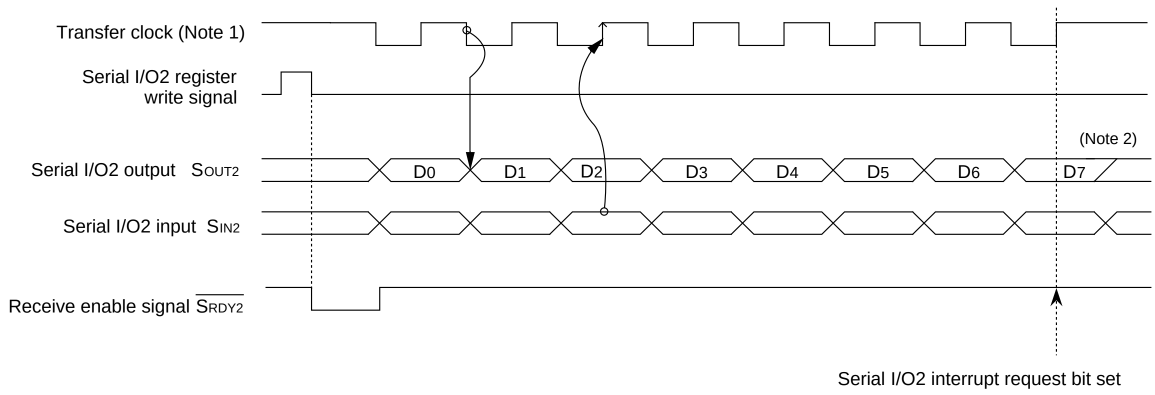


Fig. 16 Block diagram of serial I/O2 function



Notes 1: When the internal clock is selected as the transfer clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O2 control register.
2: When the internal clock is selected as the transfer clock, the S_{OUT2} pin goes to high impedance after transfer completion.

Fig. 17 Timing of serial I/O2 function

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register]

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

[AD/DA control register]

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion. Bits 6 and 7 are used to control the output of the D-A converter.

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} into 256, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of the ports $P6_0/AN_0$ to $P6_7/AN_7$, and inputs the voltage to the comparator.

[Comparator and Control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage, then stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".
Note that the comparator is constructed linked to a capacitor, so set $f(X_{IN})$ to 500 kHz or more during an A-D conversion.

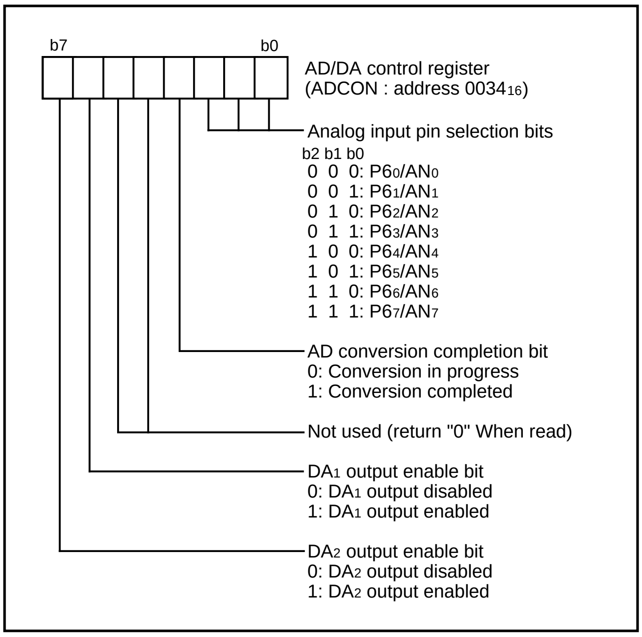


Fig.18 Structure of AD/DA control register

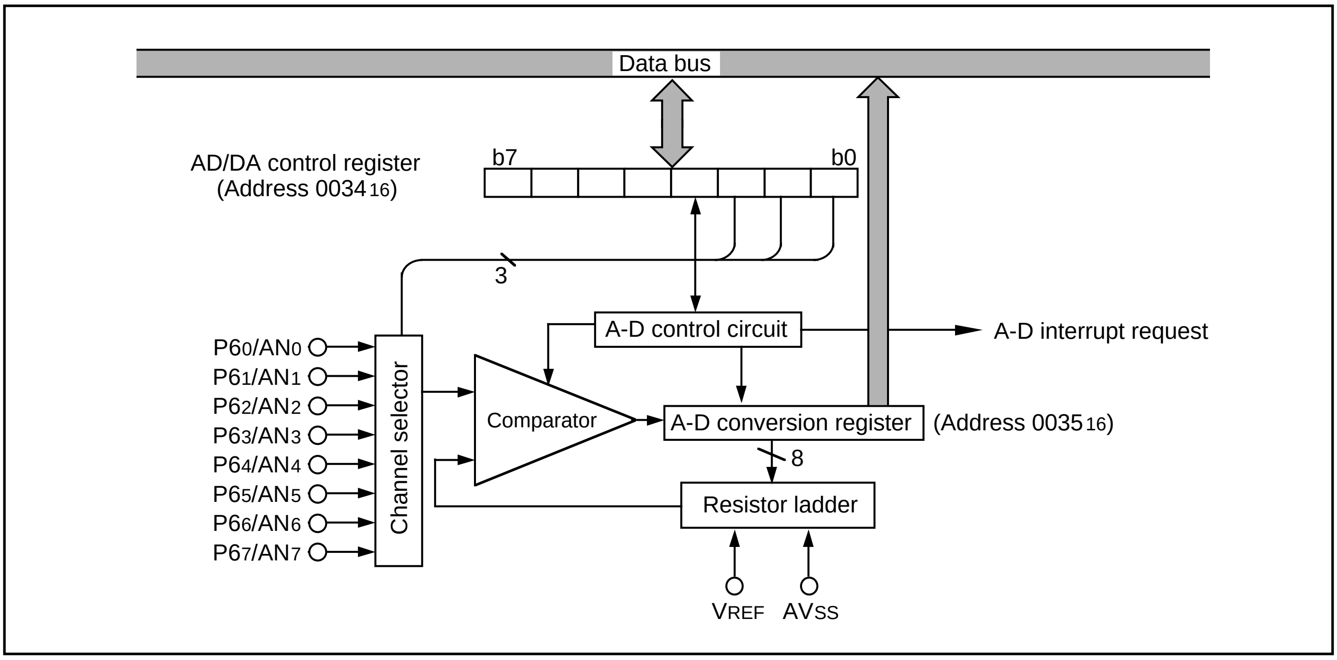


Fig. 19 Block diagram of A-D converter

D-A Converter

The 3806 group has two internal D-A converters (DA1 and DA2) with 8-bit resolutions.
The D-A converter is performed by setting the value in the D-A conversion register. The result of D-A converter is output from the DA_1 or DA_2 pin by setting the DA output enable bit to “1”.
When using the D-A converter, the corresponding port direction register bit ($DA_1/P5_6$ or $DA_2/P5_7$) should be set to “0” (input status).
The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$V = V_{REF} \times n/256$ (n = 0 to 255)
Where V_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to “00_{16}”, the DA output enable bits are cleared to “0”, and the $P5_6/DA_1$ and $P5_7/DA_2$ pins are set to input (high impedance).
The D-A output is not buffered, so connect an external buffer when driving a low-impedance load.
Set V_{CC} to 4.0 V or more when using the D-A converter.

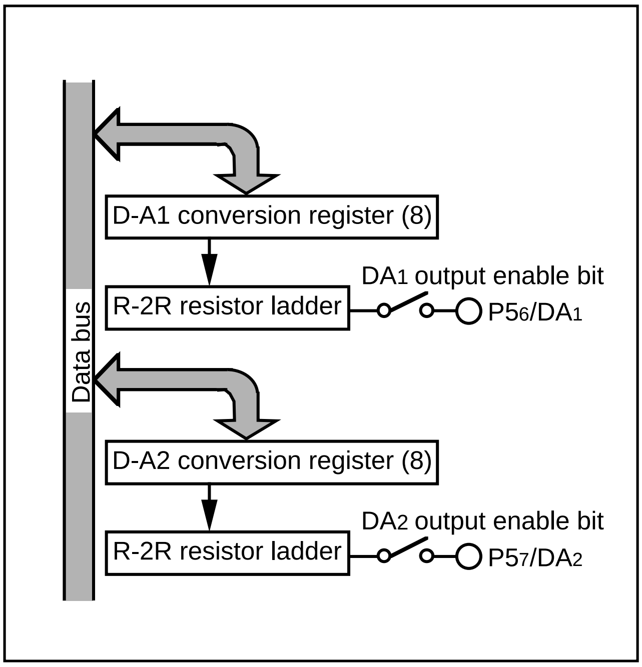


Fig. 20 Block diagram of D-A converter

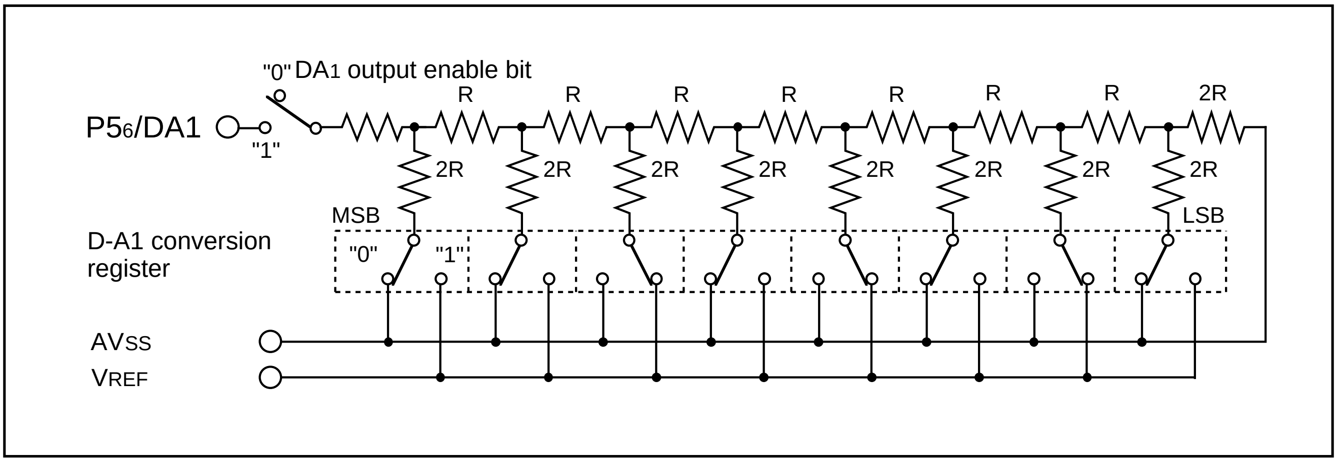


Fig. 21 Equivalent connection circuit of D-A converter

Reset Circuit

To reset the microcomputer, the $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (Note 1), reset is released. Internal operation does not begin until after 8 to 13 X_{IN} clock cycles are completed. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte).

Make sure that the reset input voltage is less than 0.8 V for V_{CC} of 4.0 V (Note 2).

Note 1. The power source voltage should be between the following voltage.
- Between 3.0 V and 5.5 V for standard version
- Between 4.0 V and 5.5 V for extended operating temperature version
- Between 2.7 V and 5.5 V for high-speed version

Note 2. Reset input voltage is less than the following voltage.
- 0.6 V for V_{CC} = 3.0 V
- 0.8 V for V_{CC} = 4.0 V
- 0.54 V for V_{CC} = 2.7 V

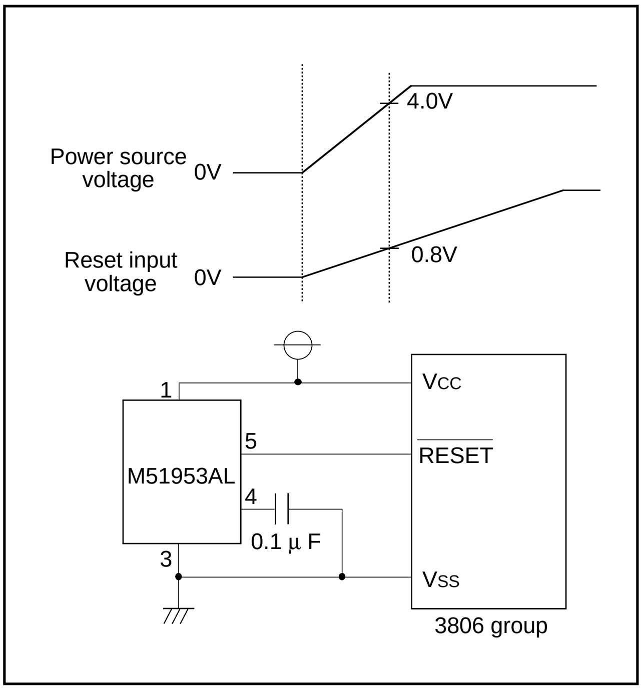


Fig. 22 Example of reset circuit

		Address	Register contents
(1)	Port P0 direction register	(0001_{16}) • • •	00_{16}
(2)	Port P1 direction register	(0003_{16}) • • •	00_{16}
(3)	Port P2 direction register	(0005_{16}) • • •	00_{16}
(4)	Port P3 direction register	(0007_{16}) • • •	00_{16}
(5)	Port P4 direction register	(0009_{16}) • • •	00_{16}
(6)	Port P5 direction register	$(000B_{16})$ • • •	00_{16}
(7)	Port P6 direction register	$(000D_{16})$ • • •	00_{16}
(8)	Port P7 direction register	$(000F_{16})$ • • •	00_{16}
(9)	Port P8 direction register	(0011_{16}) • • •	00_{16}
(10)	Serial I/O1 status register	(0019_{16}) • • •	1 0 0 0 0 0 0 0
(11)	Serial I/O1 control register	$(001A_{16})$ • • •	00_{16}
(12)	UART control register	$(001B_{16})$ • • •	1 1 1 0 0 0 0 0
(13)	Serial I/O2 control register	$(001D_{16})$ • • •	00_{16}
(14)	Prescaler 12	(0020_{16}) • • •	FF_{16}
(15)	Timer 1	(0021_{16}) • • •	01_{16}
(16)	Timer 2	(0022_{16}) • • •	FF_{16}
(17)	Timer XY mode register	(0023_{16}) • • •	00_{16}
(18)	Prescaler X	(0024_{16}) • • •	FF_{16}
(19)	Timer X	(0025_{16}) • • •	FF_{16}
(20)	Prescaler Y	(0026_{16}) • • •	FF_{16}
(21)	Timer Y	(0027_{16}) • • •	FF_{16}
(22)	AD/DA control register	(0034_{16}) • • •	0 0 0 0 1 0 0 0
(23)	D-A1 conversion register	(0036_{16}) • • •	00_{16}
(24)	D-A2 conversion register	(0037_{16}) • • •	00_{16}
(25)	Interrupt edge selection register	$(003A_{16})$ • • •	00_{16}
(26)	CPU mode register	$(003B_{16})$ • • •	0 0 0 0 0 0 ✻ 0
(27)	Interrupt request register 1	$(003C_{16})$ • • •	00_{16}
(28)	Interrupt request register 2	$(003D_{16})$ • • •	00_{16}
(29)	Interrupt control register 1	$(003E_{16})$ • • •	00_{16}
(30)	Interrupt control register 2	$(003F_{16})$ • • •	00_{16}
(31)	Processor status register	(PS)	× × × × × 1 × ×
(32)	Program counter	(PC_H)	Contents of address $FFFD_{16}$
		(PC_L)	Contents of address $FFFC_{16}$

Note. × : Undefined
✻ : The initial values of CM_1 are determined by the level at the CNV_{SS} pin.
The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software.

Fig. 23 Internal status of microcomputer after reset

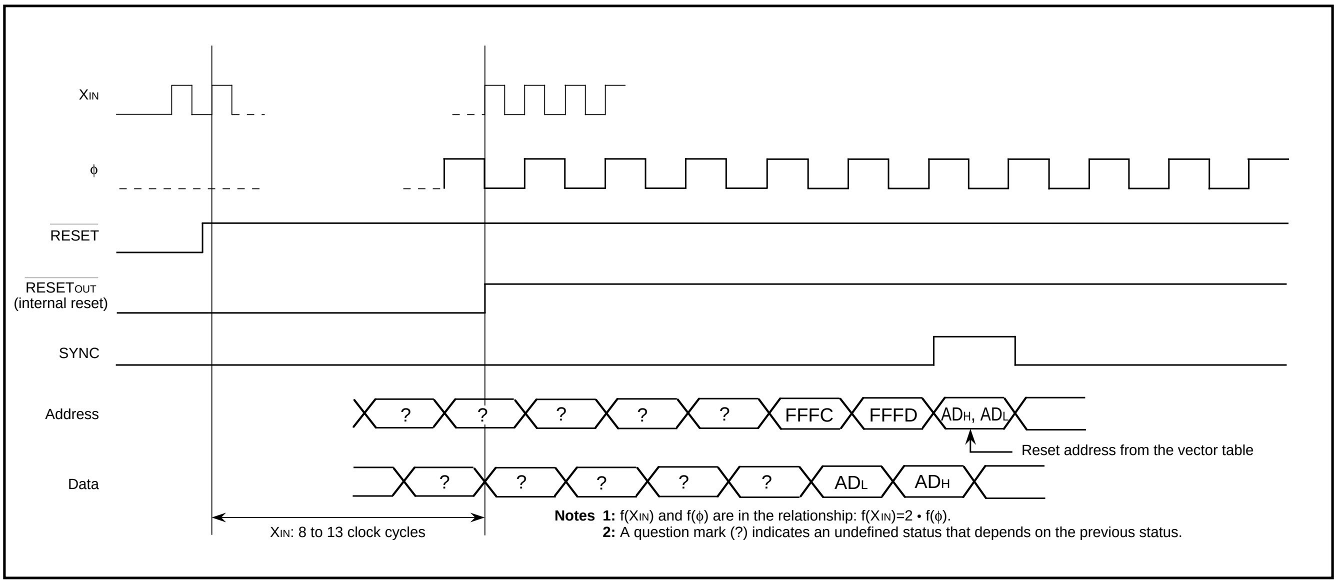


Fig. 24 Timing of reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT. To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open.

Oscillation control

Stop Mode

If the STP instruction is executed, the internal clock ϕ stops at an “H”. Timer 1 is set to “01_{16}” and prescaler 12 is set to “FF_{16}”. Oscillator restarts when an external interrupt is received, but the internal clock ϕ remains at an “H” until timer 1 underflow.
This allows time for the clock circuit oscillation to stabilize.
If oscillator is restarted by a reset, no wait time is generated, so keep the $\overline{\text{RESET}}$ pin at an “L” level until oscillation has stabilized.

Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an “H” level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received.
Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.
To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to “1” before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 underflows, so set the timer 1 interrupt enable bit to “0” before the STP instruction is executed.

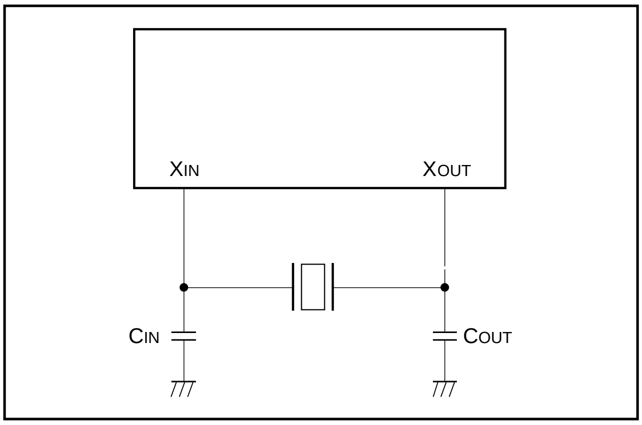


Fig. 25 Ceramic resonator circuit

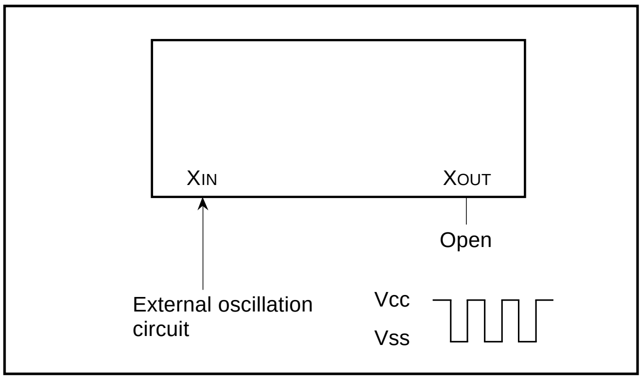


Fig. 26 External clock input circuit

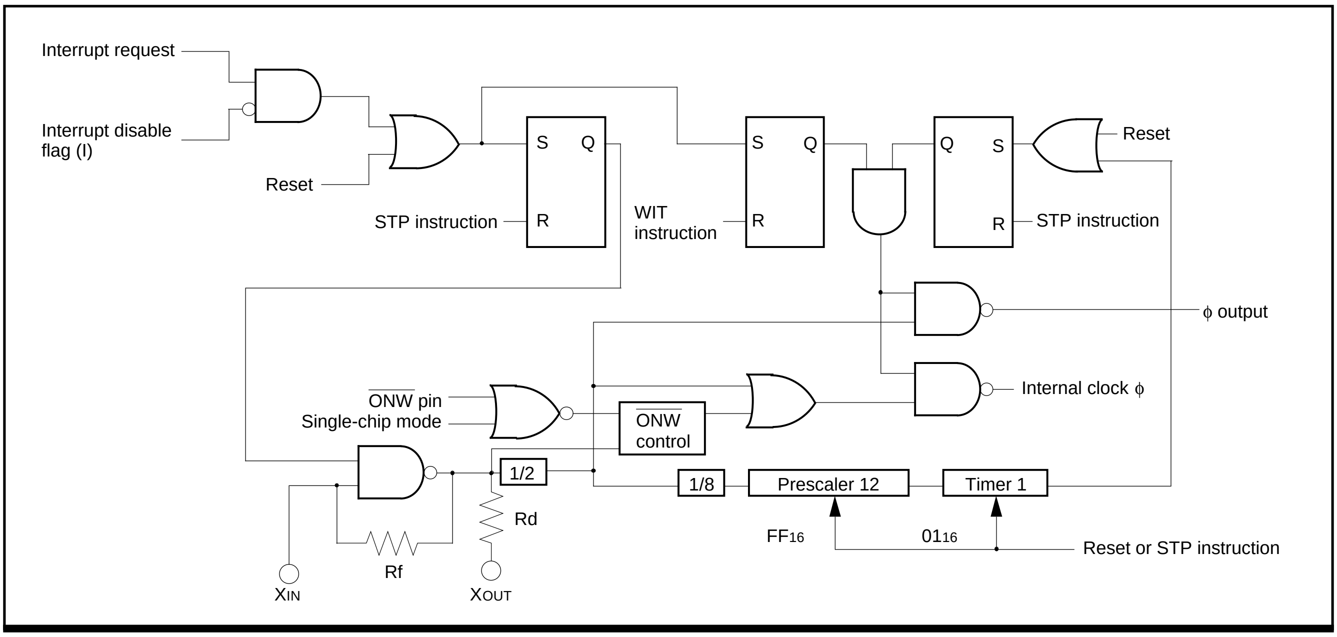


Fig. 27 Block diagram of clock generating circuit

Processor Modes

Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits CM_0 and CM_1 (bits 0 and 1 of address $003B_{16}$). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

Table 2. Functions of ports in memory expansion mode and microprocessor mode

Port Name	Function
Port P0	Outputs low-order byte of address.
Port P1	Outputs high-order byte of address.
Port P2	Operates as I/O pins for data D_7 to D_0 (including instruction codes).
Port P3	$P3_0$ and $P3_1$ function only as output pins (except that the port latch cannot be read). $P3_2$ is the $\overline{ONW}$ input pin. $P3_3$ is the $\overline{RESET_{OUT}}$ output pin. (Note) $P3_4$ is the ϕ output pin. $P3_5$ is the SYNC output pin. $P3_6$ is the $\overline{WR}$ output pin, and $P3_7$ is the $\overline{RD}$ output pin.

Note: If CNVss is connected to Vss, the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the $\overline{RESET_{OUT}}$ output pin.

Single-Chip Mode
Select this mode by resetting the microcomputer with CNVss connected to Vss.

Memory Expansion Mode
Select this mode by setting the processor mode bits to "01" in software with CNVss connected to Vss. This mode enables external memory expansion while maintaining the validity of the internal ROM. Internal ROM will take precedence over external memory if addresses conflict.

Microprocessor Mode
Select this mode by resetting the microcomputer with CNVss connected to Vcc, or by setting the processor mode bits to "10" in software with CNVss connected to Vss. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.

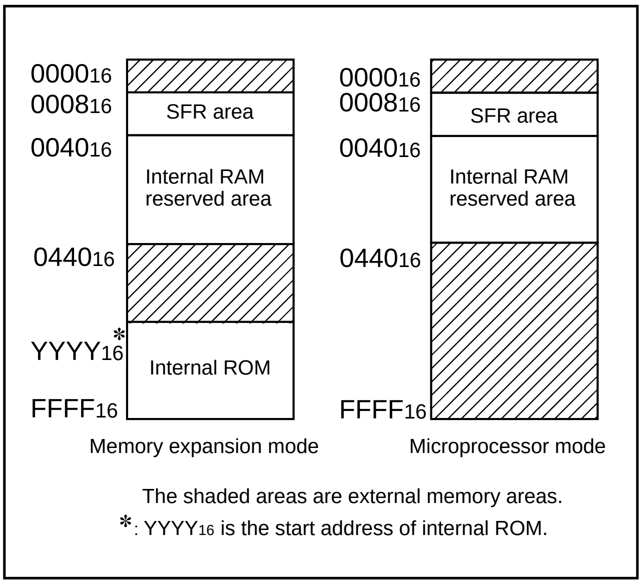


Fig. 28 Memory maps in various processor modes

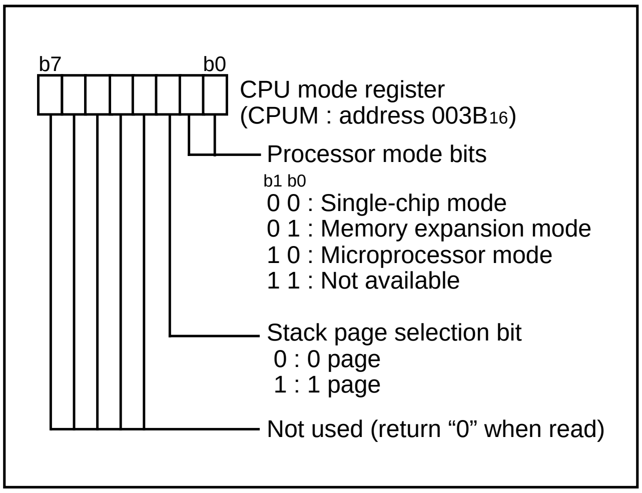
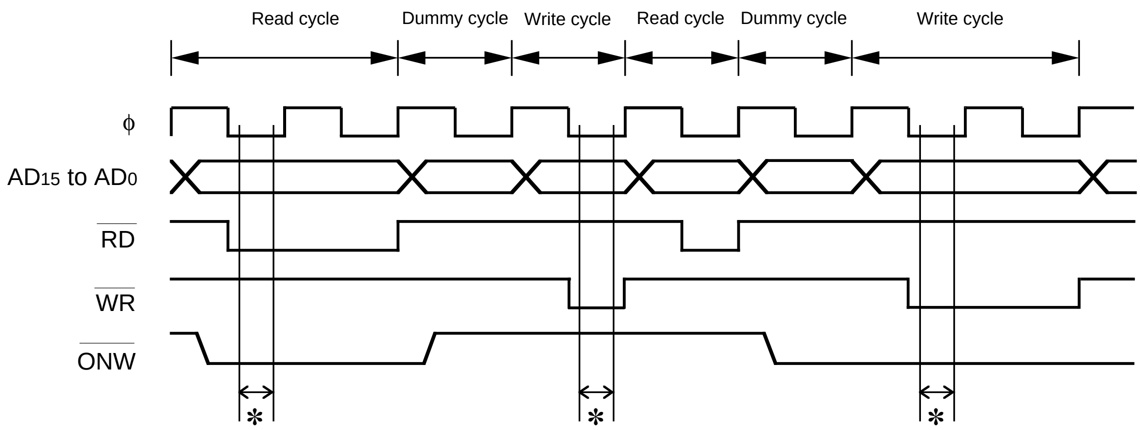


Fig. 29 Structure of CPU mode register

Bus control with memory expansion

The 3806 group has a built-in $\overline{\text{ONW}}$ function to facilitate access to external memory and I/O devices in memory expansion mode or microprocessor mode.

If an "L" level signal is input to the $\overline{\text{ONW}}$ pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ. During this extended period, the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal remains at "L". This extension period is valid only for writing to and reading from addresses 0000_{16} to 0007_{16} and 0440_{16} to $FFFF_{16}$ in microprocessor mode, 0440_{16} to $YYYY_{16}$ in memory expansion mode, and only read and write cycles are extended.



✻ : Period during which $\overline{\text{ONW}}$ input signal is received
During this period, the $\overline{\text{ONW}}$ signal must be fixed at either "H" or "L". At all other times, the input level of the $\overline{\text{ONW}}$ signal has no affect on operations.
The bus cycles is not extended for an address in the area 0008_{16} to $043F_{16}$, regardless of whether the $\overline{\text{ONW}}$ signal is received.

Fig. 30 $\overline{\text{ONW}}$ function timing

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.
The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n + 1).

Multiplication and Division Instructions

The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used:
- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY1}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY1}}$ output enable bit to “1”.
Serial I/O1 continues to output the final bit from the T_XD pin after transmission is completed. The S_{OUT2} pin from serial I/O2 goes to high impedance after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(X_{IN}) is at least 500 kHz during an A-D conversion. (If the $\overline{ONW}$ pin has been set to “L”, the A-D conversion will take twice as long to match the longer bus cycle, and so f(X_{IN}) must be at least 1 MHz.)
Do not execute the STP or WIT instruction during an A-D conversion.

D-A Converter

The accuracy of the D-A converter becomes poor rapidly under the V_{CC} = 4.0 V or less condition.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the X_{IN} frequency.
When the $\overline{ONW}$ function is used in modes other than single-chip mode, the frequency of the internal clock ϕ may be one fourth the X_{IN} frequency.

Memory Expansion Mode and Microprocessor Mode

Execute the LDM or STA instruction for writing to port P3 (address 0006_{16}) in memory expansion mode and microprocessor mode.
Set areas which can be read out and write to port P3 (address 0006_{16}) in a memory, using the read-modify-write instruction (SEB, CLB).

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

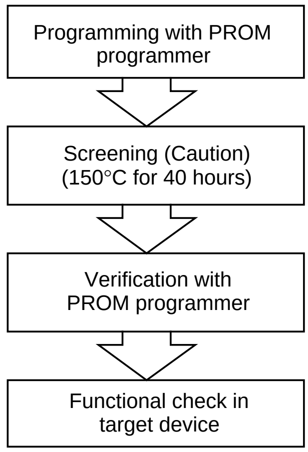
1. Mask ROM Order Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80P6S-A	PCA4738G-80A
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 40 is recommended to verify programming.



Caution : The screening temperature is far higher than the storage temperature. Never expose to 150 °C exceeding 100 hours.

Fig. 31 Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	T_a = 25 °C	500	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (Vcc=3.0 to 5.5v, Ta=-20 to 85°C,unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage ($f(X_{IN})$ **<** 2 MHz) (Note 1)		3.0	5.0	5.5	V
	Power source voltage ($f(X_{IN})$ = 8 MHz) (Note 1)		4.0	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage (when A-D converter is used)		2.0		V_{CC}	V
	Analog reference voltage (when D-A converter is used)		3.0		V_{CC}	
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage	AN_0–AN_7	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}, CNV_{SS}	0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.16 V_{CC}	V
V_{IL}	"L" input voltage	CNV_{SS}	0		0.2 V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 2)			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ (Note 2)			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 2)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ (Note 2)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 2)			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ (Note 2)			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 2)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ (Note 2)			40	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 3)			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ (Note 3)			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 4)			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ (Note 4)			5	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC} = 4.0 to 5.5 V)				8	MHz
	Internal clock oscillation frequency (V_{CC} = 3.0 to 4.0 V)				6 V_{CC}–16	

Note 1: The minimum power source voltage is $\frac{X+16}{6}$ [V] ($f(X_{IN})$ = XMHz) on the condition of 2 MHz < $f(X_{IN})$ < 8 MHz.
2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
3: The peak output current is the peak current flowing in each port.
4: The average output current $I_{OL(avg)}$, $I_{OH(avg)}$ in an average value measured over 100 ms.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	“H” output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 1)	I_{OH} = –10 mA, V_{CC} = 4.0 to 5.5 V	V_{CC}–2.0			V
			I_{OH} = –1.0 mA, V_{CC} = 3.0 to 5.5 V	V_{CC}–1.0			V
V_{OL}	“L” output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OL} = 10 mA, V_{CC} = 4.0 to 5.5 V			2.0	V
			I_{OL} = 1.0 mA, V_{CC} = 3.0 to 5.5 V			1.0	V
V_{T+} – V_{T-}	Hysteresis	$CNTR_0$, $CNTR_1$, INT_0–INT_4			0.4		V
V_{T+} – V_{T-}	Hysteresis	RxD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.5		V
V_{T+} – V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	“H” input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{CC}			5.0	µA
I_{IH}	“H” input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	“H” input current	X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	“L” input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{SS}			–5.0	µA
I_{IL}	“L” input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	“L” input current	X_{IN}	V_I = V_{SS}		–4		µA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V
I_{CC}	Power source current		f(X_{IN}) = 8 MHz, V_{CC} = 5 V		6.4	13	mA
			f(X_{IN}) = 5 MHz, V_{CC} = 5 V		4	8	mA
			f(X_{IN}) = 2 MHz, V_{CC} = 3 V		0.8	2.0	mA
			When WIT instruction is executed with f(Xin) = 8MHz,Vcc=5V		1.5		mA
			When WIT instruction is executed with f(Xin) = 5MHz,Vcc=5V		1		mA
			When WIT instruction is executed with f(Xin) = 2MHz,Vcc=3V		0.2		mA
			When STP instruction is executed with clock stopped, output transistors isolated. T_a = 25 °C (Note 2)		0.1	1	µA
			When STP instruction is executed with clock stopped, output transistors isolated. T_a = 85 °C (Note 2)			10	µA

Note 1: $P4_5$ is measured when the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: With output transistors isolated and A-D converter having completed conversion, and not including current flowing through V_{REF} pin.

A-D CONVERTER CHARACTERISTICS

(V_{CC} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 2.0 V to V_{CC}, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			±1	±2.5	LSB
t_{CONV}	Conversion time				50	$t_C(\phi)$
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current (Note)	V_{REF} = 5.0 V	50	150	200	µA
$I_{I(AD)}$	A-D port input current			0.5	5.0	µA

Note: When D-A conversion registers (addresses 0036_{16} and 0037_{16}) contain “00_{16}”.

D-A CONVERTER CHARACTERISTICS

(V_{CC} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 3.0 V to V_{CC}, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy	V_{CC} = 4.0 to 5.5 V				1.0	%
		V_{CC} = 3.0 to 4.0 V				2.5	
t_{su}	Setting time					3	µs
R_O	Output resistor			1	2.5	4	kΩ
I_{VREF}	Reference power source input current (Note)					3.2	mA

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00_{16}", and excluding currents flowing through the A-D resistance ladder.

TIMING REQUIREMENTS 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	External clock input cycle time	125			ns
$t_{wH(X_{IN})}$	External clock input “H” pulse width	50			ns
$t_{wL(X_{IN})}$	External clock input “L” pulse width	50			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{wH(INT)}$	INT_0 to INT_4 input “H” pulse width	80			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_4 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	1000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	100			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1”. Divide this value by four when bit 6 of address $001A_{16}$ is “0”.

TIMING REQUIREMENTS 2 (V_{CC} = 3.0 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	External clock input cycle time	500/ (3 V_{CC}–8)			ns
$t_{wH(X_{IN})}$	External clock input “H” pulse width	200/ (3 V_{CC}–8)			ns
$t_{wL(X_{IN})}$	External clock input “L” pulse width	200/ (3 V_{CC}–8)			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	230			ns
$t_{wH(INT)}$	INT_0 to INT_4 input “H” pulse width	230			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_4 input “L” pulse width	230			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	2000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	200			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note : When bit 6 of address $001A_{16}$ is “1”. Divide this value by four when bit 6 of address $001A_{16}$ is “0”.

SWITCHING CHARACTERISTICS 1 (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	Fig. 32	$t_{C(SCLK1)}$/2–30			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width		$t_{C(SCLK1)}$/2–30			ns
$t_{d(SCLK1-TXD)}$	Serial I/O1 output delay time (Note 1)				140	ns
$t_{v(SCLK1-TXD)}$	Serial I/O1 output valid time (Note 1)		–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time				30	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time				30	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	Fig. 33	$t_{C(SCLK2)}$/2–160			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–160			ns
$t_{d(SCLK2-SOUT2)}$	Serial I/O2 output delay time				200	ns
$t_{v(SCLK2-SOUT2)}$	Serial I/O2 output valid time		0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time				40	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)	Fig. 32		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)			10	30	ns

Note1: When the P4₅/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: Pins XOUT and P7₀–P7₇ are excluded.

SWITCHING CHARACTERISTICS 2 (V_{CC} = 3.0 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	Fig. 32	$t_{C(SCLK1)}$/2–50			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width		$t_{C(SCLK1)}$/2–50			ns
$t_{d(SCLK1-TXD)}$	Serial I/O1 output delay time (Note 1)				350	ns
$t_{v(SCLK1-TXD)}$	Serial I/O1 output valid time (Note 1)		–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time				50	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time				50	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	Fig. 33	$t_{C(SCLK2)}$/2–240			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–240			ns
$t_{d(SCLK2-SOUT2)}$	Serial I/O2 output delay time				400	ns
$t_{v(SCLK2-SOUT2)}$	Serial I/O2 output valid time		0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time				50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 2)	Fig. 32		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 2)			20	50	ns

Note1: When the P4₅/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: Pins XOUT and P7₀–P7₇ are excluded.

TIMING REQUIREMENTS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{su(\overline{ONW}-\phi)}$	Before ϕ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\phi-\overline{ONW})}$	After ϕ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\phi)}$	Before ϕ data bus set up time	60			ns
$t_{h(\phi-DB)}$	After ϕ data bus hold time	0			ns
$t_{su(\overline{ONW}-\overline{RD})}$ $t_{su(\overline{ONW}-\overline{WR})}$	Before $\overline{RD}$ $\overline{ONW}$ input set up time Before $\overline{WR}$ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\overline{RD}-\overline{ONW})}$ $t_{h(\overline{WR}-\overline{ONW})}$	After $\overline{RD}$ $\overline{ONW}$ input hold time After $\overline{WR}$ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\overline{RD})}$	Before $\overline{RD}$ data bus set up time	65			ns
$t_{h(\overline{RD}-DB)}$	After $\overline{RD}$ data bus hold time	0			ns

SWITCHING CHARACTERISTICS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{c(\phi)}$	ϕ clock cycle time	Fig. 32		$2t_{c(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock "H" pulse width		$t_{c(X_{IN})}$–10			ns
$t_{WL(\phi)}$	ϕ clock "L" pulse width		$t_{c(X_{IN})}$–10			ns
$t_{d(\phi-AH)}$	After ϕ AD_{15}–AD_8 delay time			20	40	ns
$t_{v(\phi-AH)}$	After ϕ AD_{15}–AD_8 valid time		6	10		ns
$t_{d(\phi-AL)}$	After ϕ AD_7–AD_0 delay time			25	45	ns
$t_{v(\phi-AL)}$	After ϕ AD_7–AD_0 valid time		6	10		ns
$t_{d(\phi-SYNC)}$	SYNC delay time			20		ns
$t_{v(\phi-SYNC)}$	SYNC valid time			10		ns
$t_{d(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ delay time			10	20	ns
$t_{v(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ valid time		3	5	10	ns
$t_{d(\phi-DB)}$	After ϕ data bus delay time			20	70	ns
$t_{v(\phi-DB)}$	After ϕ data bus valid time		15			ns
$t_{WL(\overline{RD})}$ $t_{WL(\overline{WR})}$	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width		$t_{c(X_{IN})}$–10			ns
	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width (When one-wait is valid)		$3t_{c(X_{IN})}$–10			ns
$t_{d(AH-\overline{RD})}$ $t_{d(AH-\overline{WR})}$	After AD_{15}–AD_8 $\overline{RD}$ delay time After AD_{15}–AD_8 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–35	$t_{c(X_{IN})}$–15		ns
$t_{d(AL-\overline{RD})}$ $t_{d(AL-\overline{WR})}$	After AD_7–AD_0 $\overline{RD}$ delay time After AD_7–AD_0 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–40	$t_{c(X_{IN})}$–20		ns
$t_{v(\overline{RD}-AH)}$ $t_{v(\overline{WR}-AH)}$	After $\overline{RD}$ AD_{15}–AD_8 valid time After $\overline{WR}$ AD_{15}–AD_8 valid time		0	5		ns
$t_{v(\overline{RD}-AL)}$ $t_{v(\overline{WR}-AL)}$	After $\overline{RD}$ AD_7–AD_0 valid time After $\overline{WR}$ AD_7–AD_0 valid time		0	5		ns
$t_{d(\overline{WR}-DB)}$	After $\overline{WR}$ data bus delay time			15	65	ns
$t_{v(\overline{WR}-DB)}$	After $\overline{WR}$ data bus valid time		10			ns
$t_{d(\overline{RESET}-\overline{RESET_{OUT}})}$	$\overline{RESET_{OUT}}$ output delay time (Note 1)				200	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{RESET_{OUT}}$ output valid time (Note 1)		0		200	ns

Note 1: The $\overline{RESET_{OUT}}$ output goes "H" in sync with the fall of the ϕ clock that is anywhere between about 8 cycle and 13 cycles after the $\overline{RESET}$ input goes "H".

TIMING REQUIREMENTS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 3.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(\overline{ONW}-\phi)}$	Before ϕ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\phi-\overline{ONW})}$	After ϕ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\phi)}$	Before ϕ data bus set up time	180			ns
$t_{h(\phi-DB)}$	After ϕ data bus hold time	0			ns
$t_{su(\overline{ONW}-\overline{RD})}$ $t_{su(\overline{ONW}-\overline{WR})}$	Before $\overline{RD}$ $\overline{ONW}$ input set up time Before $\overline{WR}$ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\overline{RD}-\overline{ONW})}$ $t_{h(\overline{WR}-\overline{ONW})}$	After $\overline{RD}$ $\overline{ONW}$ input hold time After $\overline{WR}$ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\overline{RD})}$	Before $\overline{RD}$ data bus set up time	185			ns
$t_{h(\overline{RD}-DB)}$	After $\overline{RD}$ data bus hold time	0			ns

SWITCHING CHARACTERISTICS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

(V_{CC} = 3.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{c(\phi)}$	ϕ clock cycle time	Fig. 32		$2t_{c(X_{IN})}$		ns
$t_{wH(\phi)}$	ϕ clock "H" pulse width		$t_{c(X_{IN})}$–20			ns
$t_{wL(\phi)}$	ϕ clock "L" pulse width		$t_{c(X_{IN})}$–20			ns
$t_{d(\phi-AH)}$	After ϕ AD_{15}–AD_8 delay time				150	ns
$t_{v(\phi-AH)}$	After ϕ AD_{15}–AD_8 valid time		10	15		ns
$t_{d(\phi-AL)}$	After ϕ AD_7–AD_0 delay time				150	ns
$t_{v(\phi-AL)}$	After ϕ AD_7–AD_0 valid time		10	15		ns
$t_{d(\phi-SYNC)}$	SYNC delay time			40		ns
$t_{v(\phi-SYNC)}$	SYNC valid time			20		ns
$t_{d(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ delay time			15	25	ns
$t_{v(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ valid time		3	7	15	ns
$t_{d(\phi-DB)}$	After ϕ data bus delay time				200	ns
$t_{v(\phi-DB)}$	After ϕ data bus valid time		15			ns
$t_{wL(\overline{RD})}$ $t_{wL(\overline{WR})}$	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width		$t_{c(X_{IN})}$–20			ns
	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width (when one-wait is valid)		$3t_{c(X_{IN})}$–20			ns
$t_{d(AH-\overline{RD})}$ $t_{d(AH-\overline{WR})}$	After AD_{15}–AD_8 $\overline{RD}$ delay time After AD_{15}–AD_8 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–145			ns
$t_{d(AL-\overline{RD})}$ $t_{d(AL-\overline{WR})}$	After AD_7–AD_0 $\overline{RD}$ delay time After AD_7–AD_0 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–145			ns
$t_{v(\overline{RD}-AH)}$ $t_{v(\overline{WR}-AH)}$	After $\overline{RD}$ AD_{15}–AD_8 valid time After $\overline{WR}$ AD_{15}–AD_8 valid time		5	10		ns
$t_{v(\overline{RD}-AL)}$ $t_{v(\overline{WR}-AL)}$	After $\overline{RD}$ AD_7–AD_0 valid time After WR AD_7–AD_0 valid time		5	10		ns
$t_{d(\overline{WR}-DB)}$	After $\overline{WR}$ data bus delay time				195	ns
$t_{v(\overline{WR}-DB)}$	After $\overline{WR}$ data bus valid time		10			ns
$t_{d(\overline{RESET}-\overline{RESET_{OUT}})}$	$\overline{RESET_{OUT}}$ output delay time (Note 1)				300	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{RESET_{OUT}}$ output valid time (Note 1)		0		300	ns

Note1: The $\overline{RESET_{OUT}}$ output goes "H" in sync with the fall of the ϕ clock that is anywhere between about 8 cycle and 13 cycles after the $\overline{RESET}$ input goes "H".

ABSOLUTE MAXIMUM RATINGS (Extended operating temperature version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltage are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	T_a = 25 °C	500	mW
T_{opr}	Operating temperature		–40 to 85	°C
T_{stg}	Storage temperature		–65 to 150	°C

RECOMMENDED OPERATING CONDITIONS (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit
V_{CC}	Power source voltage		4.0	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage (when A-D converter is used)		2.0		V_{CC}	V
	Analog reference voltage (when D-A converter is used)		4.0		V_{CC}	
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage	AN_0–AN_7	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}, CNV_{SS}	0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.16 V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ (Note 1)			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ (Note 1)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ (Note 1)			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ (Note 1)			40	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 2)			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 3)			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ (Note 3)			5	mA
$f(X_{IN})$	Internal clock oscillation frequency				8	MHz

Note 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current $I_{OL(avg)}$, $I_{OH(avg)}$ in an average value measured over 100 ms.

ELECTRICAL CHARACTERISTICS (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 1)	I_{OH} = –10 mA	V_{CC}–2.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OL} = 10 mA			2.0	V
V_{T+} – V_{T-}	Hysteresis	$CNTR_0$, $CNTR_1$, INT_0–INT_4			0.4		V
V_{T+} – V_{T-}	Hysteresis	RXD, SCLK1, SIN2, SCLK2			0.5		V
V_{T+} – V_{T-}	Hysteresis	$\overline{\text{RESET}}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	$\overline{\text{RESET}}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	$\overline{\text{RESET}}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4		µA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V
I_{CC}	Power source current		$f(X_{IN})$ = 8 MHz		6.4	13	mA
			$f(X_{IN})$ = 5 MHz		4	8	mA
			When WIT instruction is executed with $f(X_{IN})$ = 8 MHz		1.5		mA
			When WIT instruction is executed with $f(X_{IN})$ = 5 MHz		1		mA
			When STP instruction is executed with clock stopped, output transistors isolated. T_a = 25 °C (Note 2)		0.1	1	µA
			When STP instruction is executed with clock stopped, output transistors isolated. T_a = 85 °C (Note 2)			10	µA

Note 1: $P4_5$ is measured when the $P4_5$/TXD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: With output transistors isolated and A-D converter having completed conversion, and not including current flowing through V_{REF} pin.

A-D CONVERTER CHARACTERISTICS(Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 2.0 V to V_{CC}, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			±1	±2.5	LSB
t_{CONV}	Conversion time				50	$t_C(\phi)$
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current (Note)	V_{REF} = 5.0 V	50	150	200	µA
$I_{I(AD)}$	A-D port input current			0.5	5.0	µA

Note: When D-A conversion registers (addresses 0036_{16} and 0037_{16}) contain "00_{16}".

D-A CONVERTER CHARACTERISTICS (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 3.0 V to V_{CC}, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
t_{su}	Setting time				3	µs
R_O	Output resistor		1	2.5	4	kΩ
I_{VREF}	Reference power source input current (Note)				3.2	mA

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being “00_{16}”, and excluding currents flowing through the A-D resistance ladder.

TIMING REQUIREMENTS (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	External clock input cycle time	125			ns
$t_{wH(X_{IN})}$	External clock input “H” pulse width	50			ns
$t_{wL(X_{IN})}$	External clock input “L” pulse width	50			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{wH(INT)}$	INT_0 to INT_4 input “H” pulse width	80			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_4 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	1000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	100			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1”. Divide this value by four when bit 6 of address $001A_{16}$ is “0”.

SWITCHING CHARACTERISTICS (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{wH(S_{CLK1})}$	Serial I/O1 clock output “H” pulse width	Fig. 32	$t_{c(S_{CLK1})}$/2–30			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock output “L” pulse width		$t_{c(S_{CLK1})}$/2–30			ns
$t_{d(S_{CLK1}-T_XD)}$	Serial I/O1 output delay time (Note 1)				140	ns
$t_{v(S_{CLK1}-T_XD)}$	Serial I/O1 output valid time (Note 1)		–30			ns
$t_{r(S_{CLK1})}$	Serial I/O1 clock output rise time				30	ns
$t_{f(S_{CLK1})}$	Serial I/O1 clock output fall time				30	ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock output “H” pulse width	Fig. 33	$t_{c(S_{CLK2})}$/2–160			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock output “L” pulse width		$t_{c(S_{CLK2})}$/2–160			ns
$t_{d(S_{CLK2}-S_{OUT2})}$	Serial I/O2 output delay time				200	ns
$t_{v(S_{CLK2}-S_{OUT2})}$	Serial I/O2 output valid time		0			ns
$t_{f(S_{CLK2})}$	Serial I/O2 clock output fall time				40	ns
$t_{r(CMOS)}$	CMOS output rise time (Note 2)	Fig. 32		10	30	ns
$t_{f(CMOS)}$	CMOS output fall time (Note 2)			10	30	ns

Note1: When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: Pins X_{OUT} pin and $P7_0$–$P7_7$ are excluded.

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TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (Extended operating temperature version) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(\overline{ONW}-\phi)}$	Before ϕ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\phi-\overline{ONW})}$	After ϕ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\phi)}$	Before ϕ data bus set up time	60			ns
$t_{h(\phi-DB)}$	After ϕ data bus hold time	0			ns
$t_{su(\overline{ONW}-\overline{RD})}$ $t_{su(\overline{ONW}-\overline{WR})}$	Before $\overline{RD}$ $\overline{ONW}$ input set up time Before $\overline{WR}$ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\overline{RD}-\overline{ONW})}$ $t_{h(\overline{WR}-\overline{ONW})}$	After $\overline{RD}$ $\overline{ONW}$ input hold time After $\overline{WR}$ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\overline{RD})}$	Before $\overline{RD}$ data bus set up time	65			ns
$t_{h(\overline{RD}-DB)}$	After $\overline{RD}$ data bus hold time	0			ns

SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (Extended operating temperature version) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{c(\phi)}$	ϕ clock cycle time	Fig. 32		$2t_{c(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock “H” pulse width		$t_{c(X_{IN})}$–10			ns
$t_{WL(\phi)}$	ϕ clock “L” pulse width		$t_{c(X_{IN})}$–10			ns
$t_{d(\phi-AH)}$	After ϕ AD_{15}–AD_8 delay time			20	40	ns
$t_{v(\phi-AH)}$	After ϕ AD_{15}–AD_8 valid time		6	10		ns
$t_{d(\phi-AL)}$	After ϕ AD_7–AD_0 delay time			25	45	ns
$t_{v(\phi-AL)}$	After ϕ AD_7–AD_0 valid time		6	10		ns
$t_{d(\phi-SYNC)}$	SYNC delay time			20		ns
$t_{v(\phi-SYNC)}$	SYNC valid time			10		ns
$t_{d(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ delay time			10	20	ns
$t_{v(\phi-\overline{WR})}$	$\overline{RD}$ and $\overline{WR}$ valid time		3	5	10	ns
$t_{d(\phi-DB)}$	After ϕ data bus delay time			20	70	ns
$t_{v(\phi-DB)}$	After ϕ data bus valid time		15			ns
$t_{WL(\overline{RD})}$ $t_{WL(\overline{WR})}$	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width		$t_{c(X_{IN})}$–10			ns
	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width (When one-wait is valid)		$3t_{c(X_{IN})}$–10			ns
$t_{d(AH-\overline{RD})}$ $t_{d(AH-\overline{WR})}$	After AD_{15}–AD_8 $\overline{RD}$ delay time After AD_{15}–AD_8 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–35	$t_{c(X_{IN})}$–15		ns
$t_{d(AL-\overline{RD})}$ $t_{d(AL-\overline{WR})}$	After AD_7–AD_0 $\overline{RD}$ delay time After AD_7–AD_0 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–40	$t_{c(X_{IN})}$–20		ns
$t_{v(\overline{RD}-AH)}$ $t_{v(\overline{WR}-AH)}$	After $\overline{RD}$ AD_{15}–AD_8 valid time After $\overline{WR}$ AD_{15}–AD_8 valid time		0	5		ns
$t_{v(\overline{RD}-AL)}$ $t_{v(\overline{WR}-AL)}$	After $\overline{RD}$ AD_7–AD_0 valid time After $\overline{WR}$ AD_7–AD_0 valid time		0	5		ns
$t_{d(\overline{WR}-DB)}$	After $\overline{WR}$ data bus delay time			15	65	ns
$t_{v(\overline{WR}-DB)}$	After $\overline{WR}$ data bus valid time		10			ns
$t_{d(\overline{RESET}-\overline{RESET_{OUT}})}$	$\overline{RESET_{OUT}}$ output delay time (Note 1)				200	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{RESET_{OUT}}$ output valid time (Note 1)		0		200	ns

Note 1: The $\overline{RESET_{OUT}}$ output goes “H” in sync with the fall of the ϕ clock that is anywhere between about 8 cycle and 13 cycles after the $\overline{RESET}$ input goes “H”.

ABSOLUTE MAXIMUM RATINGS (High-speed version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, V_{REF}, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$		–0.3 to 7.0	V
V_I	Input voltage CNV_{SS} Mask ROM version		–0.3 to 7.0	V
	Input voltage CNV_{SS} PROM version		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	T_a = 25 °C	500	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (High-speed version)

(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit
V_{CC}	Power source voltage ($f(X_{IN})$ < 4.15 MHz)		2.7	5.0	5.5	V
	Power source voltage ($f(X_{IN})$ = 10 MHz)		4.0	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage (when A-D converter is used)		2.0		V_{CC}	V
	Analog reference voltage (when D-A converter is used)		2.7		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage	AN_0–AN_7	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $\overline{RESET}$, CNV_{SS}	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.16 V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ (Note 1)			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ (Note 1)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$ (Note 1)			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$ (Note 1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$ (Note 1)			40	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 2)			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 3)			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ (Note 3)			5	mA
$f(X_{IN})$	Internal clock oscillation frequency (4.0 V < V_{CC} < 5.5 V)				10	MHz
	Internal clock oscillation frequency (2.7 V < V_{CC} < 4.0 V)				$4.5V_{CC}$–8	MHz

Note 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current $I_{OL(avg)}$, $I_{OH(avg)}$ in an average value measured over 100 ms.

ELECTRICAL CHARACTERISTICS (High-speed version)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ (Note 1)	I_{OH} = –10 mA, V_{CC} = 4.0 to 5.5 V		V_{CC}–2.0			V
			I_{OH} = –1.0 mA, V_{CC} = 2.7 to 5.5 V		V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OL} = 10 mA, V_{CC} = 4.0 to 5.5 V				2.0	V
			I_{OL} = 1.0 mA, V_{CC} = 2.7 to 5.5 V				1.0	V
V_{T+} – V_{T-}	Hysteresis	$CNTR_0$, $CNTR_1$, INT_0–INT_4				0.4		V
V_{T+} – V_{T-}	Hysteresis	R_XD, S_{CLK1}, S_{IN2}, S_{CLK2}				0.5		V
V_{T+} – V_{T-}	Hysteresis	$\overline{RESET}$				0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{CC}				5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{CC}				5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}			4		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $\overline{RESET}$, CNV_{SS}	V_I = V_{SS}				–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}			–4		µA
V_{RAM}	RAM hold voltage		With clock stopped		2.0		5.5	V
I_{CC}	Power source current		f(X_{IN}) = 10 MHz, V_{CC} = 5 V			8	16	mA
			f(X_{IN}) = 4 MHz, V_{CC} = 2.7 V			1.3	2	mA
			When WIT instruction is executed with f(X_{IN}) = 10 MHz, V_{CC} = 5 V			2		mA
			When WIT instruction is executed with f(X_{IN}) = 4 MHz, V_{CC} = 2.7 V			0.3		mA
			When STP instruction is executed with clock stopped, output transistors isolated.	T_a = 25 °C (Note 2)		0.1	1	µA
				T_a = 85 °C (Note 2)			10	µA

Note 1: $P4_5$ is measured when the $P4_5$/T_XD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: With output transistors isolated and A-D converter having completed conversion, and not including current flowing through V_{REF} pin.

A-D CONVERTER CHARACTERISTICS (High-speed version)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 2.0 V to V_{CC}, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			±1	±2.5	LSB
t_{CONV}	Conversion time				50	$t_C(\phi)$
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current (Note)	V_{REF} = 5.0 V	50	150	200	µA
$I_{I(AD)}$	A-D port input current			0.5	5.0	µA

Note: When D-A conversion registers (addresses 0036_{16} and 0037_{16}) contain "00_{16}".

D-A CONVERTER CHARACTERISTICS (High-speed version)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 2.7 V to V_{CC}, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy	V_{CC} = 4.0 to 5.5 V				1.0	%
		V_{CC} = 2.7 to 5.5 V				2.5	
t_{su}	Setting time					3	µs
R_O	Output resistor			1	2.5	4	kΩ
I_{VREF}	Reference power source input current (Note)					3.2	mA

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00_{16}", and excluding currents flowing through the A-D resistance ladder.

TIMING REQUIREMENTS 1 (High-speed version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	External clock input cycle time	100			ns
$t_{wH(X_{IN})}$	External clock input “H” pulse width	40			ns
$t_{wL(X_{IN})}$	External clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{wH(INT)}$	INT_0 to INT_4 input “H” pulse width	80			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_4 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	1000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	100			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “1”. Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address $001A_{16}$ is “0”.

TIMING REQUIREMENTS 2 (High-speed version)

V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	External clock input cycle time	1000/ (4.5 V_{CC}–8)			ns
$t_{wH(X_{IN})}$	External clock input “H” pulse width	400/ (4.5 V_{CC}–8)			ns
$t_{wL(X_{IN})}$	External clock input “L” pulse width	400/ (4.5 V_{CC}–8)			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	230			ns
$t_{wH(INT)}$	INT_0 to INT_4 input “H” pulse width	230			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_4 input “L” pulse width	230			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time	2000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(R_XD-S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK1}-R_XD)}$	Serial I/O1 input hold time	200			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note: When f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “1”. Divide this value by four when f(X_{IN}) = 2 MHz and bit 6 of address $001A_{16}$ is “0”.

SWITCHING CHARACTERISTICS 1 (High-speed version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	Fig. 32	$t_c(S_{CLK1})/2–30$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width		$t_c(S_{CLK1})/2–30$			ns
$t_d(S_{CLK1}–T_XD)$	Serial I/O1 output delay time (Note 1)				140	ns
$t_v(S_{CLK1}–T_XD)$	Serial I/O1 output valid time (Note 1)		–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time				30	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time				30	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	Fig. 33	$t_c(S_{CLK2})/2–160$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width		$t_c(S_{CLK2})/2–160$			ns
$t_d(S_{CLK2}–S_{OUT2})$	Serial I/O2 output delay time				200	ns
$t_v(S_{CLK2}–S_{OUT2})$	Serial I/O2 output valid time		0			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time				30	ns
$t_r(CMOS)$	CMOS output rising time (Note 2)	Fig. 32		10	30	ns
$t_f(CMOS)$	CMOS output falling time (Note 2)			10	30	ns

Note1: When the P4$_5$/T$_X$D P-channel output disable bit of the UART control register (bit 4 of address 001B$_{16}$) is “0”.
2: X$_{OUT}$ pin is excluded.

SWITCHING CHARACTERISTICS 2 (High-speed version)

(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	Fig. 32	$t_c(S_{CLK1})/2–50$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width		$t_c(S_{CLK1})/2–50$			ns
$t_d(S_{CLK1}–T_XD)$	Serial I/O1 output delay time (Note 1)				350	ns
$t_v(S_{CLK1}–T_XD)$	Serial I/O1 output valid time (Note 1)		–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time				50	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time				50	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	Fig. 33	$t_c(S_{CLK2})/2–240$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width		$t_c(S_{CLK2})/2–240$			ns
$t_d(S_{CLK2}–S_{OUT2})$	Serial I/O2 output delay time				400	ns
$t_v(S_{CLK2}–S_{OUT2})$	Serial I/O2 output valid time		0			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time				50	ns
$t_r(CMOS)$	CMOS output rising time (Note 2)	Fig. 32		20	50	ns
$t_f(CMOS)$	CMOS output falling time (Note 2)			20	50	ns

Note 1: When the P4$_5$/T$_X$D P-channel output disable bit of the UART control register (bit 4 of address 001B$_{16}$) is “0”.
2: X$_{OUT}$ pin is excluded.

TIMING REQUIREMENTS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (High-speed version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(\overline{ONW}-\phi)}$	Before ϕ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\phi-\overline{ONW})}$	After ϕ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\phi)}$	Before ϕ data bus set up time	50	25		ns
$t_{h(\phi-DB)}$	After ϕ data bus hold time	0			ns
$t_{su(\overline{ONW}-\overline{RD})}$ $t_{su(\overline{ONW}-\overline{WR})}$	Before $\overline{RD}$ $\overline{ONW}$ input set up time Before $\overline{WR}$ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\overline{RD}-\overline{ONW})}$ $t_{h(\overline{WR}-\overline{ONW})}$	After $\overline{RD}$ $\overline{ONW}$ input hold time After $\overline{WR}$ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\overline{RD})}$	Before $\overline{RD}$ data bus set up time	50	25		ns
$t_{h(\overline{RD}-DB)}$	After $\overline{RD}$ data bus hold time	0			ns

SWITCHING CHARACTERISTICS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (High-speed version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{c(\phi)}$	ϕ clock cycle time	Fig. 32		$2t_{c(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock “H” pulse width		$t_{c(X_{IN})}$–10			ns
$t_{WL(\phi)}$	ϕ clock “L” pulse width		$t_{c(X_{IN})}$–10			ns
$t_{d(\phi-AH)}$	After ϕ AD_{15}–AD_8 delay time			16	35	ns
$t_{v(\phi-AH)}$	After ϕ AD_{15}–AD_8 valid time		2	5		ns
$t_{d(\phi-AL)}$	After ϕ AD_7–AD_0 delay time			20	40	ns
$t_{v(\phi-AL)}$	After ϕ AD_7–AD_0 valid time		2	5		ns
$t_{d(\phi-SYNC)}$	SYNC delay time			16		ns
$t_{v(\phi-SYNC)}$	SYNC valid time			5		ns
$t_{d(\phi-DB)}$	After ϕ data bus delay time			15	30	ns
$t_{v(\phi-DB)}$	After ϕ data bus valid time		10			ns
$t_{WL(\overline{RD})}$ $t_{WL(\overline{WR})}$	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width		$t_{c(X_{IN})}$–10			ns
	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width (when one-wait is valid)		$3t_{c(X_{IN})}$–10			ns
$t_{d(AH-\overline{RD})}$ $t_{d(AH-\overline{WR})}$	After AD_{15}–AD_8 $\overline{RD}$ delay time After AD_{15}–AD_8 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–35	$t_{c(X_{IN})}$–16		ns
$t_{d(AL-\overline{RD})}$ $t_{d(AL-\overline{WR})}$	After AD_7–AD_0 $\overline{RD}$ delay time After AD_7–AD_0 $\overline{WR}$ delay time		$t_{c(X_{IN})}$–40	$t_{c(X_{IN})}$–20		ns
$t_{v(\overline{RD}-AH)}$ $t_{v(\overline{WR}-AH)}$	After $\overline{RD}$ AD_{15}–AD_8 valid time After $\overline{WR}$ AD_{15}–AD_8 valid time		2	5		ns
$t_{v(\overline{RD}-AL)}$ $t_{v(\overline{WR}-AL)}$	After $\overline{RD}$ AD_7–AD_0 valid time After $\overline{WR}$ AD_7–AD_0 valid time		2	5		ns
$t_{d(\overline{WR}-DB)}$	After $\overline{WR}$ data bus delay time			15	30	ns
$t_{v(\overline{WR}-DB)}$	After $\overline{WR}$ data bus valid time		10			ns
$t_{d(\overline{RESET}-\overline{RESET}_{OUT})}$	$\overline{RESET_{OUT}}$ output delay time (Note 1)				200	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{RESET_{OUT}}$ output valid time (Note 1)		0		100	ns

Note 1: The $\overline{RESET_{OUT}}$ output goes “H” in sync with the fall of the ϕ clock that is anywhere between about 8 cycle and 13 cycles after the $\overline{RESET}$ input goes “H”.

TIMING REQUIREMENTS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (High-speed version)

(V_{CC} = 2.7 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{su(\overline{ONW}-\phi)}$	Before ϕ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\phi-\overline{ONW})}$	After ϕ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\phi)}$	Before ϕ data bus set up time	120	60		ns
$t_{h(\phi-DB)}$	After ϕ data bus hold time	0			ns
$t_{su(\overline{ONW}-\overline{RD})}$ $t_{su(\overline{ONW}-\overline{WR})}$	Before $\overline{RD}$ $\overline{ONW}$ input set up time Before $\overline{WR}$ $\overline{ONW}$ input set up time	–20			ns
$t_{h(\overline{RD}-\overline{ONW})}$ $t_{h(\overline{WR}-\overline{ONW})}$	After $\overline{RD}$ $\overline{ONW}$ input hold time After $\overline{WR}$ $\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\overline{RD})}$	Before $\overline{RD}$ data bus set up time	120	60		ns
$t_{h(\overline{RD}-DB)}$	After $\overline{RD}$ data bus hold time	0			ns

SWITCHING CHARACTERISTICS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (High-Speed Version)

(V_{CC} = 2.7 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{c(\phi)}$	ϕ clock cycle time	Fig. 32		$2t_{c(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock "H" pulse width		$t_{c(X_{IN})}-20$			ns
$t_{WL(\phi)}$	ϕ clock "L" pulse width		$t_{c(X_{IN})}-20$			ns
$t_{d(\phi-AH)}$	AD_{15}–AD_8 delay time			40	100	ns
$t_{v(\phi-AH)}$	AD_{15}–AD_8 valid time		5	10		ns
$t_{d(\phi-AL)}$	AD_7–AD_0 delay time			50	100	ns
$t_{v(\phi-AL)}$	AD_7–AD_0 valid time		5	10		ns
$t_{d(\phi-SYNC)}$	SYNC delay time			40		ns
$t_{v(\phi-SYNC)}$	SYNC valid time			10		ns
$t_{d(\phi-DB)}$	Data bus delay time			30	80	ns
$t_{v(\phi-DB)}$	Data bus valid time		10			ns
$t_{WL(\overline{RD})}$ $t_{WL(\overline{WR})}$	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width		$t_{c(X_{IN})}-20$			ns
	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width (when one-wait is valid)		$3t_{c(X_{IN})}-20$			ns
$t_{d(AH-\overline{RD})}$ $t_{d(AH-\overline{WR})}$	After AD_{15}–AD_8 $\overline{RD}$ delay time After AD_{15}–AD_8 $\overline{WR}$ delay time		$t_{c(X_{IN})}-100$	$t_{c(X_{IN})}-40$		ns
$t_{d(AL-\overline{RD})}$ $t_{d(AL-\overline{WR})}$	After AD_7–AD_0 $\overline{RD}$ delay time After AD_7–AD_0 $\overline{WR}$ delay time		$t_{c(X_{IN})}-100$	$t_{c(X_{IN})}-50$		ns
$t_{v(\overline{RD}-AH)}$ $t_{v(\overline{WR}-AH)}$	After $\overline{RD}$ AD_{15}–AD_8 valid time After $\overline{WR}$ AD_{15}–AD_8 valid time		5	10		ns
$t_{v(\overline{RD}-AL)}$ $t_{v(\overline{WR}-AL)}$	After $\overline{RD}$ AD_7–AD_0 valid time After $\overline{WR}$ AD_7–AD_0 valid time		5	10		ns
$t_{d(\overline{WR}-DB)}$	After $\overline{WR}$ data bus delay time			30	80	ns
$t_{v(\overline{WR}-DB)}$	After $\overline{WR}$ data bus valid time		10			ns
$t_{d(\overline{RESET}-\overline{RESET}_{OUT})}$	$\overline{RESET}_{OUT}$ output delay time (Note 1)				300	ns
$t_{v(\phi-\overline{RESET})}$	$\overline{RESET}_{OUT}$ output valid time (Note 1)		0		150	ns

Note 1: The $\overline{RESET}_{OUT}$ output goes "H" in sync with the rise of the ϕ clock that is anywhere between about 8 cycle and 13 cycles after the $\overline{RESET}$ input goes "H".

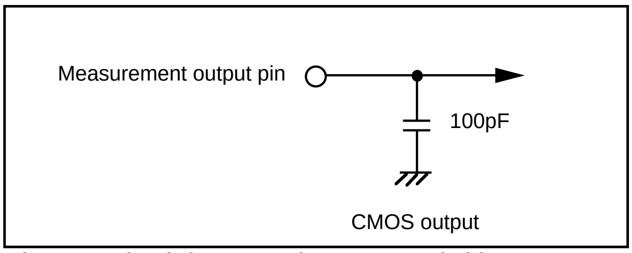


Fig. 32 Circuit for measuring output switching characteristics (1)

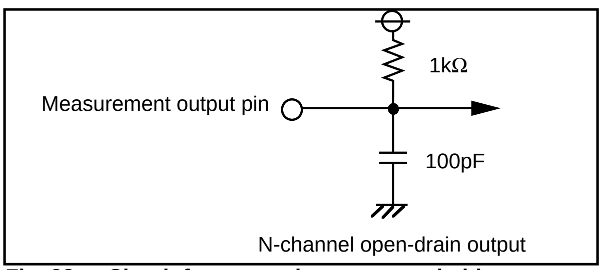
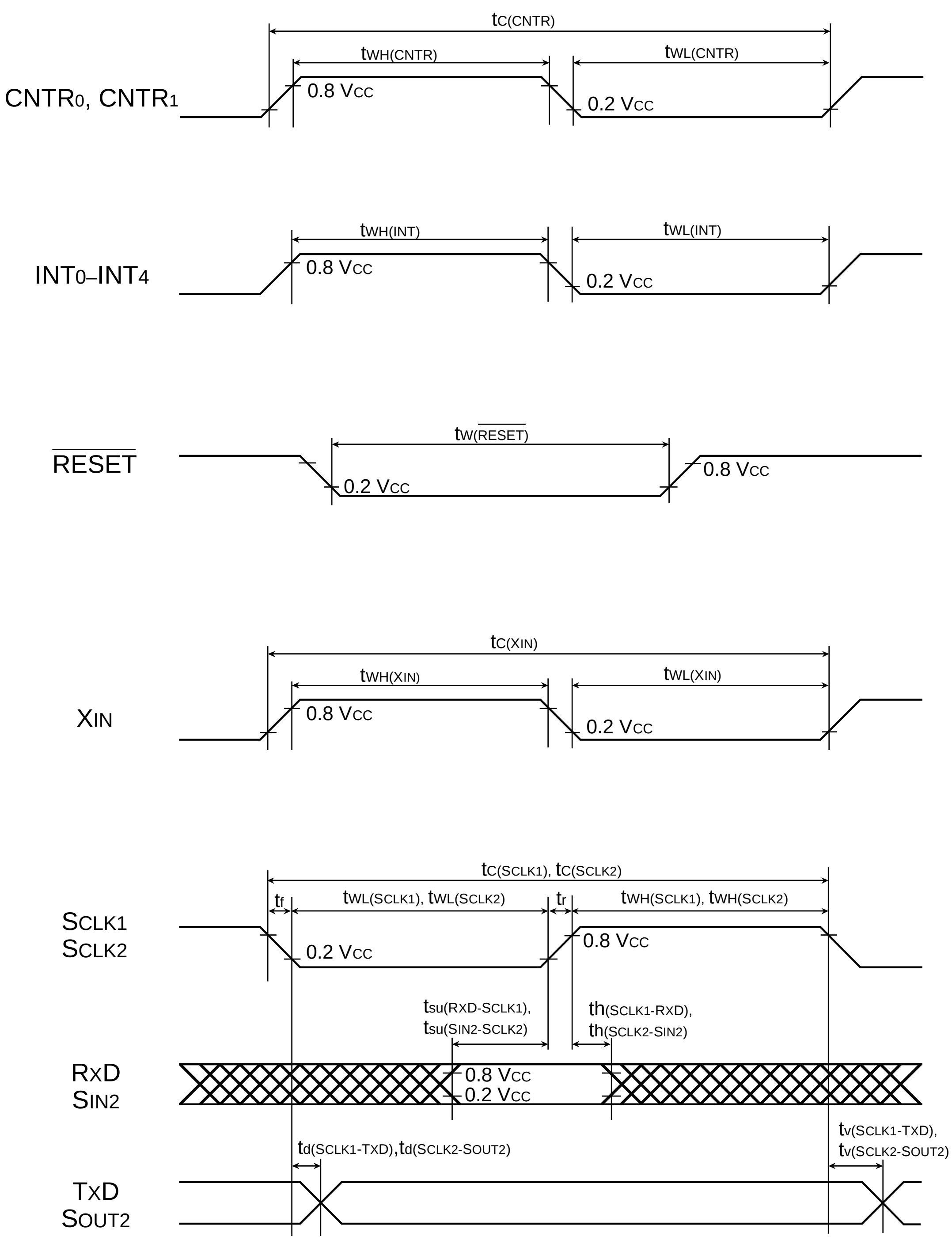


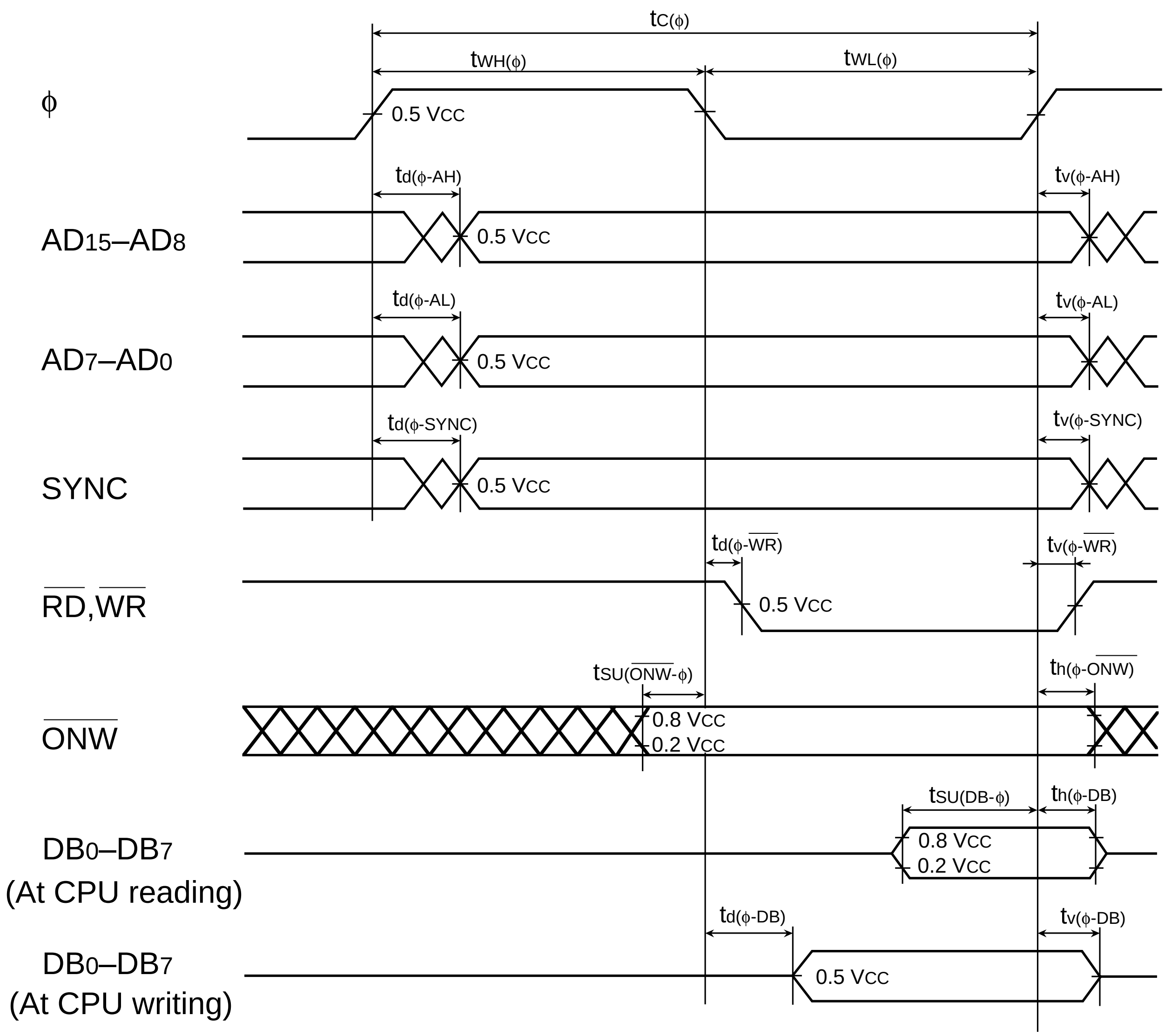
Fig. 33 Circuit for measuring output switching characteristics (2)

TIMING DIAGLAM

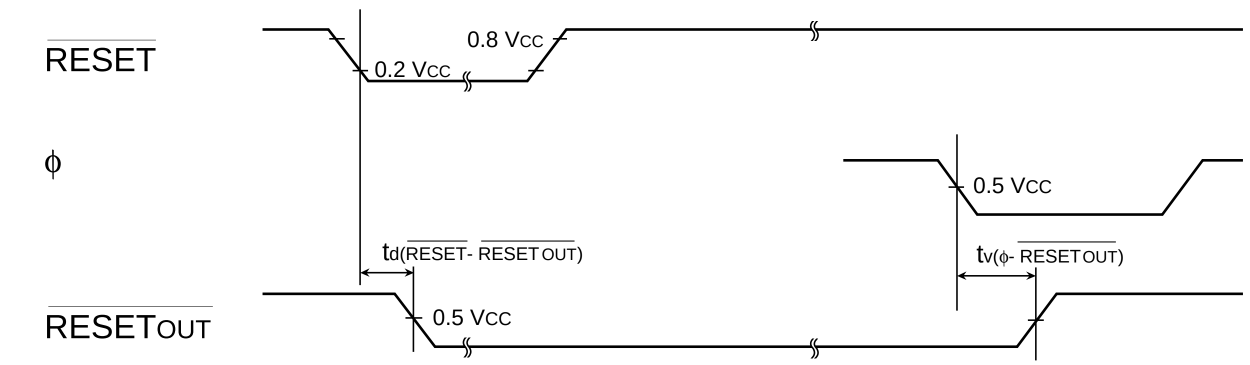
(1) Timing Diagram



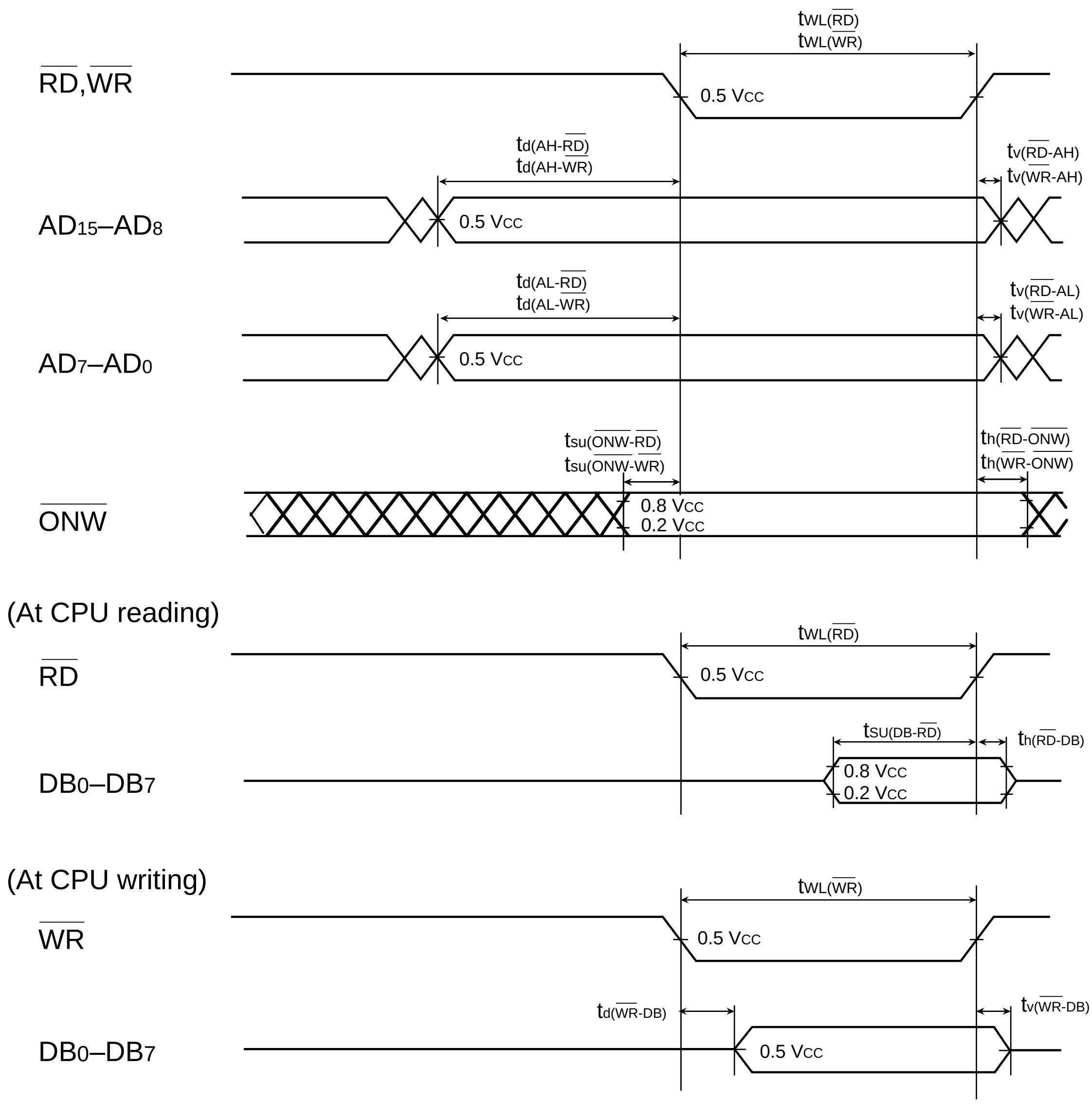
(2)Timing Diagram in Memory Expansion Mode and Microprocessor Mode (a)



(3)Timing Diagram in Microprocessor Mode



(4) Timing Diagram in Memory Expansion Mode and Microprocessor Mode (b)



Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

H-DF047-C KI-9609
New publication, effective Sep. 1996.
Specifications subject to change without notice.

REVISION DESCRIPTION LIST	3806GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	971128