DS07-16905-1ET1

Errata

FR80
32-BIT MICROCONTROLLER
MB91660 Series
DATA SHEET

2008.4.15

Page	Item	Description
54	■ I/O MAP	Address $000004FE_H$ was corrected as indicated by the shading below. ICSEL14[R/W] B,H → ICSEL14[R/W] B
89	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics	(2)Sub Clock (SBCLK) Input Standard was corrected as indicated by the shading below. Unit of input clock cycle "ms" → "μs"

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16905-1E

32-bit Microcontrollers

CMOS

FR80 MB91660 Series

MB91F662/V650

■ DESCRIPTION

The MB91660 series is a line of Fujitsu microcontrollers based on a 32-bit RISC CPU core that feature a variety of peripheral functions for embedded applications that demand high-performance and high-speed CPU processing.
This series is based on the FR80* family CPU and is implemented as a single chip.

* : FR is a line of products of FUJITSU MICROELECTRONICS Limited.

■ FEATURES

- FR80 CPU
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - General-purpose registers : 32-bit × 16
  - 16-bit fixed-length instructions (basic instructions) : 1 instruction per cycle
  - Instructions suitable for embedded applications
    - Memory-to-memory transfer, bit processing, barrel shift instructions, etc.
    - Instruction support for high level languages
      Function entry and exit instructions, instructions for register multi-load and multi-store
    - Bit search instruction
      “1” detection, “0” detection, transition point detection
    - Branch instructions with delay slots
      Reduced overhead when processing branches

(Continued)

The information for microcontroller supports is shown in the following homepage.
Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

http://edevice.fujitsu.com/micom/en-support/

2008.4

- Register interlock functions
  Facilitate coding in assembly language
- Built-in multiplier/instruction-level support
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupts (save PC and PS) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
  Instruction prefetch function has been added with 4 word instruction queue of CPU

- Instruction compatible with FR family CPU
  - Additional bit search instructions
  - No resource instructions or coprocessor instructions

- Maximum operating frequency
  - CPU : 33 MHz
  - Resources : 33 MHz
  - External bus : 33 MHz

- External bus interface
  - Operating frequency : Max 33 MHz
  - 24 address lines, 8- or 16-bit data I/O (separate busses or multiplexed bus)
  - Chip select output available for 4 independent programmable areas
    Programmable automatic wait cycle insertion for each area

- DMA controller (DMAC)
  - 8 channels
  - Address space : 32 bits (4 Gbytes)
  - Transfer modes : Block transfer/burst transfer/demand transfer
  - Address update : Increment/decrement/fixed (increment/decrement step size of 1, 2, or 4)
  - Transfer data length : Selectable from 8-bit, 16-bit, 32-bit
  - Block size : 1 to 16
  - Number of transfers : 1 to 65535
  - Transfer requests
    - Requests from software
    - Interrupt requests from peripheral resources (interrupt requests are shared, including external interrupts)
    - Requests from external pins
  - Reload functions : Reload can be specified on all channels
  - Priority order : Fixed (ch.0 > ch.1 > ch.2 > ch.3 > ...) or round-robin
  - Interrupt requests : Interrupts can be generated for transfer complete, transfer error, and transfer interrupted.

(Continued)

- Multifunction serial interface
  - 4 channels with 16-byte FIFO, 8 channels without FIFO
  - Operation mode is selectable from UART/CSIO/I²C for each channel (For ch.0, I²C is not available.)
    - UART
      - Full-duplex double buffer
      - Selectable parity on/off
      - Built-in dedicated baud rate generator
      - External clock can be used as a serial clock
      - Error detection function for parity, frame and overrun errors
    - CSIO
      - Full-duplex double buffer
      - Built-in dedicated baud rate generator
      - Overrun error detection function
    - I²C*
      - Supports both standard mode (Max 100 kbps)and Fast mode (Max 400 kbps)
      - Some channels are 5 V tolerant

- Interrupts
  - Total of 32 external interrupts (some pins are 5 V tolerant)
  - Interrupts from peripheral resources
  - Programmable interrupt levels (16 levels)
  - Can be used to return from stop mode, sleep mode

- A/D converter
  - 24 channels, 1 unit
  - 10-bit resolution
  - Conversion time : approx. 1.2 μs (PCLK = 33 MHz)
  - Priority conversion (2 levels)
  - Conversion modes : Single-shot conversion mode, scan conversion mode
  - Activation sources : Software, external trigger, base timer
  - Built-in FIFO for storing conversion data (for scan conversion:16, for priority conversion:4)

- D/A converter
  - 3 channels
  - 8-bit resolution

- Base timer
  - 16 channels
  - Operation mode is selectable from the followings for each channel
    - 16/32-bit reload timer
    - 16-bit PWM timer
    - 16/32-bit PWC timer
    - 16-bit PPG timer
  - Cascading connection between 2 channels allows them to be used as one 32-bit timer
  - Multiple channels can be started simultaneously
  - Input/output select function

- 16-bit reload timer
  - 3 channels (including 1 channel for REALOS)
  - Interval timer function
  - Count clock select function (peripheral clock (PCLK) divided by 2 to 64)

(Continued)

- Compare timer
  - 32-bit input capture : 8 channels
  - 32-bit output compare : 8 channels
  - 32-bit free-run timer : 2 channels

- Other interval timers
  - Up/down counter : 4 channels
  - Watch counter : 1 channel
  - Watchdog timer : 1 channel

- USB function with Mini-HOST
  - 1 channel
  - Supports Full-Speed only
  - USB I/O multiplexed

- Slave interface
  - Equipped with a register for communication along with large-capacity transmission/ reception FIFO that enables large amount of data transmission and reception.
  - Buffer: reception 1.5 Kbytes, transmission 1.5 Kbytes
  - Host function: A function to process by storing to a buffer. Once the buffer is full, this function stops data reception.
    Communication control is possible during data transmission/ reception. This enables CPU load reduction and efficiency of communication.
  - 16-bit data port
  - Transmission/ reception data port control function

- Main timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the main clock (MCLK)
  - Counts the oscillation stabilization wait time of the PLL clock (PLLCLK)
  - Can be used as an interval timer while the main clock (MCLK) oscillations is stable

- Sub timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the sub clock (SBCLK)
  - Can be used as an interval timer while the sub clock (SBCLK) oscillations is stable

- Clock generation
  - Main clock (MCLK) oscillator
  - Sub clock (SBCLK) oscillator
  - PLL clock (PLLCLK) oscillator

- Low-power dissipation mode
  - Stop mode
  - Watch mode
  - Sleep mode
  - Doze mode
  - Clock division function

(Continued)

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- Other features
  - I/O port
  - $\overline{\text{INIT}}$ pin is provided as a reset pin
  - Watchdog timer reset, software reset
  - Delay interrupt
  - Power supply
    - When USB not used : 2.7 V to 3.6 V
    - When USB used : 3.0 V to 3.6 V

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PRODUCT LINEUP

Part number / Parameter	MB91V650	MB91F662
Product type	Evaluation product	Flash memory product
Built-in program memory capacity	— (Support by emulation memory)	512 Kbytes (Flash)
Built-in RAM capacity	128 Kbytes	48 Kbytes
External bus interface	Yes	
DMA controller (DMAC)	8 channels	
Base timer	16 channels	
Multifunction serial interface	Without FIFO : 8 channels (ch.0 to ch.7) With FIFO : 4 channels (ch.8 to ch.11)	
External interrupt	32 (some pins are 5 V tolerant)	
10-bit A/D converter	32 channels (2 units)	24 channels (1 unit)
8-bit D/A converter	3 channels	
16-bit reload timer	3 channels	
Compare timer	32-bit input capture : 8 channels 32-bit output compare : 8 channels 32-bit free-run timer : 2 channels	
Up/Down counter	4 channels	
Watch counter	1 channel	
I/O port	154	99
USB function with Mini-HOST	1 channel	
Slave interface	Yes	
Main timer	1 channel	
Sub timer	1 channel	
Wild register	16 channels	
Debug function	DSU4	—

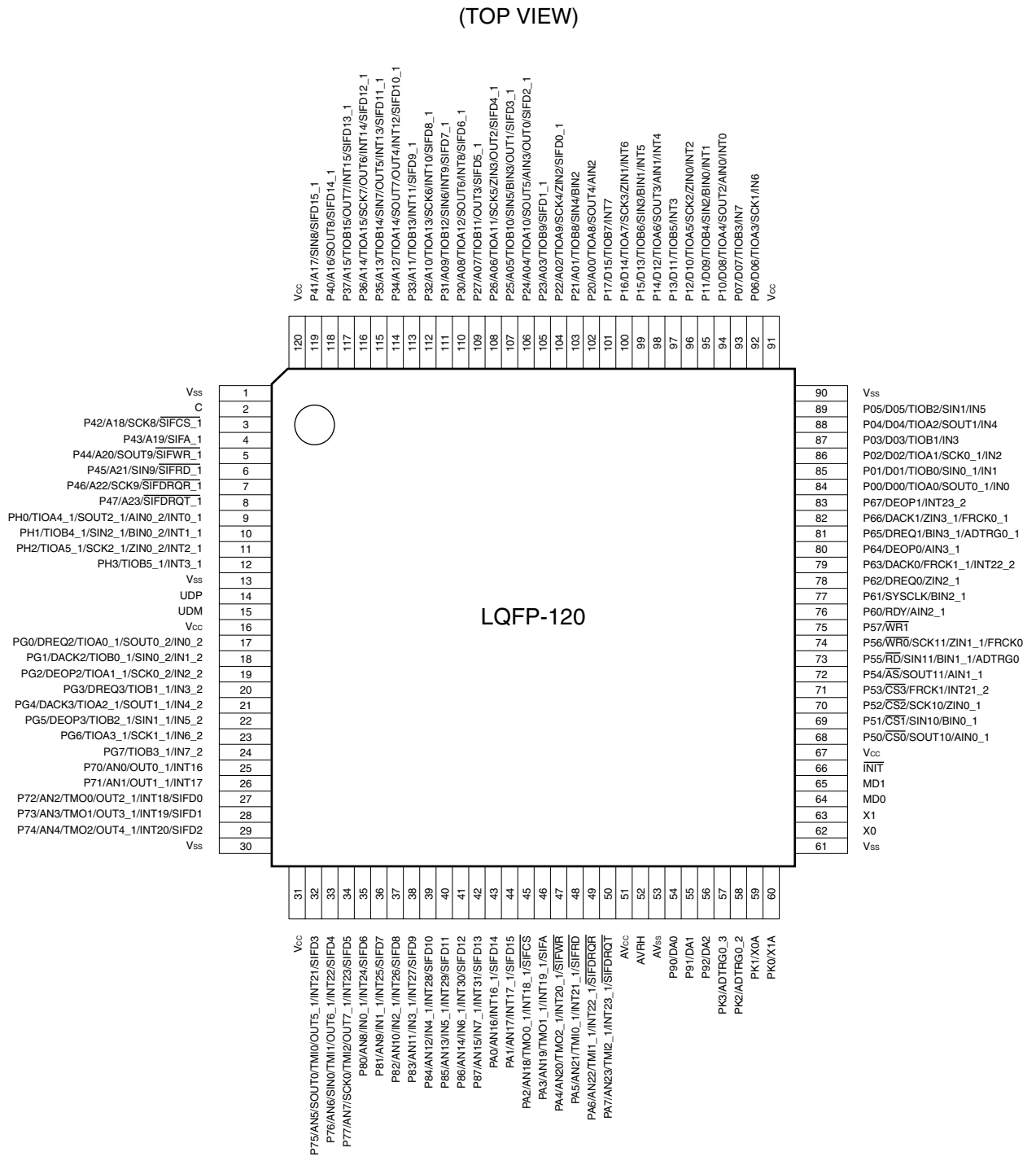
■ PACKAGES

Product name / Package	MB91F662
FPT-120P-M21	○

○ : Supported

Note: Refer to "■ PACKAGE DIMENSIONS" for detailed information on each package.

■ PIN ASSIGNMENT



Note : The number after the underscore (“_”) in pin names such as XXX_1 and XXX_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ PIN DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
1	V_{SS}	—	GND pin	—	—
2	C	—	Power stabilization capacity pin	—	—
3	P42	Q*2	General-purpose I/O port	—	○
	A18		External bus interface address bus bit18	—	—
	SCK8 (SCL8)		Multifunction serial interface ch.8 clock I/O pin. This pin operates as SCK8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL8 when it is used in an I²C (operation mode 4).	—	○
	$\overline{\text{SIFCS\_1}}$		Slave interface chip select signal input pin (Port 1)	○	—
4	P43	Q*2	General-purpose I/O port	—	○
	A19		External bus interface address bus bit19	—	—
	SIFA_1		Slave interface address signal input pin (Port 1)	○	—
5	P44	Q*2	General-purpose I/O port	—	○
	A20		External bus interface address bus bit20	—	—
	SOUT9 (SDA9)		Multifunction serial interface ch.9 output pin. This pin operates as SOUT9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA9 when it is used in an I²C (operation mode 4).	—	—
	$\overline{\text{SIFWR\_1}}$		Slave interface write strobe signal input pin (Port 1)	○	—
6	P45	Q*2	General-purpose I/O port	—	○
	A21		External bus interface address bus bit21	—	—
	SIN9		Multifunction serial interface ch.9 input pin	—	○
	$\overline{\text{SIFRD\_1}}$		Slave interface read strobe signal input pin (Port 1)	○	—
7	P46	D*2	General-purpose I/O port	—	○
	A22		External bus interface address bus bit22	—	—
	SCK9 (SCL9)		Multifunction serial interface ch.9 clock I/O pin. This pin operates as SCK9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL9 when it is used in an I²C (operation mode 4).	—	○
	$\overline{\text{SIFDRQR\_1}}$		Slave interface received data request signal output pin (Port 1)	—	—
8	P47	D*2	General-purpose I/O port	—	○
	A23		External bus interface address bus bit23	—	—
	$\overline{\text{SIFDRQT\_1}}$		Slave interface transmitted data request signal output pin (Port 1)	—	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
9	PH0	D*2	General-purpose I/O port	—	○
	TIOA4_1		Base timer ch.4 TIOA pin (Port 1)	—	○
	SOUT2_1 (SDA2_1)		Multifunction serial interface ch.2 output pin (Port 1). This pin operates as SOUT2_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2_1 when it is used in an I²C (operation mode 4).	—	—
	AIN0_2		Up/Down counter ch.0 AIN input pin (Port 2)	—	○
	INT0_1		External interrupt request 0 input pin (Port 1)	—	○
10	PH1	D*2	General-purpose I/O port	—	○
	TIOB4_1		Base timer ch.4 TIOB pin (Port 1)	—	○
	SIN2_1		Multifunction serial interface ch.2 input pin (Port 1)	—	○
	BIN0_2		Up/Down counter ch.0 BIN input pin (Port 2)	—	○
	INT1_1		External interrupt request 1 input pin (Port 1)	—	○
11	PH2	D*2	General-purpose I/O port	—	○
	TIOA5_1		Base timer ch.5 TIOA pin (Port 1)	—	○
	SCK2_1 (SCL2_1)		Multifunction serial interface ch.2 clock I/O pin (Port 1). This pin operates as SCK2_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2_1 when it is used in an I²C (operation mode 4).	—	○
	ZIN0_2		Up/Down counter ch.0 ZIN input pin (Port 2)	—	○
	INT2_1		External interrupt request 2 input pin (Port 1)	—	○
12	PH3	D*2	General-purpose I/O port	—	○
	TIOB5_1		Base timer ch.5 TIOB pin (Port 1)	—	○
	INT3_1		External interrupt request 3 input pin (Port 1)	—	○
13	V_{SS}	—	GND pin	—	—
14	UDP	USB	D+ pin of USB function in Mini-HOST	—	—
15	UDM	USB	D- pin of USB function in Mini-HOST	—	—
16	V_{CC}	—	Power pin	—	—
17	PG0	D*2	General-purpose I/O port	—	○
	DREQ2		DMA controller (DMAC) ch.2 transfer request input pin	—	○
	TIOA0_1		Base timer ch.0 TIOA pin (Port 1)	—	○
	SOUT0_2		Multifunction serial interface ch.0 output pin (Port 2). This pin operates as SOUT0_2 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
	IN0_2		32-bit input capture ch.0 input pin (Port 2)	—	○

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
18	PG1	D*2	General-purpose I/O port	—	○
	DACK2		DMA controller (DMAC) ch.2 transfer request acceptance signal output pin	—	—
	TIOB0_1		Base timer ch.0 TIOB pin (Port 1)	—	○
	SIN0_2		Multifunction serial interface ch.0 input pin (Port 2)	—	○
	IN1_2		32-bit input capture ch.1 input pin (Port 2)	—	○
19	PG2	D*2	General-purpose I/O port	—	○
	DEOP2		DMA controller (DMAC) ch.2 last transfer signal output pin	—	—
	TIOA1_1		Base timer ch.1 TIOA pin (Port 1)	—	○
	SCK0_2		Multifunction serial interface ch.0 clock I/O pin (Port 2). This pin operates as SCK0_2 when it is used in a UART/ CSIO (operation modes 0 to 2).	—	○
	IN2_2		32-bit input capture ch.2 input pin (Port 2)	—	○
20	PG3	D*2	General-purpose I/O port	—	○
	DREQ3		DMA controller (DMAC) ch.3 transfer request input pin	—	○
	TIOB1_1		Base timer ch.1 TIOB pin (Port 1)	—	○
	IN3_2		32-bit input capture ch.3 input pin (Port 2)	—	○
21	PG4	D*2	General-purpose I/O port	—	○
	DACK3		DMA controller (DMAC) ch.3 transfer request acceptance signal output pin	—	—
	TIOA2_1		Base timer ch.2 TIOA pin (Port 1)	—	○
	SOUT1_1 (SDA1_1)		Multifunction serial interface ch.1 output pin (Port 1). This pin operates as SOUT1_1 when it is used in a UART/ CSIO (operation modes 0 to 2) and as SDA1_1 when it is used in an I²C (operation mode 4).	—	—
	IN4_2		32-bit input capture ch.4 input pin (Port 2)	—	○
22	PG5	D*2	General-purpose I/O port	—	○
	DEOP3		DMA controller (DMAC) ch.3 last transfer signal output pin	—	—
	TIOB2_1		Base timer ch.2 TIOB pin (Port 1)	—	○
	SIN1_1		Multifunction serial interface ch.1 input pin (Port 1)	—	○
	IN5_2		32-bit input capture ch.5 input pin (Port 2)	—	○
23	PG6	D*2	General-purpose I/O port	—	○
	TIOA3_1		Base timer ch.3 TIOA pin (Port 1)	—	○
	SCK1_1 (SCL1_1)		Multifunction serial interface ch.1 clock I/O pin (Port 1). This pin operates as SCK1_1 when it is used in a UART/ CSIO (operation modes 0 to 2) and as SCL1_1 when it is used in an I²C (operation mode 4).	—	○
	IN6_2		32-bit input capture ch.6 input pin (Port 2)	—	○

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
24	PG7	D*2	General-purpose I/O port	—	○
	TIOB3_1		Base timer ch.3 TIOB pin (Port 1)	—	○
	IN7_2		32-bit input capture ch.7 input pin (Port 2)	—	○
25	P70	E	General-purpose I/O port	—	○
	AN0		10-bit A/D converter ch.0 analog input pin	—	—
	OUT0_1		32-bit output compare ch.0 output pin (Port 1)	—	—
	INT16		External interrupt request 16 input pin	—	○
26	P71	E	General-purpose I/O port	—	○
	AN1		10-bit A/D converter ch.1 analog input pin	—	—
	OUT1_1		32-bit output compare ch.1 output pin (Port 1)	—	—
	INT17		External interrupt request 17 input pin	—	○
27	P72	R	General-purpose I/O port	—	○
	AN2		10-bit A/D converter ch.2 analog input pin	—	—
	TMO0		16-bit reload timer ch.0 output pin	—	—
	OUT2_1		32-bit output compare ch.2 output pin (Port 1)	—	—
	INT18		External interrupt request 18 input pin	—	○
	SIFD0		Slave interface data I/O pin bit0	○	—
28	P73	R	General-purpose I/O port	—	○
	AN3		10-bit A/D converter ch.3 analog input pin	—	—
	TMO1		16-bit reload timer ch.1 output pin	—	—
	OUT3_1		32-bit output compare ch.3 output pin (Port 1)	—	—
	INT19		External interrupt request 19 input pin	—	○
	SIFD1		Slave interface data I/O pin bit1	○	—
29	P74	R	General-purpose I/O port	—	○
	AN4		10-bit A/D converter ch.4 analog input pin	—	—
	TMO2		16-bit reload timer ch.2 output pin	—	—
	OUT4_1		32-bit output compare ch.4 output pin (Port 1)	—	—
	INT20		External interrupt request 20 input pin	—	○
	SIFD2		Slave interface data I/O pin bit2	○	—
30	V_{SS}	—	GDN input pin	—	—
31	V_{CC}	—	Power pin	—	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
32	P75	R	General-purpose I/O port	—	○
	AN5		10-bit A/D converter ch.5 analog input pin	—	—
	SOUT0		Multifunction serial interface ch.0 output pin. This pin operates as SOUT0 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
	TMI0		16-bit reload timer ch.0 input pin	—	○
	OUT5_1		32-bit output compare ch.5 output pin (Port 1)	—	—
	INT21		External interrupt request 21 input pin	—	○
	SIFD3		Slave interface data I/O pin bit3	○	—
33	P76	R	General-purpose I/O port	—	○
	AN6		10-bit A/D converter ch.6 analog input pin	—	—
	SIN0		Multifunction serial interface ch.0 input pin	—	○
	TMI1		16-bit reload timer ch.1 input pin	—	○
	OUT6_1		32-bit output compare ch.6 output pin (Port 1)	—	—
	INT22		External interrupt request 22 input pin	—	○
	SIFD4		Slave interface data I/O pin bit4	○	—
34	P77	R	General-purpose I/O port	—	○
	AN7		10-bit A/D converter ch.7 analog input pin	—	—
	SCK0		Multifunction serial interface ch.0 clock I/O pin This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2).	—	○
	TMI2		16-bit reload timer ch.2 input pin	—	○
	OUT7_1		32-bit output compare ch.7 output pin (Port 1)	—	—
	INT23		External interrupt request 23 input pin	—	○
	SIFD5		Slave interface data I/O pin bit5	○	—
35	P80	R	General-purpose I/O port	—	○
	AN8		10-bit A/D converter ch.8 analog input pin	—	—
	IN0_1		32-bit input capture ch.0 input pin (Port 1)	—	○
	INT24		External interrupt request 24 input pin	—	○
	SIFD6		Slave interface data I/O pin bit6	○	—
36	P81	R	General-purpose I/O port	—	○
	AN9		10-bit A/D converter ch.9 analog input pin	—	—
	IN1_1		32-bit input capture ch.1 input pin (Port 1)	—	○
	INT25		External interrupt request 25 input pin	—	○
	SIFD7		Slave interface data I/O pin bit7	○	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
37	P82	R	General-purpose I/O port	—	○
	AN10		10-bit A/D converter ch.10 analog input pin	—	—
	IN2_1		32-bit input capture ch.2 input pin (Port 1)	—	○
	INT26		External interrupt request 26 input pin	—	○
	SIFD8		Slave interface data I/O pin bit8	○	—
38	P83	R	General-purpose I/O port	—	○
	AN11		10-bit A/D converter ch.11 analog input pin	—	—
	IN3_1		32-bit input capture ch.3 input pin (Port 1)	—	○
	INT27		External interrupt request 27 input pin	—	○
	SIFD9		Slave interface data I/O pin bit9	○	—
39	P84	R	General-purpose I/O port	—	○
	AN12		10-bit A/D converter ch.12 analog input pin	—	—
	IN4_1		32-bit input capture ch.4 input pin (Port 1)	—	○
	INT28		External interrupt request 28 input pin	—	○
	SIFD10		Slave interface data I/O pin bit10	○	—
40	P85	R	General-purpose I/O port	—	○
	AN13		10-bit A/D converter ch.13 analog input pin	—	—
	IN5_1		32-bit input capture ch.5 input pin (Port 1)	—	○
	INT29		External interrupt request 29 input pin	—	○
	SIFD11		Slave interface data I/O pin bit11	○	—
41	P86	R	General-purpose I/O port	—	○
	AN14		10-bit A/D converter ch.14 analog input pin	—	—
	IN6_1		32-bit input capture ch.6 input pin (Port 1)	—	○
	INT30		External interrupt request 30 input pin	—	○
	SIFD12		Slave interface data I/O pin bit12	○	—
42	P87	R	General-purpose I/O port	—	○
	AN15		10-bit A/D converter ch.15 analog input pin	—	—
	IN7_1		32-bit input capture ch.7 input pin (Port 1)	—	○
	INT31		External interrupt request 31 input pin	—	○
	SIFD13		Slave interface data I/O pin bit13	○	—
43	PA0	R	General-purpose I/O port	—	○
	AN16		10-bit A/D converter ch.16 analog input pin	—	—
	INT16_1		External interrupt request 16 input pin (Port 1)	—	○
	SIFD14		Slave interface data I/O pin bit14	○	—

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Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
44	PA1	R	General-purpose I/O port	—	○
	AN17		10-bit A/D converter ch.17 analog input pin	—	—
	INT17_1		External interrupt request 17 input pin (Port 1)	—	○
	SIFD15		Slave interface data I/O pin bit15	○	—
45	PA2	R	General-purpose I/O port	—	○
	AN18		10-bit A/D converter ch.18 analog input pin	—	—
	TMO0_1		16-bit reload timer ch.0 output pin (Port 1)	—	—
	INT18_1		External interrupt request 18 input pin (Port 1)	—	○
	$\overline{\text{SIFCS}}$		Slave interface chip select signal input pin	○	—
46	PA3	R	General-purpose I/O port	—	○
	AN19		10-bit A/D converter ch.19 analog input pin	—	—
	TMO1_1		16-bit reload timer ch.1 output pin (Port 1)	—	—
	INT19_1		External interrupt request 19 input pin (Port 1)	—	○
	SIFA		Slave interface address signal input pin	○	—
47	PA4	R	General-purpose I/O port	—	○
	AN20		10-bit A/D converter ch.20 analog input pin	—	—
	TMO2_1		16-bit reload timer ch.2 output pin (Port 1)	—	—
	INT20_1		External interrupt request 20 input pin (Port 1)	—	○
	$\overline{\text{SIFWR}}$		Slave interface write strobe signal input pin	○	—
48	PA5	R	General-purpose I/O port	—	○
	AN21		10-bit A/D converter ch.21 analog input pin	—	—
	TMI0_1		16-bit reload timer ch.0 input pin (Port 1)	—	○
	INT21_1		External interrupt request 21 input pin (Port 1)	—	○
	$\overline{\text{SIFRD}}$		Slave interface read strobe signal input pin	○	—
49	PA6	E	General-purpose I/O port	—	○
	AN22		10-bit A/D converter ch.22 analog input pin	—	—
	TMI1_1		16-bit reload timer ch.1 input pin (Port 1)	—	○
	INT22_1		External interrupt request 22 input pin (Port 1)	—	○
	$\overline{\text{SIFDRQR}}$		Slave interface received data request signal output pin	—	—
50	PA7	E	General-purpose I/O port	—	○
	AN23		10-bit A/D converter ch.23 analog input pin	—	—
	TMI2_1		16-bit reload timer ch.2 input pin (Port 1)	—	○
	INT23_1		External interrupt request 23 input pin (Port 1)	—	○
	$\overline{\text{SIFDRQT}}$		Slave interface transmitted data request signal output pin	—	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
51	AV_{CC}	—	10-bit A/D converter and 8-bit D/A converter analog power pin	—	—
52	AVRH	—	10-bit A/D converter analog reference voltage input pin	—	—
53	AV_{SS}	—	10-bit A/D converter and 8-bit D/A converter GND pin	—	—
54	P90	F	General-purpose I/O port	—	○
	DA0		8-bit D/A converter ch.0 analog output pin	—	—
55	P91	F	General-purpose I/O port	—	○
	DA1		8-bit D/A converter ch.1 analog output pin	—	—
56	P92	F	General-purpose I/O port	—	○
	DA2		8-bit D/A converter ch.2 analog output pin	—	—
57	PK3	C	General-purpose I/O port	—	○
	ADTRG0_3		10-bit A/D converter external trigger input pin (Port 3)	—	○
58	PK2	C	General-purpose I/O port	—	○
	ADTRG0_2		10-bit A/D converter external trigger input pin (Port 2)	—	○
59	PK1	I	General-purpose I/O port	—	○
	X0A		Sub clock (oscillation) input pin	—	○
60	PK0	I	General-purpose I/O port	—	○
	X1A		Sub clock (oscillation) I/O pin	—	—
61	V_{SS}	—	GND pin	—	—
62	X0	A	Main clock (oscillation) input pin	—	○
63	X1	A	Main clock (oscillation) I/O pin	—	—
64	MD0	P	Mode 0 pin. The I/O circuit type for the flash memory products is P. During normal communication, MD0=L must be input. During serial programming to flash memory, MD0=H must be input.	—	○
65	MD1	P	Mode 1 pin. Input must always be at the "L" level. The I/O circuit type for the flash memory products is P.	—	○
66	$\overline{INIT}$	P	External reset input pin. A reset is valid when $\overline{INIT}$=L. The I/O circuit type for the flash memory products is P.	—	○
67	V_{CC}	—	Power pin	—	—
68	P50	C	General-purpose I/O port	—	○
	$\overline{CS0}$		External bus interface chip select 0 output pin	—	—
	SOUT10 (SDA10)		Multifunction serial interface ch.10 output pin. This pin operates as SOUT10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA10 when it is used in an I^2C (operation mode 4).	—	—
	AIN0_1		Up/Down counter ch.0 AIN input pin (Port 1)	—	○

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
69	P51	C	General-purpose I/O port	—	○
	$\overline{CS1}$		External bus interface chip select 1 output pin	—	—
	SIN10		Multifunction serial interface ch.10 input pin	—	○
	BIN0_1		Up/Down counter ch.0 BIN input pin (Port 1)	—	○
70	P52	C	General-purpose I/O port	—	○
	$\overline{CS2}$		External bus interface chip select 2 output pin	—	—
	SCK10 (SCL10)		Multifunction serial interface ch.10 clock I/O pin. This pin operates as SCK10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL10 when it is used in an I²C (operation mode 4).	—	○
	ZIN0_1		Up/Down counter ch.0 ZIN input pin (Port 1)	—	○
71	P53	C	General-purpose I/O port	—	○
	$\overline{CS3}$		External bus interface chip select 3 output pin	—	—
	FRCK1		32-bit free-run timer ch.1 external clock input pin	—	○
	INT21_2		External interrupt request 21 input pin (Port 2)	—	○
72	P54	C	General-purpose I/O port	—	○
	$\overline{AS}$		External bus interface address strobe output pin	—	—
	SOUT11 (SDA11)		Multifunction serial interface ch.11 output pin. This pin operates as SOUT11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA11 when it is used in an I²C (operation mode 4).	—	—
	AIN1_1		Up/Down counter ch.1 AIN input pin (Port 1)	—	○
73	P55	C	General-purpose I/O port	—	○
	$\overline{RD}$		External bus interface read strobe output pin	—	—
	SIN11		Multifunction serial interface ch.11 input pin	—	○
	BIN1_1		Up/Down counter ch.1 BIN input pin (Port 1)	—	○
	ADTRG0		10-bit A/D converter external trigger input pin	—	○
74	P56	C	General-purpose I/O port	—	○
	$\overline{WR0}$		External bus interface write strobe 0 output pin	—	—
	SCK11 (SCL11)		Multifunction serial interface ch.11 clock I/O pin. This pin operates as SCK11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL11 when it is used in an I²C (operation mode 4).	—	○
	ZIN1_1		Up/Down counter ch.1 ZIN input pin (Port 1)	—	○
	FRCK0		32-bit free-run timer ch.0 external clock input pin	—	○
75	P57	C	General-purpose I/O port	—	○
	$\overline{WR1}$		External bus interface write strobe 1 output pin	—	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
76	P60	B	General-purpose I/O port	—	○
	RDY		External bus interface ready input pin	○	—
	AIN2_1		Up/Down counter ch.2 AIN input pin (Port 1)	—	○
77	P61	C	General-purpose I/O port	—	○
	SYSCLK		External bus interface bus clock output pin	—	—
	BIN2_1		Up/Down counter ch.2 BIN input pin (Port 1)	—	○
78	P62	C	General-purpose I/O port	—	○
	DREQ0		DMA controller (DMAC) ch.0 transfer request input pin	—	○
	ZIN2_1		Up/Down counter ch.2 ZIN input pin (Port 1)	—	○
79	P63	C	General-purpose I/O port	—	○
	DACK0		DMA controller (DMAC) ch.0 transfer request acceptance signal output pin	—	—
	FRCK1_1		32-bit free-run timer ch.1 external clock input pin (Port 1)	—	○
	INT22_2		External interrupt request 22 input pin (Port 2)	—	○
80	P64	C	General-purpose I/O port	—	○
	DEOP0		DMA controller (DMAC) ch.0 last transfer signal output pin	—	—
	AIN3_1		Up/Down counter ch.3 AIN input pin (Port 1)	—	○
81	P65	C	General-purpose I/O port	—	○
	DREQ1		DMA controller (DMAC) ch.1 transfer request input pin	—	○
	BIN3_1		Up/Down counter ch.3 BIN input pin (Port 1)	—	○
	ADTRG0_1		10-bit A/D converter external trigger input pin (Port 1)	—	○
82	P66	C	General-purpose I/O port	—	○
	DACK1		DMA controller (DMAC) ch.1 transfer request acceptance signal output pin	—	—
	ZIN3_1		Up/Down counter ch.3 ZIN input pin (Port 1)	—	○
	FRCK0_1		32-bit free-run timer ch.0 external clock input pin (Port 1)	—	○
83	P67	C	General-purpose I/O port	—	○
	DEOP1		DMA controller (DMAC) ch.1 last transfer signal output pin	—	—
	INT23_2		External interrupt request 23 input pin (Port 2)	—	○
84	P00	B	General-purpose I/O port	—	○
	D00		External bus interface data bus bit0	○	—
	TIOA0		Base timer ch.0 TIOA pin	—	—
	SOUT0_1		Multifunction serial interface ch.0 output pin (Port 1). This pin operates as SOUT0_1 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
	IN0		32-bit input capture ch.0 input pin	—	○

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
85	P01	B	General-purpose I/O port	—	○
	D01		External bus interface data bus bit1	○	—
	TIOB0		Base timer ch.0 TIOB pin	—	○
	SIN0_1		Multifunction serial interface ch.0 input pin (Port 1)	—	○
	IN1		32-bit input capture ch.1 input pin	—	○
86	P02	B	General-purpose I/O port	—	○
	D02		External bus interface data bus bit2	○	—
	TIOA1		Base timer ch.1 TIOA pin	—	○
	SCK0_1		Multifunction serial interface ch.0 clock I/O pin (Port 1). This pin operates as SCK0_1 when it is used in a UART/CSIO (operation modes 0 to 2).	—	○
	IN2		32-bit input capture ch.2 input pin	—	○
87	P03	B	General-purpose I/O port	—	○
	D03		External bus interface data bus bit3	○	—
	TIOB1		Base timer ch.1 TIOB pin	—	○
	IN3		32-bit input capture ch.3 input pin	—	○
88	P04	B	General-purpose I/O port	—	○
	D04		External bus interface data bus bit4	○	—
	TIOA2		Base timer ch.2 TIOA pin	—	—
	SOUT1 (SDA1)		Multifunction serial interface ch.1 output pin. This pin operates as SOUT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I²C (operation mode 4).	—	—
	IN4		32-bit input capture ch.4 input pin	—	○
89	P05	B	General-purpose I/O port	—	○
	D05		External bus interface data bus bit5	○	—
	TIOB2		Base timer ch.2 TIOB pin	—	○
	SIN1		Multifunction serial interface ch.1 input pin	—	○
	IN5		32-bit input capture ch.5 input pin	—	○
90	V_{SS}	—	GND pin	—	—
91	V_{CC}	—	Power pin	—	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
92	P06	B	General-purpose I/O port	—	○
	D06		External bus interface data bus bit6	○	—
	TIOA3		Base timer ch.3 TIOA pin	—	○
	SCK1 (SCL1)		Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I²C (operation mode 4).	—	○
	IN6		32-bit input capture ch.6 input pin	—	○
93	P07	B	General-purpose I/O port	—	○
	D07		External bus interface data bus bit7	○	—
	TIOB3		Base timer ch.3 TIOB pin	—	○
	IN7		32-bit input capture ch.7 input pin	—	○
94	P10	B	General-purpose I/O port	—	○
	D08		External bus interface data bus bit8	○	—
	TIOA4		Base timer ch.4 TIOA pin	—	—
	SOUT2 (SDA2)		Multifunction serial interface ch.2 output pin. This pin operates as SOUT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I²C (operation mode 4).	—	—
	AIN0		Up/Down counter ch.0 AIN input pin	—	○
	INT0		External interrupt request 0 input pin	—	○
95	P11	B	General-purpose I/O port	—	○
	D09		External bus interface data bus bit9	○	—
	TIOB4		Base timer ch.4 TIOB pin	—	○
	SIN2		Multifunction serial interface ch.2 input pin	—	○
	BIN0		Up/Down counter ch.0 BIN input pin	—	○
	INT1		External interrupt request 1 input pin	—	○
96	P12	B	General-purpose I/O port	—	○
	D10		External bus interface data bus bit10	○	—
	TIOA5		Base timer ch.5 TIOA pin	—	○
	SCK2 (SCL2)		Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I²C (operation mode 4).	—	○
	ZIN0		Up/Down counter ch.0 ZIN input pin	—	○
	INT2		External interrupt request 2 input pin	—	○

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
97	P13	B	General-purpose I/O port	—	○
	D11		External bus interface data bus bit11	○	—
	TIOB5		Base timer ch.5 TIOB pin	—	○
	INT3		External interrupt request 3 input pin	—	○
98	P14	B	General-purpose I/O port	—	○
	D12		External bus interface data bus bit12	○	—
	TIOA6		Base timer ch.6 TIOA pin	—	—
	SOUT3 (SDA3)		Multifunction serial interface ch.3 output pin. This pin operates as SOUT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I²C (operation mode 4).	—	—
	AIN1		Up/Down counter ch.1 AIN input pin	—	○
	INT4		External interrupt request 4 input pin	—	○
99	P15	B	General-purpose I/O port	—	○
	D13		External bus interface data bus bit13	○	—
	TIOB6		Base timer ch.6 TIOB pin	—	○
	SIN3		Multifunction serial interface ch.3 input pin	—	○
	BIN1		Up/Down counter ch.1 BIN input pin	—	○
	INT5		External interrupt request 5 input pin	—	○
100	P16	B	General-purpose I/O port	—	○
	D14		External bus interface data bus bit14	○	—
	TIOA7		Base timer ch.7 TIOA pin	—	○
	SCK3 (SCL3)		Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I²C (operation mode 4).	—	○
	ZIN1		Up/Down counter ch.1 ZIN input pin	—	○
	INT6		External interrupt request 6 input pin	—	○
101	P17	B	General-purpose I/O port	—	○
	D15		External bus interface data bus bit15	○	—
	TIOB7		Base timer ch.7 TIOB pin	—	○
	INT7		External interrupt request 7 input pin	—	○

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
102	P20	D*2	General-purpose I/O port	—	○
	A00		External bus interface address bus bit0	—	—
	TIOA8		Base timer ch.8 TIOA pin	—	—
	SOUT4 (SDA4)		Multifunction serial interface ch.4 output pin. This pin operates as SOUT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I²C (operation mode 4).	—	—
	AIN2		Up/Down counter ch.2 AIN input pin	—	○
103	P21	D*2	General-purpose I/O port	—	○
	A01		External bus interface address bus bit1	—	—
	TIOB8		Base timer ch.8 TIOB pin	—	○
	SIN4		Multifunction serial interface ch.4 input pin	—	○
	BIN2		Up/Down counter ch.2 BIN input pin	—	○
104	P22	Q*2	General-purpose I/O port	—	○
	A02		External bus interface address bus bit2	—	—
	TIOA9		Base timer ch.9 TIOA pin	—	○
	SCK4 (SCL4)		Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I²C (operation mode 4).	—	○
	ZIN2		Up/Down counter ch.2 ZIN input pin	—	○
	SIFD0_1		Slave interface data I/O pin bit0 (Port 1)	○	—
105	P23	Q*2	General-purpose I/O port	—	○
	A03		External bus interface address bus bit3	—	—
	TIOB9		Base timer ch.9 TIOB pin	—	○
	SIFD1_1		Slave interface data I/O pin bit1 (Port 1)	○	—
106	P24	Q*2	General-purpose I/O port	—	○
	A04		External bus interface address bus bit4	—	—
	TIOA10		Base timer ch.10 TIOA pin	—	—
	SOUT5 (SDA5)		Multifunction serial interface ch.5 output pin. This pin operates as SOUT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I²C (operation mode 4).	—	—
	AIN3		Up/Down counter ch.3 AIN input pin	—	○
	OUT0		32-bit output compare ch.0 output pin	—	—
	SIFD2_1		Slave interface data I/O pin bit2 (Port 1)	○	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
107	P25	Q*2	General-purpose I/O port	—	○
	A05		External bus interface address bus bit5	—	—
	TIOB10		Base timer ch.10 TIOB pin	—	○
	SIN5		Multifunction serial interface ch.5 input pin	—	○
	BIN3		Up/Down counter ch.3 BIN input pin	—	○
	OUT1		32-bit output compare ch.1 output pin	—	—
	SIFD3_1		Slave interface data I/O pin bit3 (Port 1)	○	—
108	P26	Q*2	General-purpose I/O port	—	○
	A06		External bus interface address bus bit6	—	—
	TIOA11		Base timer ch.11 TIOA pin	—	○
	SCK5 (SCL5)		Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I²C (operation mode 4).	—	○
	ZIN3		Up/Down counter ch.3 ZIN input pin	—	○
	OUT2		32-bit output compare ch.2 output pin	—	—
	SIFD4_1		Slave interface data I/O pin bit4 (Port 1)	○	—
109	P27	Q*2	General-purpose I/O port	—	○
	A07		External bus interface address bus bit7	—	—
	TIOB11		Base timer ch.11 TIOB pin	—	○
	OUT3		32-bit output compare ch.3 output pin	—	—
	SIFD5_1		Slave interface data I/O pin bit5 (Port 1)	○	—
110	P30	Q*2	General-purpose I/O port	—	○
	A08		External bus interface address bus bit8	—	—
	TIOA12		Base timer ch.12 TIOA pin	—	—
	SOUT6 (SDA6)		Multifunction serial interface ch.6 output pin. This pin operates as SOUT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I²C (operation mode 4).	—	○
	INT8		External interrupt request 8 input pin	—	○
	SIFD6_1		Slave interface data I/O pin bit6 (Port 1)	○	—
111	P31	Q*2	General-purpose I/O port	—	○
	A09		External bus interface address bus bit9	—	—
	TIOB12		Base timer ch.12 TIOB pin	—	○
	SIN6		Multifunction serial interface ch.6 input pin	—	○
	INT9		External interrupt request 9 input pin	—	○
	SIFD7_1		Slave interface data I/O pin bit7 (Port 1)	○	—

(Continued)

Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
112	P32	Q*2	General-purpose I/O port	—	○
	A10		External bus interface address bus bit10	—	—
	TIOA13		Base timer ch.13 TIOA pin	—	○
	SCK6 (SCL6)		Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I²C (operation mode 4).	—	○
	INT10		External interrupt request 10 input pin	—	○
	SIFD8_1		Slave interface data I/O pin bit8 (Port 1)	○	—
113	P33	Q*2	General-purpose I/O port	—	○
	A11		External bus interface address bus bit11	—	—
	TIOB13		Base timer ch.13 TIOB pin	—	○
	INT11		External interrupt request 11 input pin	—	○
	SIFD9_1		Slave interface data I/O pin bit9 (Port 1)	○	—
114	P34	Q*2	General-purpose I/O port	—	○
	A12		External bus interface address bus bit12	—	—
	TIOA14		Base timer ch.14 TIOA pin	—	—
	SOUT7 (SDA7)		Multifunction serial interface ch.7 output pin. This pin operates as SOUT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I²C (operation mode 4).	—	○
	OUT4		32-bit output compare ch.4 output pin	—	—
	INT12		External interrupt request 12 input pin	—	○
	SIFD10_1		Slave interface data I/O pin bit10 (Port 1)	○	—
115	P35	Q*2	General-purpose I/O port	—	○
	A13		External bus interface address bus bit13	—	—
	TIOB14		Base timer ch.14 TIOB pin	—	○
	SIN7		Multifunction serial interface ch.7 input pin	—	○
	OUT5		32-bit output compare ch.5 output pin	—	—
	INT13		External interrupt request 13 input pin	—	○
	SIFD11_1		Slave interface data I/O pin bit11 (Port 1)	○	—

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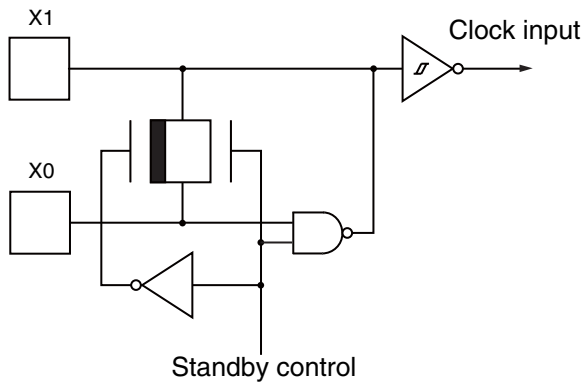
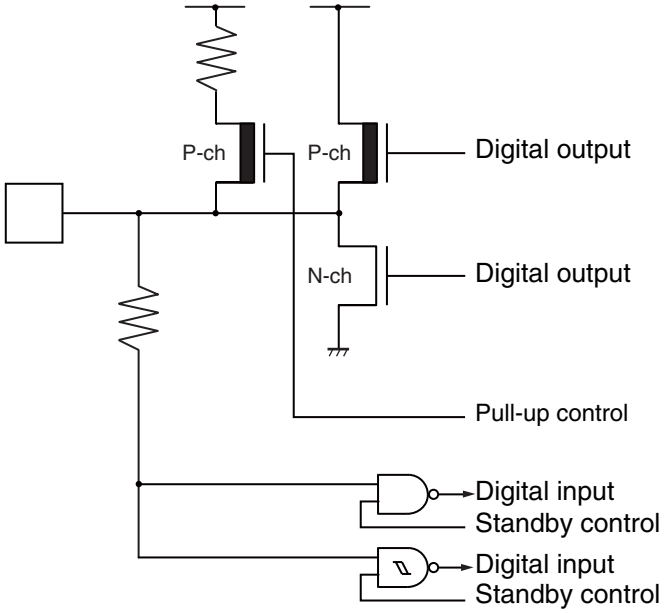
Pin Number	Pin Name	I/O Circuit Type*1	Function	CMOS level input	CMOS level hysteresis input
116	P36	Q*2	General-purpose I/O port	—	○
	A14		External bus interface address bus bit14	—	—
	TIOA15		Base timer ch.15 TIOA pin	—	○
	SCK7 (SCL7)		Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/ CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I²C (operation mode 4).	—	○
	OUT6		32-bit output compare ch.6 output pin	—	—
	INT14		External interrupt request 14 input pin	—	○
	SIFD12_1		Slave interface data I/O pin bit12 (Port 1)	○	—
117	P37	Q*2	General-purpose I/O port	—	○
	A15		External bus interface address bus bit15	—	—
	TIOB15		Base timer ch.15 TIOB pin	—	○
	OUT7		32-bit output compare ch.7 output pin	—	—
	INT15		External interrupt request 15 input pin	—	○
	SIFD13_1		Slave interface data I/O pin bit13 (Port 1)	○	—
118	P40	Q*2	General-purpose I/O port	—	○
	A16		External bus interface address bus bit16	—	—
	SOUT8 (SDA8)		Multifunction serial interface ch.8 output pin. This pin operates as SOUT8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA8 when it is used in an I²C (operation mode 4).	—	—
	SIFD14_1		Slave interface data I/O pin bit14 (Port 1)	○	—
119	P41	Q*2	General-purpose I/O port	—	○
	A17		External bus interface address bus bit17	—	—
	SIN8		Multifunction serial interface ch.8 input pin	—	○
	SIFD15_1		Slave interface data I/O pin bit15 (Port 1)	○	—
120	V_{CC}	—	Power pin	—	—

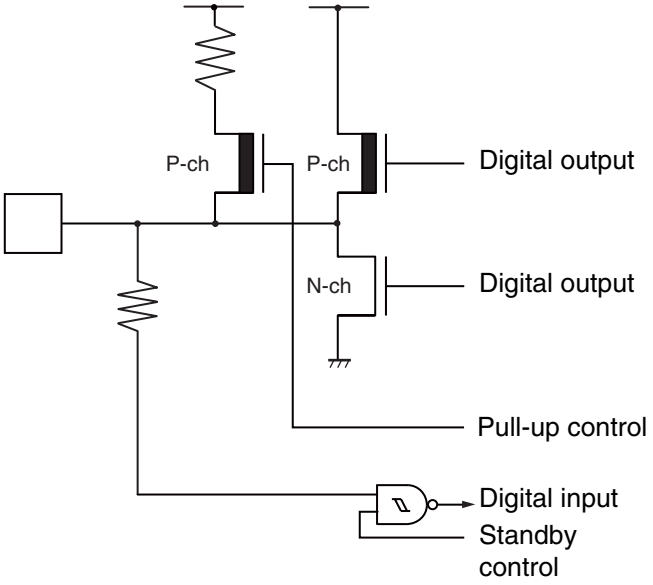
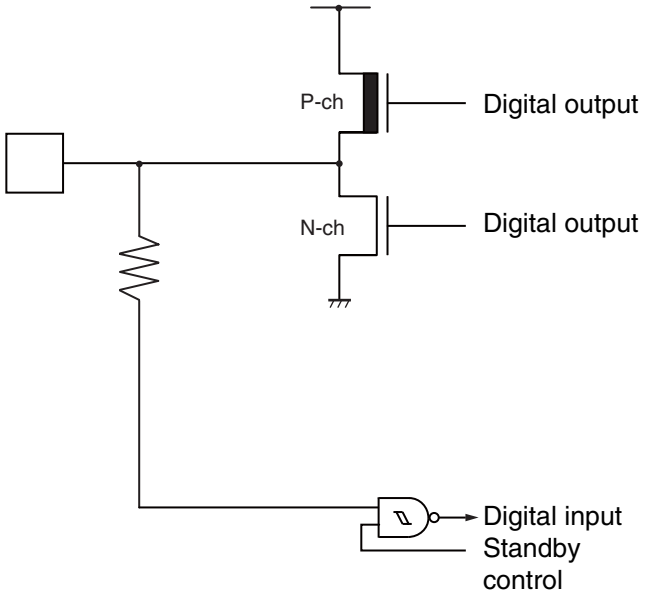
*1 : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

*2 : 5 V tolerant pin (I/O circuit type “D” only)

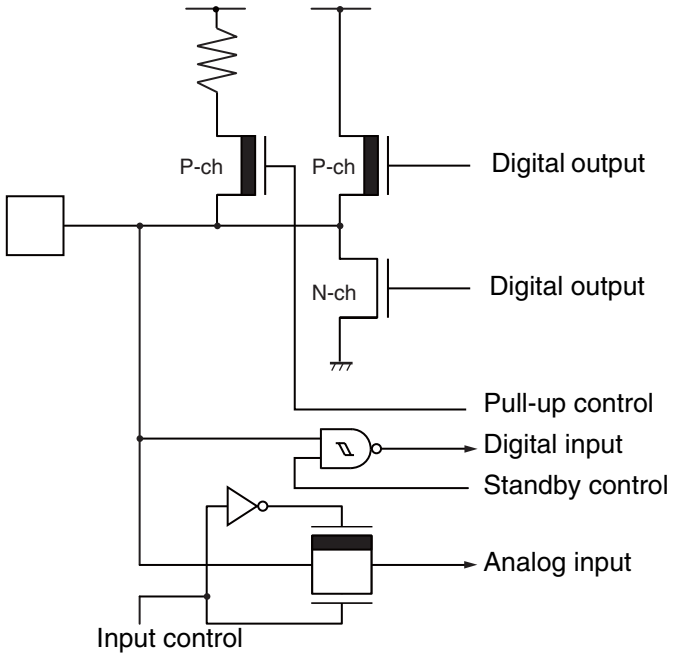
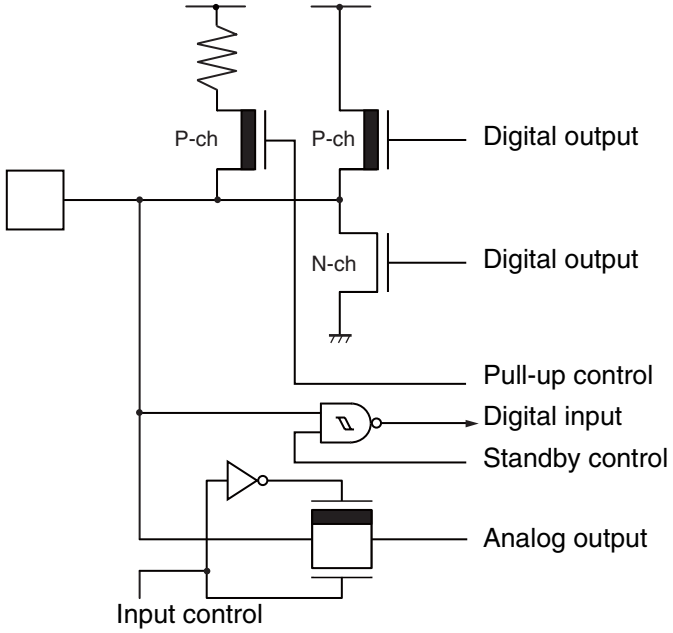
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance approx. 1 MΩ • With standby control
B		• CMOS level output • CMOS level input • CMOS level hysteresis input • With pull-up control • With standby control Note: CMOS level input when input address/ data, RDY pin of external bus interface and slave interface. Input other than above situations, CMOS level hysteresis input.

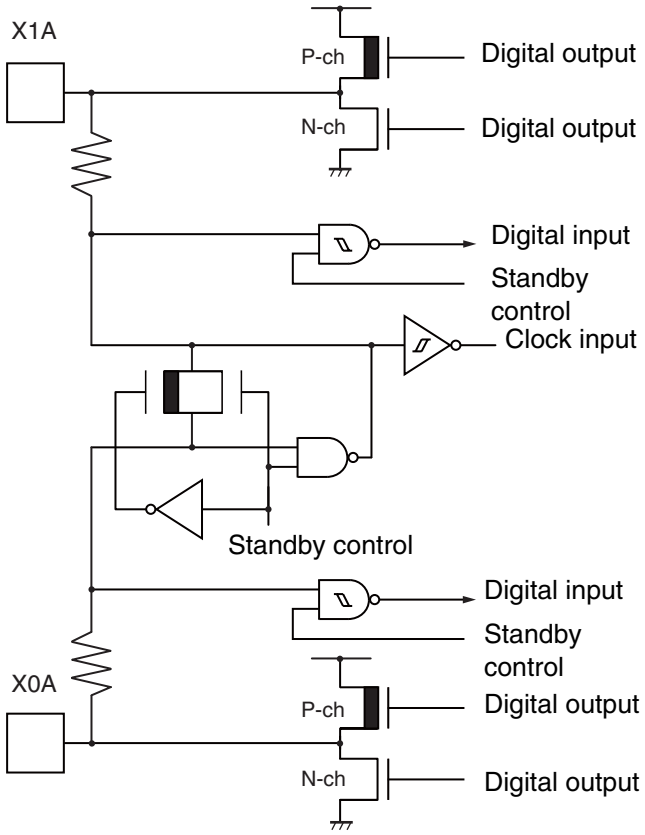
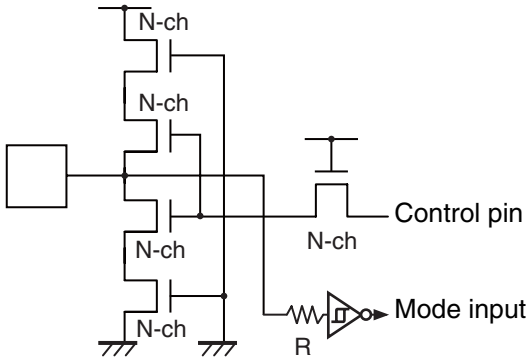
(Continued)

Type	Circuit	Remarks
C		• CMOS level output • CMOS level hysteresis input • With pull-up control • With standby control
D		• CMOS level output • CMOS level hysteresis input • 5 V tolerant input • With standby control

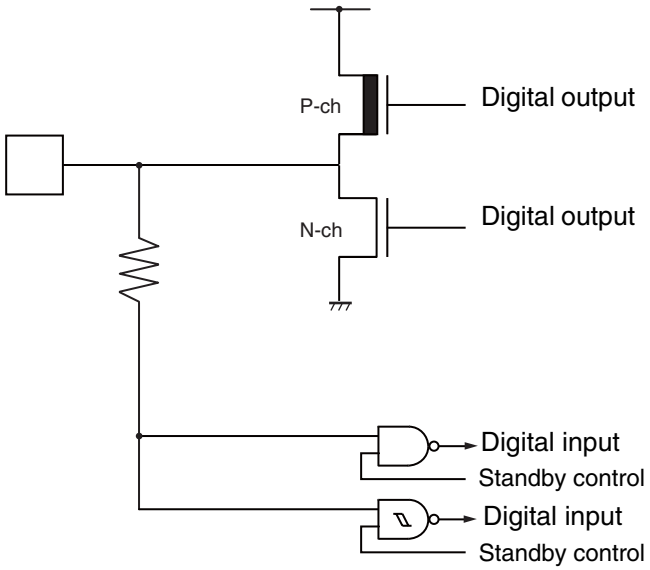
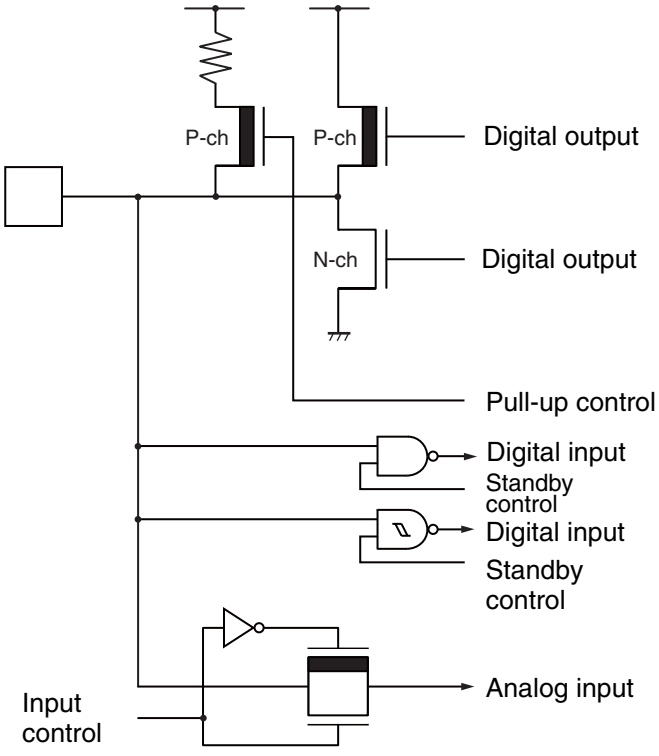
(Continued)

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up control • With standby control
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up control • With standby control

(Continued)

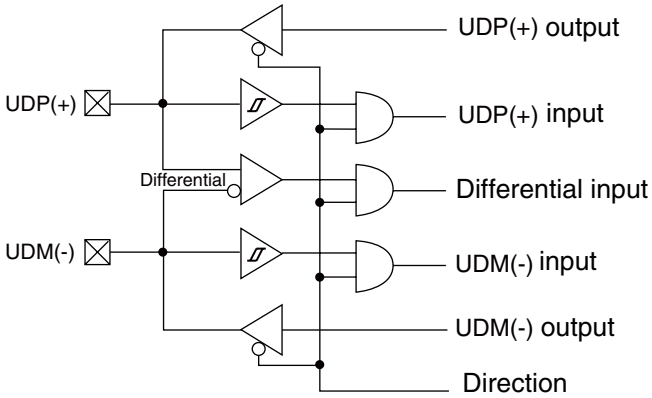
Type	Circuit	Remarks
I		• Oscillation feedback resistance approx.10 MΩ • CMOS level output • CMOS level hysteresis input • With standby control
P		• Flash memory product only • CMOS level hysteresis input • High voltage control for testing Flash memory

(Continued)

Type	Circuit	Remarks
Q		• CMOS level output • CMOS level input • CMOS level hysteresis input • 5 V tolerant input • With standby control
R		• CMOS level output • CMOS level input • CMOS level hysteresis input • With input control • Analog input • With pull-up control • With standby control

(Continued)

(Continued)

Type	Circuit	Remarks
USB		USB I/O pin

■ PRECAUTIONS FOR HANDLING THE DEVICES

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

• Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

• Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

• Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

• Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

Note: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:
(a) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
(b) Be sure that abnormal current flows do not occur during the power-on sequence.

• Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

• Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

• Precautions Related to Usage of Devices

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU's recommended conditions. For detailed information about mount conditions, contact your FUJITSU sales representative.

• Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder.

In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

• Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU ranking of recommended conditions.

• Lead-Free Packaging

Note: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

• Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(a) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(b) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(c) When necessary, FUJITSU packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(d) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

• Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU recommended conditions for baking.

Condition: 125 °C/24 h

• Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(a) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(b) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(c) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(d) Ground all fixtures and instruments, or protect with anti-static measures.

(e) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

• Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

Note : Plastic molded devices are flammable, and therefore should not be used near combustible substances.

If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU products in other special environmental conditions should consult with FUJITSU sales representatives.

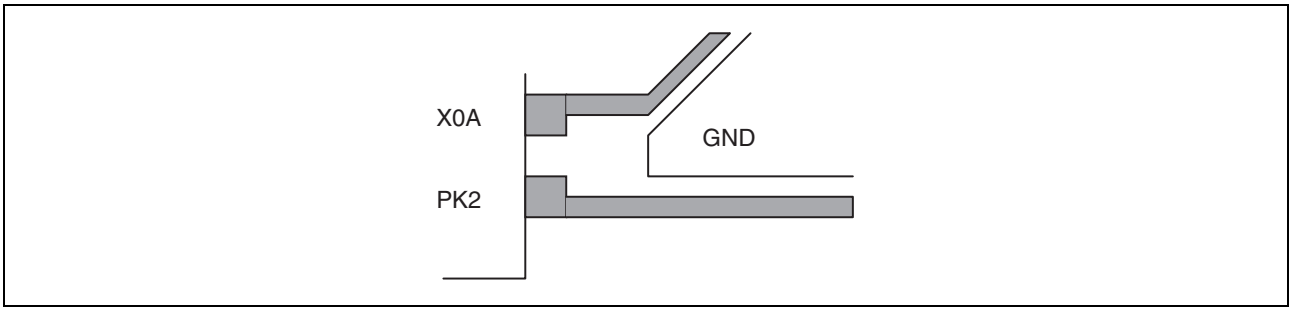
■ HANDLING DEVICES

• Power supply pins

In products with multiple V_{CC} and V_{SS} pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at low impedance.
It is also advisable that a ceramic capacitor of approximately 0.1 μF be connected as a bypass capacitor between V_{CC} and V_{SS} near this device.

• Crystal oscillator circuit

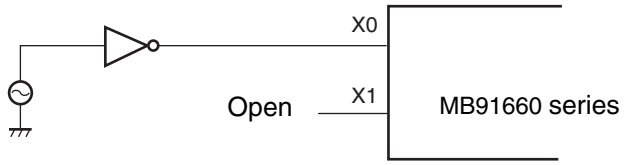
Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.
It is strongly recommended that the PC board artwork be designed such that the X0 and X1 pins are surrounded by ground plane as this is expected to produce stable operation.
If a 32 kHz oscillator is used (X0A, X1A), use the PK2 pin for an input that changes as infrequently as possible. Furthermore, take steps such as shown in the following figure to prevent the X0A and PK2 wiring from running parallel to each other.
If 32 kHz oscillation is not used, there are no limitations.



• Using an external clock

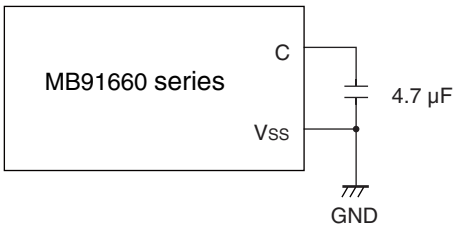
When using an external clock, the clock signal should be input to the X0 pin only and the X1 pin should be kept open.

• Example of Using an External Clock



• C Pin

As MB91660 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 µF to the C pin for use by the regulator.



• Mode pins (MD0, MD1)

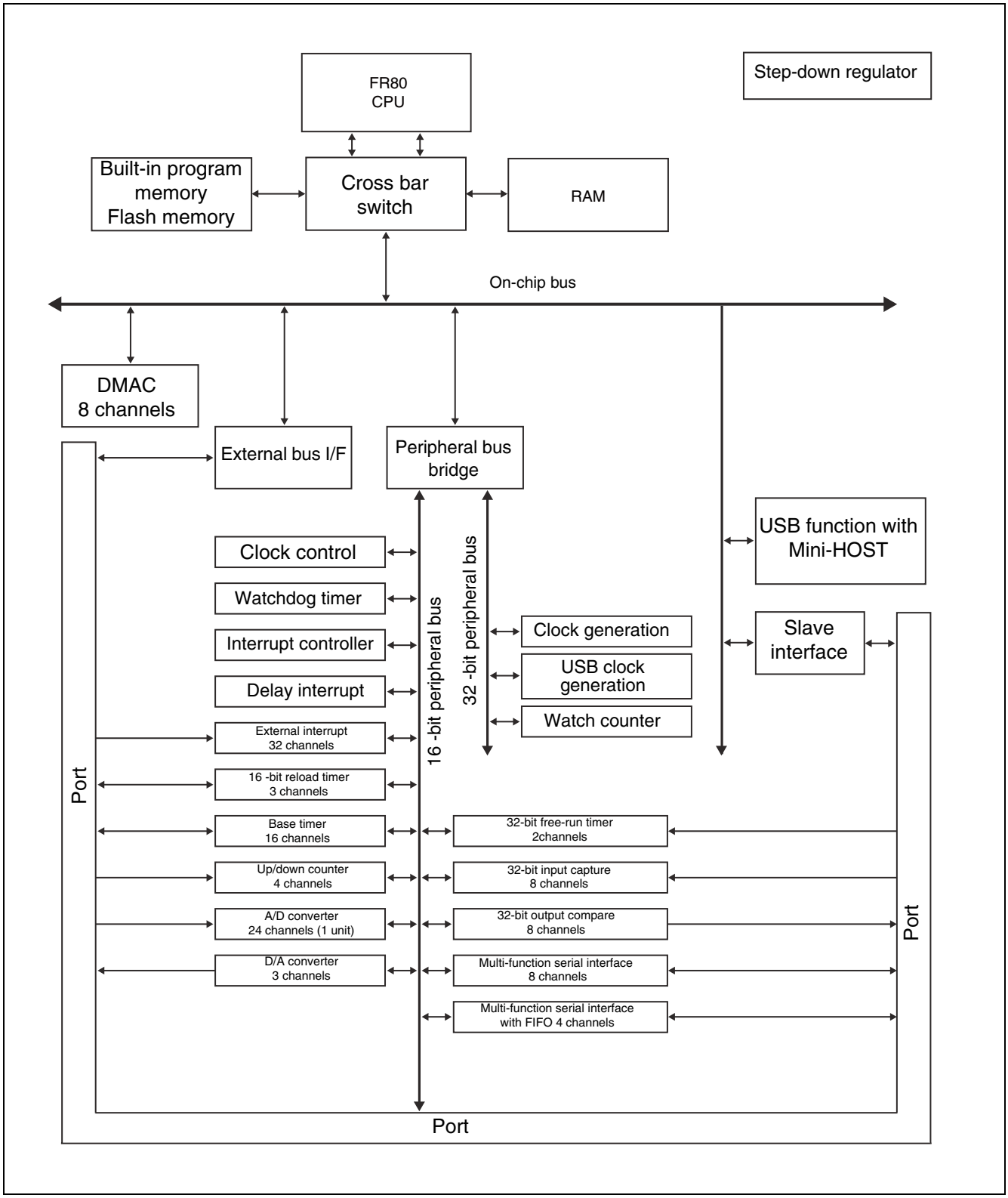
Connect the MD pin (MD0, MD1) directly to V_{CC} or V_{SS} pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and V_{CC} pins or V_{SS} pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

• Notes on power-on
  - To ensure that the internal regulator and the oscillator have stabilized immediately after the power is turned on, keep an "L" level input connected to the $\overline{INIT}$ pin for the duration of the regulator voltage stabilization wait time + the oscillator start time of the oscillator + the main oscillator stabilization wait time.
  - Turn power on/off in the following order
    Turning on : $V_{CC} \rightarrow AV_{CC} \rightarrow AVRH$
    Turning off : $AVRH \rightarrow AV_{CC} \rightarrow V_{CC}$
  - Release the reset ($\overline{INIT}$ pin "L" level to "H" level) after the power supply has stabilized.

• Caution on operations during PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency.
However, Fujitsu will not guarantee results of operations if such failure occurs.

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory Space

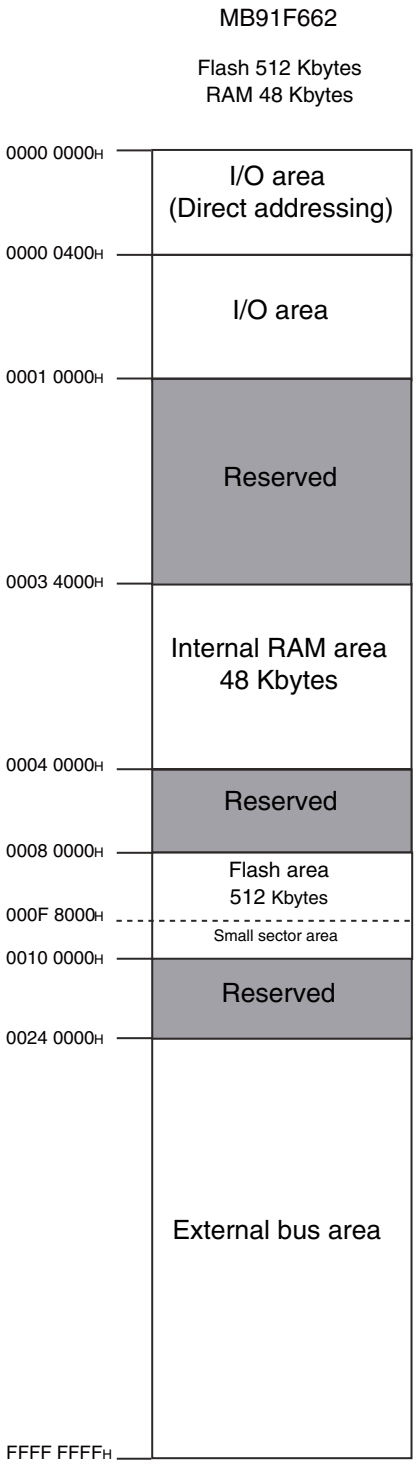
The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

• Direct Addressing Areas

The following areas in the address space are used as I/O areas.
These areas are called direct addressing areas, and the address of an operand in these areas can be specified directly within an instruction. The size of the directly addressable area depends on the length of the data being accessed as follows.

- Byte data access : 0000 0000$_H$ to 0000 00FF$_H$
- Half word data access : 0000 0000$_H$ to 0000 01FF$_H$
- Word data access : 0000 0000$_H$ to 0000 03FF$_H$

2. Memory Map



Notes :
- Small sector area is related to flash products only. Please refer to the Flash Memory section of the Hardware Manual for more details.
- Do not access the reserved areas.

■ I/O MAP

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port data register
0000 003CH	WDTCR0 [R/W] B, H, W 00000000	WDTCPR0 [R/W] B, H, W 00000000	—		Watchdog timer
0000 0040H	EIRR0 [R/W] B, H, W 000 0000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt 0 to 7

Internal value after reset
"1" : Internal value"1"
"0" : Internal value"0"
"X" : Internal value undefined
" - " : Reserved bit or undefined bit

— : Reserved area

Access unit
(B : byte, H : half word, W : word)

Read/write attribute

Register name (column 1 of the register is at address 4n, column 2 is at address 4 n + 2...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

Notes : • When performing a data access, the addresses should be as below.
- Word access : Address should be multiples of 4 (least significant 2 bits should be "00B")
- Half word access : Address should be multiples of 2 (least significant bit should be "0")
- Byte access : —

• Do not access the reserved areas.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000H	PDR0 [R/W] B,H XXXXXXXX	PDR1 [R/W] B,H XXXXXXXX	PDR2 [R/W] B,H XXXXXXXX	PDR3 [R/W] B,H XXXXXXXX	Port data register
0000 0004H	PDR4 [R/W] B,H XXXXXXXX	PDR5 [R/W] B,H XXXXXXXX	PDR6 [R/W] B,H XXXXXXXX	PDR7[R/W] B,H XXXXXXXX	
0000 0008H	PDR8 [R/W] B,H XXXXXXXX	PDR9 [R/W] B,H -- - - - XXX	PDRA [R/W] B XXXXXXXX	—	
0000 000CH	—				
0000 0010H	PDRG [R/W] B,H XXXXXXXX	PDRH [R/W] B,H ----XXXX	—		
0000 0014H	PDRK [R/W] B ----XXXX	—			
0000 0018H to 0000 001CH	—				
0000 0020H to 0000 0038H	—				Reserved
0000 003CH	WDTCR0[R/W] B,H - 0- - 0000	WDTCPR0[R/W] B,H 00000000	—		Watchdog timer
0000 0040H	EIRR0[R/W] B,H,W - - - - - - - 0	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt 0 to 7
0000 0044H	DICR [R/W] B 11111110	—			Delay interrupt
0000 0048H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.0
0000 004CH	—		TMCSR0 [R/W] H - - 000000 - - 000000		
0000 0050H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.1
0000 0054H	—		TMCSR1 [R/W] H - - 000000 - - 000000		
0000 0058H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.2
0000 005CH	—		TMCSR2 [R/W] H - - 000000 - - 000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0060H	SCR0 [R/W] B,H,W*2 0 - - 00000	SMR0 [R/W] B,H,W 000 - 0000	SSR0 [R,R/W] B,H,W 0 - 000011	ESCR0 [R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.0
0000 0064H	RDR0[R]/TDR0[W] B,H,W*1 - - - - - - - 0 00000000		BGR10[R/W]H,W 00000000	BGR00[R/W] H,W 00000000	
0000 0068H	SCR1[R/W] IBCR1[R,R/W] B,H,W*2 0 - - 00000	SMR1 [R/W] B,H,W 000 - 0000	SSR1 [R,R/W] B,H,W 0 - 000011	ESCR1[R/W] IBSR1[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.1
0000 006CH	RDR1[R]/TDR1[W] B,H,W*1 - - - - - - - 0 00000000		BGR11[R/W] H,W 00000000	BGR01[R/W] H,W 00000000	
0000 0070H	ISMK1 [R/W] B,H*2 - - - - - - - -	ISBA1 [R/W] B,H*2 - - - - - - - -	—		
0000 0074H	SCR2[R/W] IBCR2[R,R/W] B,H,W*2 0 - - 00000	SMR2 [R/W] B,H,W 000 - 0000	SSR2 [R,R/W] B,H,W 0 - 000011	ESCR2[R/W] IBSR2 [R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.2
0000 0078H	RDR2[R]/TDR2[W] B,H,W*1 - - - - - - - 0 00000000		BGR12[R/W] H,W 00000000	BGR02[R/W] H,W 00000000	
0000 007CH	ISMK2 [R/W] B,H*2 - - - - - - - -	ISBA2 [R/W] B,H*2 - - - - - - - -	—		
0000 0080H	SCR3[R/W] IBCR3[R,R/W] B,H,W*2 0 - - 00000	SMR3 [R/W] B,H,W 000 - 0000	SSR3 [R,R/W] B,H,W 0 - 000011	ESCR3[R/W] IBSR3[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.3
0000 0084H	RDR3[R]/TDR3[W] B,H,W*1 - - - - - - - 0 00000000		BGR13[R/W] H,W 00000000	BGR03[R/W] H,W 00000000	
0000 0088H	ISMK3 [R/W] B,H*2 - - - - - - - -	ISBA3 [R/W] B,H*2 - - - - - - - -	—		
0000 008CH	SCR4[R/W] IBCR4[R,R/W] B,H,W*2 0 - - 00000	SMR4 [R/W] B,H,W 000 - 0000	SSR4 [R,R/W] B,H,W 0 - 000011	ESCR4[R/W] IBSR4[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.4
0000 0090H	RDR4[R]/TDR4[W] B,H,W*1 - - - - - - - 0 00000000		BGR14[R/W] H,W 00000000	BGR04[R/W] H,W 00000000	
0000 0094H	ISMK4 [R/W] B,H*2 - - - - - - - -	ISBA4 [R/W] B,H*2 - - - - - - - -	—		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0098H	SCR5[R/W] IBCR5[R,R/W] B,H,W*2 0 - - 00000	SMR5 [R/W] B,H,W 000 - 0000	SSR5 [R,R/W] B,H,W 0- 000011	ESCR5[R/W] IBSR5[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.5
0000 009CH	RDR5[R]/TDR5[W] B,H,W*1 - - - - - - - 0 00000000		BGR15 [R/W] H,W 00000000	BGR05 [R/W] H,W 00000000	
0000 00A0H	ISMK5 [R/W] B,H*2 - - - - - - - -	ISBA5 [R/W] B,H*2 - - - - - - - -	—		
0000 00A4H	SCR6[R/W] IBCR6[R,R/W] B,H,W*2 0 - - 00000	SMR6 [R/W] B,H,W 000 - 0000	SSR6 [R,R/W] B,H,W 0 - 000011	ESCR6[R/W] IBSR6[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.6
0000 00A8H	RDR6[R]/TDR6[W] B,H,W*1 - - - - - - - 0 00000000		BGR16 [R/W] H,W 00000000	BGR06 [R/W] H,W 00000000	
0000 00ACH	ISMK6 [R/W] B,H*2 - - - - - - - -	ISBA6 [R/W] B,H*2 - - - - - - - -	—		
0000 00B0H	SCR7 [R/W] IBCR7[R,R/W] B,H,W*2 0 - - 00000	SMR7 [R/W] B,H,W 000 - 0000	SSR7 [R,R/W] B,H,W 0 - 000011	ESCR7 [R/W] IBSR7 [R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.7
0000 00B4H	RDR7[R]/TDR7[W] B,H,W*1 - - - - - - - 0 00000000		BGR17 [R/W] H,W 00000000	BGR07 [R/W] H,W 00000000	
0000 00B8H	ISMK7 [R/W] B,H*2 - - - - - - - -	ISBA7 [R/W] B,H*2 - - - - - - - -	—		
0000 00BCH	—				Reserved
0000 00C0H	RDRM0 [R]/ TDRM0[W] B,H,W 00000000	RDRM1 [R]/ TDRM1[W] B,H,W 00000000	RDRM2 [R]/ TDRM2[W] B,H,W 00000000	RDRM3 [R]/ TDRM3[W] B,H,W 00000000	Multi-function serial interface data register (mirror)
0000 00C4H	RDRM4 [R]/ TDRM4[W] B,H,W 00000000	RDRM5 [R]/ TDRM5[W] B,H,W 00000000	RDRM6 [R]/ TDRM6[W] B,H,W 00000000	RDRM7 [R]/ TDRM7[W] B,H,W 00000000	
0000 00C8H	SSEL0123 [R/W] B - - - - - - 00	—	SSEL4567 [R/W] B - - - - - - 00	—	Multi-function serial interface serial clock selection
0000 00CCH	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 00D0H	SCR8 [R/W] IBCR8 [R,R/W] B,H,W*2 0 - - 00000	SMR8 [R/W] B,H,W 000 - 0000	SSR8 [R,R/W] B,H,W 0 - 000011	ESCR8 [R/W] IBSR8 [R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch. 8 (FIFO)
0000 00D4H	RDR8[R]/TDR8[W] B,H,W*1 - - - - - - - 0 00000000		BGR18 [R/W] H,W 00000000	BGR08 [R,R/W] H,W 00000000	
0000 00D8H	ISMK8 [R/W] B,H*2 - - - - - - - -	ISBA8 [R/W] B,H*2 - - - - - - - -	—		
0000 00DCH	FCR18 [R/W] B,H,W - - - 00100	FCR08 [R,R/W] B,H,W 00000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	
0000 00E0H	SCR9 [R/W] IBCR9 [R,R/W] B,H,W*2 0- - 00000	SMR9 [R/W] B,H,W 000 - 0000	SSR9 [R,R/W] B,H,W 0 - 000011	ESCR9 [R/W] IBSR9[R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch. 9 (FIFO)
0000 00E4H	RDR9[R]/TDR9[W] B,H,W*1 - - - - - - - 0 00000000		BGR19 [R/W] H,W 00000000	BGR09 [R/W] H,W 00000000	
0000 00E8H	ISMK9 [R/W] B,H*2 - - - - - - - -	ISBA9 [R/W] B,H*2 - - - - - - - -	—		
0000 00ECH	FCR19 [R/W] B,H,W - - - 00100	FCR09 [R,R/W] B,H,W 00000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	
0000 00F0H	SCR10 [R/W] IBCR10 [R,R/W] B,H,W*2 0- - 00000	SMR10 [R/W] B,H,W 000- 0000	SSR10 [R,R/W] B,H,W 0- 000011	ESCR10 [R/W] IBSR10 [R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.10 (FIFO)
0000 00F4H	RDR10[R]/TDR10[W] B,H,W*1 - - - - - - - 0 00000000		BGR110 [R/W] H,W 00000000	BGR010 [R/W] H,W 00000000	
0000 00F8H	ISMK10 [R/W] B,H*2 - - - - - - - -	ISBA10 [R/W] B,H*2 - - - - - - - -	—		
0000 00FCH	FCR110 [R/W] B,H,W - - - 00100	FCR010 [R,R/W] B,H,W 00000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0100H	SCR11 [R/W] IBCR11 [R,R/W] B,H,W*2 0- - 00000	SMR11 [R/W] B,H,W 000- 0000	SSR11 [R,R/W] B,H,W 0- 000011	ESCR11 [R/W] IBSR11 [R,R/W] B,H,W*2 - 0000000	Multi-function serial interface ch.11 (FIFO)
0000 0104H	RDR11[R]/TDR11[W] B,H,W*1 - - - - - - - 0 00000000		BGR111 [R/W] H,W 00000000	BGR011 [R/W] H,W 00000000	
0000 0108H	ISMK11 [R/W] B,H*2 - - - - - - - -	ISBA11 [R/W] B,H*2 - - - - - - - -	—		
0000 010CH	FCR111 [R/W] B,H,W - - - 00100	FCR011 [R,R/W] B,H,W 00000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	
0000 0110H	EIRR1[R/W] B,H,W 00000000	ENIR1[R/W] B,H,W 00000000	ELVR1[R/W] B,H,W 00000000 00000000		External interrupt 8 to 15
0000 0114H	EIRR2[R/W] B,H,W 00000000	ENIR2[R/W] B,H,W 00000000	ELVR2[R/W] B,H,W 00000000 00000000		External interrupt 16 to 23
0000 0118H	EIRR3[R/W] B,H,W 00000000	ENIR3[R/W] B,H,W 00000000	ELVR3[R/W] B,H,W 00000000 00000000		External interrupt 24 to 31
0000 011CH	—				Reserved
0000 0120H	ADCR0[R/W] B,H 000- 0000	ADSR0[R,R/W] B,H 00- - - 000	—		A/D converter
0000 0124H	SCCR0[R,R/W] B,H 1000- 000	SFNS0[R/W] B,H - - - - 0000	SCFD0[R] B,H XXXXXXXX XX- XXXXX		
0000 0128H	—	SCIS20[R/W] B 00000000	SCIS10[R/W] B,H 00000000	SCIS00[R/W] B,H 00000000	
0000 012CH	PCCR0[R,R/W] B,H 1000- 000	PFNS0[R/W] B,H - - - - - - 00	PCFD0[R] B,H XXXXXXXX XXXXXXXX		
0000 0130H	PCIS0[R/W] B 00000000	—	CMPD0[R/W] B,H 00000000	CMPCR0[R/W] B,H 00000000	
0000 0134H	—	ADSS20[R/W] B 00000000	ADSS10[R/W] B,H 00000000	ADSS00[R/W] B,H 00000000	
0000 0138H	ADST00[R/W] B,H 00100000	ADST10[R/W] B,H 00100000	ADCT0[R/W] B - - - - - 111	—	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 013CH	—				Reserved
0000 0140H	BT0TMR[R]H 00000000 00000000		BT0TMCR[R/W] B,H -0000000 00000000		Base timer ch.0
0000 0144H	—	BT0STC[R/W]B 0000-000	—		
0000 0148H	BT0PCSR/BT0PRLL[R/W]H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 014CH	—				
0000 0150H	BT1TMR[R]H 00000000 00000000		BT1TMCR[R/W] B,H -0000000 00000000		Base timer ch.1
0000 0154H	—	BT1STC[R/W]B 0000-000	—		
0000 0158H	BT1PCSR/BT1PRLL[R/W]H XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 015CH	—				
0000 0160H	BT2TMR[R]H 00000000 00000000		BT2TMCR [R/W] B,H -0000000 00000000		Base timer ch.2
0000 0164H	—	BT2STC[R/W]B 0000-000	—		
0000 0168H	BT2PCSR/BT2PRLL[R/W]H XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH/BT2DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 016CH	—				
0000 0170H	BT3TMR[R]H 00000000 00000000		BT3TMCR[R/W] B,H -0000000 00000000		Base timer ch.3
0000 0174H	—	BT3STC[R/W]B 0000-000	—		
0000 0178H	BT3PCSR/BT3PRLL[R/W]H XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH/BT3DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 017CH	BTSEL0123 [R/W] B 00000000	—			
0000 0180H	DACR0[R/W] B,H,W - - - - - - - 0	DADR0[R/W] B,H,W XXXXXXXX	DACR1[R/W] B,H,W - - - - - - - 0	DADR1[R/W] B,H,W XXXXXXXX	D/A converter
0000 0184H	DACR2[R/W] B,H - - - - - - - 0	DADR2[R/W] B,H XXXXXXXX	—		
0000 0188H to 0000 018CH	—				

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0190H to 0000 01A8H	—				Reserved
0000 01ACH	ADCHE [R/W] B,H,W -------- 11111111 11111111 11111111				A/D channel enable
0000 01B0H	IRPR0H [R] B 000- - - - -	—	IRPR1H [R] B,H 000- 000-	IRPR1L [R] B,H 000- 000-	Interrupt request batch read function
0000 01B4H	IRPR2H [R] B,H,W 0000- - - -	IRPR2L [R] B,H,W 000- - - - -	IRPR3H [R] B,H,W 0000- - - -	IRPR3L [R] B,H,W 00000 - - -	
0000 01B8H	IRPR4H [R] B,H,W 0000- - - -	IRPR4L [R] B,H,W 000000- -	IRPR5H [R] B,H,W 0000- - - -	IRPR5L [R] B,H,W 0000- - - -	
0000 01BCH	IRPR6H [R] B,H,W 0000- - - -	IRPR6L [R] B,H,W 0000- - - -	IRPR7H [R] B,H,W 0000- 0- -	IRPR7L [R] B,H,W 0000- - - -	
0000 01C0H	RCRH0 [W] H,W 00000000	RCRL0 [W] B,H,W 00000000	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/down counter ch.0
0000 01C4H	CCR0 [R, R/W] B,H 00000000 -0001000		—	CSR0 [R,R/W] B 00000000	
0000 01C8H	—				
0000 01CCH	—				Reserved
0000 01D0H	RCRH1 [W] H,W 00000000	RCRL1 [W] B,H,W 00000000	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/down counter ch.1
0000 01D4H	CCR1 [R,R/W] B,H 00000000 -0001000		—	CSR1 [R,R/W] B 00000000	
0000 01D8H	—				
0000 01DCH	—				Reserved
0000 01E0H	RCRH2 [W] H,W 00000000	RCRL2 [W] B,H,W 00000000	UDCRH2 [R] H,W 00000000	UDCRL2 [R] B,H,W 00000000	Up/down counter ch.2
0000 01E4H	CCR2 [R, R/W] B,H 00000000 -0001000		—	CSR2 [R,R/W] B 00000000	
0000 01E8H	—				
0000 01ECH	—				Reserved

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 01F0H	RCRH3 [W] H,W 00000000	RCRL3 [W] B,H,W 00000000	UDCRH3 [R] H,W 00000000	UDCRL3 [R] B,H,W 00000000	Up/down counter ch.3
0000 01F4H	CCR3 [R,R/W] B,H 00000000 -0001000		—	CSR3 [R,R/W] B 00000000	
0000 01F8H	—				
0000 01FCH	—				Reserved
0000 0200H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.0
0000 0204H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
0000 0208H	TCCSH0 [R/W] B,H 0- - - - - 00	TCCSL0 [R/W] B,H - 1- 00000	—		
0000 020CH	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.0 to ch.3
0000 0210H	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0214H	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0218H	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 021CH	—	ICS01 [R/W] B 00000000	—	ICS23 [R/W] B 00000000	
0000 0220H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.4 to ch.7
0000 0224H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0228H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 022CH	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0230H	—	ICS45 [R/W] B 00000000	—	ICS67 [R/W] B 00000000	

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0234H	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.0 to ch.3
0000 0238H	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0000 023CH	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				
0000 0240H	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0000 0244H	OCSH1 [R/W] B,H,W - - - 0- - 00	OCSL0 [R/W] B,H,W 0000- - 00	OCSH3 [R/W] B,H,W - - - 0- - 00	OCSL2 [R/W] B,H,W 0000- - 00	
0000 0248H	OCCP4 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.4 to ch.7
0000 024CH	OCCP5 [R/W] W 00000000 00000000 00000000 00000000				
0000 0250H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				
0000 0254H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
0000 0258H	OCSH5 [R/W] B,H,W - - - 0- - 00	OCSL4 [R/W] B,H,W 0000- - 00	OCSH7 [R/W] B,H,W - - - 0- - 00	OCSL6 [R/W] B,H,W 0000- - 00	
0000 025CH	FRTSEL [R/W] B - - - - - - 00	—			Free-run timer selector
0000 0260H	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.1
0000 0264H	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
0000 0268H	TCCSH1 [R/W] B,H 0- - - - - 00	TCCSL1 [R/W] B,H - 1- 00000	—		
0000 026CH to 0000 031CH	—				Reserved
0000 0320H	FCTLR[R/W] H - 0- - 1011 - - - - - - - -		—	FSTR[R] B - - - - - - - 0	Flash memory control
0000 0324H to 0000 0334H	—				Reserved
0000 0338H	—		WREN[R/W] B,H 00000000 00000000		Wild register
0000 033CH	—				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0340H to 0000 037CH	—				Reserved
0000 0380H	WRAR00[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				Wild register
0000 0384H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0388H	WRAR01[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 038CH	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0390H	WRAR02[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 0394H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0398H	WRAR03[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 039CH	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A0H	WRAR04[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03A4H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A8H	WRAR05[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03ACH	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B0H	WRAR06[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03B4H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B8H	WRAR07[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03BCH	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C0H	WRAR08[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03C4H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 03C8H	WRAR09[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				Wild register
0000 03CCH	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D0H	WRAR10[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03D4H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D8H	WRAR11[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03DCH	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E0H	WRAR12[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03E4H	WRDR12[R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E8H	WRAR13[R/W] - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03ECH	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F0H	WRAR14[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03F4H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F8H	WRAR15[R/W] W - - - - - - - - - - XXXXXX XXXXXXXX XXXXXX- -				
0000 03FCH	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0400H	DDR0 [R/W] B,H 00000000	DDR1 [R/W] B,H 00000000	DDR2 [R/W] B,H 00000000	DDR3 [R/W] B,H 00000000	Data direction register
0000 0404H	DDR4 [R/W] B,H 00000000	DDR5 [R/W] B,H 00000000	DDR6 [R/W] B,H 00000000	DDR7[R/W] B,H 00000000	
0000 0408H	DDR8 [R/W] B,H 00000000	DDR9 [R/W] B,H - - - - - 000	DDRA [R/W] B 00000000	—	
0000 040CH	—				
0000 0410H	DDRG [R/W] B,H 00000000	DDRH [R/W] B,H - - - - 0000	—		
0000 0414H	DDRK [R/W] B - - - - 0000	—			

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0418H to 0000 041CH	—				Data direction register
0000 0420H	PCR0 [R/W] B,H 00000000	PCR1 [R/W] B,H 00000000	—		Pull-up control register
0000 0424H	—	PCR5 [R/W] B 00000000	PCR6 [R/W] B,H 00000000	PCR7[R/W] B,H 00000000	
0000 0428H	PCR8 [R/W] B,H 00000000	PCR9 [R/W] B,H - - - - - 000	PCRA [R/W] B 00000000	—	
0000 042CH to 0000 0430H	—				
0000 0434H	PCRK [R/W] B - - - - 00- -	—			
0000 0438H to 0000 043CH	—				
0000 0440H	ICR00 [R,R/W] B,H,W - - - 11111	ICR01 [R,R/W] B,H,W - - - 11111	ICR02 [R,R/W] B,H,W - - - 11111	ICR03 [R,R/W] B,H,W - - - 11111	Interrupt control
0000 0444H	ICR04 [R,R/W] B,H,W - - - 11111	ICR05 [R,R/W] B,H,W - - - 11111	ICR06 [R,R/W] B,H,W - - - 11111	ICR07 [R,R/W] B,H,W - - - 11111	
0000 0448H	ICR08 [R,R/W] B,H,W - - - 11111	ICR09 [R,R/W] B,H,W - - - 11111	ICR10 [R,R/W] B,H,W - - - 11111	ICR11 [R,R/W] B,H,W - - - 11111	
0000 044CH	ICR12 [R,R/W] B,H,W - - - 11111	ICR13 [R,R/W] B,H,W - - - 11111	ICR14 [R,R/W] B,H,W - - - 11111	ICR15 [R,R/W] B,H,W - - - 11111	
0000 0450H	ICR16 [R,R/W] B,H,W - - - 11111	ICR17 [R,R/W] B,H,W - - - 11111	ICR18 [R,R/W] B,H,W - - - 11111	ICR19 [R,R/W] B,H,W - - - 11111	
0000 0454H	ICR20 [R,R/W] B,H,W - - - 11111	ICR21 [R,R/W] B,H,W - - - 11111	ICR22 [R,R/W] B,H,W - - - 11111	ICR23 [R,R/W] B,H,W - - - 11111	
0000 0458H	ICR24 [R,R/W] B,H,W - - - 11111	ICR25 [R,R/W] B,H,W - - - 11111	ICR26 [R,R/W] B,H,W - - - 11111	ICR27 [R,R/W] B,H,W - - - 11111	
0000 045CH	ICR28 [R,R/W] B,H,W - - - 11111	ICR29 [R,R/W] B,H,W - - - 11111	ICR30 [R,R/W] B,H,W - - - 11111	ICR31 [R,R/W] B,H,W - - - 11111	

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0460H	ICR32 [R,R/W] B,H,W - - - 11111	ICR33 [R,R/W] B,H,W - - - 11111	ICR34 [R,R/W] B,H,W - - - 11111	ICR35 [R,R/W] B,H,W - - - 11111	Interrupt control
0000 0464H	ICR36 [R,R/W] B,H,W - - - 11111	ICR37 [R,R/W] B,H,W - - - 11111	ICR38 [R,R/W] B,H,W - - - 11111	ICR39 [R,R/W] B,H,W - - - 11111	
0000 0468H	ICR40 [R,R/W] B,H,W - - - 11111	ICR41 [R,R/W] B,H,W - - - 11111	ICR42 [R,R/W] B,H,W - - - 11111	ICR43 [R,R/W] B,H,W - - - 11111	
0000 046CH	ICR44 [R,R/W] B,H,W - - - 11111	ICR45 [R,R/W] B,H,W - - - 11111	ICR46 [R,R/W] B,H,W - - - 11111	ICR47 [R,R/W] B,H,W - - - 11111	
0000 0470H to 0000 047CH	—				Reserved
0000 0480H	RSTRR [R] B,H,W*3 11-X- - - X	RSTCR [R/W] B,H,W 00000000	STBCR [R/W] B,H,W 0000XX11	SLPRR [W] B,H,W 00000000	Reset control/ Power consumption control
0000 0484H	—				
0000 0488H	DIVR0 [R/W] B,H 000- - - - -	DIVR1 [R/W] B,H 0001- - - -	DIVR2 [R/W] B 0011- - - -	—	Clock division control
0000 048CH	—				
0000 0490H	IORR0 [R/W] B,H,W - 0000000	IORR1 [R/W] B,H,W - 0000000	IORR2 [R/W] B,H,W - 0000000	IORR3 [R/W] B,H,W - 0000000	Peripheral DMA transmission request control
0000 0494H	IORR4 [R/W] B,H,W - 0000000	IORR5 [R/W] B,H,W - 0000000	IORR6 [R/W] B,H,W - 0000000	IORR7 [R/W] B,H,W - 0000000	
0000 0498H to 0000 049CH	—				
0000 04A0H	PFR0 [R/W] B,H 00000000	PFR1 [R/W] B,H 00000000	PFR2 [R/W] B,H 00000000	PFR3 [R/W] B,H 00000000	Port function register
0000 04A4H	PFR4 [R/W] B,H 00000000	PFR5 [R/W] B,H 00000000	PFR6 [R/W] B,H 00- 00- 0-	PFR7[R/W] B,H 00000000	
0000 04A8H	PFR8 [R/W] B 00000000	—	PFRA [R/W] B 00- 00000	—	
0000 04ACH	—				
0000 04B0H	PFRG [R/W] B,H - 000- 000	PFRH [R/W] B,H - - - - - 0- 0	—		
0000 04B4H	—				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 04B8H	EPFR0 [R/W] B,H - - 000000	EPFR1 [R/W] B,H - - 000000	EPFR2 [R/W] B,H - - 000000	EPFR3 [R/W] B,H - - 000000	Extended port function register
0000 04BCH	EPFR4 [R/W] B,H 00000000	EPFR5 [R/W] B,H 00000000	EPFR6 [R/W] B,H 00000000	EPFR7 [R/W] B,H - - - 00000	
0000 04C0H	EPFR8 [R/W] B,H - - - 00000	EPFR9 [R/W] B,H - - - 00000	EPFR10 [R/W] B,H - - - 00000	EPFR11 [R/W] B,H - - - 00000	
0000 04C4H	EPFR12 [R/W] B,H - - - 00000	EPFR13 [R/W] B,H - - - 00000	EPFR14 [R/W] B,H - - - 00000	EPFR15 [R/W] B,H - - - 00000	
0000 04C8H	EPFR16 [R/W] B,H - - - 00000	EPFR17 [R/W] B,H - - - 00000	EPFR18 [R/W] B,H 00000000	EPFR19 [R/W] B,H - - - - 0001	
0000 04CCH	EPFR20 [R/W] B,H - - 000000	EPFR21 [R/W] B,H - - 000000	EPFR22 [R/W] B,H - - 000000	EPFR23 [R/W] B,H - - 000000	
0000 04D0H	EPFR24 [R/W] B,H - - 000000	EPFR25 [R/W] B,H - - 000000	EPFR26 [R/W] B,H - - 000000	EPFR27 [R/W] B,H - - 000000	
0000 04D4H	EPFR28 [R/W] B,H 00000000	EPFR29 [R/W] B,H 00000000	EPFR30 [R/W] B,H - - - - 0000	EPFR31 [R/W] B,H - 0000000	
0000 04D8H	EPFR32 [R/W] B,H 00000000	EPFR33 [R/W] B,H - - 000000	EPFR34 [R/W] B,H - 0000000	EPFR35 [R/W] B,H - - - - - - 00	
0000 04DCH	—				
0000 04E0H to 0000 04ECH	—				Reserved
0000 04F0H	ICSEL0[R/W] B,H,W - - - - - 000	ICSEL1[R/W] B,H,W - - - - - 000	ICSEL2[R/W] B,H,W - - - - - 000	ICSEL3[R/W] B,H,W - - - - - 000	DMA start request clear select function
0000 04F4H	ICSEL4[R/W] B,H,W - - - - - - 00	ICSEL5[R/W] B,H,W - - - - - 000	ICSEL6[R/W] B,H,W - - - - - - 00	ICSEL7[R/W] B,H,W - - - - - - - 0	
0000 04F8H	ICSEL8[R/W] B,H,W - - - - - - 00	ICSEL9[R/W] B,H,W - - - - - 000	ICSEL10[R/W] B,H,W - - - - 0000	ICSEL11[R/W] B,H,W - - - - 0000	
0000 04FCH	ICSEL12[R/W] B,H - - - 00000	ICSEL13[R/W] B,H - - - - 0000	ICSEL14[R/W] B,H - - - - - 000	—	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0500H to 0000 050CH	—				Reserved
0000 0510H	CSELR [R/W] B,H,W 001- - - 00	CMONR [R] B,H,W 001- - - 00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000- 111	Clock generation
0000 0514H	PLLCR [R/W] B,H - - 000000 11110000		CSTBR [R/W] B - 0000000	—	
0000 0518H	WCRD [R] B,H - - 000000	WCRL [R/W] B,H - - 000000	WCCR [R,R/W] B 00- - 0000	—	Clock counter
0000 051CH	UCCR [R/W] B - - - - - 001	—			USB clock generation
0000 0520H to 0000 05FCH	—				Reserved
0000 0600H	ASR0 [R/W] W 00000000 00000000 - - - - - - - - 1111- 001				External bus I/F
0000 0604H	ASR1 [R/W] W XXXXXXXX XXXXXXXX - - - - - - - - XXXX- XX0				
0000 0608H	ASR2 [R/W] W XXXXXXXX XXXXXXXX - - - - - - - - XXXX- XX0				
0000 060CH	ASR3 [R/W] W XXXXXXXX XXXXXXXX - - - - - - - - XXXX- XX0				
0000 0610H to 0000 063CH	—				
0000 0640H	ACR0[R/W] W - 00- - 00- 0				
0000 0644H	ACR1[R/W] W - XX- - XX- X				
0000 0648H	ACR2[R/W] W - XX- - XX- X				
0000 064CH	ACR3[R/W] W - XX- - XX- X				
0000 0650H to 0000 067CH	—				
0000 0680H	AWR0 [R/W] W - - - - 1111 00000000 11110000 00000- 0-				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0684H	AWR1 [R/W] W - - - - XXXX XXXXXXXX XXXXXXXX XXXXX- X-				External bus I/F
0000 0688H	AWR2 [R/W] W - - - - XXXX XXXXXXXX XXXXXXXX XXXXX- X-				
0000 068CH	AWR3 [R/W] W - - - - XXXX XXXXXXXX XXXXXXXX XXXXX- X-				
0000 0690H to 0000 06BCH	—				
0000 06C0H	DMAR0 [R/W] W - 0000				
0000 06C4H	DMAR1 [R/W] W - 0000				
0000 06C8H	DMAR2 [R/W] W - 0000				
0000 06CCH	DMAR3 [R/W] W - 0000				
0000 06D0H to 0000 06FCH	—				Reserved
0000 0700H to 0000 0BFCH	—				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0C00H	DCCR0 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				DMAC
0000 0C04H	DCSR0 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR0 [R/W] H 00000000 00000000		
0000 0C08H	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C0CH	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C10H	DCCR1 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C14H	DCSR1 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR1 [R/W] H 00000000 00000000		
0000 0C18H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C1CH	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C20H	DCCR2 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C24H	DCSR2 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR2 [R/W] H 00000000 00000000		
0000 0C28H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C2CH	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C30H	DCCR3 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C34H	DCSR3 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR3 [R/W] H 00000000 00000000		
0000 0C38H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C3CH	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C40H	DCCR4 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C44H	DCSR4 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR4 [R/W] H 00000000 00000000		
0000 0C48H	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C4CH	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0C50H	DCCR5 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				DMAC
0000 0C54H	DCSR5 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR5 [R/W] H 00000000 00000000		
0000 0C58H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C5CH	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C60H	DCCR6 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C64H	DCSR6 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR6 [R/W] H 00000000 00000000		
0000 0C68H	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C6CH	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C70H	DCCR7 [R/W] W 0- - - - 000 - - 00- - 00 00000000 0- 000000				
0000 0C74H	DCSR7 [R/W] H 0- - - - - - - - - - - - - - - 000		DTCR7 [R/W] H 00000000 00000000		
0000 0C78H	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C7CH	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C80H to 0000 0DF0H	—				
0000 0DF4H	—			DILVR [R,R/W] B - - - 11111	
0000 0DF8H	DMACR [R/W] W 0- - - - - - - - - - - - - - - - 0- - - - - - - - - - - - - - - -				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0DFCH to 0000 0F3CH	—				Reserved
0000 0F40H	BT4TMR[R]H 00000000 00000000		BT4TMCR[R/W] B,H -0000000 00000000		Base timer ch.4
0000 0F44H	—	BT4STC[R/W]B 0000-000	—		
0000 0F48H	BT4PCSR/BT4PRLL[R/W]H XXXXXXXX XXXXXXXX		BT4PDUT/BT4PRLH/BT4DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 0F4CH	—				
0000 0F50H	BT5TMR[R]H 00000000 00000000		BT5TMCR[R/W] B,H -0000000 00000000		Base timer ch.5
0000 0F54H	—	BT5STC[R/W]B 0000-000	—		
0000 0F58H	BT5PCSR/BT5PRLL[R/W]H XXXXXXXX XXXXXXXX		BT5PDUT/BT5PRLH/BT5DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 0F5CH	—				
0000 0F60H	BT6TMR[R]H 00000000 00000000		BT6TMCR[R/W] B,H -0000000 00000000		Base timer ch.6
0000 0F64H	—	BT6STC[R/W]B 0000-000	—		
0000 0F68H	BT6PCSR/BT6PRLL[R/W]H XXXXXXXX XXXXXXXX		BT6PDUT/BT6PRLH/BT6DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 0F6CH	—				
0000 0F70H	BT7TMR[R]H 00000000 00000000		BT7TMCR[R/W] B,H -0000000 00000000		Base timer ch.7
0000 0F74H	—	BT7STC[R/W]B 0000-000	—		
0000 0F78H	BT7PCSR/BT7PRLL[R/W]H XXXXXXXX XXXXXXXX		BT7PDUT/BT7PRLH/BT7DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 0F7CH	BTSEL4567 [R/W] B 00000000	—			
0000 0F80H	BT8TMR[R]H 00000000 00000000		BT8TMCR[R/W] B,H -0000000 00000000		Base timer ch.8
0000 0F84H	—	BT8STC[R/W]B 0000-000	—		
0000 0F88H	BT8PCSR/BT8PRLL[R/W]H XXXXXXXX XXXXXXXX		BT8PDUT/BT8PRLH/BT8DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 0F8CH	—				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0F90H	BT9TMR[R]H 00000000 00000000		BT9TMCR[R/W] B,H -0000000 00000000		Base timer ch.9
0000 0F94H	—	BT9STC[R/W]B 0000-000	—		
0000 0F98H	BT9PCSR/BT9PRLL[R/W]H XXXXXXXX XXXXXXXX		BT9PDUT/BT9PRLH/BT9DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 0F9CH	—				
0000 0FA0H	BTATMR[R]H 00000000 00000000		BTATMCR[R/W] B,H -0000000 00000000		Base timer ch.10
0000 0FA4H	—	BTASTC[R/W]B 0000-000	—		
0000 0FA8H	BTAPCSR/BTAPRLL [R/W]H XXXXXXXX XXXXXXXX		BTAPDUT/BTAPRLH/BTADTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FACH	—				
0000 0FB0H	BTBTMR[R]H 00000000 00000000		BTBTMCR[R/W] B,H -0000000 00000000		Base timer ch.11
0000 0FB4H	—	BTBSTC[R/W]B 0000-000	—		
0000 0FB8H	BTBPCSR/BTBPRLL [R/W]H XXXXXXXX XXXXXXXX		BTBPDUT/BTBPRLH/BTBDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FBCH	BTSEL89AB [R/W] B 00000000	—			
0000 0FC0H	BTCTMR[R]H 00000000 00000000		BTCTMCR[R/W] B,H -0000000 00000000		Base timer ch.12
0000 0FC4H	—	BTCSTC[R/W]B 0000-000	—		
0000 0FC8H	BTCPCSR/BTCPRLL[R/W]H XXXXXXXX XXXXXXXX		BTCPDUT/BTCPRLH/BTCDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FCCH	—				
0000 0FD0H	BTDTMR[R]H 00000000 00000000		BTDTMCR[R/W] B,H -0000000 00000000		Base timer ch.13
0000 0FD4H	—	BTDSTC[R/W]B 0000-000	—		
0000 0FD8H	BTDPCSR/BTDPRLL[R/W]H XXXXXXXX XXXXXXXX		BTDPDUT/BTDPRLH/BTDDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FDCH	—				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0FE0H	BTETMR[R]H 00000000 00000000		BTETMCR[R/W] B,H -0000000 00000000		Base timer ch.14
0000 0FE4H	—	BTESTC[R/W]B 0000-000	—		
0000 0FE8H	BTEPCSR/BTEPRLL[R/W]H XXXXXXXX XXXXXXXX		BTEPDUT/BTEPRLH/BTEDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FECH	—				
0000 0FF0H	BTFTMR[R]H 00000000 00000000		BTFTMCR[R/W] B,H -0000000 00000000		Base timer ch.15
0000 0FF4H	—	BTFSTC[R/W]B 0000-000	—		
0000 0FF8H	BTFPCSR/BTFPRLL[R/W]H XXXXXXXX XXXXXXXX		BTFPDUT/BTFPRLH/BTFDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FFCH	BTSELCDEF [R/W] B 00000000	—	BTSSSR [W] H XXXXXXXX XXXXXXXX		
0000 1000H to 0000 20FCH	—				Reserved
0000 2100H	HCNT1[R/W] B,H - - - - - 001	HCNT0[R/W] B,H 00000000	—		USB function with Mini- HOST
0000 2104H	HERR[R/W] B,H 00000011	HIRQ[R/W] B,H 0- 000000	—		
0000 2108H	HFCOMP[R/W] B,H 00000000	HSTATE[R,R/W] B,H - - 010010	—		
0000 210CH	HRTIMER1[R/W] B,H 00000000	HRTIMER0[R/W] B,H 00000000	—		
0000 2110H	HADR[R/W] B,H - 0000000	HRTIMER2[R/W] B,H - - - - - - 00	—		
0000 2114H	HEOF1[R/W] B,H - - 000000	HEOF0[R/W] B,H 00000000	—		
0000 2118H	HFRAME1[R/W] B,H - - - - - 000	HFRAME0[R/W] B,H 00000000	—		
0000 211CH	—	HTOKEN[R/W] B 00000000	—		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 2120H	—	UDCC[R/W] B 1010- - 00	—		USB function with Mini- HOST
0000 2124H	EP0C[R/W] H - - - - - - 0- - 1000000		—		
0000 2128H	EP1C[R/W] H 01100001 00000000		—		
0000 212CH	EP2C[R/W] H 01100000 01000000		—		
0000 2130H	EP3C[R/W] H 01100000 01000000		—		
0000 2134H	EP4C[R/W] H 01100000 01000000		—		
0000 2138H	EP5C[R/W] H 01100000 01000000		—		
0000 213CH	TMSP[R] H - - - - - 000 00000000		—		
0000 2140H	UDCIE[R,R/W] B,H - - 000000	UDCS[R/W] B,H - - 000000	—		
0000 2144H	EP0IS[R,R/W] H 10- - - 1- - - - - - - - -		—		
0000 2148H	EP00S[R,R/W] H 100- - 00- - XXXXXXX		—		
0000 214CH	EP1S[R,R/W] H 100- 000X XXXXXXXX		—		
0000 2150H	EP2S[R,R/W] H 100- 000- - XXXXXXX		—		
0000 2154H	EP3S[R,R/W] H 100- 000- - XXXXXXX		—		
0000 2158H	EP4S[R,R/W] H 100- 000- - XXXXXXX		—		
0000 215CH	EP5S[R,R/W] H 100- 000- - XXXXXXX		—		
0000 2160H	EP0DTH [R/W] B,H XXXXXXXX	EP0DTL [R/W] B,H XXXXXXXX	—		
0000 2164H	EP1DTH [R/W] B,H XXXXXXXX	EP1DTL [R/W] B,H XXXXXXXX	—		
0000 2168H	EP2DTH [R/W] B,H XXXXXXXX	EP2DTL [R/W] B,H XXXXXXXX	—		
0000 216CH	EP3DTH [R/W] B,H XXXXXXXX	EP3DTL [R/W] B,H XXXXXXXX	—		
0000 2170H	EP4DTH [R/W] B,H XXXXXXXX	EP4DTL [R/W] B,H XXXXXXXX	—		

(Continued)

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 2174H	EP5DTH [R/W] B,H XXXXXXXX	EP5DTL [R/W] B,H XXXXXXXX	—		USB function with Mini- HOST
0000 2178H to 0000 217CH	—				
0000 2180H	SLIFRXDR [R] W 00000000 00000000 00000000 00000000				Slave interface
0000 2184H	SLIFTXDR [W] W 00000000 00000000 00000000 00000000				
0000 2188H	SLIFRXR[R] W 00000000 00000000 - - - - - - - - - - - - - - - -				
0000 218CH	SLIFTXR[W] W 00000000 00000000 - - - - - - - - - - - - - - - -				
0000 2190H	SLIFCR[W] W - 0 00000000				
0000 2194H	SLIFSR[R] W - 00000000				
0000 2198H	SLIFRXSR[R] W 00000000 00000000 00000000 00000000				
0000 219CH	SLIFTXSR[R] W 00000000 00000000 - - - - - - - - - - - - - - - -				
0000 21A0H	SLIFDRXR[R] W 00000000 00000000 00000000 00000000				
0000 21A4H	DREQSEL [R/W] B,H 00111011	USBSEL [R/W] B,H - - - - - - - 0	USBEN [R/W] B - - - - - - - 0	—	DREQ/DACK select circuit USB select circuit
0000 21A8H to 0000 FFFFH	—				Reserved

*1 : Byte access is available only when accessing the lower 8 bits within 9 bits.

*2 : The resistor of I²C can not be read immediate after reset.

*3 : Value just after reset by $\overline{\text{INIT}}$ pin.
Do not access the reserved areas.

■ VECTOR TABLE

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Reset	0	00	—	3FC$_H$	000F FFFC$_H$
System reserved	1	01	—	3F8$_H$	000F FFF8$_H$
System reserved	2	02	—	3F4$_H$	000F FFF4$_H$
System reserved	3	03	—	3F0$_H$	000F FFF0$_H$
System reserved	4	04	—	3EC$_H$	000F FFEC$_H$
System reserved	5	05	—	3E8$_H$	000F FFE8$_H$
System reserved	6	06	—	3E4$_H$	000F FFE4$_H$
System reserved	7	07	—	3E0$_H$	000F FFE0$_H$
System reserved	8	08	—	3DC$_H$	000F FFDC$_H$
INTE instruction	9	09	—	3D8$_H$	000F FFD8$_H$
System reserved	10	0A	—	3D4$_H$	000F FFD4$_H$
System reserved	11	0B	—	3D0$_H$	000F FFD0$_H$
Step trace trap	12	0C	—	3CC$_H$	000F FFCC$_H$
System reserved	13	0D	—	3C8$_H$	000F FFC8$_H$
Undefined instruction exception	14	0E	—	3C4$_H$	000F FFC4$_H$
—	15	0F	15(F$_H$) fixed	3C0$_H$	000F FFC0$_H$
External interrupt request ch.0 to ch.7	16	10	ICR00	3BC$_H$	000F FFBC$_H$
External interrupt request ch.8 to ch.15	17	11	ICR01	3B8$_H$	000F FFB8$_H$
External interrupt request ch.16 to ch.23	18	12	ICR02	3B4$_H$	000F FFB4$_H$
External interrupt request ch.24 to ch.31	19	13	ICR03	3B0$_H$	000F FFB0$_H$
16-bit reload timer ch.0 to ch.2	20	14	ICR04	3AC$_H$	000F FFAC$_H$
Reception interrupt request of UART/CSIO ch.0	21	15	ICR05	3A8$_H$	000F FFA8$_H$
Transmission interrupt request of UART/CSIO ch.0 Transmission bus idle interrupt request of UART/CSIO ch.0	22	16	ICR06	3A4$_H$	000F FFA4$_H$
Reception interrupt request of UART/CSIO/ I^{2}C ch.1	23	17	ICR07	3A0$_H$	000F FFA0$_H$
Transmission interrupt request of UART/CSIO/ I^{2}C ch.1 Transmission bus idle interrupt request of UART/CSIO ch.1	24	18	ICR08	39C$_H$	000F FF9C$_H$
Status interrupt request of I^{2}C ch.1	25	19	ICR09	398$_H$	000F FF98$_H$
Reception interrupt request of UART/CSIO/I^{2}C ch.2	26	1A	ICR10	394$_H$	000F FF94$_H$
Transmission interrupt request of UART/CSIO/I^{2}C ch.2 Transmission bus idle interrupt request of UART/CSIO ch.2	27	1B	ICR11	390$_H$	000F FF90$_H$

(Continued)

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Status interrupt request of I²C ch.2	28	1C	ICR12	38C$_H$	000F FF8C$_H$
Reception interrupt request of UART/CSIO/I²C ch.3	29	1D	ICR13	388$_H$	000F FF88$_H$
Transmission interrupt request of UART/CSIO/I²C ch.3. Transmission bus idle interrupt request of UART/CSIO ch.3. Status interrupt request of I²C ch.3	30	1E	ICR14	384$_H$	000F FF84$_H$
Reception interrupt request of UART/CSIO/I²C ch.4	31	1F	ICR15	380$_H$	000F FF80$_H$
Transmission interrupt request of UART/CSIO/I²C ch.4. Transmission bus idle interrupt request of UART/CSIO ch.4. Status interrupt request of I²C ch.4	32	20	ICR16	37C$_H$	000F FF7C$_H$
Reception interrupt request of UART/CSIO/I²C ch.5	33	21	ICR17	378$_H$	000F FF78$_H$
Transmission interrupt request of UART/CSIO/I²C ch.5. Transmission bus idle interrupt request of UART/CSIO ch.5. Status interrupt request of I²C ch.5	34	22	ICR18	374$_H$	000F FF74$_H$
Reception interrupt request of UART/CSIO/ I²C ch.6	35	23	ICR19	370$_H$	000F FF70$_H$
Transmission interrupt request of UART/CSIO/I²C ch.6. Transmission bus idle interrupt request of UART/CSIO ch.6. Status interrupt request of I²C ch.6	36	24	ICR20	36C$_H$	000F FF6C$_H$
Reception interrupt request of UART/CSIO/I²C ch.7 32-bit input capture ch.4 to ch.7	37	25	ICR21	368$_H$	000F FF68$_H$
Transmission interrupt request of UART/CSIO/I²C ch.7. Transmission bus idle interrupt request of UART/CSIO ch.7. Status interrupt request of I²C ch.7 32-bit output compare ch.4 to ch.7	38	26	ICR22	364$_H$	000F FF64$_H$
Reception interrupt request of UART/CSIO/I²C ch.8 to ch.11. Transmission interrupt request of UART/CSIO/I²C ch.8 to ch.11. Transmission bus idle interrupt request of UART/CSIO ch.8 to ch.11. Transmission FIFO interrupt request UART/CSIO/I²C ch.8 to ch.11 Status interrupt request of I²C ch.8 to ch.11	39	27	ICR23	360$_H$	000F FF60$_H$
16-bit up/down counter ch.0 to ch.3	40	28	ICR24	35C$_H$	000F FF5C$_H$
Main timer/Sub timer/Watch counter	41	29	ICR25	358$_H$	000F FF58$_H$
10-bit A/D converter • Scan conversion interrupt request • Priority conversion interrupt request • FIFO overrun interrupt request • Conversion result compare interrupt request	42	2A	ICR26	354$_H$	000F FF54$_H$
32-bit free-run timer ch.0, ch.1	43	2B	ICR27	350$_H$	000F FF50$_H$
32-bit input capture ch.0 to ch.3	44	2C	ICR28	34C$_H$	000F FF4C$_H$
32-bit output compare ch.0 to ch.3	45	2D	ICR29	348$_H$	000F FF48$_H$

(Continued)

(Continued)

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Base timer ch.0	46	2E	ICR30	344H	000F FF44H
Base timer ch.1	47	2F	ICR31	340H	000F FF40H
Base timer ch.2	48	30	ICR32	33CH	000F FF3CH
Base timer ch.3	49	31	ICR33	338H	000F FF38H
Base timer ch.4, ch.5	50	32	ICR34	334H	000F FF34H
Base timer ch.6, ch.7	51	33	ICR35	330H	000F FF30H
Base timer ch.8, ch.9	52	34	ICR36	32CH	000F FF2CH
Base timer ch.10, ch.11	53	35	ICR37	328H	000F FF28H
Base timer ch.12/USB function (DRQ of End Point 1 to 5)	54	36	ICR38	329H	000F FF24H
Base timer ch.13/USB function (DRQI of End Point 0, DRQO and each status/ USB Mini-HOST(each status)	55	37	ICR39	320H	000F FF20H
Base timer ch.14, ch.15/Slave interface	56	38	ICR40	31CH	000F FF1CH
DMA controller (DMAC) ch.0	57	39	ICR41	318H	000F FF18H
DMA controller (DMAC) ch.1	58	3A	ICR42	314H	000F FF14H
DMA controller (DMAC) ch.2	59	3B	ICR43	310H	000F FF10H
DMA controller (DMAC) ch.3	60	3C	ICR44	30CH	000F FF0CH
DMA controller (DMAC) ch.4 to ch.7	61	3D	ICR45	308H	000F FF08H
System reserved	62	3E	ICR46	304H	000F FF04H
Delay interrupt	63	3F	ICR47	300H	000F FF00H
System reserved (Used by REALOS)	64	40	—	2FCH	000F FEFCH
System reserved (Used by REALOS)	65	41	—	2F8H	000F FEF8H
Used by INT instruction	66 to 255	42 to FF	—	2F4H to 000H	000F FEF4H to 000F FC00H

* : USB interrupt source

Number		USB interrupt source	Details
Decimal	Hexadecimal		
54	36	USB function (DRQ of End Point 1 to 5)	DRQ (End Point1 to 5)
55	37	USB function (DRQI, DRQO of End Point 0 and each status)	DRQI, DRQO, SPK, SUSP, SOF, BRST, CONF, WKUP
		USB Mini-HOST (Each status)	DIRQ, URIRQ, RWKIRQ, CNNIRQ, SOFIRQ, CMPIRQ

■ PIN STATUS IN EACH CPU STATE

- When $\overline{\text{INIT}}$ = “L”

This is the period when the $\overline{\text{INIT}}$ pin is the “L” level.

- When $\overline{\text{INIT}}$ = “H”

The status immediately after the $\overline{\text{INIT}}$ pin changes from the “L” level to the “H” level.

- Input enabled

Indicates that the input function can be used.

- Input disabled

Indicates that the input function cannot be used.

- Output Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

- Maintain previous state

Maintains the state that was being output immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

- Internal input fixed at “0”

The input gate connected to the pin is disconnected from the external input and internally connected to “0”.

- Input enabled when interrupt function selected and enabled

Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

• List of pin status

Pin name	Function	During initialization		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
$\overline{INIT}$	$\overline{INIT}$	—	—	Input enabled	Input enabled	Input enabled
X0	X0	Input enabled	Input enabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1	X1	Input enabled	Input enabled		"H" output or Input enabled	"H"output or Input enabled
X0A	X0A (When $\overline{INIT}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1A	X1A (When $\overline{INIT}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled		"H"output or Input enabled	"H"output or Input enabled
MD0	MD0	Input enabled	Input enabled		Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled			
P00	P00/D00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P01	P01/D01/TIOB0/SIN0_1/IN1					
P02	P02/D02/TIOA1/SCK0_1/IN2					
P03	P03/D03/TIOB1/IN3					
P04	P04/D04/TIOA2/SOUT1/IN4					
P05	P05/D05/TIOB2/SIN1/IN5					
P06	P06/D06/TIOA3/SCK1/IN6					
P07	P07/D07/TIOB3/IN7					

(Continued)

Pin name	Function	During initialization		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P10	P10/D08/TIOA4/SOUT2/AIN0/INT0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P11	P11/D09/TIOB4/SIN2/BIN0/INT1					
P12	P12/D10/TIOA5/SCK2/ZIN0/INT2					
P13	P13/D11/TIOB5/INT3					
P14	P14/D12/TIOA6/SOUT3/AIN1/INT4					
P15	P15/D13/TIOB6/SIN3/BIN1/INT5					
P16	P16/D14/TIOA7/SCK3/ZIN1/INT6					
P17	P17/D15/TIOB7/INT7					
P20	P20/A00/TIOA8/SOUT4/AIN2	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P21	P21/A01/TIOB8/SIN4/BIN2					
P22	P22/A02/TIOA9/SCK4/ZIN2					
P23	P23/A03/TIOB9					
P24	P24/A04/TIOA10/SOUT5/AIN3/ OUT0					
P25	P25/A05/TIOB10/SIN5/BIN3/OUT1					
P26	P26/A06/TIOA11/SCK5/ZIN3/ OUT2					
P27	P27/A07/TIOB11/OUT3					
P30	P30/A08/TIOA12/SOUT6/INT8/ SIFD6_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P31	P31/A09/TIOB12/SIN6/INT9/ SIFD7_1					
P32	P32/A10/TIOA13/SCK6/INT10/ SIFD8_1					
P33	P33/A11/TIOB13/INT11/SIFD9_1					
P34	P34/A12/TIOA14/SOUT7/OUT4/ INT12/SIFD10_1					
P35	P35/A13/TIOB14/SIN7/OUT5/ INT13/SIFD11_1					
P36	P36/A14/TIOA15/SCK7/OUT6/ INT14/SIFD12_1					
P37	P37/A15/TIOB15/OUT7/INT15/ SIFD13_1					

(Continued)

Pin name	Function	During initialization		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P40	P40/A16/SOUT8/SIFD14_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P41	P41/A17/SIN8/SIFD15_1					
P42	P42/A18/SCK8/$\overline{SIFCS\_1}$					
P43	P43/A19/SIFA_1					
P44	P44/A20/SOUT9/$\overline{SIFWR\_1}$					
P45	P45/A21/SIN9/$\overline{SIFRD\_1}$					
P46	P46/A22/SCK9/$\overline{SIFDRQR\_1}$					
P47	P47/A23/$\overline{SIFDRQT\_1}$					
P50	P50/$\overline{CS0}$/SOUT10/AIN0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P51	P51/$\overline{CS1}$/SIN10/BIN0_1					
P52	P52/$\overline{CS2}$/SCK10/ZIN0_1					
P53	P53/$\overline{CS3}$/FRCK1/INT21_2					Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P54	P54/$\overline{AS}$/SOUT11/AIN1_1					Output Hi-Z/ Internal input fixed at "0"
P55	P55/$\overline{RD}$/SIN11/BIN1_1/ADTRG0					
P56	P56/$\overline{WR0}$/SCK11/ZIN1_1/FRCK0					
P57	P57/$\overline{WR1}$					

(Continued)

Pin name	Function	During initialization		In sleep mode	In stop mode	
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"		HIZ = 0	HIZ = 1
P60	P60/RDY/AIN2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P61	P61/SYSCLK/BIN2_1					
P62	P62/DREQ0/ZIN2_1					
P63	P63/DACK0/FRCK1_1/INT22_2					Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P64	P64/DEOP0/AIN3_1					Output Hi-Z/ Internal input fixed at "0"
P65	P65/DREQ1/BIN3_1/ADTRG0_1					
P66	P66/DACK1/ZIN3_1/FRCK0_1					
P67	P67/DEOP1/INT23_2					Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled

(Continued)

Pin name	Function	During initialization		In sleep mode	In stop mode	
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"		HIZ = 0	HIZ = 1
P70	P70/AN0/OUT0_1/INT16	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P71	P71/AN1/OUT1_1/INT17					
P72	P72/AN2/TMO0/OUT2_1/ INT18/SIFD0					
P73	P73/AN3/TMO1/OUT3_1/ INT19/SIFD1					
P74	P74/AN4/TMO2/OUT4_1/ INT20/SIFD2					
P75	P75/AN5/SOUT0/TMI0/ OUT5_1/INT21/SIFD3					
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22/SIFD4					
P77	P77/AN7/SCK0/TMI2/OUT7_1/ INT23/SIFD5					
P80	P80/AN8/IN0_1/INT24/SIFD6	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P81	P81/AN9/IN1_1/INT25/SIFD7					
P82	P82/AN10/IN2_1/INT26/SIFD8					
P83	P83/AN11/IN3_1/INT27/SIFD9					
P84	P84/AN12/IN4_1/INT28/SIFD10					
P85	P85/AN13/IN5_1/INT29/SIFD11					
P86	P86/AN14/IN6_1/INT30/SIFD12					
P87	P87/AN15/IN7_1/INT31/SIFD13					
P90	P90/DA0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P91	P91/DA1					
P92	P92/DA2					
PA0	PA0/AN16/INT16_1/SIFD14	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
PA1	PA1/AN17/INT17_1/SIFD15					
PA2	PA2/AN18/TMO0_1/INT18_1/ $\overline{SIFCS}$					
PA3	PA3/AN19/TMO1_1/INT19_1/ $\overline{SIFA}$					
PA4	PA4/AN20/TMO2_1/INT20_1					
PA5	PA5/AN21/TMI0_1/INT21_1					
PA6	PA6/AN22/TMI1_1/INT22_1					
PA7	PA7/AN23/TMI2_1/INT23_1					

(Continued)

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Pin name	Function	During initialization		In sleep mode	In stop mode	
		$\overline{\text{INIT}}$ = "L"	$\overline{\text{INIT}}$ = "H"		HIZ = 0	HIZ = 1
PG0	PG0/DREQ2/TIOA0_1/SOUT0_2/IN0_2	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PG1	PG1/DACK2/TIOB0_1/SIN0_2/IN1_2					
PG2	PG2/DEOP2/TIOA1_1/SCK0_2/IN2_2					
PG3	PG3/DREQ3/TIOB1_1/IN3_2					
PG4	PG4/DACK3/TIOA2_1/SOUT1_1/IN4_2					
PG5	PG5/DEOP3/TIOB2_1/SIN1_1/IN5_2					
PG6	PG6/TIOA3_1/SCK1_1/IN6_2					
PG7	PG7/TIOB3_1/IN7_2					
PH0	PH0/TIOA4_1/SOUT2_1/AIN0_2/INT0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
PH1	PH1/TIOB4_1/SIN2_1/BIN0_2/INT1_1					
PH2	PH2/TIOA5_1/SCK2_1/ZIN0_2/INT2_1					
PH3	PH3/TIOB5_1/INT3_1					
PK0	PK0	Output Hi-Z	Output Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PK1	PK1					
PK2	PK2/ADTRG0_2		Output Hi-Z/ Input enabled			
PK3	PK3/ADTRG0_3					
UDP	UDP (USB)	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state/Input enabled	Maintain previous state	Maintain previous state
UDM	UDM (USB)					

• List of pin status (serial write mode)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"	
$\overline{INIT}$	$\overline{INIT}$	—	—	—
X0	X0	Input enabled	Input enabled	Input enabled
X1	X1	Input enabled	Input enabled	Input enabled
X0A	X0A (When $\overline{INIT}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
X1A	X1A (When INIT input, see PK0. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
MD0	MD0	Input enabled	Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled	Input enabled
P00	P00/D00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P01	P01/D01/TIOB0/SIN0_1/IN1			
P02	P02/D02/TIOA1/SCK0_1/IN2			
P03	P03/D03/TIOB1/IN3			
P04	P04/D04/TIOA2/SOUT1/IN4			
P05	P05/D05/TIOB2/SIN1/IN5			
P06	P06/D06/TIOA3/SCK1/IN6			
P07	P07/D07/TIOB3/IN7			
P10	P10/D08/TIOA4/SOUT2/AIN0/INT0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P11	P11/D09/TIOB4/SIN2/BIN0/INT1			
P12	P12/D10/TIOA5/SCK2/ZIN0/INT2			
P13	P13/D11/TIOB5/INT3			
P14	P14/D12/TIOA6/SOUT3/AIN1/INT4			
P15	P15/D13/TIOB6/SIN3/BIN1/INT5			
P16	P16/D14/TIOA7/SCK3/ZIN1/INT6			
P17	P17/D15/TIOB7/INT7			

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"	
P20	P20/A00/TIOA8/SOUT4/AIN2	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P21	P21/A01/TIOB8/SIN4/BIN2			
P22	P22/A02/TIOA9/SCK4/ZIN2			
P23	P23/A03/TIOB9			
P24	P24/A04/TIOA10/SOUT5/ AIN3/OUT0			
P25	P25/A05/TIOB10/SIN5/BIN3/ OUT1			
P26	P26/A06/TIOA11/SCK5/ZIN3/ OUT2			
P27	P27/A07/TIOB11/OUT3			
P30	P30/A08/TIOA12/SOUT6/ INT8	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P31	P31/A09/TIOB12/SIN6/INT9			
P32	P32/A10/TIOA13/SCK6/INT10			
P33	P33/A11/TIOB13/INT11			
P34	P34/A12/TIOA14/SOUT7/ OUT4/INT12			
P35	P35/A13/TIOB14/SIN7/OUT5/ INT13			
P36	P36/A14/TIOA15/SCK7/ OUT6/INT14			
P37	P37/A15/TIOB15/OUT7/INT15			
P40	P40/A16/SOUT8	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P41	P41/A17/SIN8			
P42	P42/A18/SCK8			
P43	P43/A19			
P44	P44/A20/SOUT9			
P45	P45/A21/SIN9			
P46	P46/A22/SCK9			
P47	P47/A23			

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"	
P50	P50/$\overline{CS0}$/SOUT10/AIN0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P51	P51/$\overline{CS1}$/SIN10/BIN0_1			
P52	P52/$\overline{CS2}$/SCK10/ZIN0_1			
P53	P53/$\overline{CS3}$/FRCK1/INT21_2			
P54	P54/$\overline{AS}$/SOUT11/AIN1_1			
P55	P55/$\overline{RD}$/SIN11/BIN1_1/ ADTRG0			
P56	P56/$\overline{WR0}$/SCK11/ZIN1_1/ FRCK0			
P57	P57/$\overline{WR1}$			
P60	P60/RDY/AIN2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P61	P61/SYSCLK/BIN2_1			
P62	P62/DREQ0/ZIN2_1			
P63	P63/DACK0/FRCK1_1/ INT22_2			
P64	P64/DEOP0/AIN3_1			
P65	P65/DREQ1/BIN3_1/ ADTRG0_1			
P66	P66/DACK1/ZIN3_1/ FRCK0_1			
P67	P67/DEOP1/INT23_2			
P70	P70/AN0/OUT0_1/INT16	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
P71	P71/AN1/OUT1_1/INT17			
P72	P72/AN2/TMO0/OUT2_1/ INT18			
P73	P73/AN3/TMO1/OUT3_1/ INT19			
P74	P74/AN4/TMO2/OUT4_1/ INT20			
P75	P75/AN5/SOUT0/TMI0/ OUT5_1/INT21	Output Hi-Z/ Input enabled	Output	Output
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P77	P77/AN7/SCK0/TMI2/ OUT7_1/INT23		Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{INIT}$ = "L"	$\overline{INIT}$ = "H"	
P80	P80/AN8/IN0_1/INT24	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
P81	P81/AN9/IN1_1/INT25			
P82	P82/AN10/IN2_1/INT26			
P83	P83/AN11/IN3_1/INT27			
P84	P84/AN12/IN4_1/INT28			
P85	P85/AN13/IN5_1/INT29			
P86	P86/AN14/IN6_1/INT30			
P87	P87/AN15/IN7_1/INT31			
P90	P90/DA0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P91	P91/DA1			
P92	P92/DA2			
PA0	PA0/AN16/INT16_1	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
PA1	PA1/AN17/INT17_1			
PA2	PA2/AN18/TMO0_1/INT18_1			
PA3	PA3/AN19/TMO1_1/INT19_1			
PA4	PA4/AN20/TMO2_1/INT20_1			
PA5	PA5/AN21/TMI0_1/INT21_1			
PA6	PA6/AN22/TMI1_1/INT22_1			
PA7	PA7/AN23/TMI2_1/INT23_1			
PG0	PG0/DREQ2/TIOA0_1/ SOUT0_2/IN0_2	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PG1	PG1/DACK2/TIOB0_1/ SIN0_2/IN1_2			
PG2	PG2/DEOP2/TIOA1_1/ SCK0_2/IN2_2			
PG3	PG3/DREQ3/TIOB1_1/IN3_2			
PG4	PG4/DACK3/TIOA2_1/ SOUT1_1/IN4_2			
PG5	PG5/DEOP3/TIOB2_1/ SIN1_1/IN5_2			
PG6	PG6/TIOA3_1/SCK1_1/IN6_2			
PG7	PG7/TIOB3_1/IN7_2			

(Continued)

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}}$ = “L”	$\overline{\text{INIT}}$ = “H”	
PH0	PH0/TIOA4_1/SOUT2_1/ AIN0_2/INT0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PH1	PH1/TIOB4_1/SIN2_1/ BIN0_2/INT1_1			
PH2	PH2/TIOA5_1/SCK2_1/ ZIN0_2/INT2_1			
PH3	PH3/TIOB5_1/INT3_1			
PK0	PK0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PK1	PK1			
PK2	PK2/ADTRG0_2			
PK3	PK3/ADTRG0_3			
UDP	UDP (USB)	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
UDM	UDM (USB)			

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	Vss – 0.3	Vss + 4.0	V	
Analog power supply voltage*1, *3	AV_{CC}	Vss – 0.3	Vss + 4.0	V	
Analog reference voltage*1, *3	AVRH	Vss – 0.3	Vss + 4.0	V	
Input voltage*1	V_I	Vss – 0.3	Vss + 4.0	V	
		Vss – 0.3	Vss + 6.0	V	5 V tolerant
		Vss – 0.5	Vss + 4.5	V	USB I/O
Analog pin input voltage*1	V_{IA}	Vss – 0.3	Vss + 4.0	V	
Output voltage*1	V_O	Vss – 0.3	Vcc + 0.3	V	
		Vss – 0.5	Vss + 4.5	V	USB I/O
“L” level maximum output current*4	I_{OL}	—	10	mA	
		—	43	mA	USB I/O
“L” level average output current*5	I_{OLAV}	—	4	mA	
		—	15	mA	USB I/O
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*6	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*4	I_{OH}	—	– 10	mA	
		—	– 43	mA	USB I/O
“H” level average output current*5	I_{OHAV}	—	– 4	mA	
		—	– 15	mA	USB I/O
“H” level total maximum output current*6	ΣI_{OH}	—	– 100	mA	
“H” level total average output current	ΣI_{OHAV}	—	– 50	mA	
Power consumption (Flash product)	P_D	—	500	mW	
Operating temperature	Ta	– 40	+ 85	°C	
Storage temperature	T_{STG}	– 55	+ 125	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : V_{CC} must not drop below $V_{SS} – 0.3$ V.

*3 : Be careful not to exceed $V_{CC} + 0.3$ V, for example, when the power is turned on.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output is the average current for a single pin over a period of 100 ms.

*6 : The total average output current is the average current for all pins over a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	3.6	V	Not using USB
		3.0	3.6	V	Using USB
Analog power supply voltage	AV_{CC}	2.7	3.6	V	Not using USB
		3.0	3.6	V	Using USB
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	Ta	− 40	+ 85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(1) DC Characteristics

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current (Flash product)	I_{CC}	V_{CC}	Normal operation	—	45	60	mA	CPU : 33 MHz, Peripheral : 33 MHz, Not using USB*1, *3
				—	55	75	mA	CPU : 32 MHz, Peripheral : 32 MHz, Using USB*1, *3
	I_{CCS}		SLEEP mode	—	15	25	mA	Peripheral : 33 MHz Not using USB*1, *3
				—	25	40	mA	Peripheral : 32 MHz Using USB*1, *3
	I_{CCL}		Sub operation	—	100	500	µA	CPU : 32 kHz Peripheral : 32 kHz *1, *2, *4
	I_{CCT}		Watch mode	—	70	400	µA	*1, *2, *4
	I_{CCH}		STOP mode	—	45	300	µA	*1, *2
"H" level input voltage	V_{IH}	P00 to P07*5, P10 to P17*6, P22 to P27*11, P30 to P37*11, P40 to P45*11, P60*7 P72 to P77*11, P80 to P87*11, PA0 to PA5*11	—	$V_{CC} \times 0.7$	—	Vcc + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07*5, P10 to P17*6, P22 to P27*11, P30 to P37*11, P40 to P45*11, P60*7 P72 to P77*11, P80 to P87*11, PA0 to PA5*11	—	V_{SS} − 0.3	—	$V_{CC} \times 0.3$	V	

(Continued)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	P00 to P07*8, P10 to P17*9, P50 to P57, P60*10, P61 to P67, P70, P71, P72 to P77*12, P80 to P87*12, P90 to P92, PA0 to PA5*12 PA6, PA7	—	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	
		P20, P21, P22 to P27*12, P30 to P37*12, P40 to P45*12, P46, P47, PG0 to PG7, PH0 to PH3	—	$V_{CC} \times 0.8$	—	$V_{SS} + 5.5$	V	5 V tolerant
"L"level input voltage (hysteresis input)	V_{ILS}	P00 to P07*8, P10 to P17*9, P20, P21, P22 to P27*12, P30 to P37*12, P40 to P45*12, P46, P47, P50 to P57, P60*10, P61 to P67, P70, P71, P72 to P77*12, P80 to P87*12, P90 to P92, PA0 to PA5*12, PA6, PA7, PG0 to PG7, PH0 to PH3	—	Vss − 0.3	—	$V_{CC} \times 0.2$	V	

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Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P92, PA0 to PA7, PG0 to PG7, PH0 to PH3, PK0 to PK3	V_{CC} = 3.0 V I_{OH} = − 4 mA	V_{CC} − 0.5	—	V_{CC}	V	
"L" level output voltage	V_{OL}		V_{CC} = 3.0 V I_{OL} = 4 mA	V_{SS}	—	0.4	V	
Input leak current	I_{IL}	—	—	− 5	—	+ 5	µA	Digital pin
				− 10	—	+ 10	µA	Analog pin
Pull-up resistance value	R_{PU}	Pull-up pin	—	16.6	33	66	kΩ	
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, AVRH	—	—	10	15	pF	

*1 : When opened, all ports are fixed to output

*2 : Ta = + 25 °C and V_{CC} = 3.3 V

*3 : X0 = 8.3 MHz, PLL = multiplied by 4 and X0A = when stopped

*4 : X0 = STOP and X0A = at 32 kHz

*5 : When using as D0 to D7 pin

*6 : When using as D8 to D15 pin

*7 : When using as RDY input

*8 : When using other than D0 to D7 pin

*9 : When using other than D8 to D15 pin

*10 : When using other than RDY input

*11 : When using as Slave interface pin

*12 : When using other than Slave interface pin

4. AC Characteristics

(1) Main Clock (MCLK) Input Standard

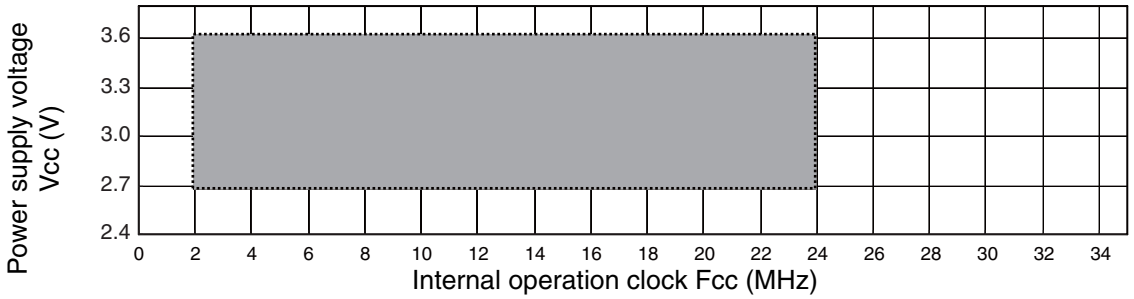
Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

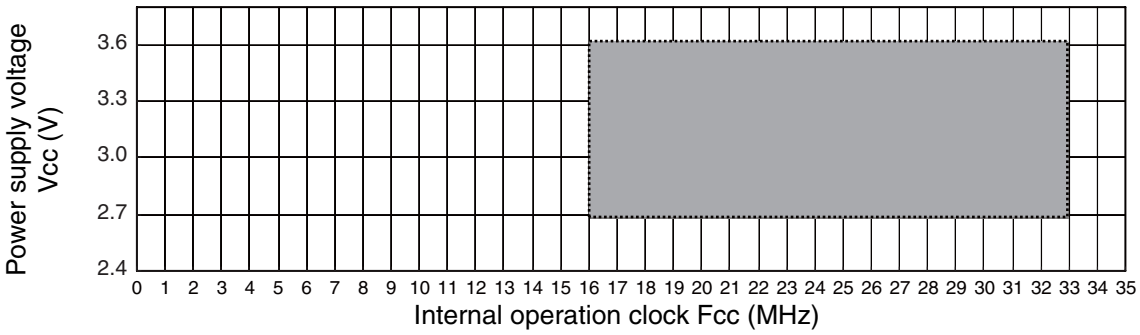
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	—	4	48	MHz	
			—	4	48	MHz	When using external clock
Input clock cycle	t_{CYLH}		—	20.83	250	ns	
Input clock pulse width	—		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	
Input clock rise time and fall time	t_{CF} t_{CR}		—	—	5	ns	When using external clock
Internal operating clock frequency	F_{CC}	—	—	—	33	MHz	CPU clock
	F_{CP}	—	—	—	33	MHz	Peripheral bus clock
	F_{CT}	—	—	—	33	MHz	External bus clock
Internal operating clock cycle time	t_{CYCC}	—	—	30	—	ns	CPU clock
	t_{CYCP}	—	—	30	—	ns	Peripheral bus clock
	t_{CYCT}	—	—	30	—	ns	External bus clock

• Operating guaranteed range

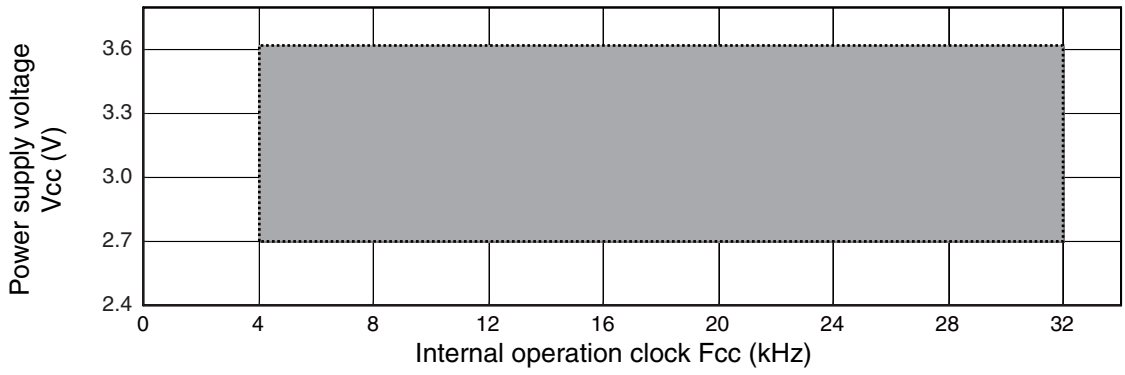
• When the main clock is selected (DIVB=000)



• When the PLL clock is selected (DIVB=000)



• When the sub clock is selected



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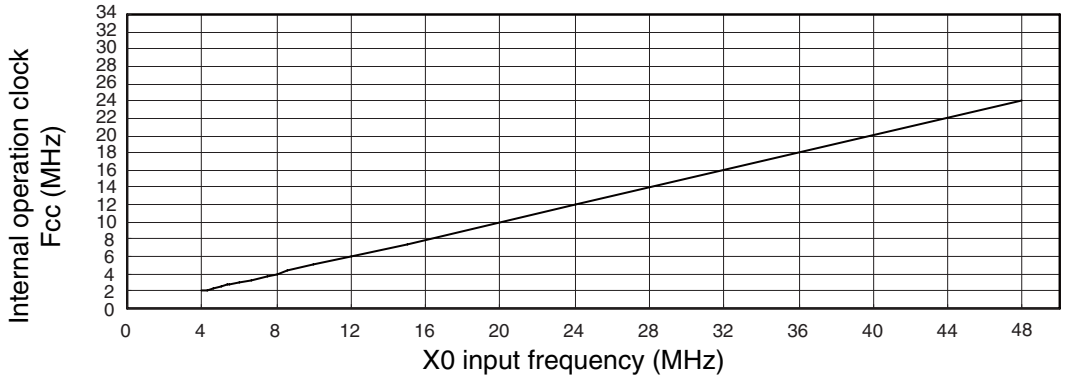
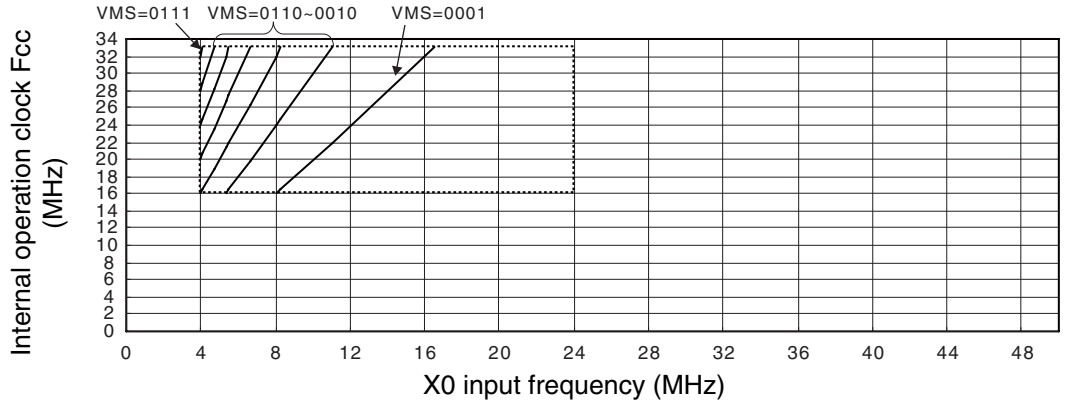
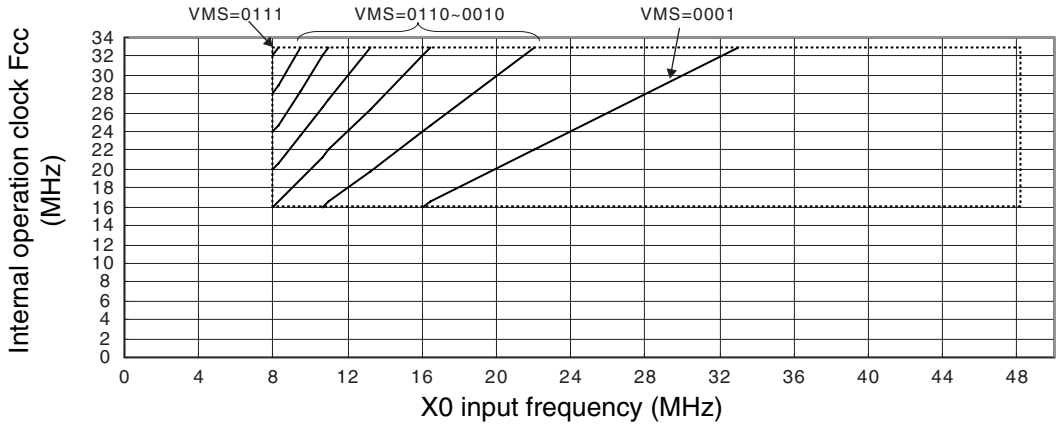
- When the main clock is selected (DIVB=000)



- When the PLL clock is selected (DIVB=000, ODS=00, PDS=0000)

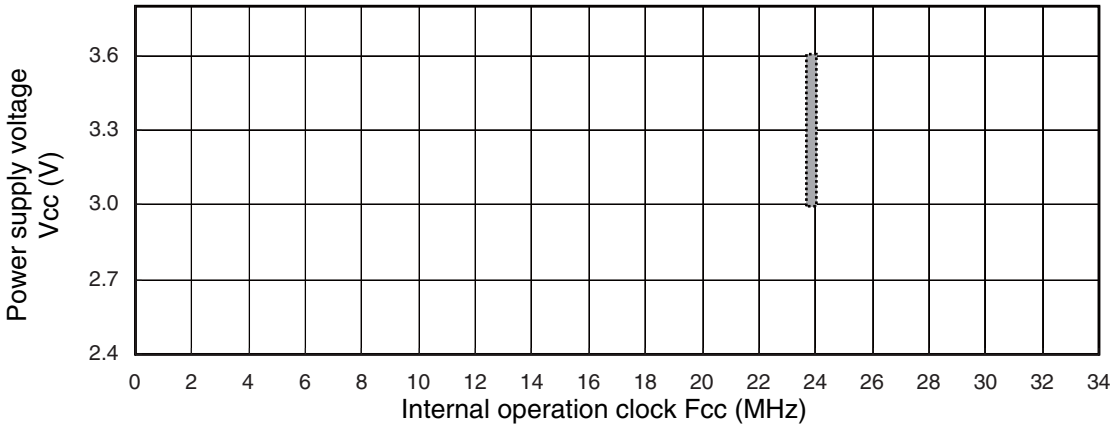


- When the PLL clock is selected (DIVB=000, ODS=00, PDS=0001)

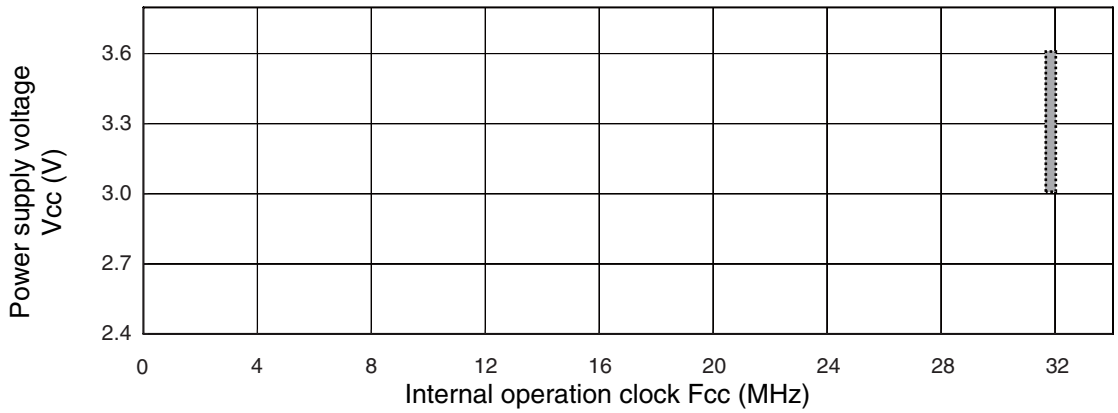


• Operating guaranteed range (at using USB)

• When the main clock is selected (DIVB=000)



• When the PLL clock is selected (DIVB=000, ODS=10, VMS=0111, PDS=0000, X0=4 MHz or DIVB=000, ODS=10, VMS=0001, PDS=0010, X0=48 MHz)



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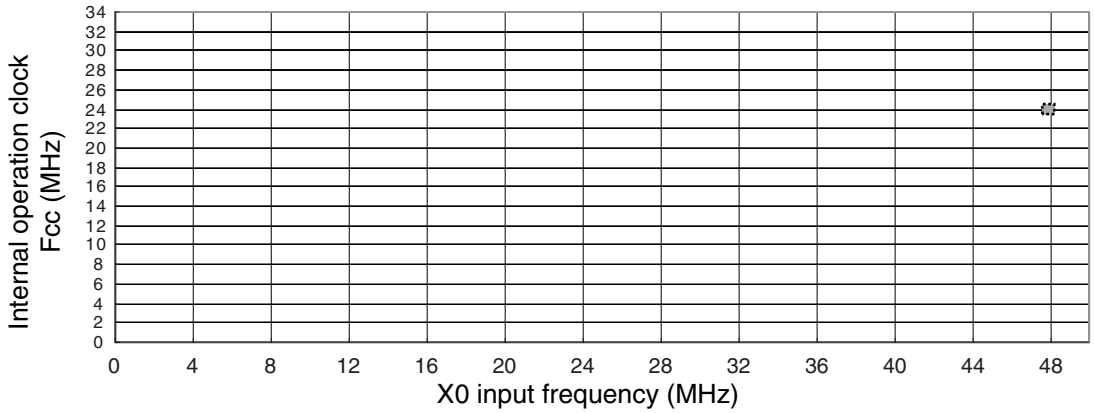
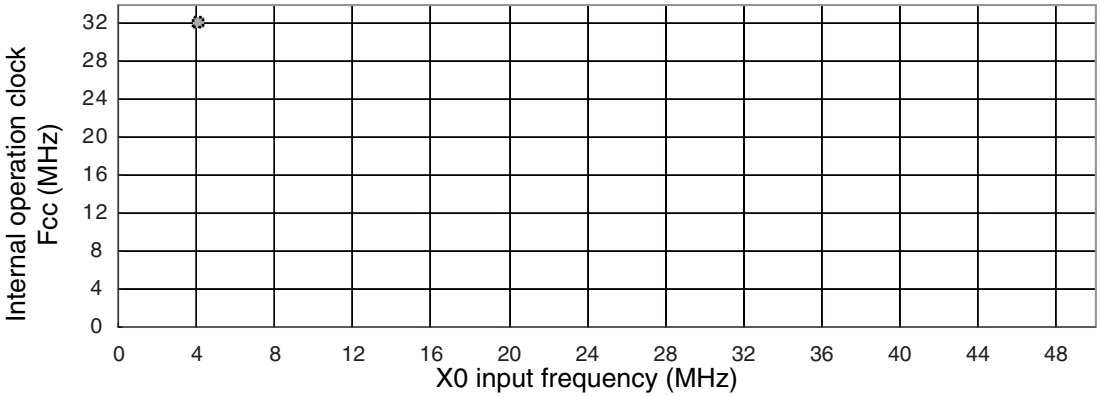
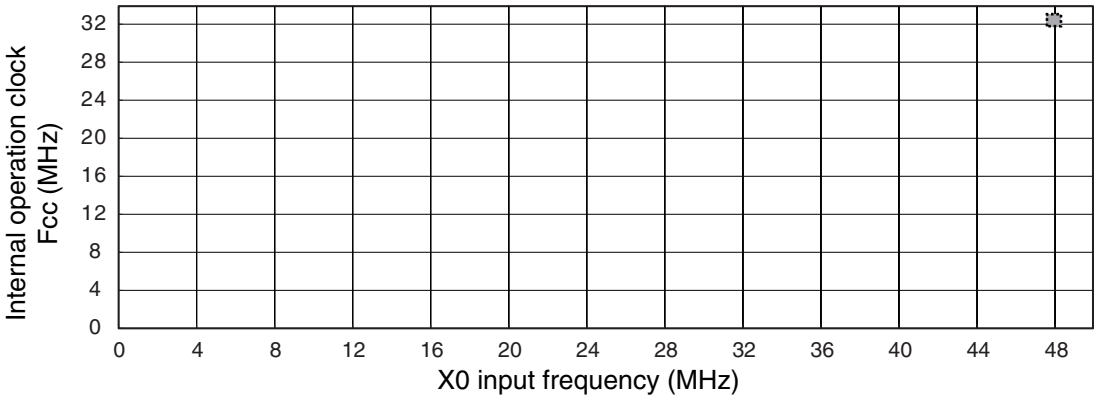
- When the main clock is selected (DIVB=000)



- When the PLL clock is selected (DIVB=000, ODS=10, VMS=0111, PDS=0000)



- When the PLL clock is selected (DIVB=000, ODS=10, VMS=0001, PDS=0010)

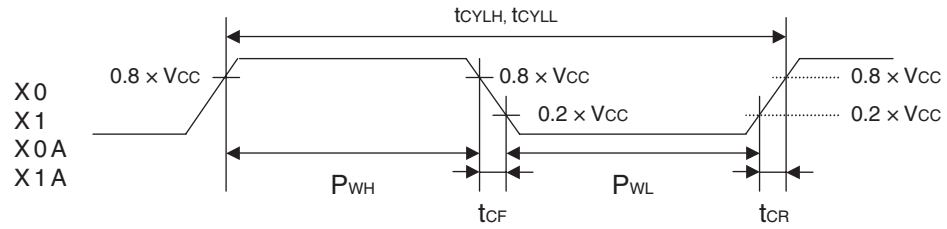


(2) Sub Clock (SBCLK) Input Standard

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	F_{CL}	X0A, X1A	—	—	32.768	—	kHz
Input clock cycle	t_{CYLL}		—	—	30.518	—	ms



(3) PLL Oscillation Stabilization Wait Time (LOCK UP Time)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	600	—	µs	Time from when the PLL starts operating until the oscillation stabilizes

(4) Regulator Voltage Stabilization Wait Time

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Regulator voltage stabilization wait time	t_{REG}	50	—	µs	Time taken for the regulator voltage to stabilize

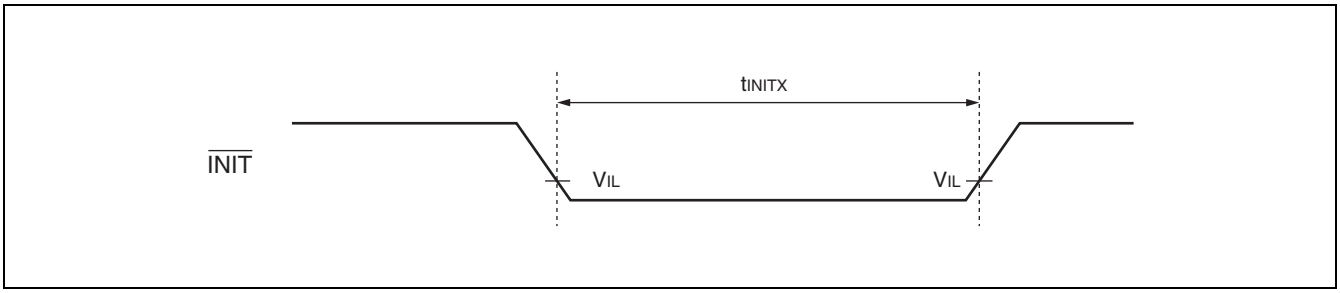
Note : This is the time from when the external power supply stabilizes (after reaching 3.0 V).

(5) Reset Input Standards

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time (At power-on, main oscillation stop mode)	t_{INITX}	$\overline{INIT}$	—	Oscillation time of oscillator + 10 t_{CYLH}	—	ns	*
Reset input time (At other times)				10 t_{CYLH}	—	ns	

* : After the supply voltage has stabilized, it takes a further 50 µs until the internal supply stabilizes. Hold the input to the $\overline{INIT}$ pin during that period.
- At power-on
- When in stop mode
- When in sub mode and sub watch mode when the main oscillation is stopped.



(6) Clock Output Timing

• t_{CHCL} : t_{CLCH} = 1 : 1 (divided by 1, 2, 4, 6, 8)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			t_{CYC} / 2 − 5	t_{CYC} / 2 + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			t_{CYC} / 2 − 5	t_{CYC} / 2 + 5	ns

Note : t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

• t_{CHCL} : t_{CLCH} = 1 : 2 (divided by 3)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			1 / 3 t_{CYC} − 5	1 / 3 t_{CYC} + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			2 / 3 t_{CYC} − 5	2 / 3 t_{CYC} + 5	ns

Note : t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

• t_{CHCL} : t_{CLCH} = 2 : 3 (divided by 5)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			2 / 5 t_{CYC} − 5	2 / 5 t_{CYC} + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			3 / 5 t_{CYC} − 5	3 / 5 t_{CYC} + 5	ns

Note : t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

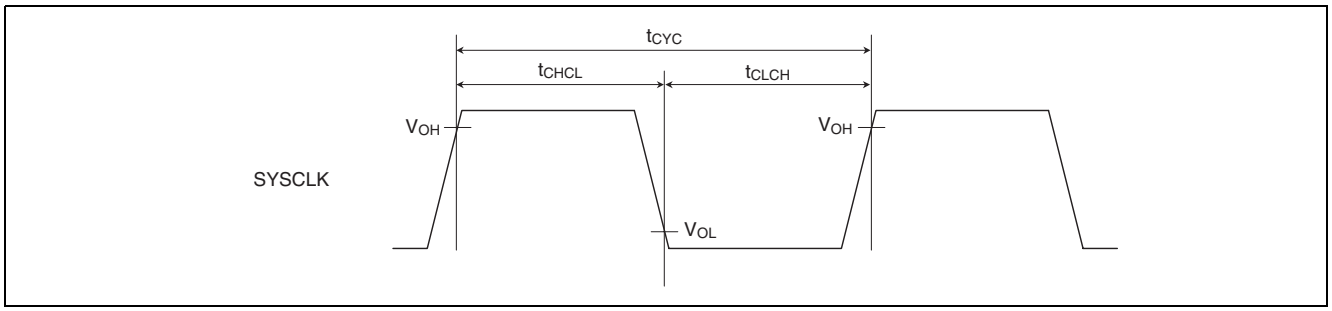
• t_{CHCL} : t_{CLCH} = 3 : 4 (divided by 7)

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	F_{CT} = F_{CC}, F_{CT} = F_{CC}/2	t_{CYCT}	—	ns
SYSCLK↑→SYSCLK↓	t_{CHCL}			3 / 7 t_{CYC} − 5	3 / 7 t_{CYC} + 5	ns
SYSCLK↓→SYSCLK↑	t_{CLCH}			4 / 7 t_{CYC} − 5	4 / 7 t_{CYC} + 5	ns

Note : t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.


tCYC
tCHCL
tCLCH
VOH
VOH
SYSCLK
VOL

(7) External Bus Access Read/Write Operation

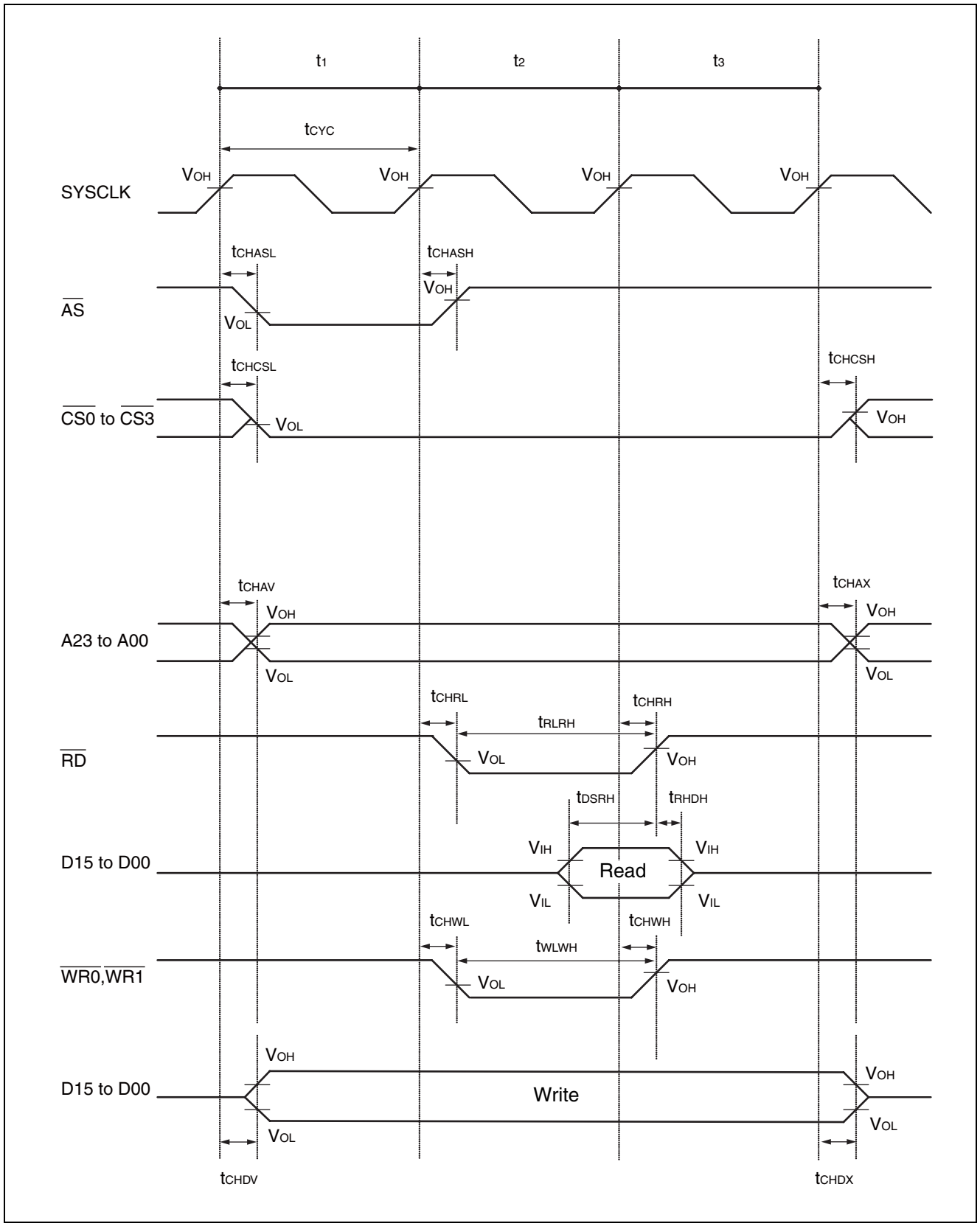
Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{AS}$ delay time	t_{CHASL}	SYSCLK $\overline{AS}$	—	0.6	10	ns	
	t_{CHASH}						
$\overline{CS0}$ to $\overline{CS3}$ delay time	t_{CHCSL}	SYSCLK $\overline{CS0}$ to $\overline{CS3}$		0.6	10	ns	
	t_{CHCSH}						
Address delay time	t_{CHAV}	SYSCLK A23 to A00		0.6	10	ns	
	t_{CHAX}						
$\overline{RD}$ delay time	t_{CHRL}	SYSCLK $\overline{RD}$		0.6	10	ns	
	t_{CHRH}						
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} − 10	—	ns	*
Data setup → $\overline{RD}$↑ time	t_{DSRH}	$\overline{RD}$ D15 to D00		18	—	ns	
$\overline{RD}$↑→ data hold time	t_{RHDH}			0	—	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	SYSCLK $\overline{WR0}$, $\overline{WR1}$		0.6	10	ns	
	t_{CHWH}						
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		t_{CYC} − 10	—	ns	*
SYSCLK↑→ Data output time	t_{CHDV}	SYSCLK D15 to D00		0.6	15	ns	
SYSCLK↑→ Data hold time	t_{CHDX}			0.6	15	ns	

* : When the bus timing is delayed by an automatic wait instruction or RDY input, add the time (t_{CYC} × the number of delay cycles added) to this rating.

Note: When the external load capacitance C = 50 pF.


t1
t2
t3
tCYC
SYSCLK
VOH
VOH
VOH
VOH
tCHASL
tCHASH
AS
VOH
VOL
tCHCSL
tCHCSH
CS0 to CS3
VOL
VOH
tCHAV
tCHAX
A23 to A00
VOH
VOL
VOH
VOL
tCHRL
tCHRH
tRLRH
RD
VOL
VOH
tDSRH
tRHDH
VIH
VIH
D15 to D00
Read
VIL
VIL
tCHWL
tCHWH
tWLWH
WR0,WR1
VOL
VOH
VOH
VOH
D15 to D00
Write
VOL
VOL
tCHDV
tCHDX

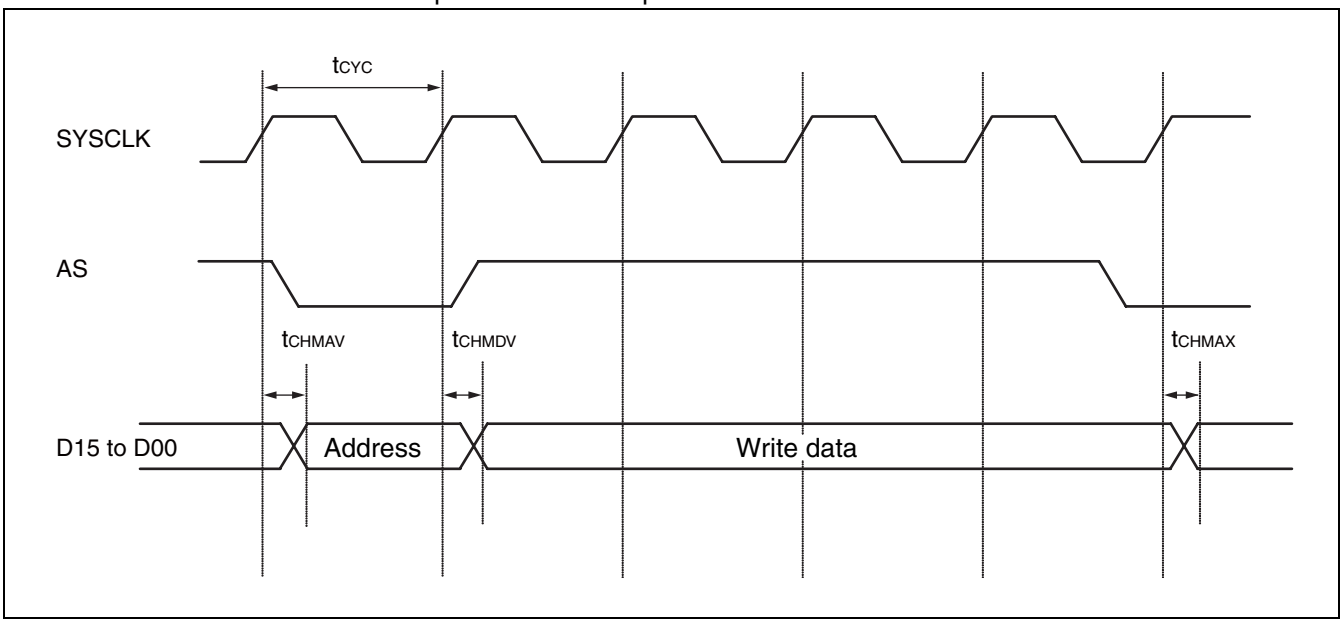
(8) Multiplexed Bus Access Read/Write Operation

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
SYSCLK↑ → D15 to D00 address delay time	t_{CHMAV} t_{CHMAX}	SYSCLK D15 to D00 (address)	—	0.6	15	ns
SYSCLK↑ → D15 to D00 data delay time	t_{CHMDV}			0.6	15	ns

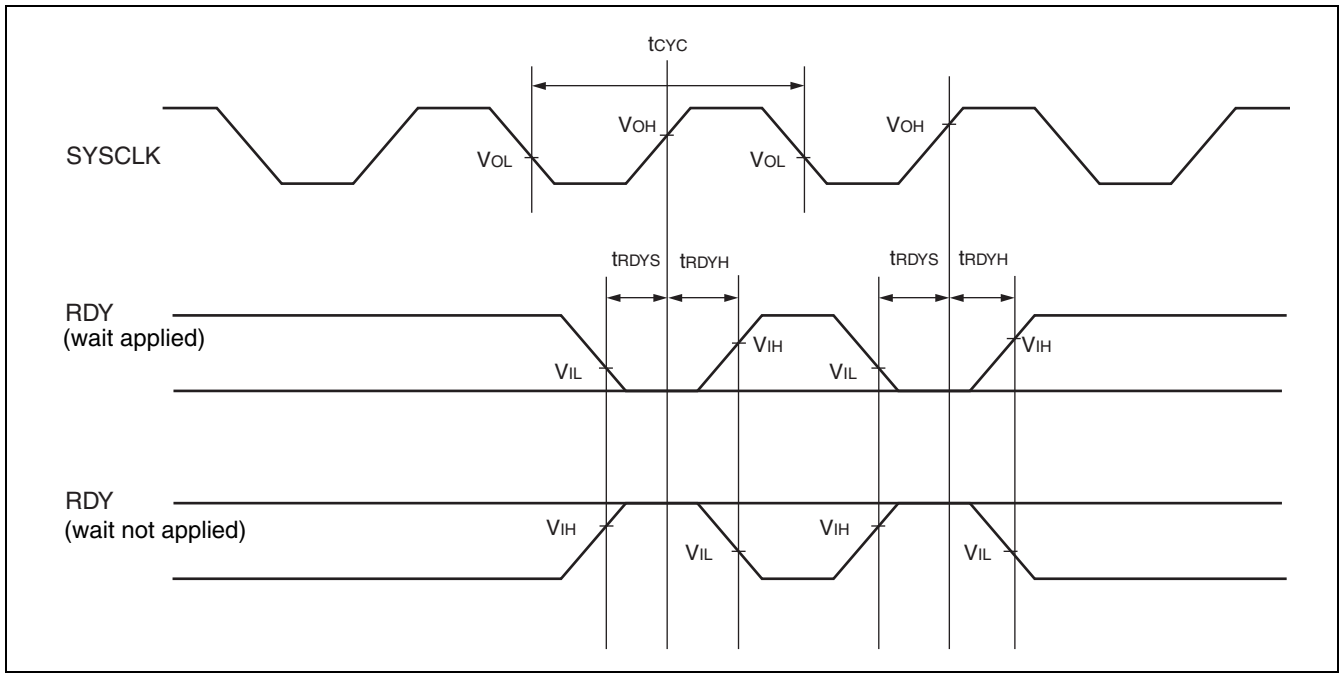
Notes : • The ratings not listed here are the same as the normal bus interface.
• When the external load capacitance C = 50 pF.



(9) Ready Input Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
RDY setup time → SYSCLK↑	t_{RDYS}	SYSCLK RDY	—	18	—	ns
SYSCLK↑→ RDY hold time	t_{RDYH}	SYSCLK RDY		0	—	ns

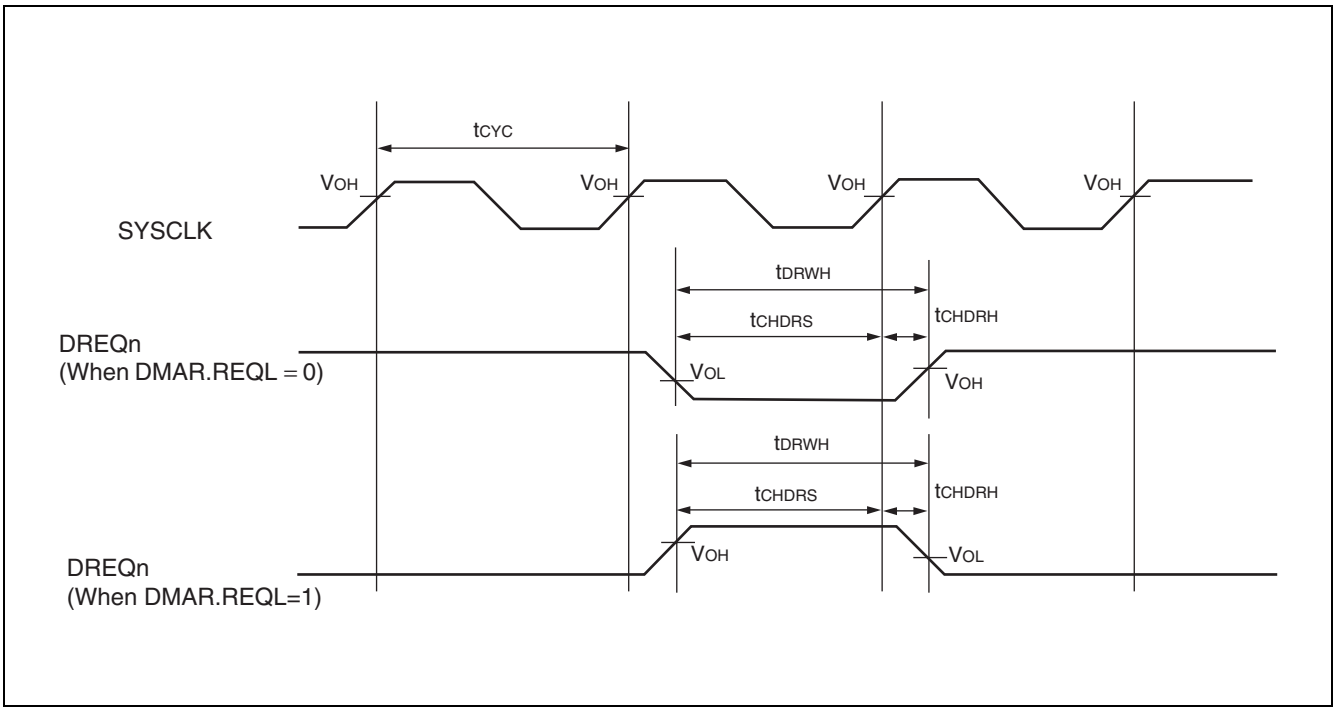


(10) DMA Controller Timing

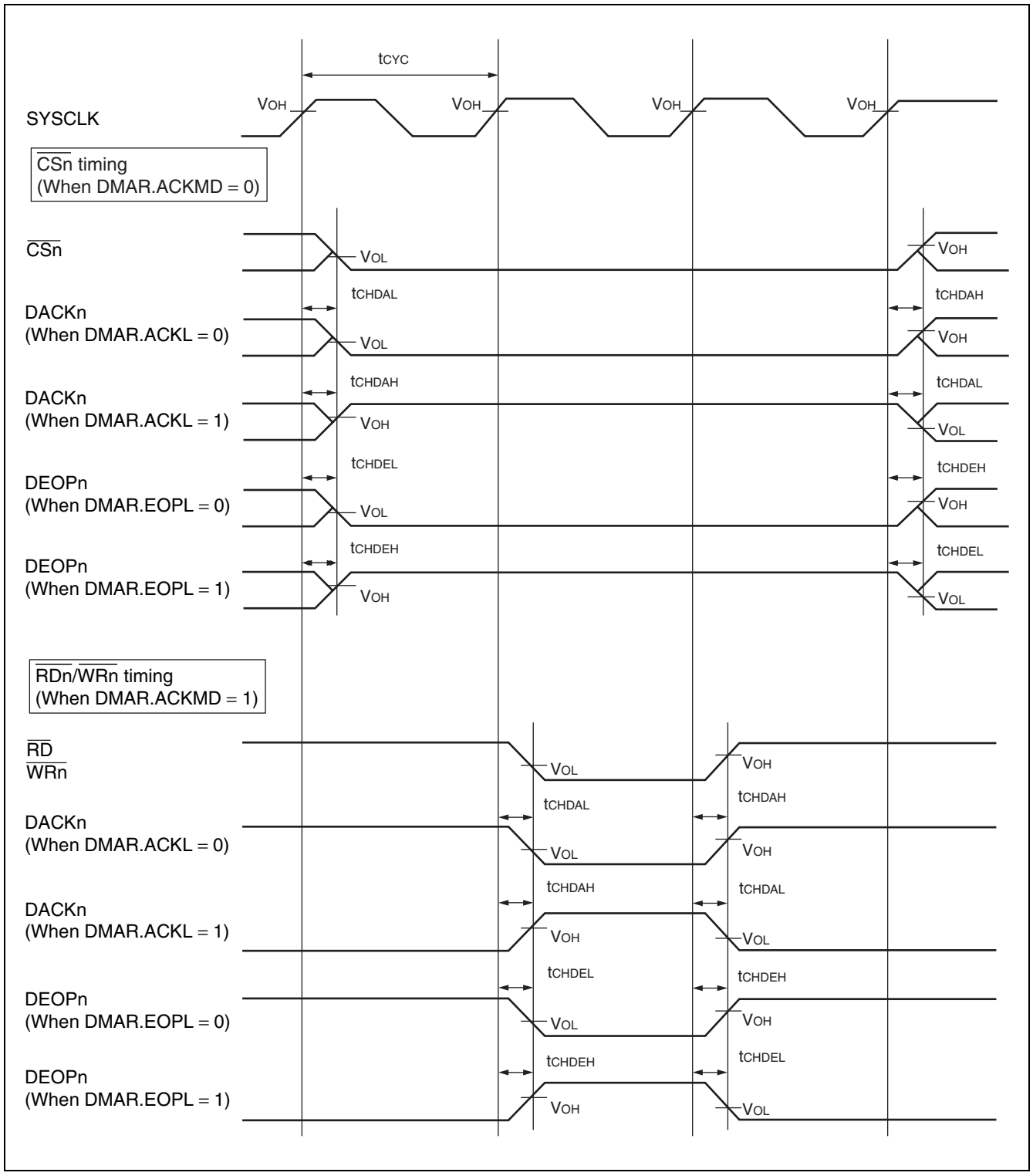
Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit
				Min	Max	
DREQ input pulse width	t_{DRWH}	DREQn	—	2 t_{CYCT}	—	ns
DACK delay time	t_{CHDAL}	SYSCLK DACKn		0.6	10	ns
	t_{CHDAH}					
DEOP delay time	t_{CHDEL}	SYSCLK DEOPn		0.6	10	ns
	t_{CHDEH}					
DREQ setup time	T_{CHDRS}	SYSCLK DREQn		18	—	ns
DREQ hold time	T_{CHDRH}	SYSCLK DREQn		0	—	ns



Note: When the external load capacitance C = 50 pF.

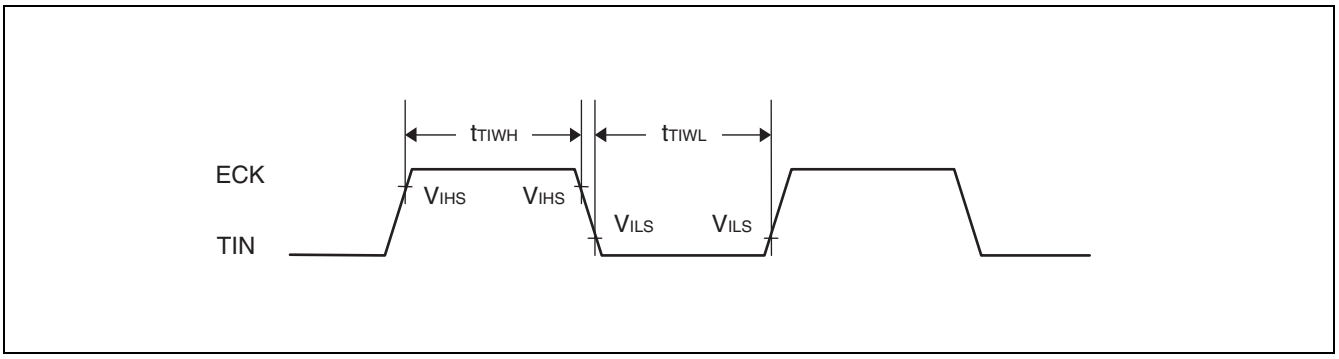

tCYC
SYSCLK
VOH
VOH
VOH
VOH
CSn timing
(When DMAR.ACKMD = 0)
CSn
VOL
VOH
tCHDAL
tCHDAH
DACKn
(When DMAR.ACKL = 0)
VOL
VOH
tCHDAH
tCHDAL
DACKn
(When DMAR.ACKL = 1)
VOH
VOL
tCHDEL
tCHDEH
DEOPn
(When DMAR.EOPL = 0)
VOL
VOH
tCHDEH
tCHDEL
DEOPn
(When DMAR.EOPL = 1)
VOH
VOL
RDn/WRn timing
(When DMAR.ACKMD = 1)
RD
WRn
VOL
VOH
tCHDAL
tCHDAH
DACKn
(When DMAR.ACKL = 0)
VOL
VOH
tCHDAH
tCHDAL
DACKn
(When DMAR.ACKL = 1)
VOH
VOL
tCHDEL
tCHDEH
DEOPn
(When DMAR.EOPL = 0)
VOL
VOH
tCHDEH
tCHDEL
DEOPn
(When DMAR.EOPL = 1)
VOH
VOL

(11) Base Timer Input Timing

• Timer input timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

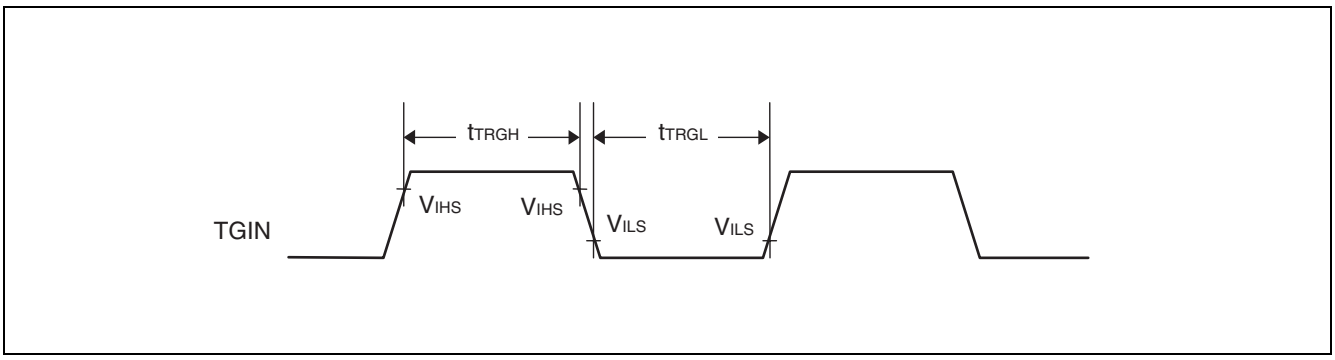
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (When used as ECK, TIN)	—	2 t_{CYCP}	—	ns



• Trigger Input Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	TIOAn/TIOBn (When used as TGIN)	—	2 t_{CYCP}	—	ns



(12) Synchronous serial (CSIO) timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

• Synchronous serial (SPI = 0, SCINV = 0)

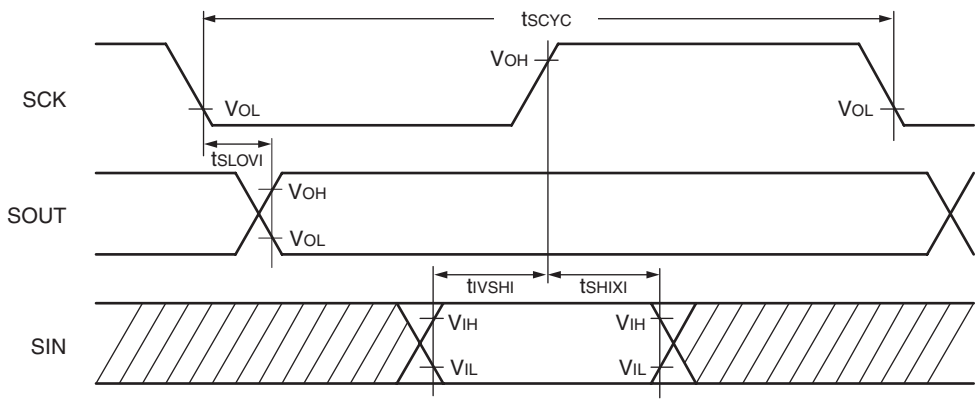
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn SOUTn		− 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		57	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn SINn		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ − 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn SOUTn		—	48	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		25	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

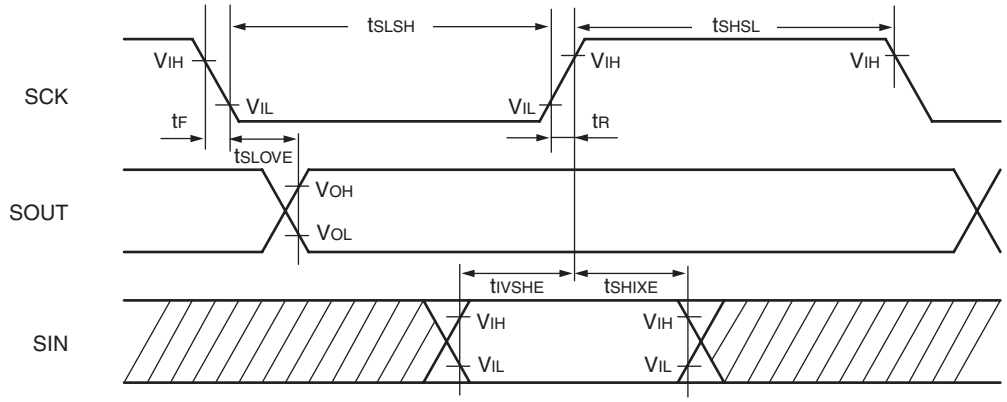
• t_{CYCP} indicates the peripheral clock cycle time.

• The above standards exclude 4ch synchronous communication.

• When the external load capacitance C = 50 pF.



MS bit = 0



MS bit = 1

• Synchronous serial (SPI = 0, SCINV = 1)

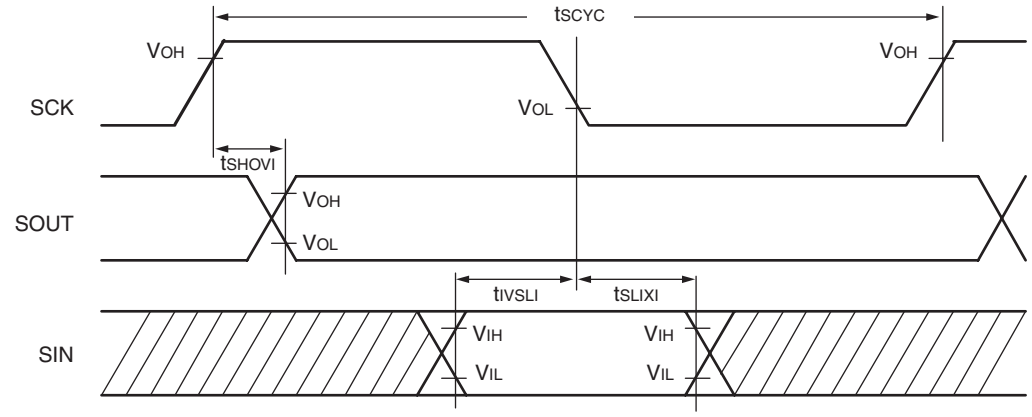
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↑→ SOUT delay time	t_{SHOVI}	SCKn SOUTn		− 30	+ 30	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKn SINn		57	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKn SINn		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ − 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↑ → SOUT delay time	t_{SHOVE}	SCKn SOUTn		—	48	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKn SINn		25	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

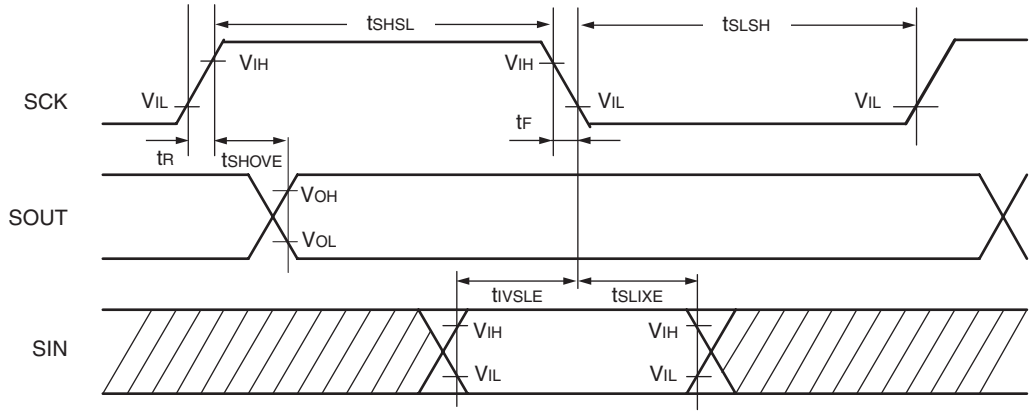
• t_{CYCP} indicates the peripheral clock cycle time.

• The above standards exclude 4ch synchronous communication.

• When the external load capacitance C = 50 pF.



MS bit = 0



MS bit = 1

• Synchronous serial (SPI = 1,SCINV = 0)

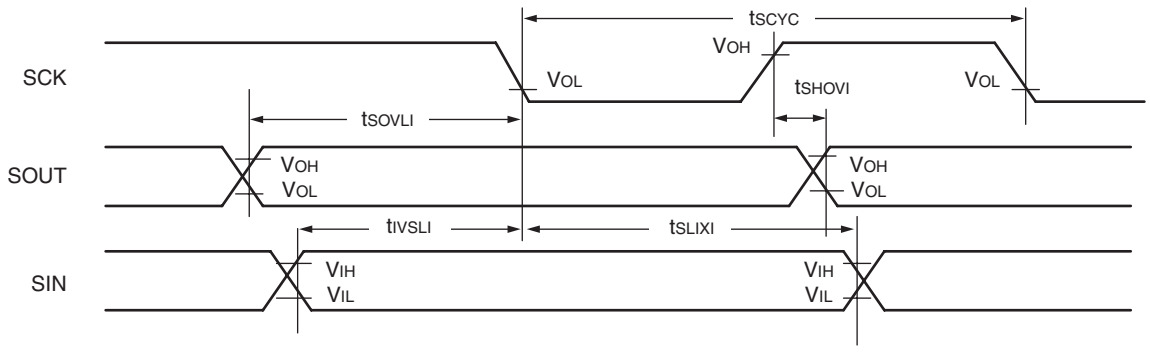
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↑→ SOUT delay time	t_{SHOVI}	SCKn SOUTn		– 30	+ 30	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKn SINn		57	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKn SINn		0	—	ns
SOUT → SCK ↓ delay time	t_{SOVLI}	SCKn SOUTn		$2t_{CYCP}$ – 30	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ – 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↑ → SOUT delay time	t_{SHOVE}	SCKn SOUTn		—	48	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKn SINn		25	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

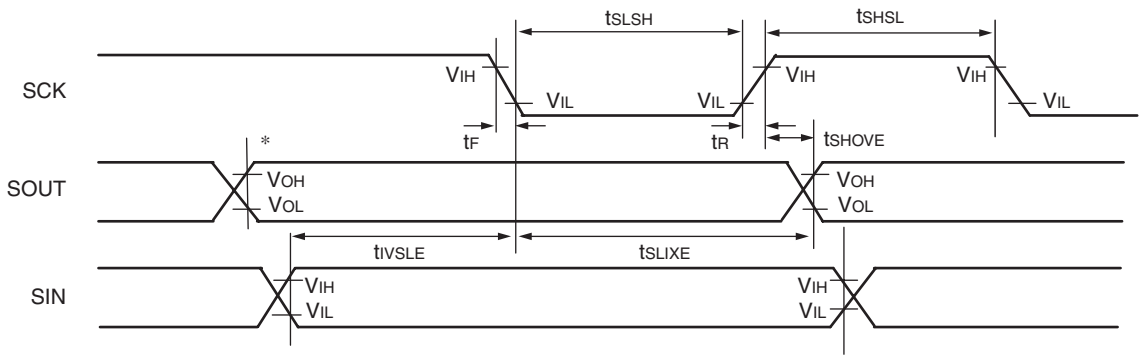
• t_{CYCP} indicates the peripheral clock cycle time.

• The above standards excludes 4ch synchronous communication.

• When the external load capacitance C = 50 pF.



MS bit = 0



MS bit = 1

* : Changes when writing to TDR register

• Synchronous serial (SPI = 1, SCINV = 1)

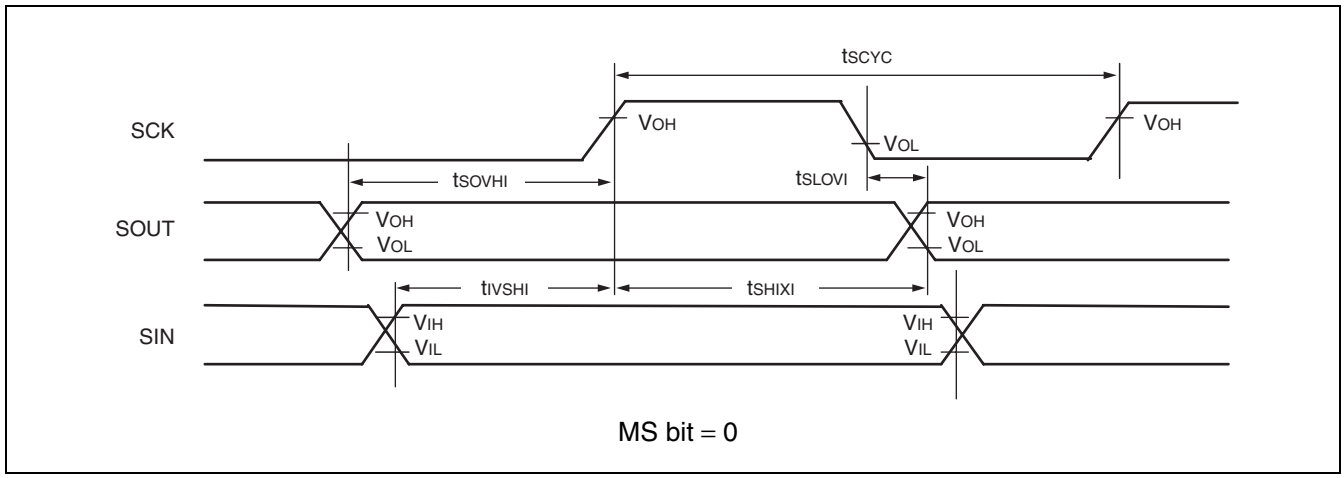
Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn SOUTn		– 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		57	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn SINn		0	—	ns
SOUT → SCK ↑ delay time	t_{SOVHI}	SCKn SOUTn		$2t_{CYCP}$ – 30	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCKn	External shift clock operation	$2t_{CYCP}$ – 10	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCKn		t_{CYCP} + 10	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn SOUTn		—	48	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		25	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

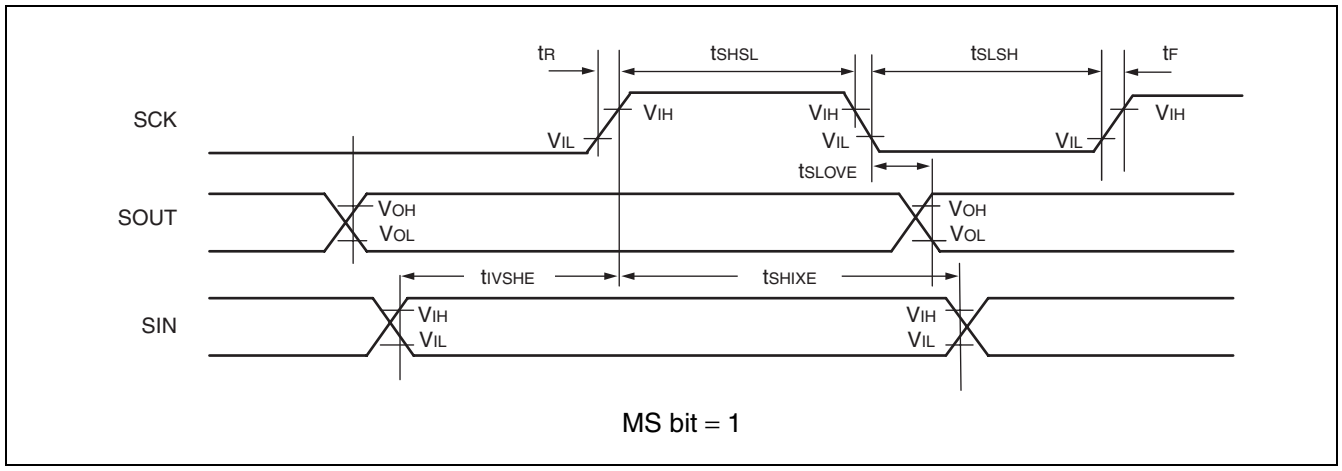
• t_{CYCP} indicates the peripheral clock cycle time.

• The above standards exclude 4ch synchronous communication.

• When the external load capacitance C = 50 pF.



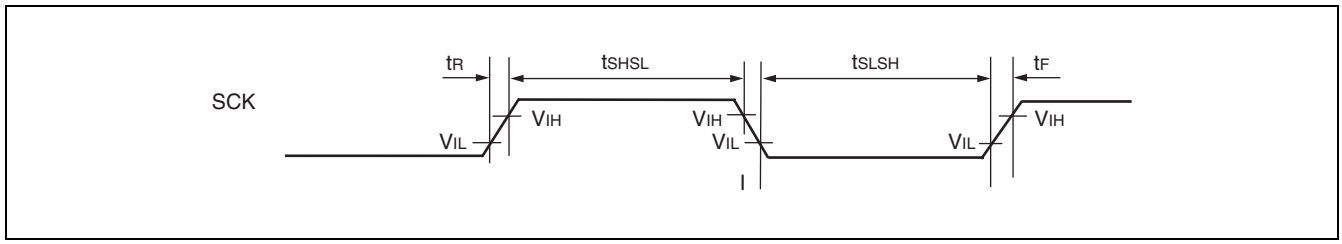
MS bit = 0



MS bit = 1

• External clock (EXT = 1) : asynchronous only

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock “L” pulse width	t_{SLSH}	C_L = 50 pF	t_{CYCP} + 10	—	ns
Serial clock “H” pulse width	t_{SHSL}		t_{CYCP} + 10	—	ns
SCK fall time	t_F		—	5	ns
SCK rise time	t_R		—	5	ns



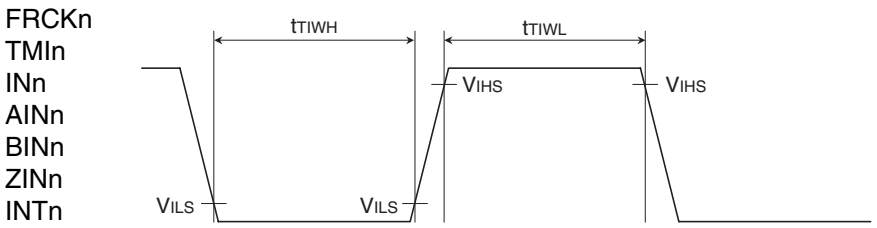
(13) Free-run Timer Clock, Reload Timer Event Input, Up/down Counter Input, Input Capture Input, Interrupt Input Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	FRCKn TMIn INn AINn BINn ZINn	—	2 t_{CYCP}	—	ns	*1
		INTn	—	3 t_{CYCP}	—	ns	*1
			—	1.0	—	µs	*2

*1 : t_{CYCP} indicates peripheral clock cycle time, except when in stop mode.

*2 : When in stop mode.

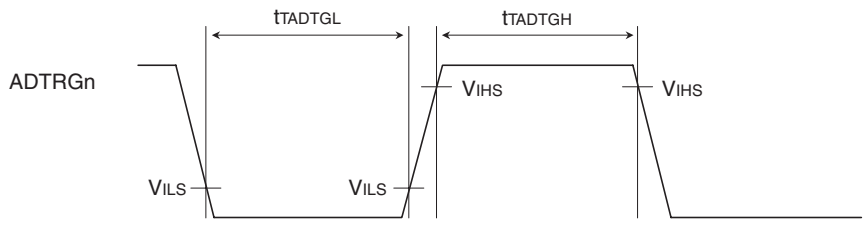


(14) A/D Converter Trigger Input Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
A/D converter trigger input	t_{TADTGL} t_{TADTGH}	ADTRGn	—	2 t_{CYCP}	—	ns	*

* : t_{CYCP} indicates peripheral clock cycle time.



(15) I²C Timing

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

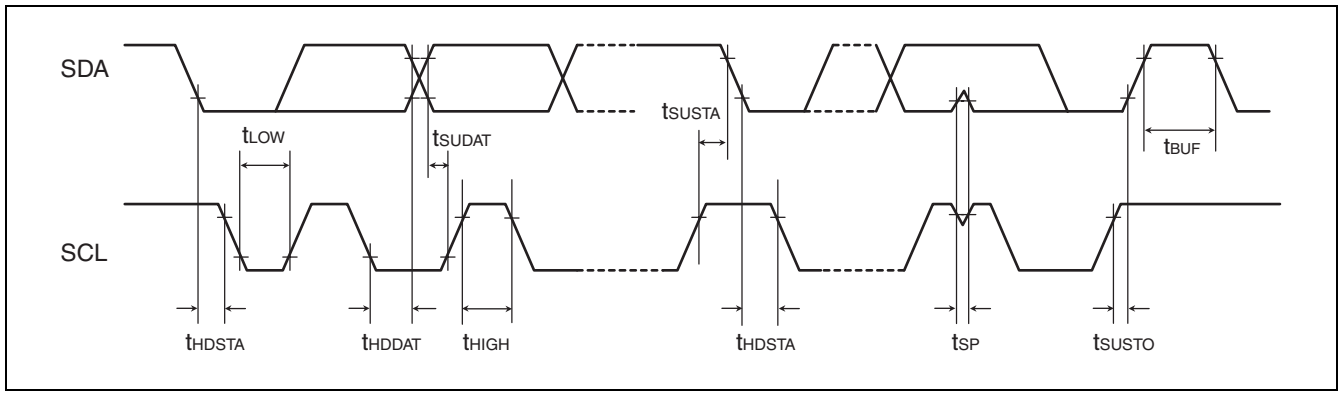
Parameter	Symbol	Pin name	Condi-tions	Typical mode		High-speed mode*3		Unit
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCKn (SCLn)	C_L = 50 pF, R = (Vp/I_{OL}) *1	0	100	0	400	kHz
"(Repeated) START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOUTn (SDAn) SCKn (SCLn)		4.0	—	0.6	—	µs
SCL clock "L" width	t_{LOW}	SCKn (SCLn)		4.7	—	1.3	—	µs
SCL clock "H" width	t_{HIGH}	SCKn (SCLn)		4.0	—	0.6	—	µs
"Repeated START condition" setup time SCL ↑→ SDA ↓	t_{SUSTA}	SCKn (SCLn)		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOUTn (SDAn) SCKn (SCLn)		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑→ SCL↑	t_{SUDAT}	SOUTn (SDAn) SCKn (SCLn)		250	—	100	—	ns
"STOP condition" setup time SCL↑→ SDA↑	t_{SUSTO}	SOUTn (SDAn) SCKn (SCLn)		4.0	—	0.6	—	µs
Bus free time between "STOP condition" and "START condition"	t_{BUF}	—		4.7	—	1.3	—	µs
Noise filter	t_{SP}	—	—	2 t_{CYCP} *4	—	2 t_{CYCP} *4	—	ns

*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4 : t_{CYCP} is the peripheral clock cycle time. To use I²C, set the peripheral bus clock at 8 MHz or more.


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

(16) Slave Interface

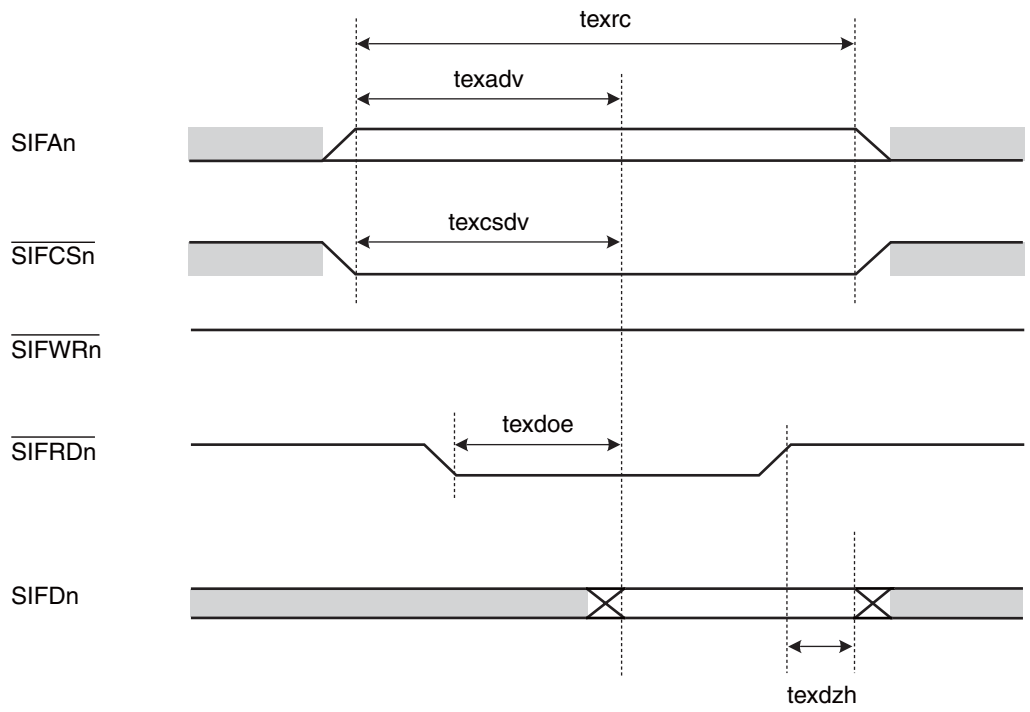
• Read Access

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
SIF write cycle time	texrc	SIFAn, $\overline{\text{SIFCSn}}$	—	6 × t_{CYC}	—	ns
SIFA → data valid	texadv	SIFAn, SIFDn	—	5 × t_{CYC}	—	ns
SIFCS → data valid	texcsdv	$\overline{\text{SIFCSn}}$, SIFDn	—	5 × t_{CYC}	—	ns
SIFRD → data output enable	texdoe	$\overline{\text{SIFRDn}}$, SIFDn	—	5 × t_{CYC}	—	ns
SIFRD “H”→ Hi-Z	texdzh	$\overline{\text{SIFRDn}}$, SIFDn	—	—	5 × t_{CYC} + 8	ns

Note: t_{CYC} indicates one cycle of on-chip bus clock.

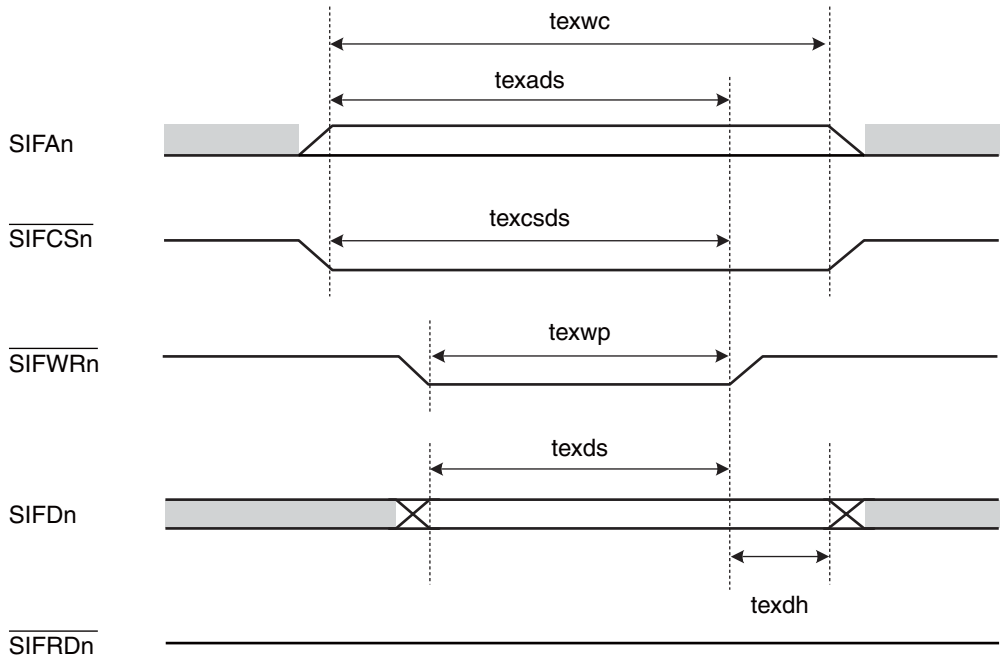


• Write Access

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)
Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
SIF write cycle time	texwc	SIFAn, $\overline{\text{SIFCSn}}$	—	5 × t_{CYC}	—	ns
SIFA → data setup time	texads	SIFAn, SIFDn	—	4 × t_{CYC}	—	ns
SIFCS → data setup time	texcsds	$\overline{\text{SIFCSn}}$, SIFDn	—	4 × t_{CYC}	—	ns
SIFWR “L” pulse width	texwp	$\overline{\text{SIFWRn}}$, SIFDn	—	4 × t_{CYC}	—	ns
SIFD setup time	texds	$\overline{\text{SIFWRn}}$, SIFDn	—	2 × t_{CYC}	—	ns
SIFD hold time	texdh	$\overline{\text{SIFWRn}}$, SIFDn	—	0	—	ns

Note: t_{CYC} indicates one cycle of on-chip bus clock.



5. Electrical Characteristics for the A/D Converter

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error	—	− 5	—	+ 5	LSB	AV_{CC} = 3.3 V, AVRH = 3.3 V
Linearity error	—	− 3.5	—	+ 3.5	LSB	
Differential linear error	—	− 3	—	+ 3	LSB	
Zero transition voltage	AN0 to AN23	− 1.5	+ 0.5	+ 4	LSB	
Full transition voltage	AN0 to AN23	AVRH − 4	AVRH − 1.5	AVRH + 0.5	LSB	
Conversion time	—	1.2*1	—	—	µs	PCLK = 33 MHz
Power supply current (analog + digital)	AV_{CC}	—	—	3.5	mA	D/A stopped
		—	—	11	µA	At power-down*2
Reference power supply current (between AVRH and AV_{SS})	AVRH	—	—	0.6	mA	AVRH = 3.0 V
		—	—	5	µA	At power-down*2
Analog input capacity	—	—	—	8.5	pF	
Interchannel disparity	—	—	—	4	LSB	
Analog port input current	AN0 to AN23	—	—	10	µA	
Analog input voltage	AN0 to AN23	AV_{SS}	—	AVRH	V	
Standard voltage	AVRH	AV_{SS}	—	AV_{CC}	V	

*1 : Depending on the clock cycle supplied to peripheral resources.
Ensure that it satisfies the value; PCLK cycle × more than 4 + the value calculated from (Equation 1).
The condition of the minimum conversion time is when PCLK = 33 MHz, the value of sampling time: 0.424 µs, external impedance: 1.4 kΩ or less and compare time: 0.73 µs.

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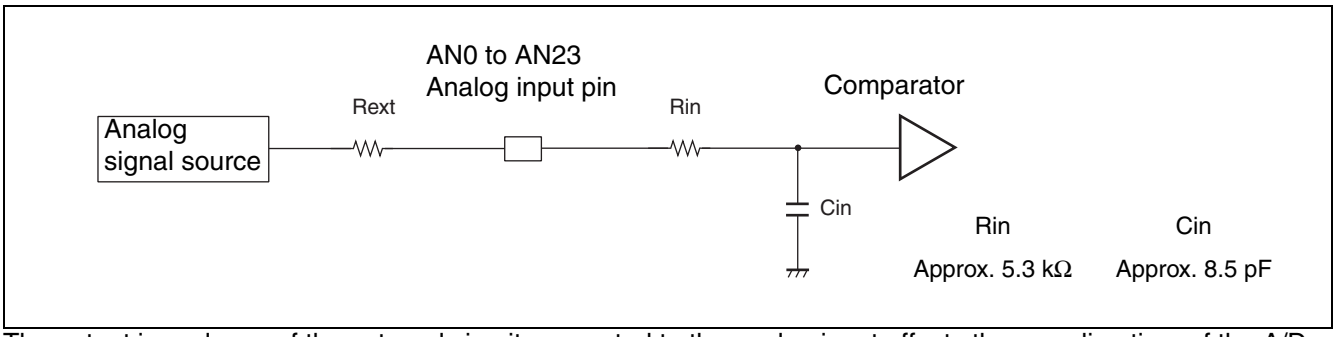
*2 : The current when the CPU is in stop mode and the A/D converter is not operating.



The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of T_S calculated from the following equation.

(Equation 1) $Ts = (Rin + Rext) \times Cin \times 8$

Ts : Sampling time
Rin : Input resistance of A/D = 5.3 kΩ
Cin : Input capacitance of A/D = 8.5 pF
Rext : Output impedance of external circuit

If the sampling time is set as 600 ns,

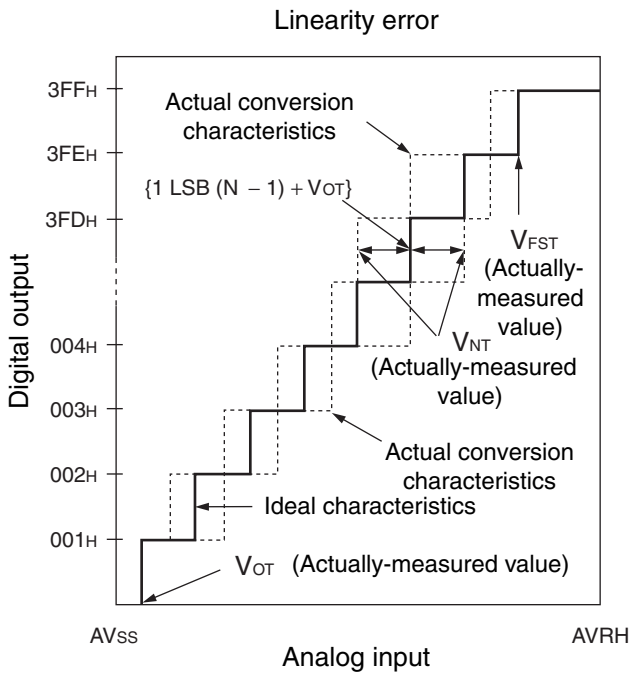
$600\ ns \geq (5.3\ k\Omega + Rext) \times 8.5\ pF \times 8$

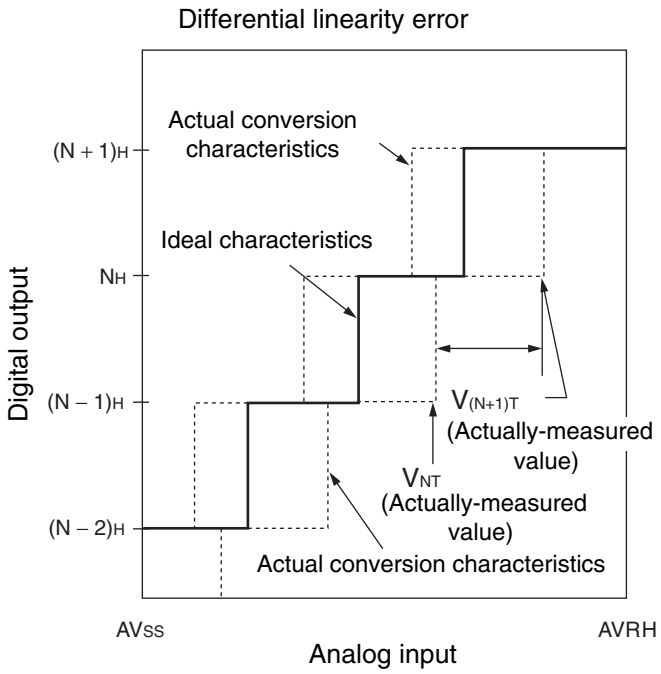
$\therefore Rext \leq 3.5\ k\Omega$

And the impedance of the external circuit therefore needs to be 3.5 kΩ or less.

• Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0000000000←→0000000001) and the full-scale transition point (1111111110←→1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.





$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.
V_{NT} : Voltage at which the digital output changes from $(N - 1)_H$ to N_H.

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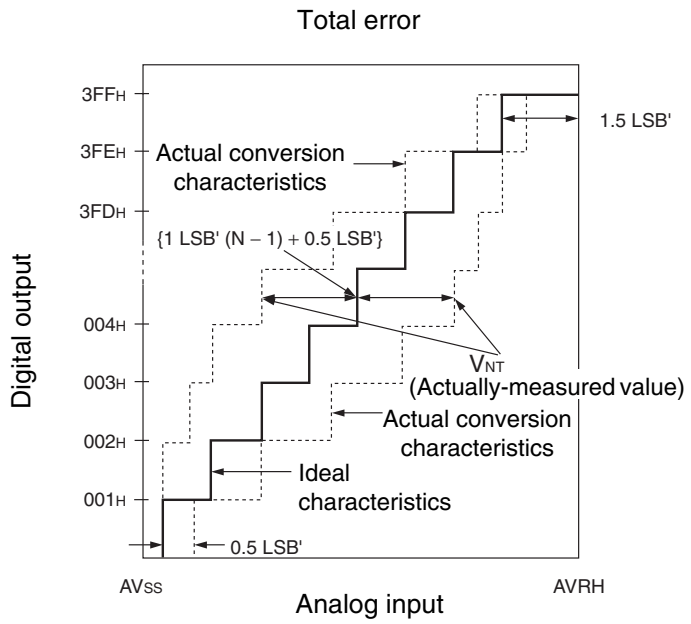

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H.
V_{OT}' (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST}' (Ideal value) = AVRH – 1.5 LSB [V]

6. Electrical Characteristics for the D/A Converter

Not using USB : (V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Using USB : (V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	8	bit	
Linear error	—	− 2.0	—	+ 2.0	LSB	When the output is unloaded
Differential linear error	—	− 1.0	—	+ 1.0	LSB	When the output is unloaded
Conversion time	—	—	0.6	—	µs	When load capacitance (C_L) = 20 pF
		—	3.0	—	µs	When load capacitance (C_L) = 100 pF
Analog output impedance	DA0 to DA2	3.19	3.5	4.55	kΩ	
Analog current	AV_{CC}	—	450	—	µA	10 µs conversion, when the output is unloaded (When 3 channels operating, A/D stopped)
		—	—	3600*	µA	When the input digital code is fixed at $7A_H$ or 85_H (When 3 channels operating, A/D stopped)
		—	—	11	µA	At power-down (When A/D stopped)

* : The current consumption of the D/A converter varies with input digital code.
The standard value indicates the current consumed when the digital code that maximizes the current consumption is input.

7. USB Characteristics

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter		Sym-bol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input High level voltage	V_{IH}	UDP, UDM	—	2.0	V_{CC} + 0.3	V	*1
	Input Low level voltage	V_{IL}		—	V_{SS} − 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		—	0.2	—	V	*2
	Differential common mode input voltage	V_{CM}		—	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output Low level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		—	1.3	2.0	V	*4
	Rise time	t_{FR}		—	4	20	nS	*5
	Fall time	t_{FF}		—	4	20	nS	*5
	Rise/fall time matching	t_{RFM}		—	90	111.11	%	*5
	Output impedance	Z_{DRV}		—	28	44	Ω	Including Rs = 27 Ω
Input capacitance	Transceiver edge rate control capacitance	C_{EDGE}		—	—	75	pF	*6
Series resistance		R_S		—	25	30	Ω	Recommended value:27 Ω

*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 [V], V_{IH} (Min) = 2.0 [V] (TTL input standard).
There are some hystereses to lower noise sensitivity.

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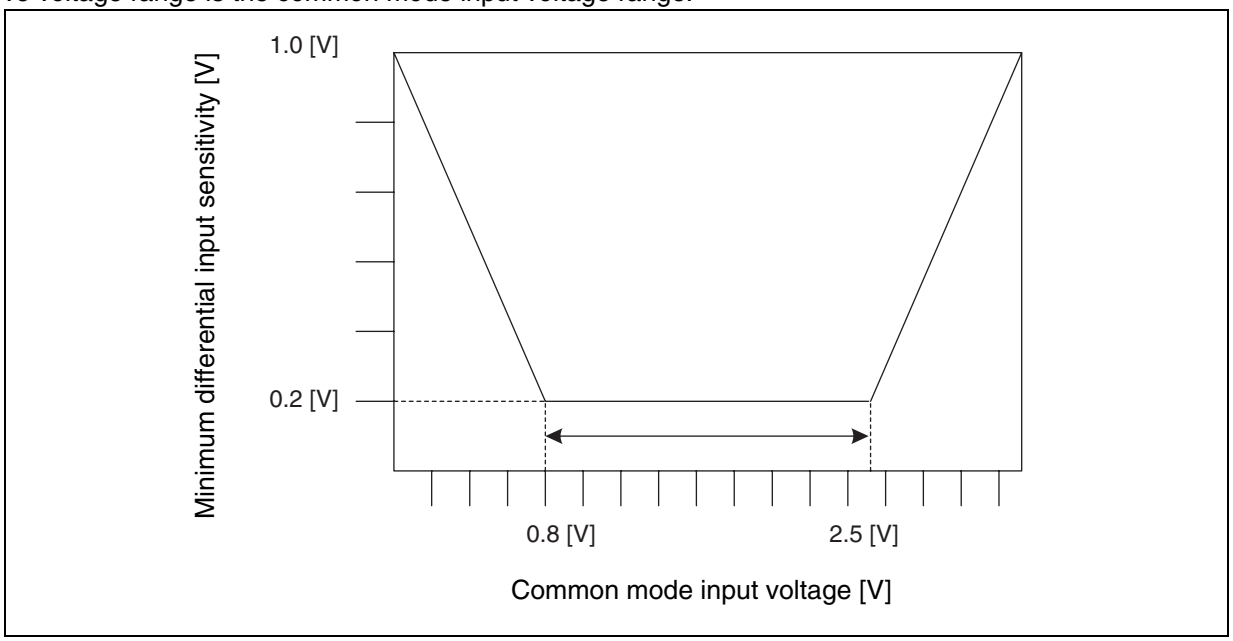
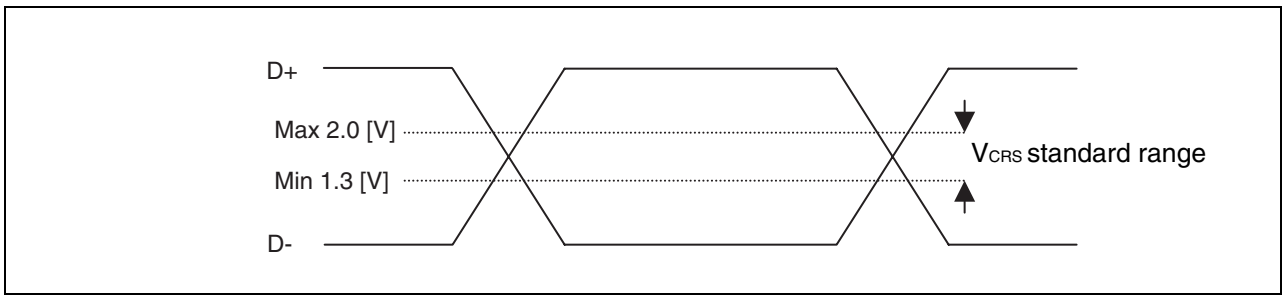
*2 : Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 [mV] of differential input sensitivity when the differential data input is within 0.8 [V] to 2.5 [V] to the local ground reference level.
Above voltage range is the common mode input voltage range.

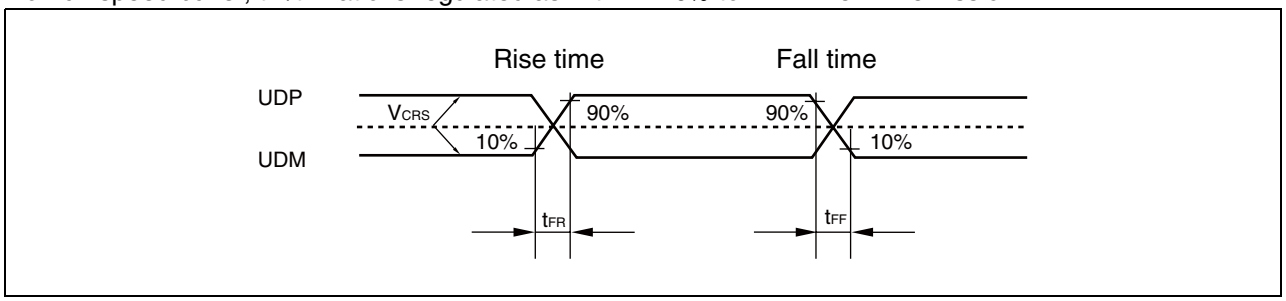


*3 : The output drive capability of the driver is below 0.3 [V] at Low-State (V_{OL}) (to 3.6 [V] and 1.5 kΩ load), and 2.8 [V] or above (to the V_{SS} and 1.5 kΩ load).

*4 : The cross voltage of the external differential output signal (D + /D –) of USB I/O buffer is within 1.3 [V] to 2.0 [V].



*5 : Regarding t_{FR} ,t_{FF}, t_{RFM}
They indicate rise time (Trise) and fall time (Tfall) of the differential data signal.
They are defined by the time between 10% to 90% of the output signal voltage.
For full-speed buffer, t_{FR}/t_{FF} ratio is regulated as within ±10% to minimize RFI emission.



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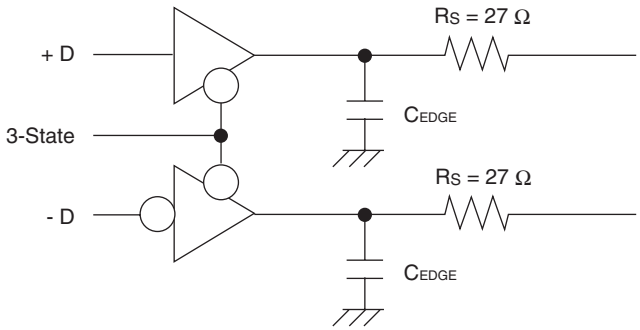
*6 : The place to connect transceiver edge rate control capacitance C_{EDGE}
For this USB I/O, it is recommended to use C_{EDGE} control capacitor.
For USB Max standard as 75 pF, please control the edge characteristic of output waveform by connecting 30 to 50 [pF] (recommended value : 47 [pF] ≒ 50[pF]) to D + and D − lines when implementing on the board.



Driver output impedance 3 Ω to 19 Ω
Rs serial resistance value 25 Ω to 30 Ω
Please apply 27 Ω of serial resistance value as a recommended value.

8. Flash Memory Write/Erase Characteristics

(V_{CC} = 3.3 V, Ta = + 25 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.9	3.6	s	Excludes write time prior to internal erase
Half word (16bits) write time	—	23	370	µs	Not including system-level overhead time.
Chip erase time*1	—	10.8	43.2	s	Excludes write time prior to internal erase (When equipped with 512 Kbytes)
Erase/write cycles	10000	—	—	cycle	Average Ta ≤ + 85 °C
Flash memory data hold time	10*2	—	—	year	Average Ta ≤ + 85 °C

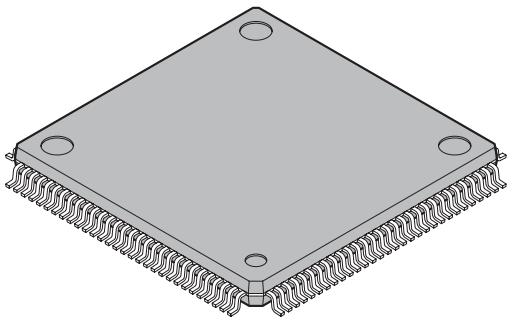
*1 : The chip erase time is the sector erase time multiplied across all sectors.

*2 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

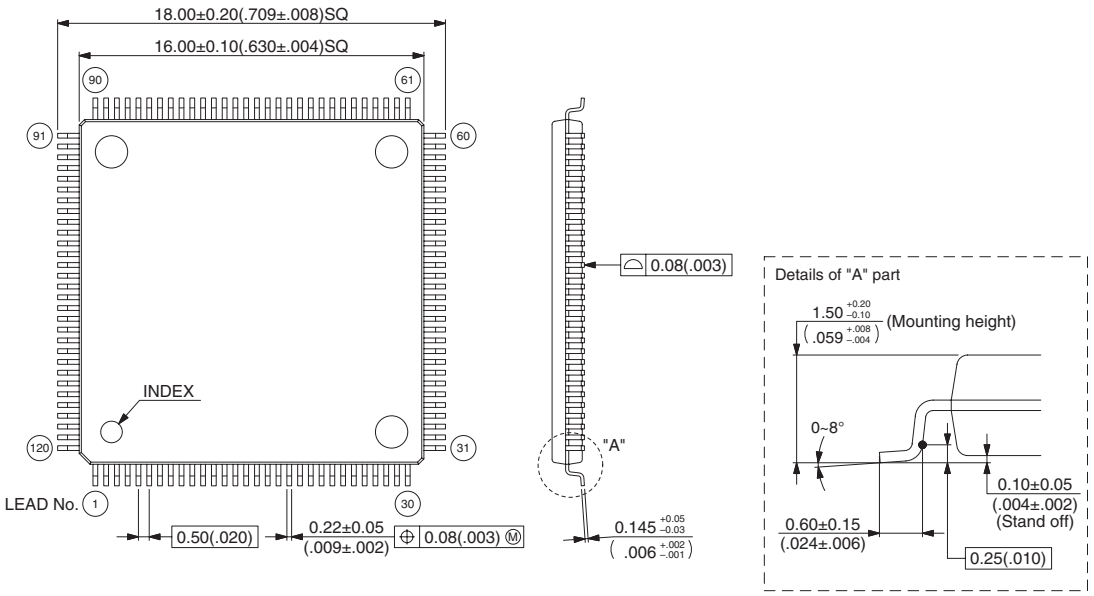
■ ORDERING INFORMATION

Part number	Package
MB91F662PMC	120-pin plastic LQFP (FPT-120P-M21)

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)		

120-pin plastic LQFP
(FPT-120P-M21)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

MEMO

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