Errata Sheet for Arria V GX and GT Devices

This errata sheet provides information about known device issues affecting Arria® V production devices.

Device Errata for Arria V Production Devices

Table 1 lists the specific device issues and the affected Arria V production devices.

Table 1. Arria V Production Device Issues (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"EMIF Maximum Frequency Specification Update" The EMIF maximum frequency specification has been updated.	All Arria V GX and GT Devices	None
"SEU Internal Scrubbing" SEU internal scrubbing has usage restrictions.	All Arria V GX and GT Devices	None
"Fractional PLL Phase Alignment Error" The fractional PLL (fPLL) has a silicon sensitivity that causes the static phase error to operate beyond the Quartus® II software expectation.	All Arria V GX and GT Devices	Refer to Table 3.
"Bit Errors on the LVDS RX Channels Using DPA" DPA or soft-CDR mode is not supported for specific LVDS data rates.	All Arria V GX and GT devices	For the Quartus®II and die revision solutions in different LVDS DPA data rate ranges, refer to Table 4 and Table 5. Devices that support the complete range of LVDS DPA data rate will begin rolling out in Q3 2013.
"Configuration via Protocol (CvP)" CvP and Autonomous HIP functionality is not supported.	All Arria V Devices except 5AGTC7, 5AGXA7, 5AGXA5, 5ASXB3, 5ASXB5, 5ASTD3 and 5ASTD5 devices.	Devices that are CvP capable will begin rolling out in Q2 2013
"Usermode High Icc" High Icc observed when entering **User** mode.	All Arria V GX and GT Devices	None

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Table 1. Arria V Production Device Issues (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"Unused or Idle Transmitter Maximum Data Rate Degradation" Currently unused or idle transmitter's maximum data rate can degrade over a period.	All Arria V GX and GT Devices	None
"False Configuration Failure in Active Serial Multi-Device Configurations" In Active Serial (AS) multi-device configuration mode, the error checking for CONF_DONE release may not operate correctly.	All Arria V devices	None

EMIF Maximum Frequency Specification Update

To achieve timing closure, the external memory interface (EMIF) maximum frequency specification has been updated in Table 2.

Table 2. Arria V EMIF Maximum Frequency Specification Update (1), (2)

Device	Speed Grade	Memory Type	Memory Topology	Depth Expansion	Interface Type	Original Maximum Specifications (MHz)	Updated Maximum Specifications (MHz)
Arria V GX	C4	DDR2	Component	2 Chip Selects	Hard Controller	350	333
Arria V GX/GT	I3	DDR2	Component	2 Chip Selects	Hard Controller	350	333
Arria V GX/GT	I3	DDR3/ DDR3L	Component	1 Chip Select	Hard Controller	533	533 (3)

Notes to Table 2:

(1) The stated performances apply to component topology only. The DIMM topology is not supported on the hard controller.

(2) For changes to other variants and slower speed grades, contact mySupport.

(3) Upgrade the DDR3 SDRAM/DDR3L SDRAM component from 533 MHz to 667 MHz to achieve the specified maximum frequency.

Solution

These maximum frequency specifications will be updated in a future release of External Memory Interface Spec Estimator.

SEU Internal Scrubbing

The SEU internal scrubbing feature has usage restrictions. For additional information, contact mySupport.

Fractional PLL Phase Alignment Error

The fPLL has a silicon sensitivity that causes the static phase error to operate beyond the Quartus II software expectation. The frequency range and jitter performance of the fPLL meet the datasheet specification. This sensitivity is a time-zero failure, which means a design affected by this issue will show failure immediately upon a given device operation over expected operating conditions or will never show the issue.

The following usage modes may be affected:

- When the fPLL is used for phase compensation. For example, applications that may use phase compensation include LVDS, board trace matching, or FPGA skew compensation, such as zero delay buffering.
- Specific IP cores that require fPLL usage
- Inter-clock domain transfers involving fPLL usage

Workaround

Customers can implement design techniques to mitigate inter-clock domain transfers and use the Altera® tool to evaluate fPLL usage and determine if designs may be affected by this issue.

To determine if your design may be affected, use the Altera fPLL Usage Evaluation Tool.

If you believe your design is affected by this issue, please contact mySupport for further assistance.

Long-Term Fix

This issue is, or will be fixed in the silicon die revision shown below. Table 3 identifies the fixed silicon by die revision for each device.

Table 3. Fixed Silicon by Die Revision

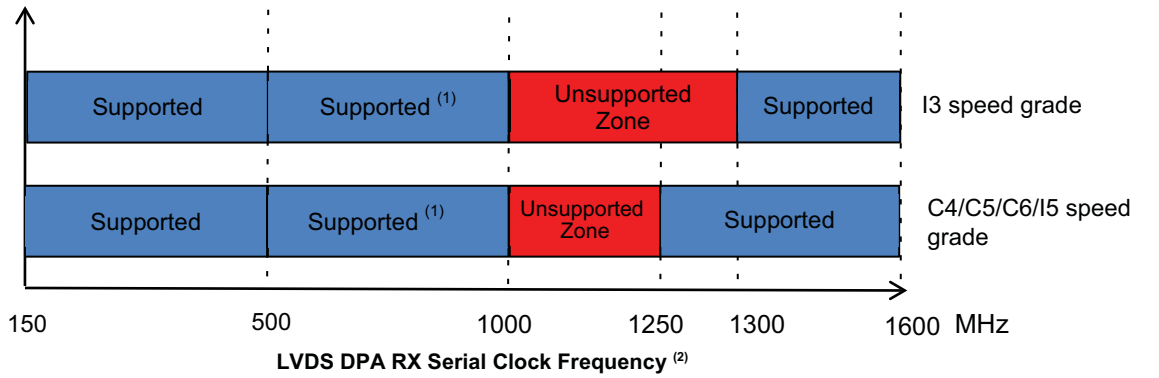
Family	Device	Fixed Die Revision
Arria V GT	5AGTD7	C
	5AGTD3	D
	5AGTC7	B
	5AGTC3	B
Arria V GX	5AGXB7	C
	5AGXB5	C
	5AGXB3	D
	5AGXB1	D
	5AGXA7	B
	5AGXA5	B
	5AGXA3	B
	5AGXA1	B
Arria V ST	5ASTD5	B
	5ASTD3	B
Arria V SX	5ASXB5	B
	5ASXB3	B

For an explanation of the date code and revision marking format, refer to Figure 2 on page 6.

Bit Errors on the LVDS RX Channels Using DPA

DPA mode or soft-CDR mode is not supported for specific LVDS data rate as shown in Figure 1. If the RX channels with DPA are operating in the unsupported zone, bit errors may occur. This limited LVDS data rate support impacts early die revision Arria V GX/GT device when LVDS receiver channels operating in DPA mode or soft-CDR mode. LVDS receiver channels operating in non-DPA are not affected. The unsupported data rate zones are dependent on device speed grade as shown in Figure 1. The affected Arria V GX/GT die revisions are shown in Table 6.

Figure 1. Arria V GX/GT LVDS DPA RX Supported and Unsupported Data Rates



Notes to Figure 1:

(1) Supported with recompilation in Quartus II version 13.0 and later. Not supported in Quartus II version 12.1SP1 and earlier. If the RX channels with DPA are operating in this zone with Quartus II version 12.1SP1 and earlier, bit errors may occur.

(2) The scale of the LVDS DPA RX serial clock frequency is for illustration purposes only.

Solution

For the LVDS data rate solutions in the unsupported zones, refer to Table 4 and Table 5.

Table 4. Arria V GX/GT Solution for C4/C5/C6/I5 Speed Grades (Part 1 of 2)

LVDS DPA RX Data rate	Solution for Die Revision without Fix	Solution for Die Revision with Fix (1)
150 Mbps ≤ Data Rate ≤ 500 Mbps	No impact. No action required.	No impact. No action required.
500 Mbps < Data Rate ≤ 730 Mbps	Design recompilation in Quartus II 13.0 and onwards	Design recompilation in Quartus II 13.0 and onwards
730 Mbps < Data Rate ≤ 1000 Mbps	Design recompilation in Quartus II 13.0 and 13.0 SP1 (2)	Design recompilation in Quartus II 13.0 and onwards (2)
1000 Mbps < Data Rate < 1250 Mbps	Requires revised silicon (1)	Design recompilation in Quartus II 13.1 (3)
1250 Mbps ≤ Data Rate < 1300 Mbps	No impact. No action required (4).	No impact. No action required (4).

Table 4. Arria V GX/GT Solution for C4/C5/C6/I5 Speed Grades (Part 2 of 2)

LVDS DPA RX Data rate	Solution for Die Revision without Fix	Solution for Die Revision with Fix (1)
1300 Mbps ≤ Data Rate ≤ 1600 Mbps	No impact. No action required.	No impact. No action required.

Notes to Table 4:

(1) The die revision for devices with fix is shown in Table 6.

(2) The designs operating at these data rates compiled in Quartus II 13.0 and 13.0 SP1 support die revisions with and without fix, and no design recompilation is required in Quartus II 13.1. The designs compiled in Quartus II 13.1 and onwards only support die revision with fix. Please contact mySupport for further assistance.

(3) Please contact mySupport for compilation support on the die revision with fix prior to Quartus II 13.1

(4) The designs operating at these data rates compiled in Quartus II prior to 13.1 support die revisions with and without fix, and no design recompilation is required in Quartus II 13.1. The designs compiled in Quartus II 13.1 and onwards only support die revision with fix. Please contact mySupport for further assistance.

Table 5. Arria V GX/GT Solution for I3 Speed Grade

Data rate	Solution for Device Revision without Fix (1)	Solution for Device Revision with Fix (1)
150 Mbps ≤ Data Rate ≤ 500 Mbps	No impact. No action required.	No impact. No action required.
500 Mbps < Data Rate ≤ 730 Mbps	Design recompilation in Quartus II 13.0 and onwards	Design recompilation in Quartus II 13.0 and onwards
730 Mbps < Data Rate ≤ 1000 Mbps	Design recompilation in Quartus II 13.0 and 13.0 SP1 (2)	Design recompilation in Quartus II 13.0 and onwards (2)
1000 Mbps < Data Rate < 1250 Mbps	Requires revised silicon (1)	Design recompilation in Quartus II 13.1 (3)
1250 Mbps ≤ Data Rate < 1300 Mbps	Requires revised silicon (1)	Design recompilation in Quartus II 13.1 (3)
1300 Mbps ≤ Data Rate ≤ 1600 Mbps	No impact. No action required.	No impact. No action required.

Notes to Table 5:

(1) The die revision for devices with fix is shown in Table 6.

(2) The designs operating at these data rates compiled in Quartus II 13.0 and 13.0SP1 support die revisions with and without fix, and no design recompilation is required in Quartus II 13.1. The designs compiled in Quartus II 13.1 and onwards only support die revision with fix. Please contact mySupport for further assistance.

(3) Please contact mySupport for compilation support on the die revision with fix prior to Quartus II 13.1

Table 6. Arria V GX/GT Device Revision with Fix (Part 1 of 2)

Member code	Revisions without Fix	Revision with Fix (1)
5AGXA1	A	B
5AGXA3	A	B
5AGXA5	A	B
5AGXA7	A	B
5AGXB1	A, B, C	D
5AGXB3	A, B, C	D
5AGXB5	A, B	C
5AGXB7	A, B	C
5AGTC3	A	B
5AGTC7	A	B
5AGTD3	C	D

Table 6. Arria V GX/GT Device Revision with Fix (Part 2 of 2)

Member code	Revisions without Fix	Revision with Fix (1)
5AGTD7	A, B	C

Note to Table 6:

(1) Refer to Figure 2 for the Arria V device's top side data code. This issue is fixed if the fourth alphanumeric character (Z) from the left printed on the top side of the device is equal to or later in the alphabet than the letter shown in the Revision with Fix column.

Dynamic Frequency Range Constraints for DPA and Soft-CDR Mode

When LVDS receivers are implemented with dynamic frequency range, either with reconfigurable PLL, or via input frequency changes, the frequency range of the serial clock (fast clock) is limited to the following range (Table 7) in a single design compilation.

Table 7. Dynamic Frequency Range Constraints for DPA and Soft-CDR mode

Frequency Range Support for PLL Reconfiguration for LVDS Receivers with DPA (1)	Device Revision without Fix	Device Revision with Fix
150 Mbps ≤ Data Rate ≤ 500 Mbps	Supported	Supported
500 Mbps < Data Rate ≤ 730 Mbps	Supported	Supported
730 Mbps < Data Rate < 1300 Mbps	Not supported	Supported
1300 Mbps ≤ Data Rate ≤ 1600 Mbps	Supported	Supported

Note to Table 7:

(1) PLL reconfiguration or dynamic input frequency changes is only allowed within the defined range.

Please contact mySupport for further assistance.

Configuration via Protocol (CvP)

The fix involves a new die revision. You can use the die revision character in the Date Code to determine whether or not the device supports CvP.

CvP update can only be used at Gen1 data rates. CvP is supported if the fourth alphanumeric character (Z) from the left printed on the top side of the device is equal to or later in the alphabet than the letter shown in the Revision with Fix column of Table 8.

Figure 2 shows an Arria V device's top side date code.

Figure 2. Altera Date Code Marking Format

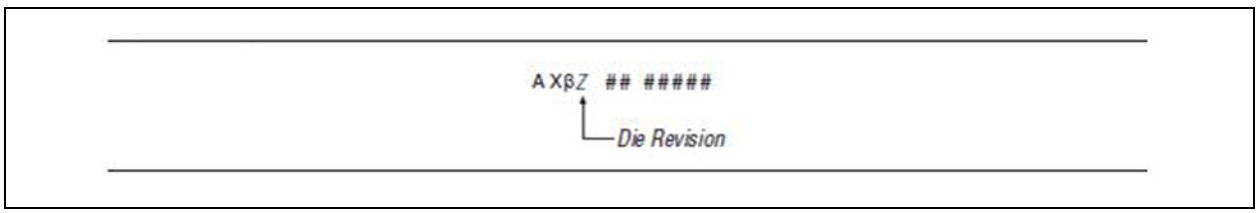


Table 8. Device and Die Revisions

Member Code	Revisions without Fix	Revision with Fix
5AGXA1	A	B
5AGXA3	A	B
5AGXA5	None	A
5AGXA7	None	A
5AGXB1	A, B and C	D
5AGXB3	A, B and C	D
5AGXB5	A and B	C
5AGXB7	A and B	C
5AGTC3	A	B
5AGTC7	None	A
5AGTD3	A, B and C	D
5AGTD7	A and B	C
5ASXB3	None	A
5ASXB5	None	A
5ASTD3	None	A
5ASTD5	None	A
Note to Table 8: Future revisions (not shown in the table above) will be CvP capable.		

For Gen2 CvP update or further inquiries, please contact mySupport.

Partial Reconfiguration (PR) with Compression Feature Not Supported

The Partial Reconfiguration (PR) with CvP is not supported when compression is turned on and encryption is turned off. There is no restriction when CvP is disabled. Table 9 shows the support of PR with CvP in different states of compression and encryption.

Table 9. PR Support with CvP in Various States of Compression and Encryption

Compression with PR	Encryption with PR	CvP mode	Support
OFF	OFF	On	Yes
OFF	ON	On	Yes
ON	OFF	On	No
ON	ON	On	Yes

Please contact mySupport for further assistance.

Usermode High Icc

When the affected device transitions into User mode, high Icc is observed, due to internal dataline contention.

Workaround

Use the following software workaround to prevent the user mode high Icc issue:

- For the Error Detection Cyclic Redundancy Check (EDCRC) user, no workaround is needed because the EDCRC feature eliminates the high Icc issue.
- For the non-EDCRC user, a software workaround is needed and is available in the Quartus II software version 12.1 sp1, or later.

Action Needed for Existing Designs (pre-Quartus II software version 12.1 sp1)

Specific action is needed when the existing design uses the EDCRC and certain versions of the Quartus II software. Table 10 lists the actions needed for the different settings.

Table 10. Action for Existing Designs

Design	Quartus II Version	Action
EDCRC enabled.	Any	None needed.
EDCRC disabled	12.1 only	Full recompilation is required using the Quartus II software version 12.1 sp1, or later release.
	Pre 12.1	Full recompilation is NOT needed, but requires the use of Quartus II software version 12.1 sp1, or later for programming file conversion (1).

Note to Table 10:

(1) Convert the existing SOF file to RBF, POF, JIC, or another format using **Convert Programming File**, under the File menu of the Quartus II software.

Unused or Idle Transmitter Maximum Data Rate Degradation

A currently unused or idle transmitter's maximum data rate can degrade over a period. The issue is caused by degradation in the local or central clock divider (used to drive the transmitter) being left idle over an extended period, with the transceiver's power supplies powered up.

The issue only impacts designs that will enable unused or idle transmit channels with idling clock dividers through a new programming file at a later date. The transmit channel in devices that do not power up the transceiver power supplies are not affected.

The idling clock divider can occur in three conditions:

1. Transmit channels in permanent reset
   a. Transmit channels that will be enabled later are instantiated in the current design, but with the PMA block or divider source clock (CMU PLL or fPLL) held in reset permanently.
2. Unused non-bonded transmit channels
   a. Non-bonded transmit channels that will be enabled later are not instantiated in the current design, resulting in an idling local clock divider.
3. Unused CMU PLL or fPLL for bonding
   a. CMU PLL or fPLL used for bonding that will be enabled later are not instantiated in the current design, resulting in an idling central clock divider.

To avoid this issue, ensure the clock dividers that will be enabled later are in the active state in the current programming file. Follow the implementation instructions in Table 11 to avoid this issue.

Table 11. Workaround Implementation Instructions

Scenario	Design Requirement	Future Design Change	Action
1	Fixed transceiver utilization design over device lifecycle (no change to design file)	Not applicable	Do nothing, not affected by issue.
2	Transceiver utilization design will change over device lifecycle	Enable transmit channel held in permanent reset	Leave transmitter `tx_analogreset` or `pll_powerdown` signals de-asserted. Keep tx_digitalreset signal asserted and transmits static `0x0` data.
3		Enable unused non-bonded transmit channel	Instantiate dummy **Transmit Only** channel in non-bonded mode on every transmit channel that will be enabled later. Share existing active clock resources (CMU PLL or fPLL and input reference clock) if available. Leave transmitter `tx_analogreset` or pll_powerdown signals de-asserted.
4		Enable unused CMU PLL or fPLL for bonding	Instantiate dummy **Transmit Only** channel in bonded mode with source PLL assigned to the CMU PLL or fPLL that will be enabled later for bonded configurations. Leave transmitter `tx_analogreset` or `pll_powerdown` signals de-asserted.

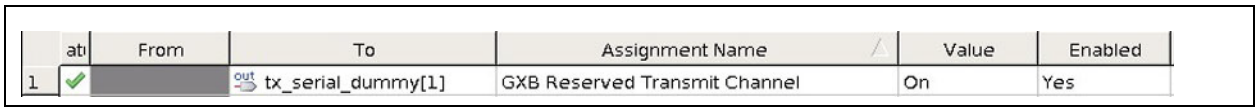
The dummy **Transmit Only** channel will increase transceiver power consumption in your design. Use the Early Power Estimator (EPE) tool or PowerPlay Power Analyzer (PPPA) in the Quartus II software to account for the power increase from the additional dummy channels.

Use the following general guidelines for reducing power consumed by the dummy **Transmit Only** channel:

1. In Arria V GT devices, instantiate the dummy channel in PMA direct mode with Native PHY IP.
2. In Arria V GX devices, keep the `tx_digitalreset` signal asserted in dummy channel to minimize PCS activity.
3. Transmit the static `0x0` data over dummy channel.
4. Configure the dummy channel with the lowest possible data rate.
5. Set the VOD = 6 (minimum value) on the transmitter output pin for dummy channel.
6. From the Quartus II software version 12.1 Service Pack 1 onwards, set **GXB Reserved Transmit Channel** assignment to **ON** on the transmitter output pin for the dummy channel using the Assignment Editor tool. This assignment powers down unnecessary blocks within the dummy channel to reduce power consumption.

Figure 3 shows an example assignment with the Assignment Editor tool.

Figure 3. Example Assignment with the Assignment Editor Tool



Example assignment with QSF:

- `set_instance_assignment` -name GXB_RESERVED_TRANSMIT_CHANNEL ON -to `tx_serial_dummy[1]`.

False Configuration Failure in Active Serial Multi-Device Configurations

In Active Serial (AS) multi-device configuration mode, the error checking for `CONF_DONE` release may not operate correctly. As a result, you may experience false configuration errors. The failure is indicated by the `CONF_DONE` going high, followed by the `nSTATUS` going low and reconfiguration repeatedly initiated.

Workaround

To resolve this issue, perform both of the following:

1. Disable the `CONF_DONE` error checking in AS multi-device configuration mode:
   a. If you are using Quartus II software version 12.0 or older, check the "Disable AS mode CONF_DONE error check" option. This option can be found in the "Advanced" button, under the Convert Programming File window.
   b. If you are using Quartus II version 12.0 SP1 or later, the error checking is disabled automatically for AS multi-device configuration POF file generation.

2. Enable the INIT_DONE pin option:
   a. To ensure a successful configuration, Altera recommends that you enable the INIT_DONE optional pin for devices in the configuration chain. On the board, route out the INIT_DONE pin separately for both the master and slave devices. Monitor the INIT_DONE status for each of the devices to ensure a successful transition into User-mode.

Other configuration modes (JTAG, Fast Passive Parallel (FPP), and Passive Serial (PS) (single and multi device configurations, and AS single-device configurations) are not affected.

Document Revision History

Table 12 lists the revision history for this errata sheet.

Table 12. Document Revision History

Date	Version	Changes
October 2013	2.1	■ Updated Table 2.
October 2013	2.0	■ Added the "EMIF Maximum Frequency Specification Update" section. ■ Updated Table 1. ■ Updated the "Configuration via Protocol (CvP)" section. ■ Updated the "SEU Internal Scrubbing" section.
July 2013	1.9	■ Added the "SEU Internal Scrubbing" section. ■ Removed the "Partial Reconfiguration (PR) with Compression Feature Not Supported" section.
June 2013	1.8	■ Updated the Altera fPLL Usage Evaluation Tool package in the "Fractional PLL Phase Alignment Error" section.
May 2013	1.7	■ Added "Fractional PLL Phase Alignment Error"
May 2013	1.6	■ Updated Table 2.
April 2013	1.5	■ Added the "Bit Errors on the LVDS RX Channels Using DPA" section.
February 2013	1.4	■ Updated Table 1. ■ Removed the "Missing Delay" section.
January 2013	1.3	■ Updated the "Unused or Idle Transmitter Maximum Data Rate Degradation" section. ■ Added the "Configuration via Protocol (CvP)" section. ■ Added the "Missing Delay" section. ■ Updated the "Usermode High Icc" section. ■ Added the "Partial Reconfiguration (PR) with Compression Feature Not Supported" section. ■ Updated Table 4.
December 2012	1.2	Added the "Usermode High Icc" section.
November 2012	1.1	Added the "Unused or Idle Transmitter Maximum Data Rate Degradation" section.
October 2012	1.0	Initial release.