Errata Sheet for Cyclone V Devices

This errata sheet provides information about known issues affecting Cyclone® V devices.

Table 1 lists the specific device issues and the affected Cyclone V devices.

Table 1. Device Issues

Issue	Affected Devices	Planned Fix
"External Memory Interface (EMIF) Maximum Frequency Specification Update"	All Cyclone V, Cyclone V SoC	None
"SEU Internal Scrubbing" The SEU internal scrubbing feature has usage restrictions.	All Cyclone V	None
"Fractional PLL Phase Alignment Error" The fractional PLL (fPLL) has a silicon sensitivity that causes the static phase error to operate beyond the Quartus® II software expectation.	All Cyclone V	Refer to Table 3.
"Power Connection Recommendation for Cyclone V SoC ES Devices" For Cyclone V SoC ES devices, Altera recommends powering both the V_{CC} and V_{CC_HPS} together.	All Cyclone V ES, SX, ST, and SE	Production Devices
"Configuration via Protocol (CvP)" CvP and Autonomous HIP functionality is not supported.	All Cyclone V, except 5CGXC3, 5CSXC2, 5CSXC4	Devices that are CvP capable will begin rolling out in Q2 2013.
"Usermode High Icc" High Icc observed when entering **User** mode.	All Cyclone V	None
"False Configuration Failure in Active Serial Multi-Device Configuration x1 Mode" In Active Serial (AS) multi-device configuration x1 mode, the error checking for CONF_DONE release may not operate correctly.	Cyclone V ES – All product lines	None

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External Memory Interface (EMIF) Maximum Frequency Specification Update

To achieve timing closure, the EMIF maximum frequency specification has been updated in Table 2.

Table 2. Cyclone V EMIF Maximum Frequency Specification Update *(1)*, *(2)*

Device	Speed Grade	Memory Type	Memory Topology	Depth Expansion	Interface Type	Original Maximum Spec (MHz)	Updated Maximum Spec (MHz)
Cyclone V GX/E	-C6	DDR2	Component	2 Chip Selects	Hard Controller	400	333
Cyclone V SoC (SE/SX)	-C6	DDR2	Component	2 Chip Selects	HPS Hard Controller	400	300
	-C6	DDR3/DDR3L	Component	2 Chip Selects	HPS Hard Controller	400	367
Cyclone V SoC (SE/SX/ST)	-I7	DDR2	Component	1 Chip Select	HPS Hard Controller	400	367

Notes to Table 2:

(1) The stated performances apply to component topology only. The DIMM topology is not supported on the hard controller.

(2) For changes to other variants and slower speed grades, contact mySupport.

Solution

These maximum frequency specifications will be updated in future releases of the External Memory Interface Spec Estimator.

SEU Internal Scrubbing

The SEU internal scrubbing feature has usage restrictions. For additional information, contact mySupport.

Fractional PLL Phase Alignment Error

The fPLL has a silicon sensitivity that causes the static phase error to operate beyond the Quartus II software expectation. The frequency range and jitter performance of the fPLL meet the Cyclone V device datasheet specifications. This sensitivity is a time zero failure, which means a design affected by this issue will show failure immediately upon a given device operation over expected operating conditions or will never show the issue.

The following usage modes may be affected:

- When the fPLL is used for phase compensation. For example, applications that may use phase compensation include LVDS, board trace matching, or FPGA skew compensation, such as zero delay buffering.
- Specific IP cores that require fPLL usage
- Inter-clock domain transfers involving fPLL usage

Workarounds

Customers can implement design techniques to mitigate inter-clock domain transfers and use the Altera® tool to evaluate fPLL usage and determine if designs may be affected by this issue.

To determine if your design may be affected, use the Altera fPLL Usage Evaluation Tool.

If you believe your design is affected by this issue, please contact mySupport for further assistance.

Long-Term Fix

This issue is, or will be fixed in the silicon die revision shown below. Table 3 identifies the fixed silicon by die revision for each device.

Table 3. Fixed Silicon by Die Revision

Family	Device	Fixed Die Revision
Cyclone V GT	5CGTD9	B
	5CGTD7	C
	5CGTD5	B
Cyclone V GX	5CGXC9	B
	5CGXC7	C
	5CGXC5	B
	5CGXC4	B
	5CGXC3	B
Cyclone V E	5CEA9	B
	5CEA7	C
	5CEA5	B
	5CEA4	B
	5CEA2	B
Cyclone V ST	5CSTD6	B
	5CSTD5	B
Cyclone V SX	5CSXC6	B
	5CSXC5	B
	5CSXC4	A
	5CSXC2	A
Cyclone V SE	5CSEA6	B
	5CSEA5	B
	5CSEA4	A
	5CSEA2	A

For an explanation of the date code and revision marking format, refer to Figure 1.

Power Connection Recommendation for Cyclone V SoC ES Devices

For Cyclone V SoC ES devices, Altera recommends powering both the V_{CC} and V_{CC_HPS} together. This will ensure that the power supplies are continually monitored by the device for proper operating levels, and allow the device to trigger a reset should any power supply voltage level fall outside of normal operating conditions.

For Cyclone V SoC ES devices in which board designs power V_{CC} and V_{CC_HPS} independently, Altera does not recommend turning off V_{CC} while leaving V_{CC_HPS} powered on. If your design requires this use case, you must ensure that your power supplies are stable and remain within the device operating conditions.

Configuration via Protocol (CvP)

The fix for this issue requires a new die revision. Use the die revision character in the Date Code (printed on the top side of the device) to determine if the device supports CvP. The CvP update can only be used at Gen1 data rates.

CvP is supported if the fourth alphanumeric character from the left ("Z" in Figure 1) is equal to, or later in the alphabet than the letter in the **Revision with Fix** column of Table 4: Device and Die Revisions.

Figure 1. Altera Date Code Marking Format

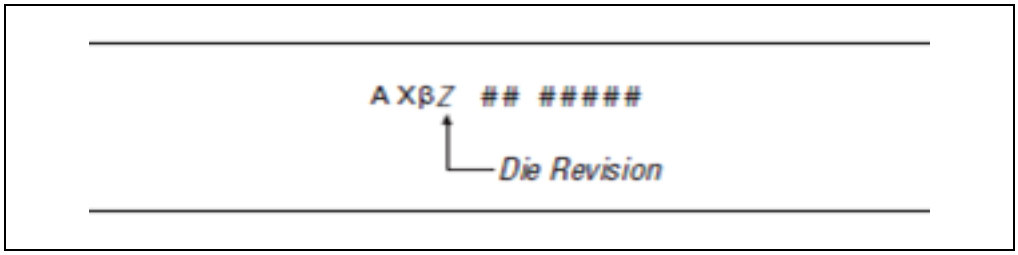

Table 4. Device and Die Revisions

Member Code	Revisions without Fix	Revision with Fix
5CGXC3	None	A
5CGXC4	A	B
5CGXC5	A	B
5CGXC7	A and B	C
5CGXC9	A	B
5CGTD5	A	B
5CGTD7	A and B	C
5CGTD9	A	B
5CSXC2	None	A
5CSXC4	None	A
5CSXC5	A	B
5CSXC6	A	B
5CSTD5	A	B

Table 4. Device and Die Revisions

Member Code	Revisions without Fix	Revision with Fix
5CSTD6	A	B

Note to Table 4:

(1) Future die revisions (not shown in Table 4) will be CvP capable.

For Gen2 CvP updates or further inquiries, please contact mySupport.

Usermode High Icc

When the affected device transitions into **User** mode, high Icc is observed, due to internal dataline contention.

Workaround

Use the following software workaround to prevent the Usermode high Icc issue:

- For the Error Detection Cyclic Redundancy Check (EDCRC) user, no workaround is needed because the EDCRC feature eliminates the high Icc issue.
- For the non-EDCRC user, a software workaround is needed and is available in the Quartus® II software version 12.1 sp1, or later.

Action Needed for Existing Designs (pre-Quartus II version 12.1 sp1)

Specific action is needed when the existing design uses the EDCRC and certain versions of the Quartus II software. Table 5 lists the actions needed for different settings.

Table 5. Action for Existing Designs

Design	Quartus II Version	Action
EDCRC enabled.	Any	None needed.
EDCRC disabled.	12.1 only	Full recompilation is required using the Quartus II software version 12.1 sp1, or later release.
	Pre-12.1	Full recompilation is NOT needed, but requires the use of Quartus II software version 12.1 sp1, or later for programming file conversion. *(1)*

Note to Table 5:

(1) Convert the existing SOF file to RBF, POF, JIC, or another format using **Convert Programming File**, under the **File** menu of the Quartus II software.

False Configuration Failure in Active Serial Multi-Device Configuration x1 Mode

In Active Serial (AS) multi-device configuration x1 mode, the error checking for CONF_DONE release may not operate correctly. Because of this, false configuration errors may result. The failure is indicated by CONF_DONE going high followed by nSTATUS going low and reconfiguration repeatedly initiated.

Workaround

To overcome this issue, perform the following steps:

1. Disable the CONF_DONE error checking in AS multi-device configuration mode:
   a. If you are using Quartus II version 12.0 software or older, check the "Disable AS mode CONF_DONE error check" option. This option can be found in the "Advanced" button under the Convert Programming File window.
   b. If you are using Quartus II version 12.0 SP1 or later, the error checking is disabled automatically for AS multi-device configuration POF file generation.
2. Enable the INIT_DONE pin option:
   a. To ensure successful configuration, Altera recommends that you enable the INIT_DONE optional pin for devices in the configuration chain. On the board, do not tie INIT_DONE pins together between master and slave devices. Monitor the INIT_DONE status for each device to ensure a successful transition into user-mode.

☞ Other configuration modes (JTAG, Fast Passive Parallel (FPP), Passive Serial (PS) single and multi device configuration, and AS single device configuration) are not affected.

Document Revision History

Table 6 lists the revision history for this errata sheet.

Table 6. Document Revision History

Date	Version	Changes
October 2013	2.0	Updated Table 2, Note 1 of the "External Memory Interface (EMIF) Maximum Frequency Specification Update"section.
October 2013	1.9	■ Added the "External Memory Interface (EMIF) Maximum Frequency Specification Update" section. ■ Updated the "SEU Internal Scrubbing" section. ■ Updated the "Configuration via Protocol (CvP)" section.
June 2013	1.8	Added the "SEU Internal Scrubbing Feature Not Supported" section.
June 2013	1.7	Updated the Altera fPLL Usage Evaluation Tool package in the "Fractional PLL Phase Alignment Error" section.
May 2013	1.6	Added the "Fractional PLL Phase Alignment Error" section.
April 2013	1.5	Updated Table 1 for the "Power Connection Recommendation for Cyclone V SoC ES Devices" section.
February 2013	1.4	Added the "Power Connection Recommendation for Cyclone V SoC ES Devices" section.
February 2013	1.3	Added the "Configuration via Protocol (CvP)" section.
January 2013	1.2	Updated the "Usermode High Icc" section and updated Table 2.
November 2012	1.1	Added the "Usermode High Icc" section.
July 2012	1.0	Initial release.