Data Sheet | December 16, 2008 | FN6820.0

## High-Speed USB 2.0 (480Mbps) Multiplexer

The Intersil ISL54221 is a single supply dual 2:1 multiplexer that can operate from a single 2.7V to 5.5V supply. It contains two SPDT (Single Pole/Double Throw) switches configured as a DPDT. The part was designed for switching or routing of USB High-Speed signals and/or USB Full-speed signals in portable battery powered products.

The 6.7Ω switches can swing rail to rail and were specifically designed to pass USB full-speed data signals that range from 0V to 3.3V and USB high-speed data signals that range from 0V to 400mV. They have high bandwidth and low capacitance to pass USB high-speed data signals with minimal distortion.

The part can be used in Personal Media Players and other portable battery powered devices that need to route USB high-speed signals or full-speed signals to different transceiver sections of the device while connected to a single USB host (computer).

The digital logic inputs are 1.8V logic compatible when operated with a 2.7V to 3.6V supply. The ISL54221 has an output enable pin to open all the switches. It can be used to facilitate proper bus disconnect and connection when switching between the USB sources.

The ISL54221 is available in a tiny 10 Ld 2.1mmx1.6mm µTQFN package. It operates over a temperature range of -40 to +85°C.

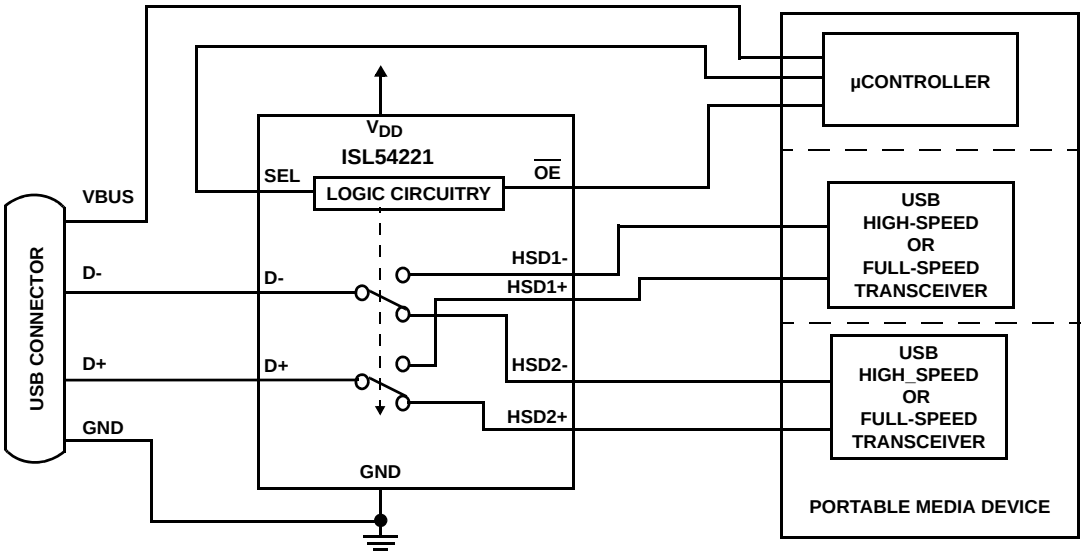
## Features

- High-Speed (480Mbps) and Full-Speed (12Mbps) Signaling Capability per USB 2.0
- 1.8V Logic Compatible (2.7V to +3.6V supply)
- Enable Pin to Open all Switches
- Power OFF Protection
- D-/D+ Pins Overvoltage Tolerant to 5.5V
- -3dB Frequency . . . . . 742MHz
- Low ON Capacitance . . . . . 7.4pF
- Low ON-Resistance . . . . . 6.7Ω
- Single Supply Operation ($V_{DD}$) . . . . . 2.7V to 5.5V
- Available in µTQFN Package
- Pb-Free (RoHS Compliant)
- Compliant with USB 2.0 Short Circuit and Overvoltage Requirements Without Additional External Components

## Applications

- MP3 and other Personal Media Players
- Cellular/Mobile Phones
- PDA's
- Digital Cameras and Camcorders
- USB Switching

## Application Block Diagram






CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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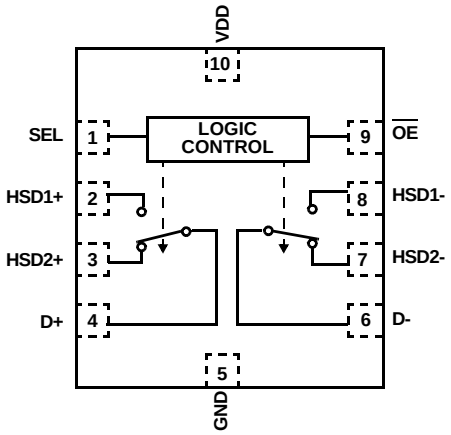
## Pinout

**ISL54221**
**10 LD 2.1 X 1.6 µTQFN**
TOP VIEW




NOTE:

1. Switches Shown for SEL = Logic “1” and $\overline{OE}$ = Logic “0”.

## Truth Table

| $\overline{OE}$ | SEL | HSD1-, HSD1+ | HSD2-, HSD2+ |
|---|---|---|---|
| 0 | 0 | ON | OFF |
| 0 | 1 | OFF | ON |
| 1 | X | OFF | OFF |

Logic “0” when ≤ 0.5V, Logic “1” when ≥ 1.4V with a 2.7V to 3.6V Supply.

## Pin Descriptions

| PIN NAME | DESCRIPTION |
|---|---|
| VDD | Power Supply |
| GND | Ground Connection |
| SEL | Select Logic Control Input |
| $\overline{OE}$ | Bus Switch Enable |
| D+, D-, HSDx+, HSDx- | USB Data Port |

## Ordering Information

| PART NUMBER (Note) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL54221IRUZ-T* | GL | -40 to +85 | 10 Ld 2.1x1.6mm µTQFN (Tape and Reel) | L10.2.1x1.6A |

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Absolute Maximum Ratings

VDD to GND . . . . . -0.3 to 6.5V
Input Voltages
HSD2x, HSD1x (Note 2). . . . . -0.3V to 6.5V
SEL, $\overline{OE}$ (Note 2) . . . . . -0.3 to (($V_{DD}$) + 0.3V)
Output Voltages
D+, D- (Note 2). . . . . -0.3V to 6.5V
Continuous Current (HSD2x, HSD1x) . . . . . ±40mA
Peak Current (HSD2x, HSD1x)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
Human Body Model . . . . . >6kV
Machine Model. . . . . >500V
Charged Device Model. . . . . >2kV

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ (°C/W) |
|---|---|
| 10 Ld µTQFN Package | 155 |

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C

## Operating Conditions

Temperature Range. . . . . -40°C to +85°C
$V_{DD}$ Supply Voltage Range. . . . . 2.7V to 5.5V
Logic Control Input Voltage . . . . . 0V to $V_{DD}$
Analog Signal Range. . . . . 0V to $V_{DD}$

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

2. Signals on HSD1x, HSD2x, D+,D- exceeding GND by specified amount are clamped. Signals on $\overline{OE}$ and SEL exceeding $V_{DD}$ or GND by specified amount are clamped. Limit current to maximum current ratings.
3. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications - 2.7V to 5.5V Supply

Test Conditions: $V_{DD}$ = +3.3V, GND = 0V, $V_{SELH}$ = 1.4V, $V_{SELL}$ = 0.5V, $V_{\overline{OE}H}$ = 1.4V, $V_{\overline{OE}L}$ = 0.5V, (Note 4), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 5, 6) | TYP | MAX (Notes 5, 6) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | $V_{DD}$ = $V_{DD}$, SEL = 0V or $V_{DD}$, $\overline{OE}$ = 0V | Full | 0 | - | $V_{DD}$ | V |
| ON-Resistance, $r_{ON}$ (High-Speed) | $V_{DD}$ = 2.7V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, $I_{Dx}$ = 40mA, $V_{HSD1x}$ or $V_{HSD2\,x}$ = 0V to 400mV (see Figure 3, Note 9) | 25 | - | 6.7 | 8 | Ω |
| | | Full | - | - | 10 | Ω |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$ (High-Speed) | $V_{DD}$ = 2.7V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, $I_{Dx}$ = 40mA, V $V_{HSD1x}$ or $V_{HSD2\,x}$ = Voltage at max $r_{ON}$, (Notes 8, 9) | 25 | - | 0.117 | 0.45 | Ω |
| | | Full | - | - | 0.55 | Ω |
| $r_{ON}$ Flatness, $R_{FLAT(ON)}$ (High-Speed) | $V_{DD}$ = 2.7V, SEL = 0.5V or 1.4V, $\overline{OE}$ = 0.5V, $I_{Dx}$ = 40mA, $V_{HSD1x}$ or $V_{HSD2\,x}$ = 0V to 400mV, (Notes 7, 9) | 25 | - | 0.94 | 1.2 | Ω |
| | | Full | - | - | 1.3 | Ω |
| OFF Leakage Current, $I_{HSD1x(OFF)}$ | $V_{DD}$ = 5.5V, SEL = $V_{DD}$ and $\overline{OE}$ = 0V or $\overline{OE}$ = $V_{DD}$, $V_{Dx}$ = 0.3V, 3.3V, $V_{HSD1X}$ = 3.3V, 0.3V, $V_{HSD2x}$ = 0.3V, 3.3V | 25 | -15 | 0.31 | 15 | nA |
| | | Full | -20 | - | 20 | nA |
| ON Leakage Current, $I_{HSD1x(ON)}$ | $V_{DD}$ = 5.5V, SEL = $\overline{OE}$ = 0V, $V_{Dx}$ = 0.3V, 3.3V, $V_{HSD1X}$ = 0.3V, 3.3V, $V_{HSD2x}$ = 3.3V, 0.3V | 25 | -20 | 2.2 | 20 | nA |
| | | Full | -25 | - | 25 | nA |
| OFF Leakage Current, $I_{HSD2x(OFF)}$ | $V_{DD}$ = 5.5V, SEL = $\overline{OE}$ = 0V or $\overline{OE}$ = $V_{DD}$, $V_{Dx}$ = 3.3V, 0.3V, $V_{HSD2x}$ = 0.3V, 3.3V, $V_{HSD1X}$ = 3.3V, 0.3V | 25 | -15 | 0.26 | 15 | nA |
| | | Full | -20 | - | 20 | nA |
| ON Leakage Current, $I_{HSD2x(ON)}$ | $V_{DD}$ = 5.5V, SEL = $V_{DD}$, $\overline{OE}$ = 0V, $V_{Dx}$= 0.3V, 3.3V, $V_{HSD2x}$ = 0.3V, 3.3V, $V_{HSD1X}$ = 3.3V, 0.3V | 25 | -20 | 2.1 | 20 | nA |
| | | Full | -25 | - | 25 | nA |
| Power OFF Leakage Current, $I_{D+}$, $I_{D-}$ | $V_{DD}$ = 0V, $V_{D+}$ = 0V to 5.25V, $V_{D-}$= 0V to 5.25V, SEL = $\overline{OE}$ = $V_{DD}$ | 25 | - | 0.0047 | 0.025 | µA |
| | | Full | - | - | 0.40 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | $V_{DD}$ = 3.3V, $R_L$ = 50Ω, $C_L$ = 10pF (see Figure 1) | 25 | - | 35 | - | ns |
| Turn-OFF Time, $t_{OFF}$ | $V_{DD}$ = 3.3V, $R_L$ = 50Ω, $C_L$ = 10pF (see Figure 1) | 25 | - | 27 | - | ns |
| Break-Before-Make Time Delay, $t_D$ | $V_{DD}$ = 3.3V, $R_L$ = 50Ω, $C_L$ = 10pF (see Figure 2) | 25 | - | 10 | - | ns |

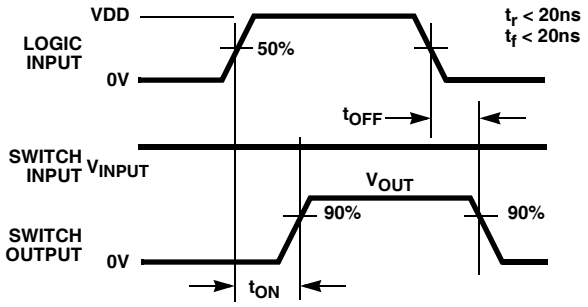
**Electrical Specifications - 2.7V to 5.5V Supply** Test Conditions: $V_{DD}$ = +3.3V, GND = 0V, $V_{SELH}$ = 1.4V, $V_{SELL}$ = 0.5V, $V_{\overline{OE}H}$ = 1.4V, $V_{\overline{OE}L}$ = 0.5V, (Note 4), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 5, 6) | TYP | MAX (Notes 5, 6) | UNITS |
|---|---|---|---|---|---|---|
| Skew, ($t_{SKEWOUT}$ - $t_{SKEWIN}$) | $V_{DD}$ = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, $R_L$ = 45Ω, $C_L$ = 10pF, $t_R$ = $t_F$ = 720ps at 480Mbps, (Duty Cycle = 50%) (see Figure 6) | 25 | - | 50 | - | ps |
| Rise/Fall Degradation (Propagation Delay), $t_{PD}$ | $V_{DD}$ = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, $R_L$ = 45Ω, $C_L$ = 10pF (see Figure 6) | 25 | - | 250 | - | ps |
| Crosstalk | $V_{DD}$ = 3.3V, $R_L$ = 50Ω, f = 240MHz (see Figure 5) | 25 | - | -36 | - | dB |
| OFF-Isolation | $V_{DD}$ = 3.3V, $\overline{OE}$ = 3.3V, $R_L$ = 50Ω, f = 240MHz | 25 | - | -32 | - | dB |
| -3dB Bandwidth | Signal = 0dBm, 0.2Vdc offset, $R_L$ = 50Ω | 25 | - | 742 | - | MHz |
| OFF Capacitance, $C_{HSxOFF}$ | f = 1MHz, $V_{DD}$ = 3.3V, SEL = 0V, $\overline{OE}$ = 3.3V, $V_{HSD1x}$ or $V_{HSD2x}$ = $V_{Dx}$ = 0V (see Figure 4) | 25 | - | 2.8 | - | pF |
| COM ON Capacitance, $C_{DX(ON)}$ | f = 1MHz, $V_{DD}$ = 3.3V, SEL = 0V or 3.3V, $\overline{OE}$ = 0V, $V_{HSD1x}$ or $V_{HSD2x}$ = $V_{Dx}$ = 0V (see Figure 4) | 25 | - | 7.4 | - | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range, $V_{DD}$ | | Full | 2.7 | | 5.5 | V |
| Positive Supply Current, $I_{DD}$ | $V_{DD}$ = 5.5V, SEL = 0V or $V_{DD}$, $\overline{OE}$ = 0V or $V_{DD}$ | 25 | - | 0.009 | 0.03 | µA |
| | | Full | - | - | 1 | µA |
| Positive Supply Current, $I_{DD}$ | $V_{DD}$ = 4.3V, SEL = 2.6V, $\overline{OE}$ = 0V or 2.6V | 25 | - | 0.159 | 0.6 | µA |
| | | Full | - | - | 1.6 | µA |
| Positive Supply Current, $I_{DD}$ | $V_{DD}$ = 3.6V, SEL = 1.4V, $\overline{OE}$ = 0V or 1.4V | 25 | - | 6.6 | 10 | µA |
| | | Full | - | - | 12 | µA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage Low, $V_{SELL}$, $V_{\overline{OE}L}$ | $V_{DD}$ = 2.7V to 3.6V | Full | - | - | 0.5 | V |
| Input Voltage High, $V_{SELH}$, $V_{\overline{OE}H}$ | $V_{DD}$ = 2.7V to 3.6V | Full | 1.4 | - | - | V |
| Input Voltage Low, $V_{SELL}$, $V_{\overline{OE}L}$ | $V_{DD}$ = 4.3V to 5.5V | Full | - | - | 0.8 | V |
| Input Voltage High, $V_{SELH}$, $V_{\overline{OE}H}$ | $V_{DD}$ = 4.3V to 5.5V | Full | 2.0 | - | - | V |
| Input Current, $I_{SELL}$, $I_{\overline{OE}L}$ | $V_{DD}$ = 5.5V, SEL = 0V, $\overline{OE}$ = 0V | Full | - | 3.3 | - | nA |
| Input Current, $I_{SELH}$ | $V_{DD}$ = 5.5V, SEL = 5.5V | Full | - | -3.6 | - | nA |
| Input Current, $I_{\overline{OE}H}$ | $V_{DD}$ = 5.5V, $\overline{OE}$ = 5.5V | Full | - | -8.2 | - | nA |

NOTES:

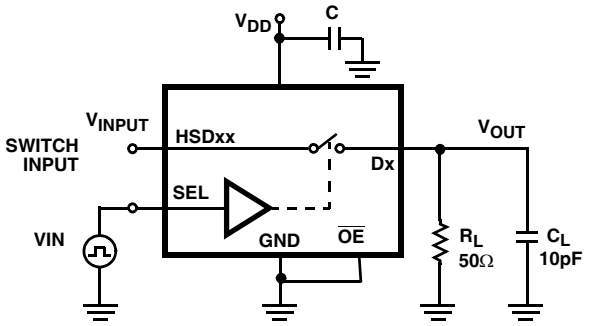
4. $V_{LOGIC}$ = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range
8. $r_{ON}$ matching between channels is calculated by subtracting the channel with the highest max $r_{ON}$ value from the channel with lowest max $r_{ON}$ value, between HSD2+ and HSD2- or between HSD1+ and HSD1-.
9. Limits established by characterization and are not production tested.

## Test Circuits and Waveforms




Logic input waveform is inverted for switches that have the opposite logic sense.

**FIGURE 1A. MEASUREMENT POINTS**




Repeat test for all switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

**FIGURE 1B. TEST CIRCUIT**

**FIGURE 1. SWITCHING TIMES**

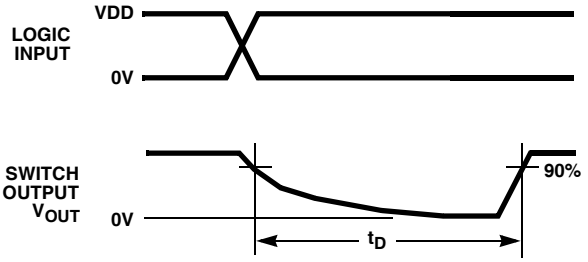
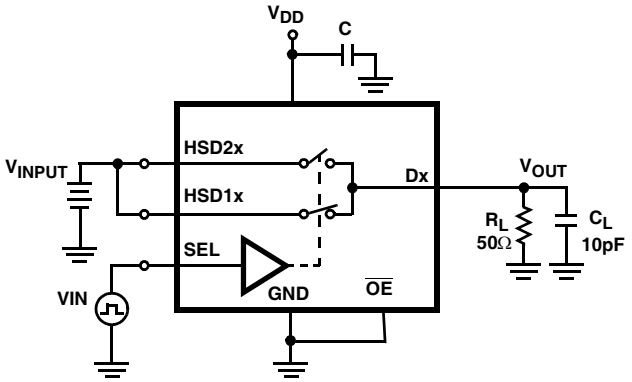


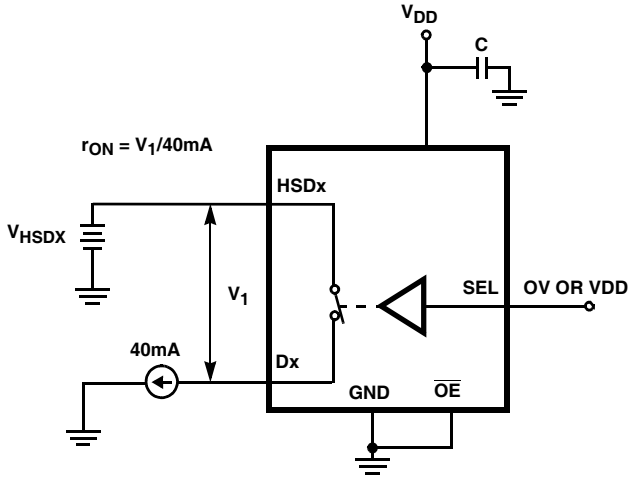

**FIGURE 2A. MEASUREMENT POINTS**




Repeat test for all switches. $C_L$ includes fixture and stray capacitance.

**FIGURE 2B. TEST CIRCUIT**

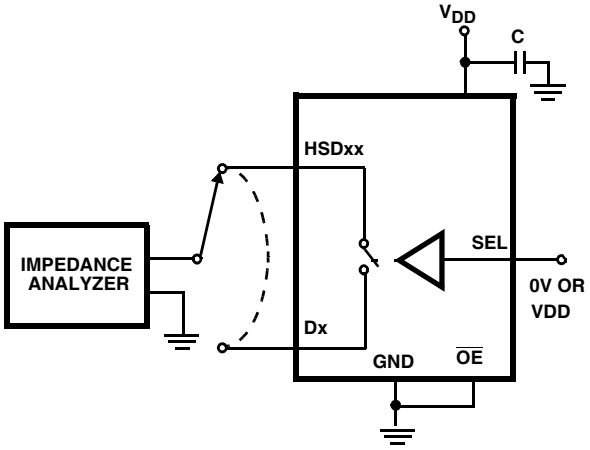
**FIGURE 2. BREAK-BEFORE-MAKE TIME**




**Repeat test for all switches.**

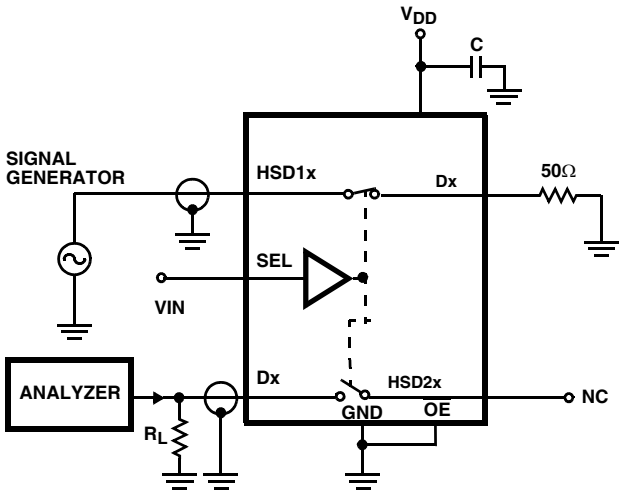
**FIGURE 3. $r_{ON}$ TEST CIRCUIT**

## Test Circuits and Waveforms (Continued)




Repeat test for all switches.

FIGURE 4. CAPACITANCE TEST CIRCUIT




Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 5. CROSSTALK TEST CIRCUIT

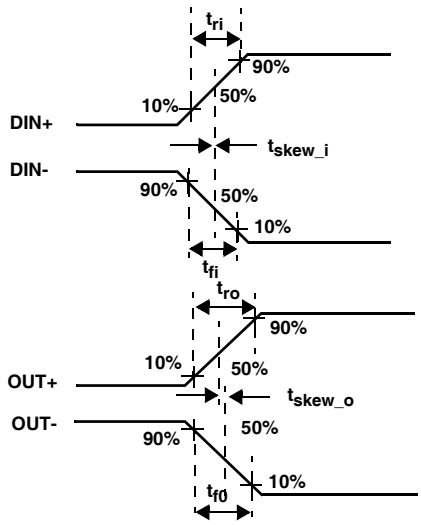
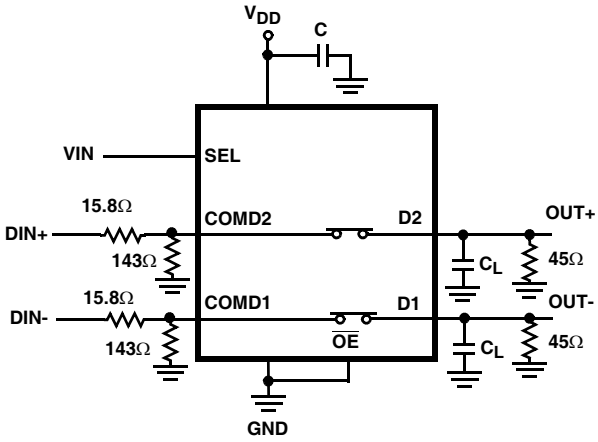



FIGURE 6A. MEASUREMENT POINTS




|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals

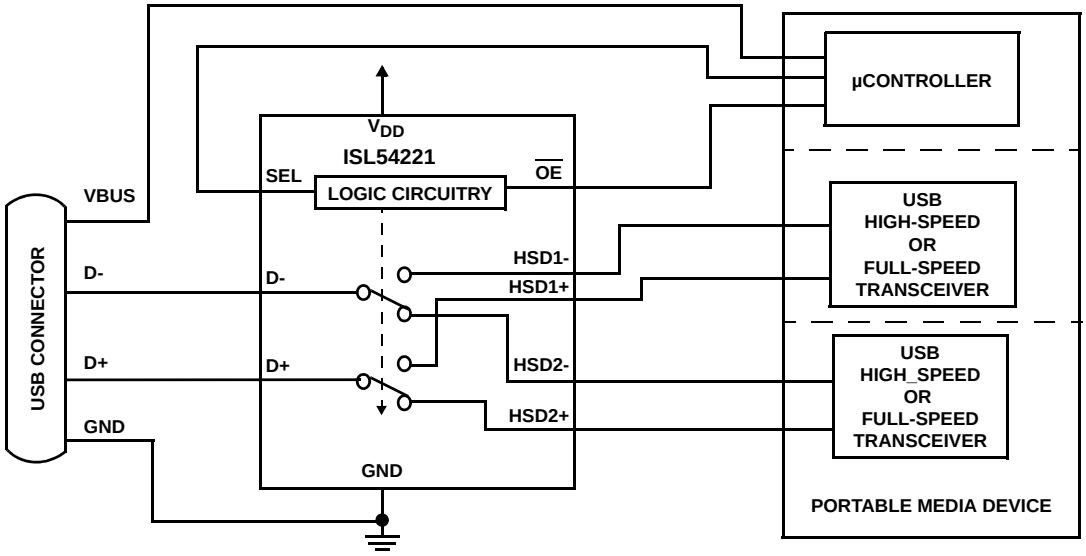
|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 6B. TEST CIRCUIT

FIGURE 6. SKEW TEST

## Application Block Diagram




## Detailed Description

The ISL54221 device is a dual single pole/double throw (SPDT) analog switch configured as a DPDT that operates from a single DC power supply in the range of 2.7V to 5.5V.

It was designed to function as a dual 2-to-1 multiplexer to select between two USB high-speed differential data signals in portable battery powered products. It is offered in a small µTQFN package for use in MP3 players, cameras, PDAs, cellphones, and other personal media players. The device has an enable pin to open all switches.

The part consists of four 6Ω high-speed (HSx) switches. These switches have high bandwidth and low capacitance to pass USB high-speed (480Mbps) differential data signals with minimal edge and phase distortion. They can also swing from 0V to $V_{DD}$ to pass USB full-speed (12Mbps) differential data signals with minimal distortion.

The ISL54221 was designed for MP3 players, cameras, cellphones, and other personal media player applications that have multiple high-speed or full-speed transceivers sections and need to multiplex between these USB sources to a single USB host (computer). A typical application block diagram of this functionality is shown on page 7.

A detailed description of the HS switches is provided in the following section.

### High-Speed (HSx) Switches

The HSx switches (HSD1-, HSD1+, HSD2-, HSD2+) are bi-directional switches that can pass rail-to-rail signals. When powered with a 3.3V supply, these switches have a nominal $r_{ON}$ of 6Ω over the signal range of 0V to 400mV with a $r_{ON}$ flatness of 0.94Ω. The $r_{ON}$ matching between the HSD1 and HSD2 switches over this signal range is only 0.12Ω, ensuring minimal impact by the switches to USB high-speed signal transitions. As the signal level increases, the $r_{ON}$ switch resistance increases. At signal level of 3.3V, the switch resistance is nominally 129Ω. See Figures 7, 8, 9 and 10 in the “Typical Performance Curves” on page 9.

The HSx switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high-speed signal quality specifications. See Figure 11 in the “Typical Performance Curves” on page 10 for USB High-speed Eye Pattern taken with switch in the signal path.

The HSx switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See Figure 12 in the “Typical Performance Curves” on page 11 for the USB Full-speed Eye Pattern taken with switch in the signal path.

The maximum normal operating signal range for the HSx switches is from 0V to $V_{DD}$. The signal voltage should not be allow to exceed the $V_{DD}$ voltage rail or go below ground by more than 0.3V for normal operation.

However in the event that the USB 5.25V $V_{BUS}$ voltage gets shorted to one or both of the D-/D+ pins, the ISL54221 has special fault protection circuitry to prevent damage to the ISL54221 part. The fault circuitry allows the signal pins (D-, D+, HS1D-, HS1D+, HS2D-, HS2D+) to be driven up to 5.5V while the $V_{DD}$ supply voltage is in the range of 0V to 5.5V. In this condition the part draws < 500µA of current and causes no stress to the IC. In addition when $V_{DD}$ is at 0V (ground)

all switches are OFF and the fault voltage is isolated from the other side of the switch. When $V_{DD}$ is in the range of 2.7V to 5.5V the fault voltage will pass through to the output of an active switch channel.

The HS1 channel switches are active (turned ON) whenever the SEL voltage is logic"0"(Low) and the $\overline{OE}$ voltage is logic"0"(Low).

The HS2 channel switches are active (turned ON) whenever the SEL voltage is logic "1" (High) and the $\overline{OE}$ voltage is logic "0" (Low).

## *ISL54221 Operation*

The following will discuss using the ISL54221 the "Application Block Diagram" on page 7.

### POWER

The power supply connected at the VDD pin provides the DC bias voltage required by the ISL54221 part for proper operation. The ISL54221 can be operated with a $V_{DD}$ voltage in the range of 2.7V to 5.5V. When used in a USB application, the $V_{DD}$ voltage should be kept in the range of 3.0V to 5.5V to ensure you get the proper signal levels for good signal quality.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the VDD pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the VDD pin as possible.

In a typical application, $V_{DD}$ will be in the range of 2.8V to 4.3V and will be connected to the battery or LDO of the portable media device.

### LOGIC CONTROL

The state of the ISL54221 device is determined by the voltage at the SEL pin and the $\overline{OE}$ pin. SEL is only active when the $\overline{OE}$ pin is logic "0" (Low). Refer to "Truth Table" on page 2.

The ISL54221 logic pins are designed to minimize current consumption when the logic control voltage is lower than the $V_{DD}$ supply voltage. With $V_{DD}$ = 3.6V and logic pins at 1.4V the part typically draws only 6.6µA. With $V_{DD}$ = 4.3V and logic pins at 2.6V the part typically draws only 0.2µA. Driving the logic pins to the $V_{DD}$ supply rail minimizes power consumption.

The logic pins must be held High or Low and must not float.

#### Logic Control Voltage Levels

With $V_{DD}$ supply voltage in the range of 2.7V to 3.6V the logic levels are:

$\overline{OE}$ = Logic "0" (Low) when $V_{\overline{OE}} \leq 0.5V$
$\overline{OE}$ = Logic "1" (High) when $V_{\overline{OE}} \geq 1.4V$
SEL = Logic "0" (Low) when $V_{SEL} \leq 0.5V$
SEL = Logic "1" (High) when $V_{SEL} \geq 1.4V$

With $V_{DD}$ supply voltage in the range of 4.3V to 5.5V the logic levels are:

$\overline{OE}$ = Logic "0" (Low) when $V_{\overline{OE}} \leq 0.8V$
$\overline{OE}$ = Logic "1" (High) when $V_{\overline{OE}} \geq 2.0V$
SEL = Logic "0" (Low) when $V_{SEL} \leq 0.8V$
SEL = Logic "1" (High) when $V_{SEL} \geq 2.0V$

#### HSD1 USB Channel

If the SEL pin = Logic "0" and the $\overline{OE}$ pin = Logic "0", high-speed Channel 1 will be ON. The HSD1- and HSD1+ switches are ON and the HSD2- and HSD2+ switches are OFF (high impedance).

When a computer or USB hub is plugged into the common USB connector and channel one is active, a link will be established between the USB 1 driver section of the media player and the computer. The device will be able to transmit and receive data from the computer at a data rate of 480Mbps.

#### HSD2 USB Channel

If the SEL pin = Logic "1" and the $\overline{OE}$ pin = Logic "0", high-speed Channel 2 will be ON. The HSD2- and HSD2+ switches are ON and the HSD1- and HSD1+ switches are OFF (high impedance).

When a USB cable from a computer or USB hub is connected at the common USB connector and the part has Channel 2 active, a link will be established between the USB 2 driver section of the media player and the computer. The device will be able to transmit and receive data from the computer at a data rate of 480Mbps.

#### All Switches OFF Mode

If the SEL pin = Logic "0" or Logic "1" and the $\overline{OE}$ pin = Logic "1", all of the switches will turn OFF (high impedance).

The all OFF state can be used to switch between the two USB sections of the media player. When disconnecting from one USB device to the other USB device, you can momentarily put the ISL54221 switch in the "all off" state in order to get the computer to disconnect from the one device so it can properly connect to the other USB device when that channel is turned ON.

## *USB 2.0 $V_{BUS}$ Short Requirements*

The USB specification in section 7.1.1 states a USB device must be able to withstand a $V_{BUS}$ short to the D+ or D- signal lines when the device is either powered off or powered on for at least 24 hours. The ISL54220 part has special fault protection circuitry to meet these short circuit requirements.

The fault protection circuitry allows the signal pins (D-, D+, HS1D-, HS1D+, HS2D-, HS2D+) to be driven up to 5.5V while the $V_{DD}$ supply voltage is in the range of 0V to 5.5V. In this overvoltage condition the part draws < 500µA of current and causes no stress/damage to the IC.

In addition when $V_{DD}$ is at 0V (ground) all switches are OFF and the shorted $V_{BUS}$ voltage is isolated from the other side of the switch. When $V_{DD}$ is in the range of 2.7V to 5.5V the shorted $V_{BUS}$ voltage will pass through to the output of an active (turned ON) switch channel but not through a turned OFF channel. Any components connected on the active channel must be able to withstand the overvoltage condition.

Note: During the fault condition normal operation of the USB channel is not guaranteed until the fault condition is removed.

## *Typical Performance Curves* $T_A$ = +25°C, Unless Otherwise Specified

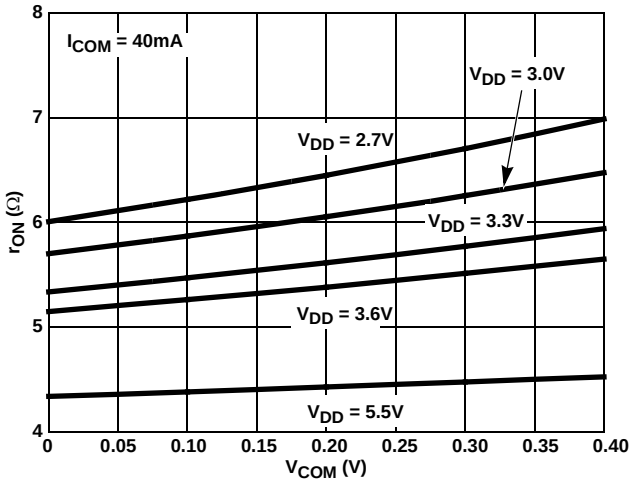



**FIGURE 7. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE**

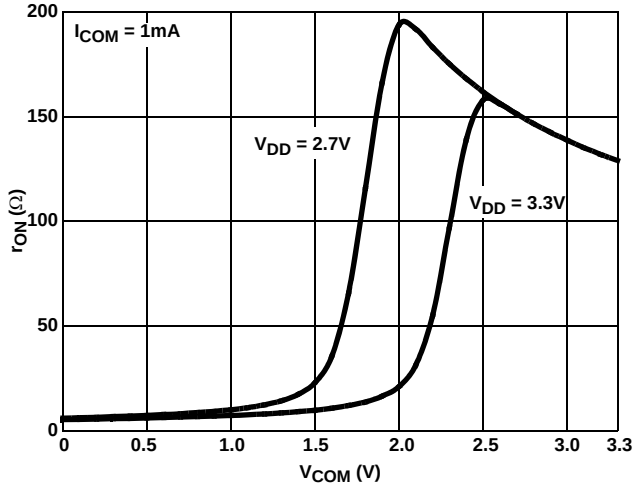



**FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE**

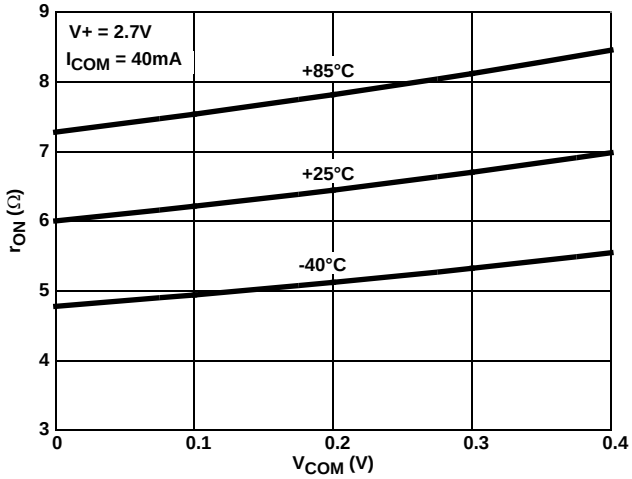



**FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE**

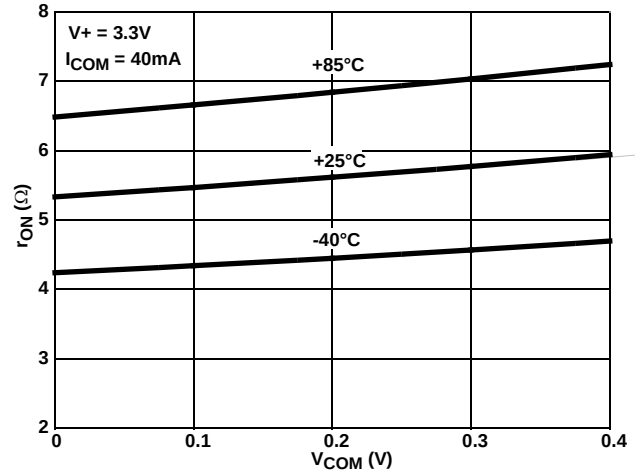



**FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE**

## Typical Performance Curves $T_A$ = +25°C, Unless Otherwise Specified **(Continued)**

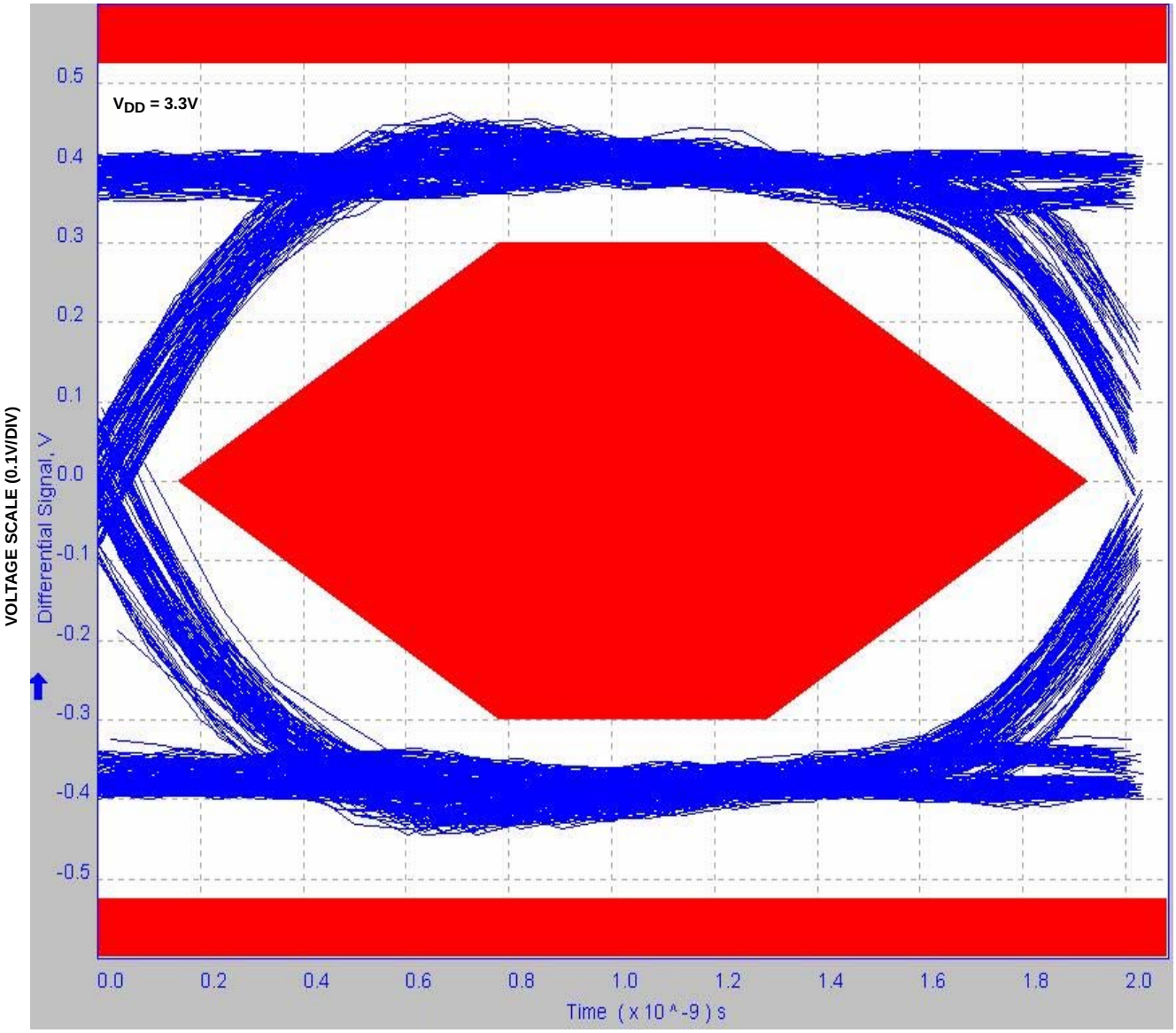



**FIGURE 11. EYE PATTERN: 480Mbps WITH SWITCHES IN THE SIGNAL PATH**

## Typical Performance Curves $T_A$ = +25°C, Unless Otherwise Specified **(Continued)**

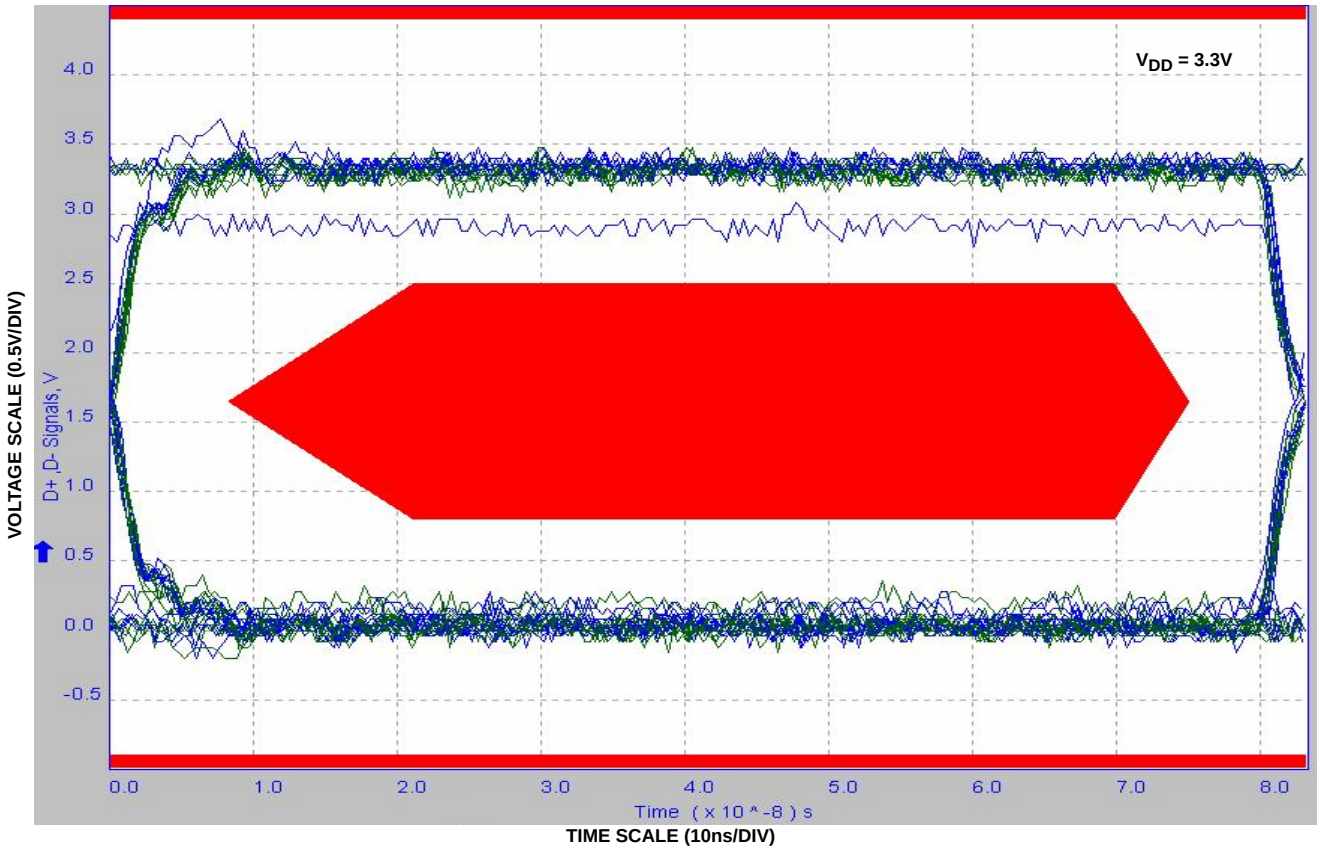



**FIGURE 12. EYE PATTERN: 12Mbps WITH SWITCHES IN THE SIGNAL PATH**

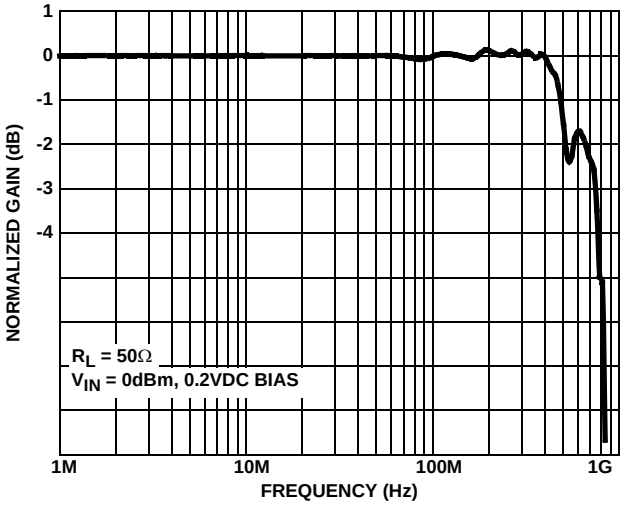



**FIGURE 13. FREQUENCY RESPONSE**

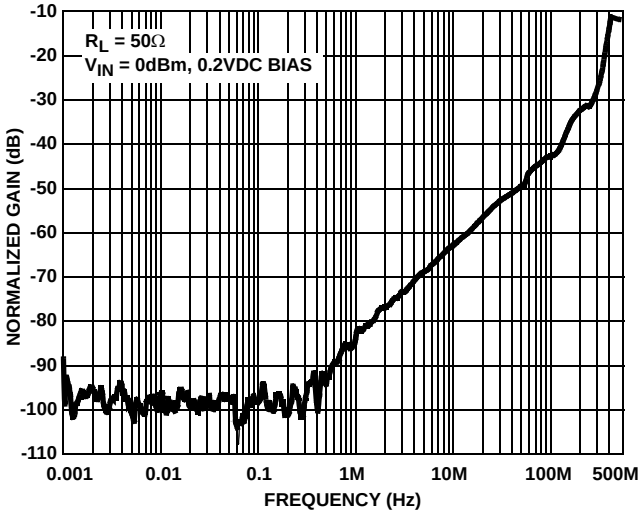



**FIGURE 14. OFF-ISOLATION**

## Typical Performance Curves $T_A$ = +25°C, Unless Otherwise Specified **(Continued)**

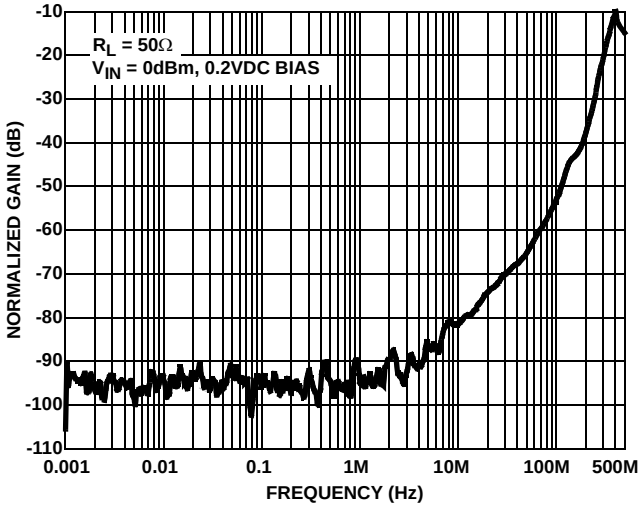



**FIGURE 15. CROSSTALK**

## Die Characteristics

**SUBSTRATE POTENTIAL (POWERED UP):**

GND

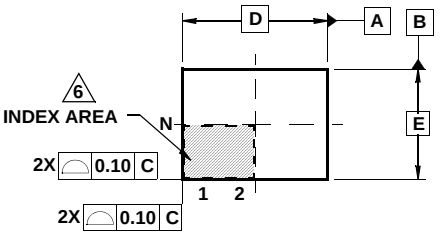
**TRANSISTOR COUNT:**

325

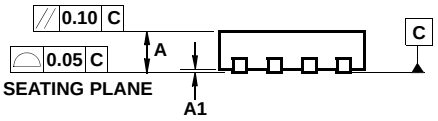
**PROCESS:**

Submicron CMOS

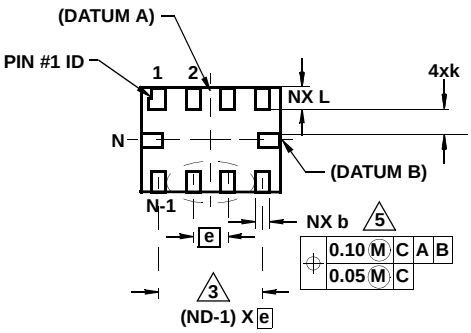
## Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



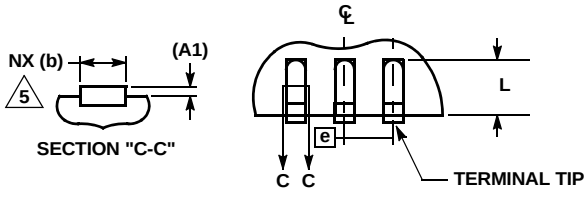

TOP VIEW



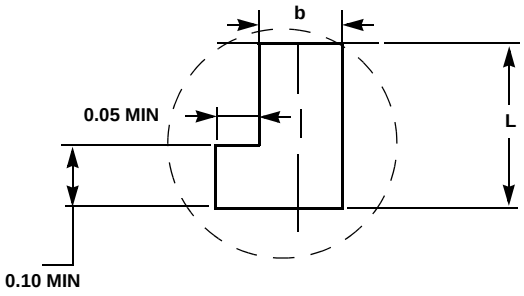

SIDE VIEW




BOTTOM VIEW




FOR ODD TERMINAL/SIDE




DETAIL "A" PIN 1 ID

### L10.2.1x1.6A

**10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**

| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | 0.45 | 0.50 | 0.55 | - |
| A1 | - | - | 0.05 | - |
| A3 | | 0.127 REF | | - |
| b | 0.15 | 0.20 | 0.25 | 5 |
| D | 2.05 | 2.10 | 2.15 | - |
| E | 1.55 | 1.60 | 1.65 | - |
| e | | 0.50 BSC | | - |
| k | 0.20 | - | - | - |
| L | 0.35 | 0.40 | 0.45 | - |
| N | | 10 | | 2 |
| Nd | | 4 | | 3 |
| Ne | | 1 | | 3 |
| θ | 0 | - | 12 | 4 |

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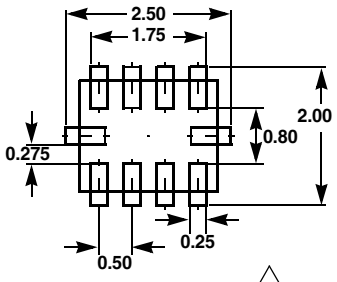
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.




LAND PATTERN 10

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