Fault Protected, Extended CMR, RS-485/RS-422 Transceivers with Cable Invert

ISL31480E, ISL31483E, ISL31485E, ISL31486E

The ISL3148xE are fault protected, 5V powered differential transceivers that exceed the RS-485 and RS-422 standards for balanced communication. The RS-485 transceiver pins (driver outputs and receiver inputs) are fault protected up to ±60V. Additionally, the extended common mode range allows these transceivers to operate in environments with common mode voltages up to ±25V (>2X the RS-485 requirement), making this fault protected RS-485 family one of the most robust on the market.

Transmitters deliver an exceptional 2.5V (typical) differential output voltage into the RS-485 specified 54Ω load. This yields better noise immunity than standard RS-485 ICs, or allows up to six 120Ω terminations in star network topologies.

Receiver (Rx) inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven (idle) bus.

The ISL31483E, ISL31485E and ISL31486E include cable invert functions that reverse the polarity of the Rx and/or Tx bus pins in case the cable is misconnected. Unlike competing devices, Rx full fail-safe operation is maintained even when the Rx input polarity is switched.

The ISL31480E and ISL31486E feature a logic supply (V_L) pin that sets the V_{OH} of the Rx outputs, and the switching points of the logic input pins, to be compatible with a lower supply voltage (down to 1.8V) in mixed voltage systems. See Table 1 on page 2 for key features and configurations by device number.

Features

- Fault Protected RS-485 Bus Pins . . . . . up to ±60V
- Extended Common Mode Range . . . . . ±25V
  More Than Twice the Range Required for RS-485
- Cable Invert Pins (Except ISL31480)
  Corrects for Reversed Cable Connections While Maintaining Rx Full Fail-safe Functionality
- Logic Supply (V_L) Pin (ISL31480E, ISL31486E)
  Simplifies Interface to Lower Voltage Logic Devices
- Full Fail-safe (Open, Short, Terminated) RS-485 Receivers
- 1/4 Unit Load (UL) for up to 128 Devices on the Bus
- High Rx I_{OL} for Opto-Couplers in Isolated Designs
- Hot Plug Circuitry - Tx and Rx Outputs Remain Three-State During Power-up/Power-down
- Slew Rate Limited RS-485 Data Rate 1Mbps
- Low Quiescent Supply Current 2.3mA
  Ultra Low Shutdown Supply Current 10µA

Applications

- Utility Meters/Automated Meter Reading Systems
- High Node Count RS-485 Systems
- PROFIBUS® and RS-485 Based Field Bus Networks, and Factory Automation
- Security Camera Networks
- Building Lighting and Environmental Control Systems
- Industrial/Process Control Networks

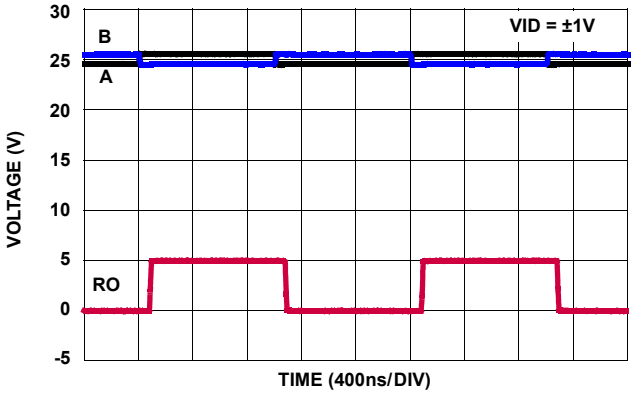


FIGURE 1. EXCEPTIONAL Rx OPERATES AT 1Mbps EVEN WITH ±25V COMMON MODE VOLTAGE

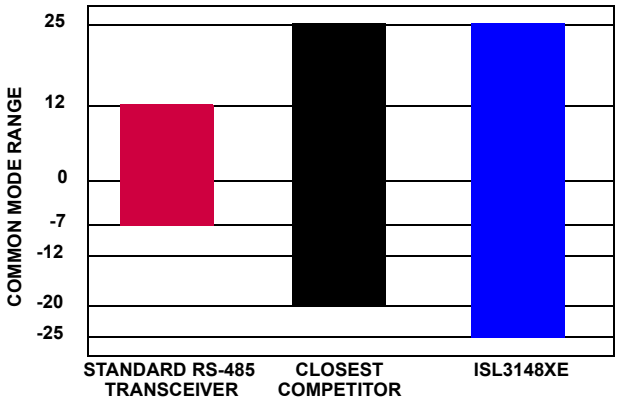


FIGURE 2. TRANSCEIVERS DELIVER SUPERIOR COMMON MODE RANGE vs. STANDARD RS-485 DEVICES

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED?	EN PINS?	HOT PLUG	V_L PIN?	POLARITY REVERSAL PINS?	QUIESCENT I_{CC} (mA)	LOW POWER SHDN?	PIN COUNT
Coming Soon ISL31480E	Half	1	Yes	Yes	Yes	Yes	No	2.3	Yes	10
ISL31483E	Full	1	Yes	Yes	Yes	No	Yes	2.3	Yes	14
ISL31485E	Half	1	Yes	Tx Only	Yes	No	Yes	2.3	No	8
Coming Soon ISL31486E	Half	1	Yes	Yes	Yes	Yes	Yes	2.3	Yes	10, 12, 14

Ordering Information

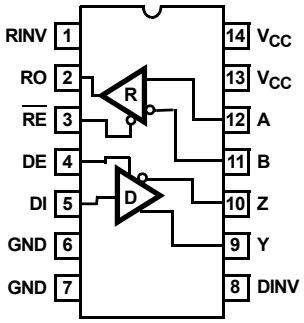
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
Coming Soon ISL31480EIRTZ	480E	-40 to +85	10 Ld TDFN	L10.3x3A
Coming Soon ISL31480EIUZ	1480E	-40 to +85	10 Ld MSOP	M10.118
ISL31483EIBZ	ISL31483 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL31485EIBZ	31485 EIBZ	-40 to +85	8 Ld SOIC	M8.15
Coming Soon ISL31486EIBZ	ISL31486 EIBZ	-40 to +85	14 Ld SOIC	M14.15
Coming Soon ISL31486EIRTZ	486E	-40 to +85	12 Ld TDFN	L12.4x3A
Coming Soon ISL31486EIUZ	1486E	-40 to +85	10 Ld MSOP	M10.118

NOTES:

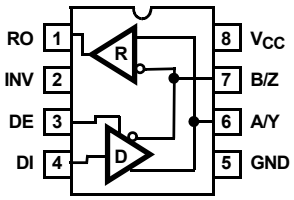
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL31480E, ISL31483E, ISL31485E, and ISL31486E. For more information on MSL please see techbrief TB363.

Pin Configurations

ISL31483E
(14 LD SOIC)
TOP VIEW



ISL31485E
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NAME	ISL31480E PIN #	ISL31483E PIN #	ISL31485E PIN #	ISL31486E (12 LD) PIN #	ISL31486E (10 LD) PIN #	ISL31486E (14 LD) PIN #	FUNCTION
RO	2	2	1	1	1	1	Receiver output. On the ISL31480E, or if INV or RINV is low, then: If A - B ≥ -10mV, RO is high; if A - B ≤ -200mV, RO is low. If INV or RINV is high, then: If B - A ≥ -10mV, RO is high; if B - A ≤ -200mV, RO is low. In all cases, RO = High if A and B are unconnected (floating), or shorted together, or connected to an undriven, terminated bus (i.e., Rx is always failsafe open, shorted, and idle, even if polarity is inverted).
$\overline{RE}$	4	3	N/A	2	2	2	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. Internally pulled low.
DE	3	4	3	4	4	4	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and they are high impedance when DE is low. Internally pulled high (to V_L on ISL31480E and ISL31486E; to V_{CC} on other versions).
DI	5	5	4	5	5	6	Driver input. On the ISL31480E, or if INV or DINV is low, a low on DI forces output Y low and output Z high, while a high on DI forces output Y high and output Z low. The output states relative to DI invert if INV or DINV is high.
GND	6	6, 7	5	7, 8	6	8, 9	Ground connection.This is also the potential of the TDFN EPAD.
A/Y	8	N/A	6	9	7	11	±60V Fault Protected RS-485/RS-422 level I/O pin. On the ISL31480E, or if INV is low, A/Y is the non-inverting receiver input and non-inverting driver output. If INV is high, A/Y is the inverting receiver input and the inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.

Pin Descriptions (Continued)

PIN NAME	ISL31480E PIN #	ISL31483E PIN #	ISL31485E PIN #	ISL31486E (12 LD) PIN #	ISL31486E (10 LD) PIN #	ISL31486E (14 LD) PIN #	FUNCTION
B/Z	9	N/A	7	10	8	12	±60V Fault Protected RS-485/RS-422 level I/O pin. On the ISL31480E, or if INV is low, B/Z is the inverting receiver input and inverting driver output. If INV is high, B/Z is the non-inverting receiver input and the non-inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	N/A	12	N/A	N/A	N/A	N/A	±60V Fault Protected RS-485/RS-422 level input. If RINV is low, then A is the non-inverting receiver input. If RINV is high, then A is the inverting receiver input.
B	N/A	11	N/A	N/A	N/A	N/A	±60V Fault Protected RS-485/RS-422 level input. If RINV is low, then B is the inverting receiver input. If RINV is high, then B is the non-inverting receiver input.
Y	N/A	9	N/A	N/A	N/A	N/A	±60V Fault Protected RS-485/RS-422 level output. If DINV is low, then Y is the non-inverting driver output. If DINV is high, then Y is the inverting driver output
Z	N/A	10	N/A	N/A	N/A	N/A	±60V Fault Protected RS-485/RS-422 level. If DINV is low, then Z is the inverting driver output. If DINV is high, then Z is the non-inverting driver output
V_{CC}	10	13, 14	8	11	9	13	System power supply input (4.5V to 5.5V).
V_L	1	N/A	N/A	12	10	14	Logic-Level Supply input (1.62V to V_{CC}) which powers all the TTL/CMOS inputs and the RO output (logic pins). V_L sets the V_{IH} and V_{IL} levels for logic input pins, and sets the V_{OH} level for the RO pin. Power up this supply after V_{CC}, and keep $V_L \leq V_{CC}$. To minimize input current, logic input pins that are strapped high externally should connect to V_L, but they may be connected to V_{CC} if necessary.
INV	N/A	N/A	2	3	3	3	Receiver and driver polarity selection input. When driven high this pin swaps the polarity of the driver output and receiver input pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.
RINV	N/A	1	N/A	N/A	N/A	N/A	Receiver polarity selection input. When driven high this pin swaps the polarity of the receiver input pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.
DINV	N/A	8	N/A	N/A	N/A	N/A	Driver polarity selection input. When driven high this pin swaps the polarity of the driver output pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.
PD	TDFN ONLY	N/A	N/A	EPAD	N/A	N/A	TDFN exposed thermal pad (EPAD). Connect to GND.
NC	7	N/A	N/A	6	N/A	5, 7, 10	No Internal Connection.

Truth Tables

TRANSMITTING					
INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	INV or DINV	Y	Z
X	1	1	0	1	0
X	1	0	0	0	1
X	1	1	1	0	1
X	1	0	1	1	0
0	0	X	X	High-Z	High-Z
1	0	X	X	High-Z*	High-Z*

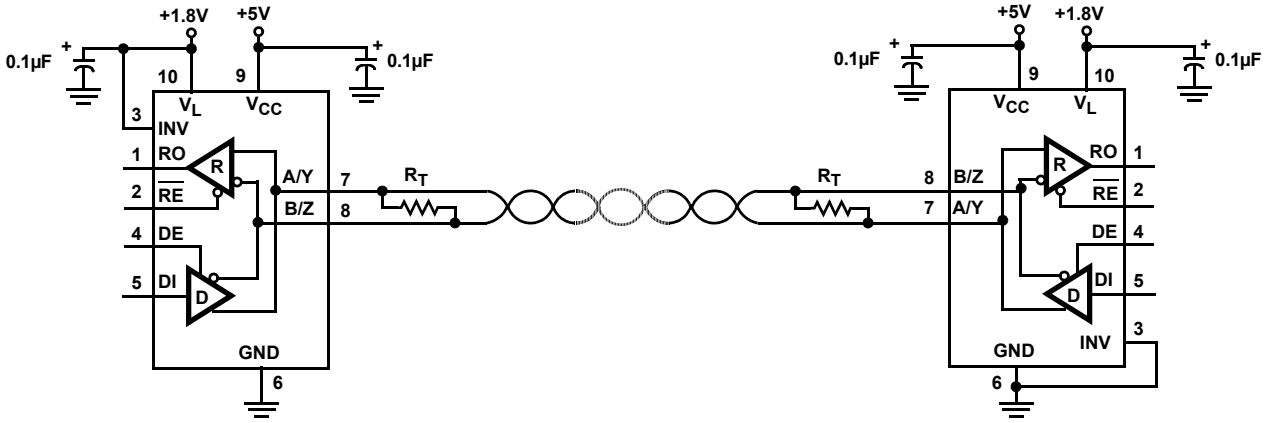
NOTE: *Low Power Shutdown Mode (See Note 13), except for ISL31485E.

RECEIVING					
INPUTS					OUTPUT
$\overline{RE}$	DE (Half Duplex)	DE (Full Duplex)	A-B	INV or RINV	RO
0	0	X	≥ -0.01V	0	1
0	0	X	≤ -0.2V	0	0
0	0	X	≤ 0.01V	1	1
0	0	X	≥ 0.2V	1	0
0	0	X	Inputs Open or Shorted	X	1
1	0	0	X	X	High-Z*
1	1	1	X	X	High-Z

NOTE: *Low Power Shutdown Mode (See Note 13), except for ISL31485E.

Typical Operating Circuits

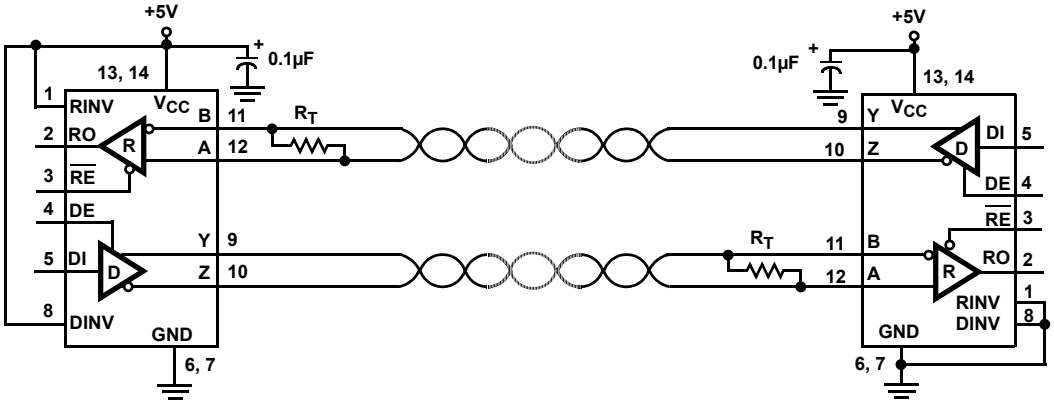
ISL31486E HALF DUPLEX EXAMPLE (MSOP PIN NUMBERS SHOWN)



THE IC ON THE LEFT HAS THE CABLE CONNECTIONS SWAPPED, SO THE INV PIN IS STRAPPED HIGH TO INVERT ITS RX AND TX POLARITY

Typical Operating Circuits (Continued)

ISL34183E FULL DUPLEX EXAMPLE (SOIC PIN NUMBERS SHOWN)



THE IC ON THE LEFT HAS THE CABLE CONNECTIONS SWAPPED, SO THE INV PINS (1, 8) ARE STRAPPED HIGH TO INVERT ITS RX AND TX POLARITY

Table of Contents

Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, INV, RINV, DINV, DE, $\overline{RE}$ . . . . . -0.3V to (V_{CC} + 0.3V)
Input/Output Voltages
A/Y, B/Z, A, B, Y, Z . . . . . ±60V
A/Y, B/Z, A, B, Y, Z (Transient Pulse Through 100Ω, Note 17) . . . . ±80V
RO (ISL31480E, ISL31486E) . . . . . -0.3V to (V_L +0.3V)
RO (ISL31483E, ISL31485E) . . . . . -0.3V to (V_{CC} +0.3V)
Short Circuit Duration
Y, Z . . . . . Indefinite
ESD Rating . . . . . See Specification Table
Latch-up per JESD78, Level 2, Class A . . . . . +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 4, 6)	116	47
10 Ld MSOP Package (Notes 4, 6)	135	50
10 Ld TDFN Package (Notes 5, 7)	58	7
12 Ld TDFN Package (Notes 5, 7)	35	3
14 Ld SOIC Package (Notes 4, 6)	88	38

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage (V_{CC}) 5V
Logic Supply Voltage (V_L) . . . . . 1.62V to V_{CC}
Temperature Range . . . . . -40°C to +85°C
Bus Pin Common Mode Voltage Range . . . . . -25V to +25V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
6. For θ_{JC}, the “case temp” location is taken at the package top center.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V, V_L = V_{CC}; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
DC CHARACTERISTICS							
Driver Differential V_{OUT} (No load)	V_{OD1}		Full	-	-	**V_{CC}**	V
Driver Differential V_{OUT} (Loaded, Figure 3A)	V_{OD2}	R_L = 100Ω (RS-422)	Full	**2.4**	3.2	-	V
		R_L = 54Ω (RS-485)	Full	**1.5**	2.5	**V_{CC}**	V
		R_L = 54Ω (PROFIBUS, V_{CC} ≥ 5V)	Full	**2.0**	2.5	-	V
		R_L = 21Ω (Six 120Ω terminations for Star Configurations, V_{CC} ≥ 4.75V)	Full	**0.8**	1.3	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 3A)	Full	-	-	**0.2**	V
Driver Differential V_{OUT} with Common Mode Load (Figure 3B)	V_{OD3}	R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V	Full	**1.5**	2.1	**V_{CC}**	V
		R_L = 60Ω, -25V ≤ V_{CM} ≤ 25V (V_{CC} ≥ 4.75V)	Full	**1.7**	2.3		V
		R_L = 21Ω, -15V ≤ V_{CM} ≤ 15V (V_{CC} ≥ 4.75V)	Full	**0.8**	1.1	-	V
Driver Common-Mode V_{OUT} (Figure 3)	V_{OC}	R_L = 54Ω or 100Ω	Full	**-1**	-	**3**	V
		R_L = 60Ω or 100Ω, -20V ≤ V_{CM} ≤ 20V	Full	**-2.5**	-	**5**	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	DV_{OC}	R_L = 54Ω or 100Ω (Figure 3A)	Full	-	-	**0.2**	V

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V, V_L = V_{CC}; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
Driver Short-Circuit Current	I_{OSD}	DE = V_{CC}, -25V ≤ V_O ≤ 25V (Note 10)		Full	**-250**	-	**250**	mA
	I_{OSD1}	At First Fold-back, 22V ≤ V_O ≤ -22V		Full	**-83**		**83**	mA
	I_{OSD2}	At Second Fold-back, 35V ≤ V_O ≤ -35V		Full	**-13**		**13**	mA
Logic Input High Voltage	V_{IH1}	DE, DI, $\overline{RE}$, INV, RINV, DINV	V_L = V_{CC} If Applicable	Full	**2.5**	-	-	V
	V_{IH2}	DE, DI, $\overline{RE}$, INV, (Only ISL31480E, ISL31486E)	2.7V ≤ V_L ≤ 3V	Full	**2**	-	-	V
	V_{IH3}		2.3V ≤ V_L < 2.7V	Full	**1.7**	-	-	V
	V_{IH4}		1.6V ≤ V_L < 2.3V	Full	**0.7*V_L**	-	-	V
Logic Input Low Voltage	V_{IL1}	DE, DI, $\overline{RE}$, INV, RINV, DINV	V_L = V_{CC} If Applicable	Full	-	-	**0.8**	V
	V_{IL2}	DE, DI, $\overline{RE}$, INV, (Only ISL31480E, ISL31486E)	2.7V ≤ V_L ≤ 3V	Full	-	-	**0.8**	V
	V_{IL3}		2.3V ≤ V_L < 2.7V	Full	-	-	**0.65**	V
	V_{IL4}		1.6V ≤ V_L < 2.3V	Full	-	-	**0.3*V_L**	V
Logic Input Current	I_{IN1}	DI		Full	**-1**	-	**1**	µA
		DE, $\overline{RE}$, INV, RINV, DINV		Full	**-15**	6	**15**	µA
Input/Output Current (A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	110	**250**	µA
			V_{IN} = -7V	Full	**-200**	-75	-	µA
			V_{IN} = ±25V	Full	**-800**	±240	**800**	µA
			V_{IN} = ±60V (Note 19)	Full	**-6**	±0.7	**6**	mA
Input Current (A, B) (Full Duplex Versions Only)	I_{IN3}	V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	90	**125**	µA
			V_{IN} = -7V	Full	**-100**	-70	-	µA
			V_{IN} = ±25V	Full	**-500**	±200	**500**	µA
			V_{IN} = ±60V (Note 19)	Full	**-3**	±0.5	**3**	mA
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{OZD}	$\overline{RE}$ = 0V, DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	20	**200**	µA
			V_{IN} = -7V	Full	**-100**	-5	-	µA
			V_{IN} = ±25V	Full	**-500**	±40	**500**	µA
			V_{IN} = ±60V (Note 19)	Full	**-3**	±0.15	**3**	mA
Receiver Differential Threshold Voltage	V_{TH}	A-B for ISL31480E or if INV or RINV = 0; B-A if INV or RINV = 1, -25V ≤ V_{CM} ≤ 25V		Full	**-200**	-100	**-10**	mV
Receiver Input Hysteresis	DV_{TH}	-25V ≤ V_{CM} ≤ 25V		25	-	25	-	mV
Receiver Output High Voltage	V_{OH1}	V_{ID} = -10mV, V_L = V_{CC} If Applicable	I_O = -2mA	Full	**V_{CC} - 0.5**	4.75	-	V
	V_{OH2}		I_O = -8mA	Full	**2.8**	4.2	-	V
	V_{OH3}	V_{ID} = -10mV, Only ISL31480E, ISL31486E	V_L ≥ 2.7V, I_O = -1.5mA	Full	**V_L-0.3**		-	V
	V_{OH4}		V_L ≥ 2.3V, I_O = -1mA	Full	**V_L-0.3**		-	V
	V_{OH5}		V_L ≥ 1.6V, I_O = -500µA	Full	**V_L-0.25**		-	V
Receiver Output Low Voltage	V_{OL}	I_O = 6mA, V_L ≥ 1.6V, V_{ID} = -200mV		Full	-	0.27	**0.4**	V

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V, V_L = V_{CC}; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
Receiver Output Low Current	I_{OL}	V_O = 1V, $V_L \geq$ 1.6V, V_{ID} = -200mV		Full	**15**	22	-	mA
Three-State (High Impedance) Receiver Output Current	I_{OZR}	0V ≤ V_O ≤ V_L (If Applicable) or V_{CC} (Note 18)		Full	**-1**	0.01	**1**	µA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}, V_L = V_{CC} if applicable		Full	**±12**	-	**±110**	mA
SUPPLY CURRENT								
No-Load Supply Current (Note 9)	I_{CC}	DE = V_{CC}, RE = 0V or V_{CC}, DI = 0V or V_{CC}		Full	-	2.3	**4.5**	mA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC} (Note 18)		Full	-	10	**50**	µA
ESD PERFORMANCE								
All Pins		Human Body Model (Tested per JESD22-A114E)		25	-	±2	-	kV
		Machine Model (Tested per JESD22-A115-A)		25	-	±700	-	V
DRIVER SWITCHING CHARACTERISTICS								
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_D = 54Ω, C_D = 50pF (Figure 4)	No CM Load	Full	-	70	**125**	ns
			-25V ≤ V_{CM} ≤ 25V	Full	-	-	**350**	ns
Driver Differential Output Skew	t_{SKEW}	R_D = 54Ω, C_D = 50pF (Figure 4)	No CM Load	Full	-	4.5	**15**	ns
			-25V ≤ V_{CM} ≤ 25V	Full	-	-	**25**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_D = 54Ω, C_D = 50pF (Figure 4)	No CM Load	Full	**70**	170	**300**	ns
			-25V ≤ V_{CM} ≤ 25V	Full	**70**	-	**400**	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF, $V_L \geq$ 1.6V (Figure 6)		Full	**1**	4	-	Mbps
Driver Enable to Output High	t_{ZH}	SW = GND (Figure 5), (Note 11)		Full	-	-	**350**	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (Figure 5), (Note 11)		Full	-	-	**300**	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (Figure 5)		Full	-	-	**120**	ns
Driver Disable from Output High	t_{HZ}	SW = GND (Figure 5)		Full	-	-	**120**	ns
Time to Shutdown	t_{SHDN}	(Notes 13, 18)		Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	SW = GND (Figure 5), (Notes 13, 14, 18)		Full	-	-	**2000**	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	SW = V_{CC} (Figure 5), (Notes 13, 14, 18)		Full	-	-	**2000**	ns
RECEIVER SWITCHING CHARACTERISTICS								
Maximum Data Rate	f_{MAX}	-25V ≤ V_{CM} ≤ 25V (Figure 7)		Full	**1**	15	-	Mbps
		-15V ≤ V_{CM} ≤ 15V, $V_L \geq$ 1.6V (Figure 7)		Full	**1**	12	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	-25V ≤ V_{CM} ≤ 25V (Figure 7)		Full	-	90	**150**	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 7)		Full	-	4	**10**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Notes 12, 18)		Full	-	-	**50**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Notes 12, 18)		Full	-	-	**50**	ns

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V, V_L = V_{CC}; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8) (Note 18)	Full	-	-	**50**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8) (Note 18)	Full	-	-	**50**	ns
Time to Shutdown	t_{SHDN}	(Notes 13, 18)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Notes 13, 15, 18)	Full	-	-	**2000**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Notes 13, 15, 18)	Full	-	-	**2000**	ns

NOTES:

8. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
9. Supply current specification is valid for loaded drivers when DE = 0V.
10. Applies to peak current. See “Typical Performance Curves” beginning on page 18 for more information
11. Keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
12. The $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
13. Transceivers (except on the ISL31485E) are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See “Low Power Shutdown Mode” on page 16.
14. Keep $\overline{RE}$ = VCC, and set the DE signal low time >600ns to ensure that the device enters SHDN.
15. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
16. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
17. Tested according to TIA/EIA-485-A, Section 4.2.6 (±80V for 15ms at a 1% duty cycle).
18. Does not apply to the ISL31485E. The ISL31485E has no Rx enable function, and thus no SHDN function.
19. See “Caution” statement under the “Recommended Operating Conditions” section on page 8.

Test Circuits and Waveforms

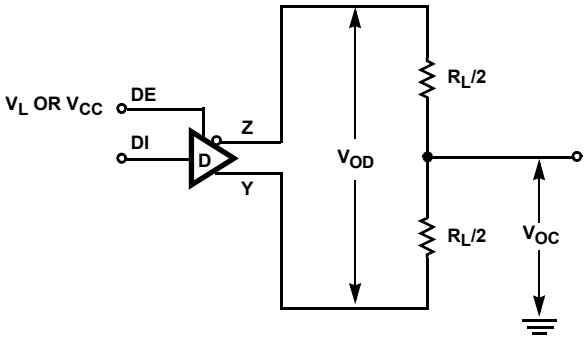


FIGURE 3A. V_{OD} AND V_{OC}

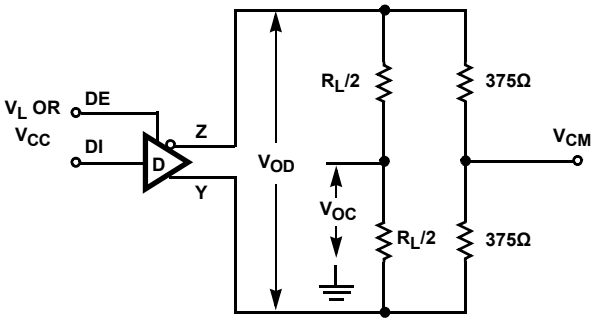


FIGURE 3B. 1B

FIGURE 3. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

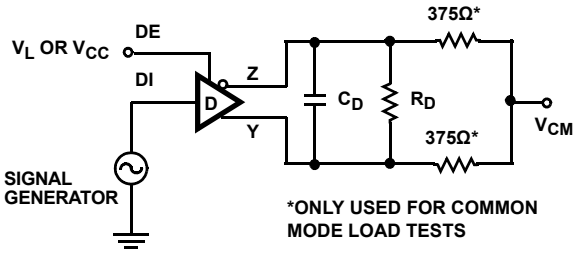


FIGURE 4A. TEST CIRCUIT

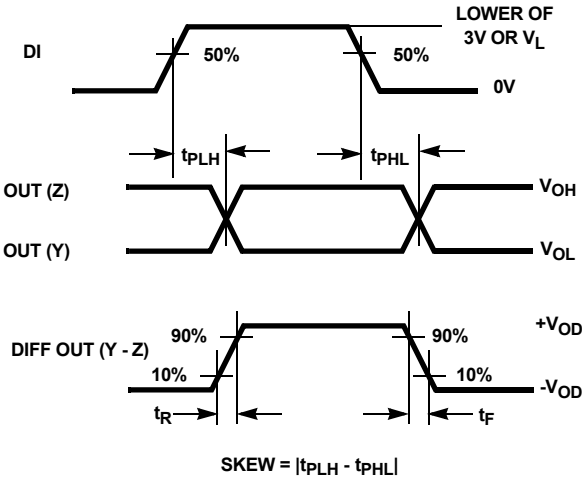
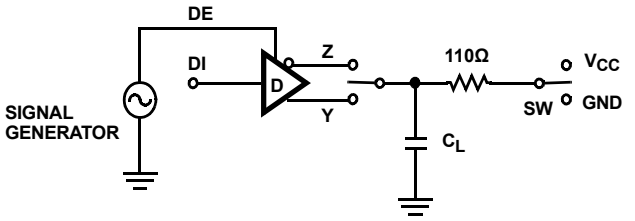


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	50
t_{LZ}	Y/Z	X	0/1	V_{CC}	50
t_{ZH}	Y/Z	0 (Note 11)	1/0	GND	100
t_{ZL}	Y/Z	0 (Note 11)	0/1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 14)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 14)	0/1	V_{CC}	100

FIGURE 5A. TEST CIRCUIT

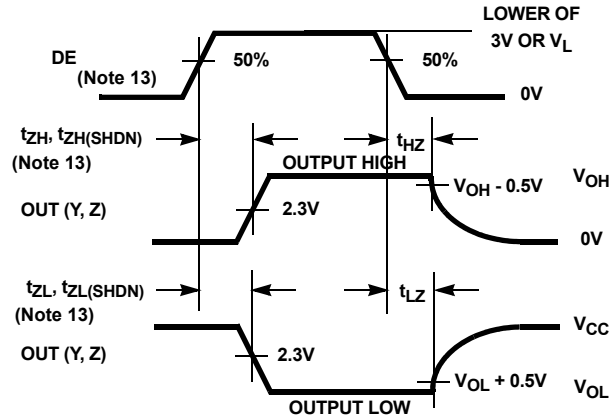


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

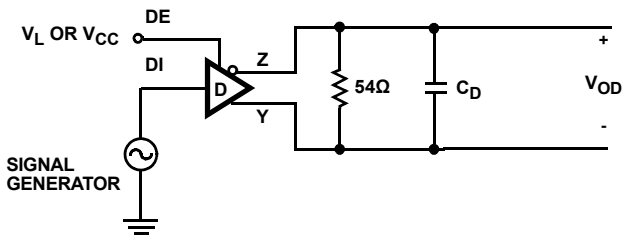


FIGURE 6A. TEST CIRCUIT

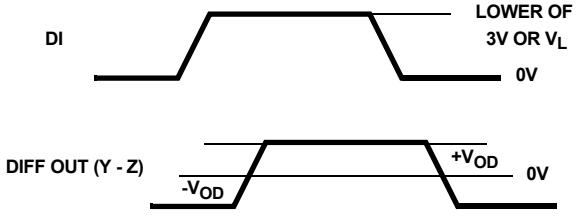


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. DRIVER DATA RATE

Test Circuits and Waveforms (Continued)

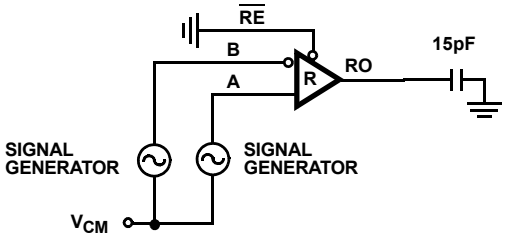


FIGURE 7A. TEST CIRCUIT

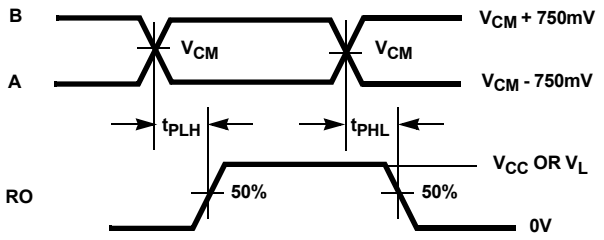
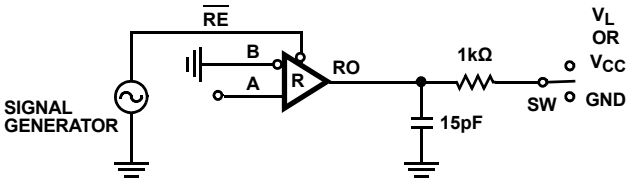


FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_L / V_{CC}
t_{ZH} (Note 12)	0	+1.5V	GND
t_{ZL} (Note 12)	0	-1.5V	V_L / V_{CC}
$t_{ZH(SHDN)}$ (Note 15)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 15)	0	-1.5V	V_L / V_{CC}

FIGURE 8A. TEST CIRCUIT

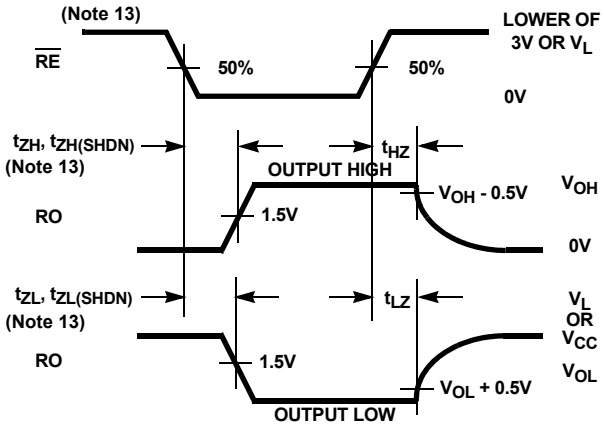


FIGURE 8B. MEASUREMENT POINTS

FIGURE 8. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards used for long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

The ISL3148xE is a family of ruggedized RS-485 transceivers that improves on the RS-485 basic requirements, and therefore increases system reliability. The CMR increases to ±25V, while the RS-485 bus pins (receiver inputs and driver outputs) include fault protection against voltages and transients up to ±60V. Additionally, larger than required differential output voltages (V_{OD}) increase noise immunity.

Receiver (Rx) Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is better than ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input (load) current surpasses the RS-422 specification of 3mA, and is four times lower than the RS-485 "Unit Load (UL)" requirement of 1mA maximum. Thus, these products are known as "one-quarter UL" transceivers, and there can be up to 128 of these devices on a network while still complying with the RS-485 loading specification.

The Rx functions with common mode voltages as great as ±25V, making them ideal for industrial, or long networks where induced voltages are a realistic concern.

All the receivers include a "full fail-safe" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled (i.e., an idle bus).

Rx outputs feature high drive levels (typically 22mA @ V_{OL} = 1V) to ease the design of optically coupled isolated interfaces. Except for the ISL31485E, Rx outputs are three-statable via the active low $\overline{RE}$ input.

The Rx includes noise filtering circuitry to reject high frequency signals, and typically rejects pulses narrower than 50ns (equivalent to 20Mbps).

Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2.4V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI, and all drivers are three-statable via the active high DE input.

The driver outputs are slew rate limited to minimize EMI, and to minimize reflections in unterminated or improperly terminated networks.

High Overvoltage (Fault) Protection Increases Ruggedness

Note: The available smaller pitch packages (e.g., MSOP and TDFN) may not meet the creepage and clearance (C&C) requirements for ±60V levels. The user is advised to determine his C&C requirements before selecting a package type.

The ±60V (referenced to the IC GND) fault protection on the RS-485 pins, makes these transceivers some of the most rugged on the market. This level of protection makes the ISL3148xE perfect for applications where power (e.g., 24V and 48V supplies) must be routed in the conduit with the data lines, or for outdoor applications where large transients are likely to occur. When power is routed with the data lines, even a momentary short between the supply and data lines will destroy an unprotected device. The ±60V fault levels of this family are at least **five times higher** than the levels specified for standard RS-485 ICs. The ISL3148xE protection is active whether the Tx is enabled or disabled, and even if the IC is powered down.

If transients or voltages (including overshoots and ringing) greater then ±60V are possible, then additional external protection is required.

Widest Common Mode Voltage (CMV) Tolerance Improves Operating Range

RS-485 networks operating in industrial complexes, or over long distances, are susceptible to large CMV variations. Either of these operating environments may suffer from large node-to-node ground potential differences, or CMV pickup from external electromagnetic sources, and devices with only the minimum required +12V to -7V CMR may malfunction. The ISL3148xE's extended ±25V CMR is the widest available, allowing operation in environments that would overwhelm lesser transceivers. Additionally, the Rx will not phase invert (erroneously change state) even with CMVs of ±40V, or differential voltages as large as 40V.

Cable Invert (Polarity Reversal) Function

With large node count RS-485 networks, it is common for some cable data lines to be wired backwards during installation. When this happens the node is unable to communicate over the network. Once a technician finds the miswired node, he must then rewire the connector which is time consuming.

The ISL31483E, ISL31485E, and ISL31486E simplify this task by including cable invert pins (INV, DINV, RINV) that allow the technician to invert the polarity of the Rx input and/or the Tx output pins simply by moving a jumper to change the state of the invert pin(s). When the invert pin(s) is low, the IC operates like any standard RS-485 transceiver and the bus pins have their normal polarity definition of A and Y being noninverting, and B

and Z being inverting. With the invert pin high, the corresponding bus pins reverse their polarity, so B and Z are now noninverting and A and Y become inverting.

Intersil's unique cable invert function is superior to that found on competing devices because the Rx full failsafe function is maintained even when the Rx polarity is reversed. Competitor devices implement the Rx invert function simply by inverting the Rx output. This means that with the Rx inputs floating or shorted together, the Rx appropriately delivers a logic 1 in normal polarity, but outputs a logic low when the IC is operated in the inverted mode. Intersil's innovative Rx design guarantees that with the Rx inputs floating, or shorted together (V_{ID} = 0V), the Rx output remains high regardless of the state of the invert pins.

The full duplex ISL31483E includes two invert pins that allow for separate control of the Rx and Tx polarities. If only the Rx cable is miswired, then only the RINV pin need be driven to a logic 1. If the Tx cable is miswired, then DINV must be connected to a logic high. The two half duplex versions have only one logic pin (INV) that, when high, switches the polarity of both the Tx and the Rx blocks.

Logic Supply (V_L Pin)

Note: Power up V_{CC} before powering up the V_L supply, and keep $V_L \leq V_{CC}$.

The ISL31480E and ISL31486E include a V_L pin that powers the logic inputs (Tx input and control pins) and the Rx output. These pins interface with "logic" devices such as UARTs, ASICs, and µcontrollers, and today many of these devices use power supplies significantly lower than 5V. Thus, a 5V output level from this transceiver IC might seriously overdrive and damage the logic device input (see Figure 9). Similarly, the logic device's low V_{OH} might not exceed the V_{IH} of a 5V powered transceiver input. Connecting the V_L pin to the power supply of the logic device - as shown in Figure 9 - limits the ISL3148xE's RO pin V_{OH} to the V_L voltage, and reduces the Tx and control input switching points to values compatible with the logic device output levels. Tailoring the logic pin input switching points and output levels to the supply voltage of the UART, ASIC, or µcontroller eliminates the need for a level shifter/translator between the two ICs.

V_L can be anywhere from V_{CC} down to 1.62V, and the transceivers easily operate at the 1Mbps data rate over this range as long as the VCM doesn't exceed ±15V. Table 2 indicates typical V_{IH} and V_{IL} values for various V_L voltages so the user can ascertain whether or not a particular V_L voltage meets his/her needs.

TABLE 2. V_{IH} AND V_{IL} vs. V_L FOR V_{CC} = 5V

V_L (V)	V_{IH} (V)	V_{IL} (V)
1.6	1.0	0.6
1.8	1.1	0.7
2.3	1.3	0.9
2.7	1.4	1.1
3.3	1.6	1.3

The V_L supply current (I_L) is typically less than 6µA. All of the DC V_L current is due to current through the DE input internal pull-up resistor when the pin is driven to the low input state.

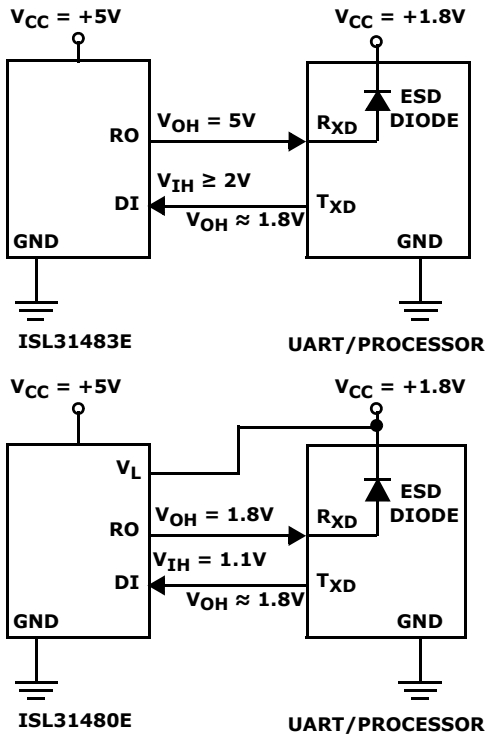


FIGURE 9. USING VL PIN TO ADJUST LOGIC LEVELS

Transceiver logic inputs that are externally tied high in an application should use the V_L supply for the high voltage level to minimize input currents. Except for DI, all logic inputs have 800kΩ pull-up (DE) or pull-down (all other pins) resistors, so connecting an input to the lower voltage V_L supply minimizes current. The DE pull-up internally connects to V_L, so connecting the DE pin to V_{CC} induces an input current of (V_{CC} - V_L)/800kΩ.

High V_{OD} Improves Noise Immunity and Flexibility

The ISL3148xE driver design delivers larger differential output voltages (V_{OD}) than the RS-485 standard requires, or than most RS-485 transmitters can deliver. The typical ±2.5V V_{OD} provides more noise immunity than networks built using many other transceivers.

Another advantage of the large V_{OD} is the ability to drive more than two bus terminations, which allows for utilizing the ISL3148xE in "star" and other multi-terminated, nonstandard network topologies.

Figure 11, details the transmitter's V_{OD} vs I_{OUT} characteristic, and includes load lines for four (30Ω) and six (20Ω) 120Ω terminations. The figure shows that the driver typically delivers ±1.3V into six terminations, and the "Electrical Specification" table guarantees a V_{OD} of ±0.8V at 21Ω over the full temperature range. The RS-485 standard requires a minimum 1.5V V_{OD} into two terminations, but the ISL3148xE deliver RS-485 voltage levels with 2x to 3x the number of terminations.

Hot Plug Function

When a piece of equipment powers up, there is a period of time where the processor or ASIC driving the RS-485 control lines (DE, $\overline{RE}$) is unable to ensure that the RS-485 Tx and Rx outputs are

kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL3148xE devices incorporate a “Hot Plug” function. Circuitry monitoring V_{CC} ensures that, during power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and $\overline{RE}$, if V_{CC} is less than ≈3.5V. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states. Figure 10 illustrates the power-up and power-down performance of the ISL3148xE compared to an RS-485 IC without the Hot Plug feature.

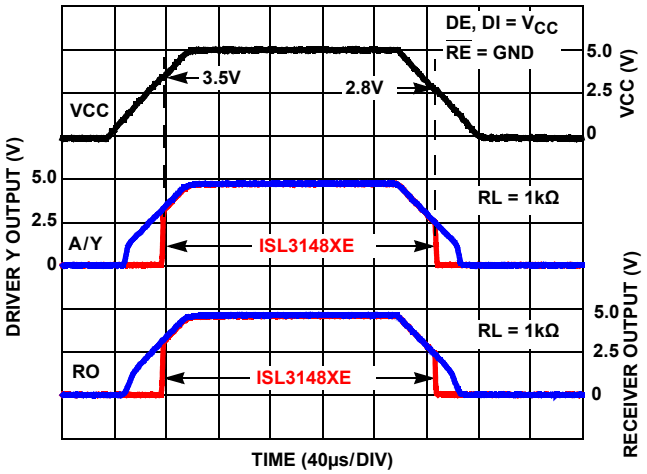


FIGURE 10. HOT PLUG PERFORMANCE ISL3148XE vs ISL83088E WITHOUT HOT PLUG CIRCUITRY

Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000’, but the maximum system data rate decreases as the transmission length increases. These 1Mbps versions can operate at full data rates with lengths up to 800’ (244m). Jitter is the limiting parameter at this data rate, so employing encoded data streams (e.g., Manchester coded or Return-to-Zero) may allow increased transmission distances.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative to minimize reflections, and terminations are recommended unless power dissipation is an overriding concern. In point-to-point, or point-to-multipoint (single driver on bus like RS-422) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These transceivers meet this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate a double foldback short circuit current limiting scheme which ensures that the output current never exceeds the RS-485 specification, even at the common mode and fault condition voltage range extremes. The first foldback current level (≈70mA) is set to ensure that the driver never folds back when driving loads with common mode voltages up to ±25V. The very low second foldback current setting (≈9mA) minimizes power dissipation if the Tx is enabled when a fault occurs.

In the event of a major short circuit condition, devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode

These CMOS transceivers all use a fraction of the power required by competitive devices, but they also include a shutdown feature (except the ISL31485E) that reduces the already low quiescent I_{CC} to a 10µA trickle. These devices enter shutdown whenever the receiver and driver are *simultaneously* disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 11, 12, 13, 14 and 15, at the end of the “Electrical Specification” table on page 11, for more information.

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified.

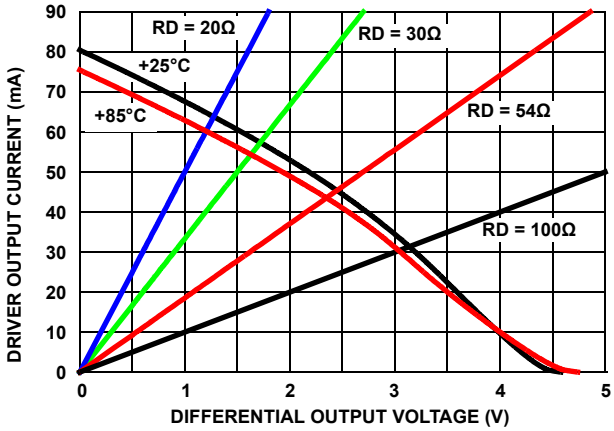


FIGURE 11. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

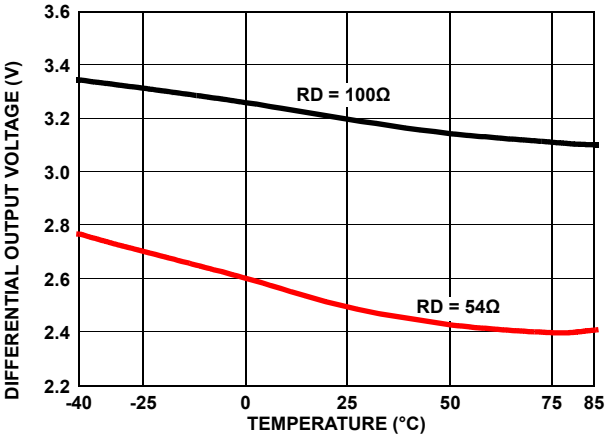


FIGURE 12. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

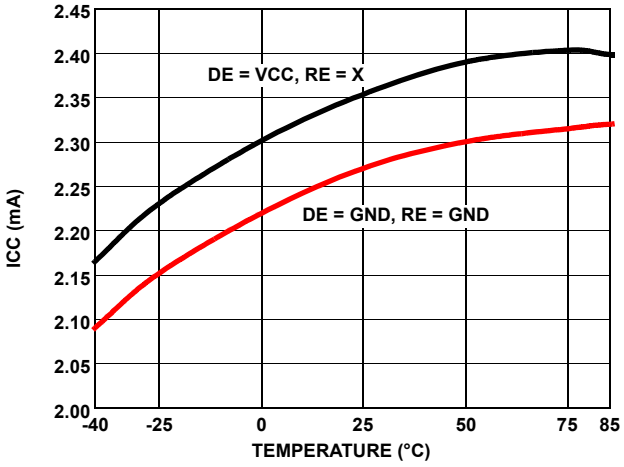


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

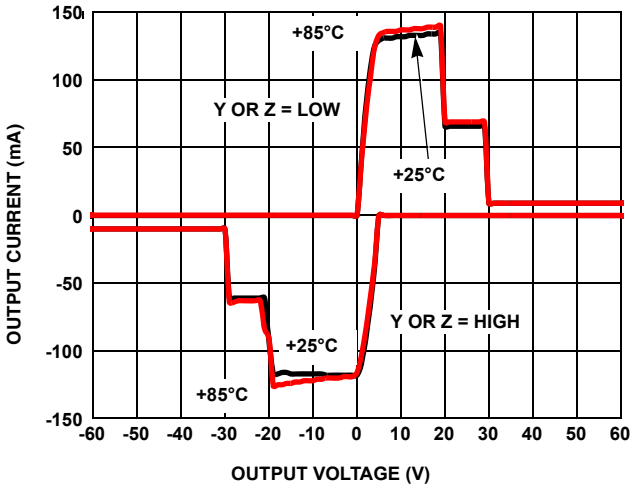


FIGURE 14. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

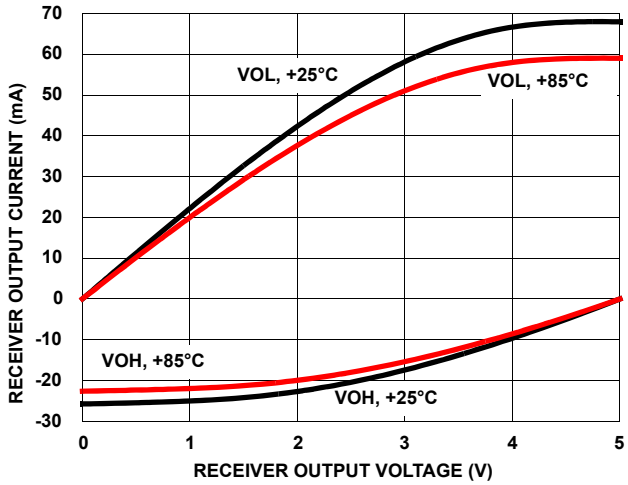


FIGURE 15. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

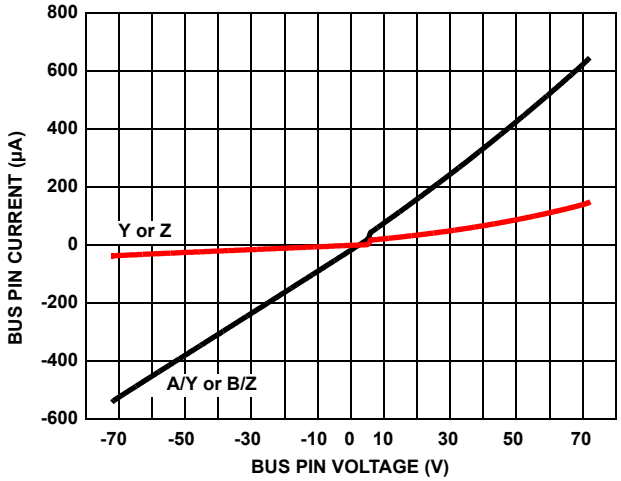


FIGURE 16. BUS PIN CURRENT vs BUS PIN VOLTAGE

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified. (Continued)

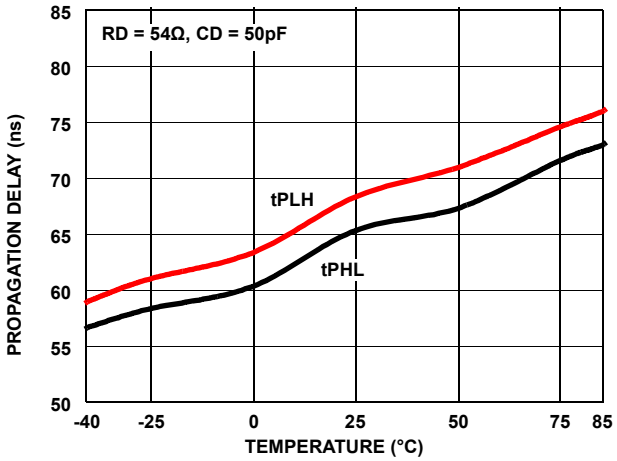


FIGURE 17. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

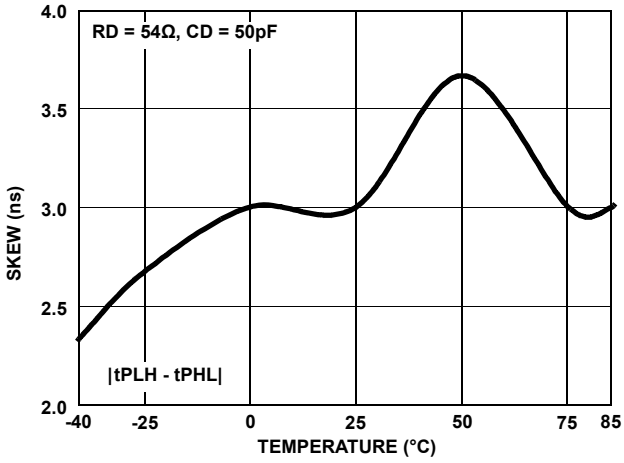


FIGURE 18. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE

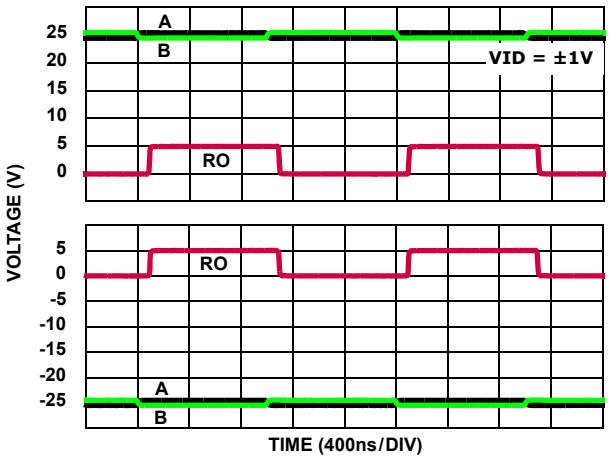


FIGURE 19. RECEIVER PERFORMANCE WITH ±25V CMV

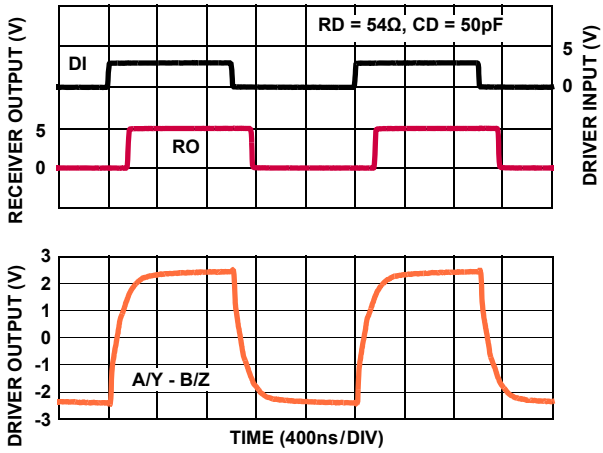


FIGURE 20. DRIVER AND RECEIVER WAVEFORMS

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

PROCESS:

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
1/7/11	FN7638.2	Changed Note 19 to Note 17 in “Absolute Maximum Ratings” on page 8 Changed Notes 12 and 15 to Notes 11 and 14 in Figure 5A on page 12 Changed Note 16 to Note 15 in Figure 8A on page 13 Deleted Note 17 (See Figure 9 for more information, and for performance over-temperature) Changed TYP on “Driver Differential Rise or Fall Time” on page 10 from 230 to 170 Added Figure 14 “DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE” Updated “Package Outline Drawing” on page 24. Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern.
09/08/10	FN7638.1	Corrected test conditions for “Receiver Output High Voltage” for “VOH5” on page 9 from “IO = -500mA” to “IO = -500µA”
06/25/10	FN7638.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL31480E, ISL31483E, ISL31485E, ISL31486E

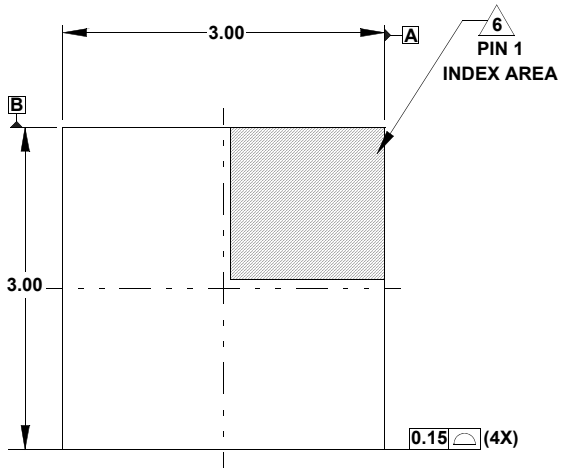
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

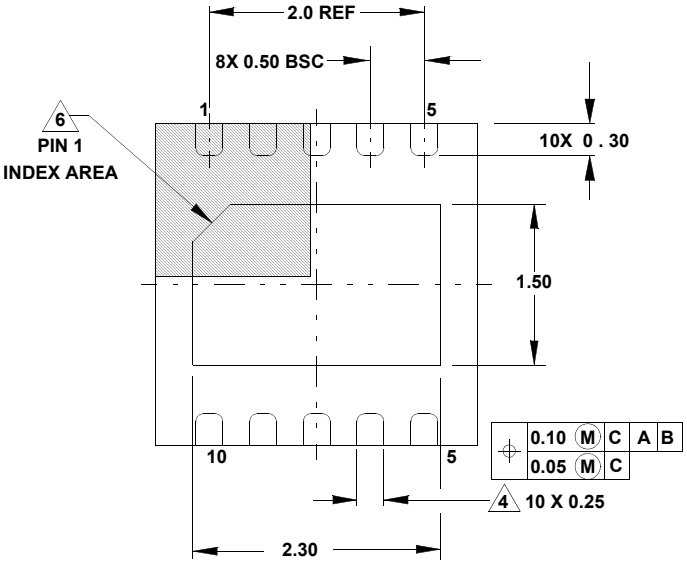
Package Outline Drawing

L10.3x3A

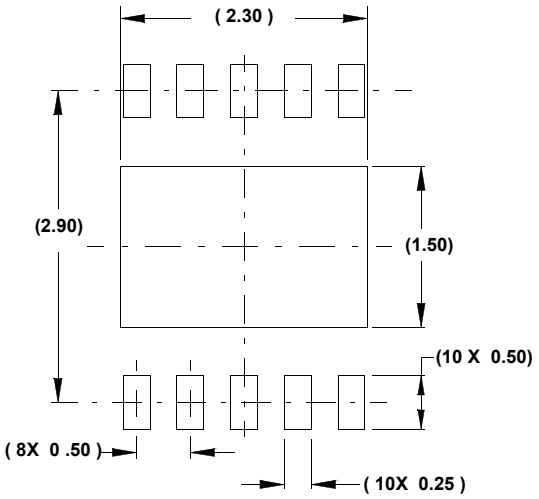
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



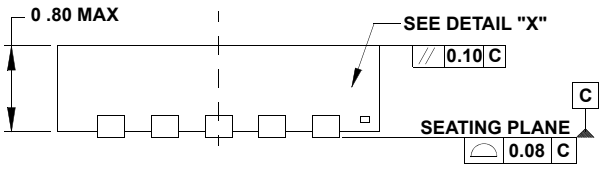
TOP VIEW



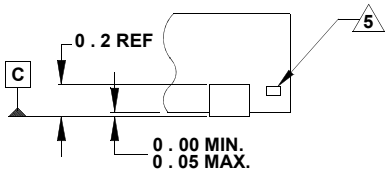
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

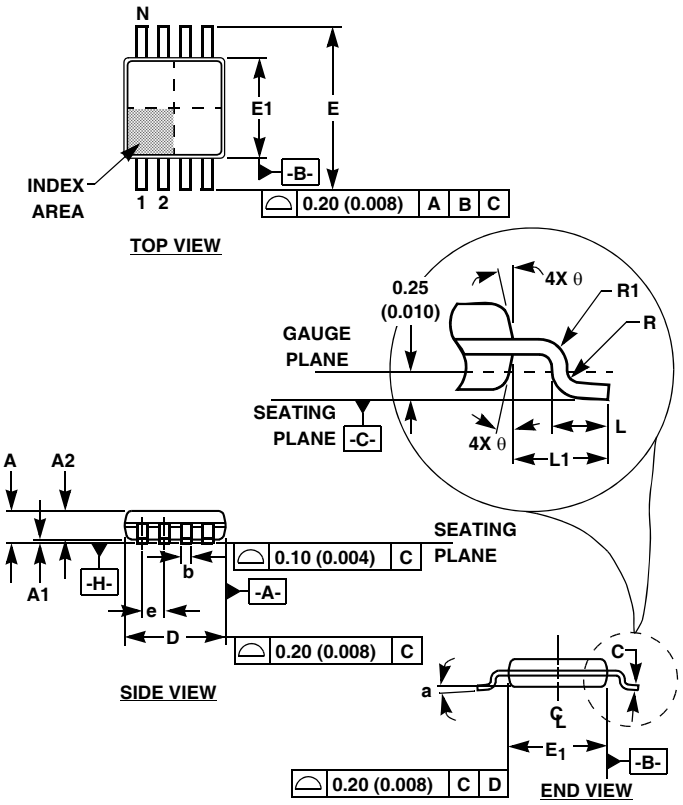


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).

Mini Small Outline Plastic Packages (MSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

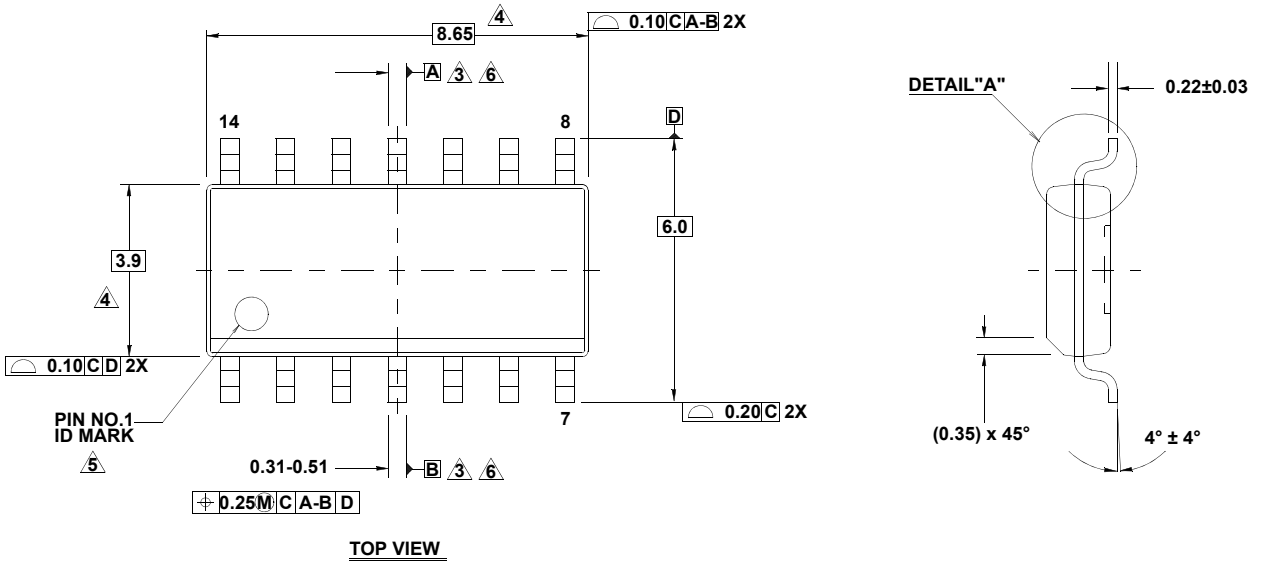
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

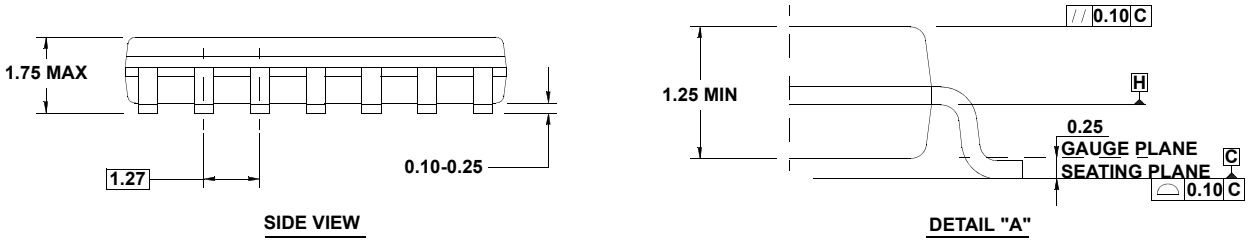
Package Outline Drawing

M14.15

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 10/09

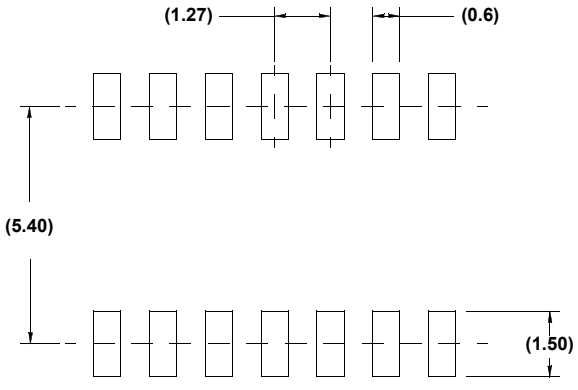


TOP VIEW



SIDE VIEW

DETAIL "A"

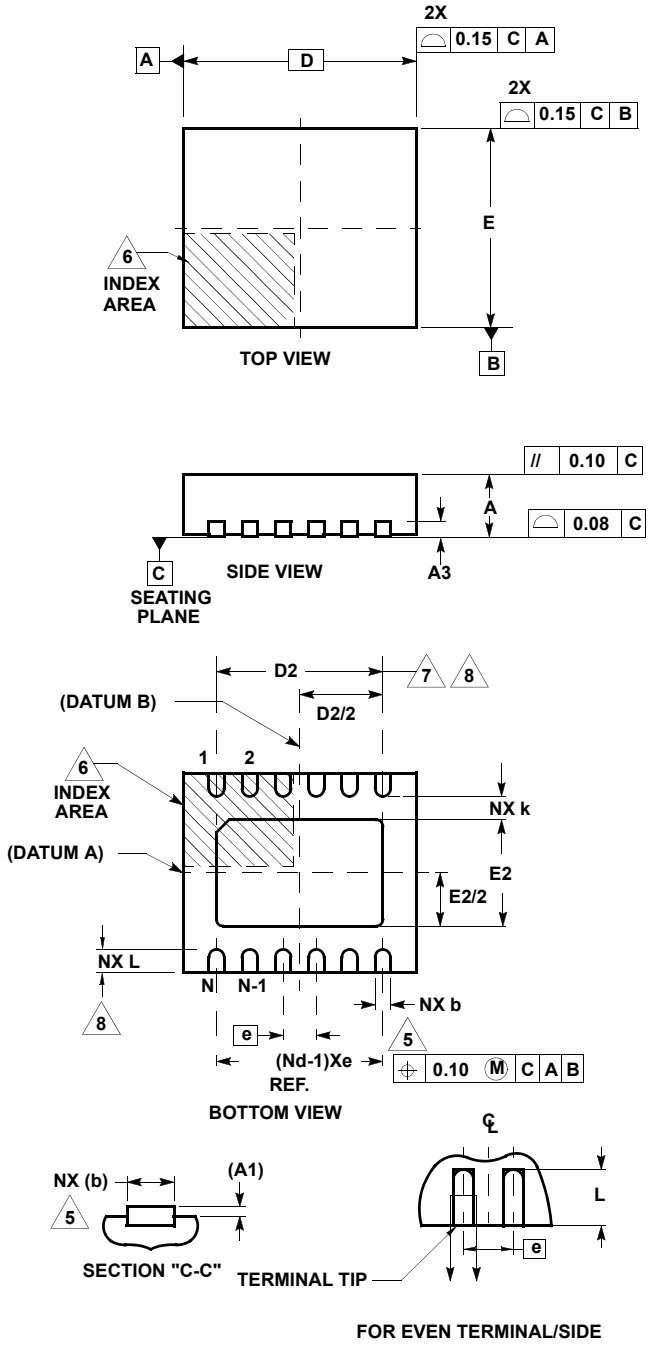


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 indentifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L12.4x3A

12 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-229-WGED-4 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.30	5,8
D		4.00 BSC		-
D2	3.15	3.30	3.40	7,8
E		3.00 BSC		-
E2	1.55	1.70	1.80	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		12		2
Nd		6		3

Rev. 0 1/06

NOTES:

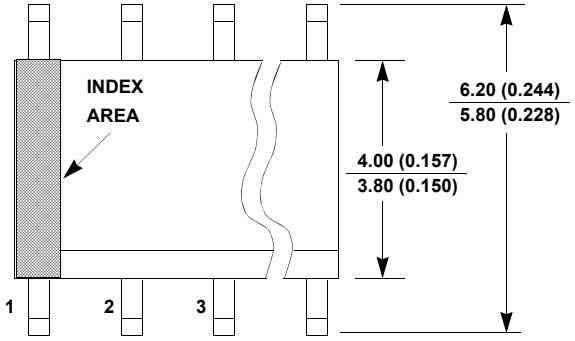
1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

Package Outline Drawing

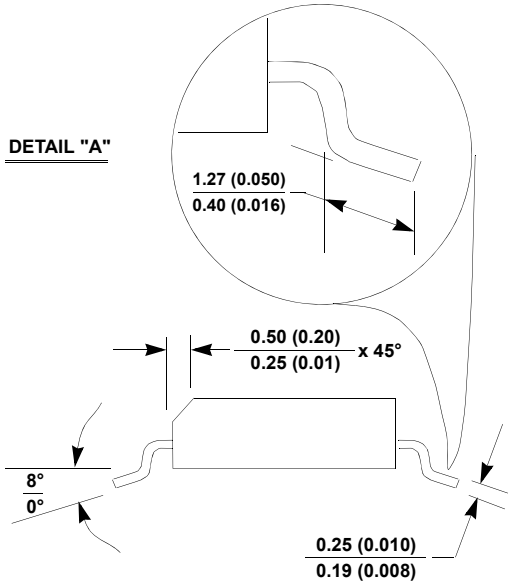
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

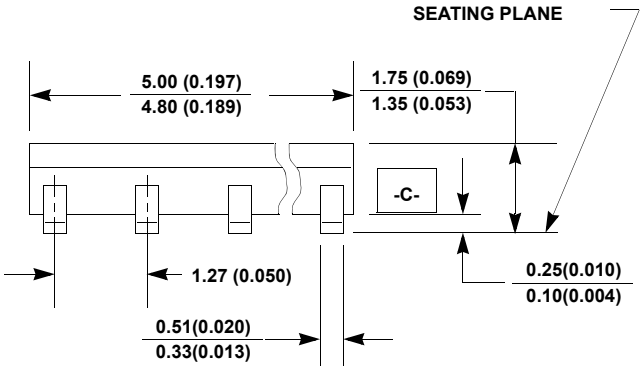
Rev 2, 11/10



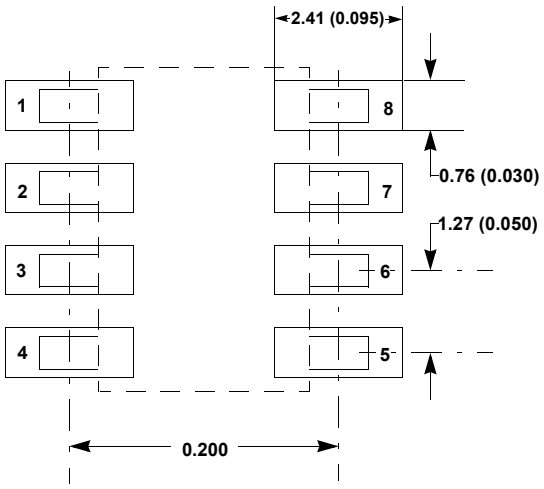
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.