6-Channel Integrated LCD Supply

ISL98604

The ISL98604 is a high power, fully programmable 6-Channel output control IC targeted at large panel LCD displays. The ISL98604 integrates a high power, boost converter and delay switch for AVDD generation, one VIO asynchronous buck regulator, two synchronous buck regulators for HAVDD and VCORE supply generation, and linear regulator controllers for V_{ON} and V_{OFF} charge pumps.

Operating at 750kHz, the AVDD boost converter features a 4.0A boost FET and 6-bit resolution programmable from 12.7V to 19.0V. The delay switch is also integrated for power sequence.

The asynchronous buck converter for VIO supply features an integrated 2A FET. It also operates at 750kHz internal clock and compensation features.

The two synchronous bucks are integrated with controller, upper, and lower side switches for HAVDD and VCORE generation with internal compensation. The HAVDD and VCORE outputs are both programmable ranging from 6.4V to 9.55V and 0.9V to 2.4V, respectively.

Dual linear regulator controllers are provided to allow generation of accurate V_{ON} and V_{OFF} voltages in conjunction with external charge pumps and bipolar power transistors. V_{ON} output voltage can be compensated adoptively by temperature sensing.

All output voltages are programmed through IIC and stored in EEPROM. Alternative factory set voltages are available for ISL98604; please contact Consumer Product Marketing via email at Consumer-All@intersil.com.

Features

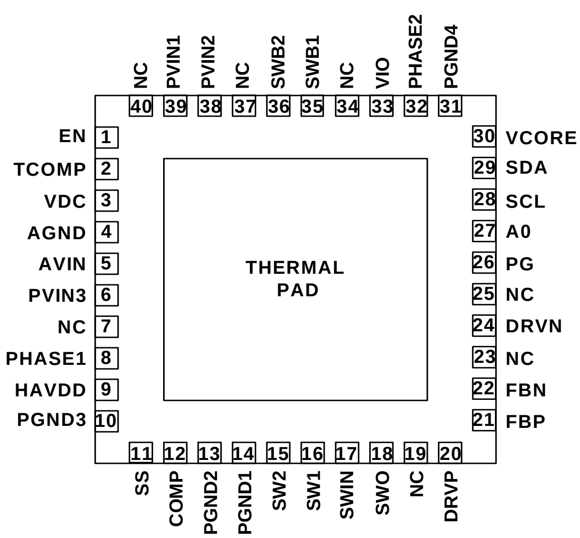
- 8V to 16.5V input supply
- AVDD boost up to 19.0V, with integrated 4.0A_{PEAK} FET
- HAVDD synchronous buck for 8V with 1A_{PEAK} FET
- Overvoltage protection (OVP)
- Internal AVDD delay FET
- Dual linear regulator controllers for V_{ON} and V_{OFF}
- V_{ON} temperature compensation
- VIO buck with integrated 2A_{PEAK} FET
- VCORE synchronous buck with integrated 1A_{PEAK} FET
- Internal feedback and compensation
- Programmable output control with IIC
- Programmable sequencing with IIC
- UVLO and OTP protection
- Thermally enhanced 5x5 Thin QFN package
- Pb-free (RoHS compliant)

Applications

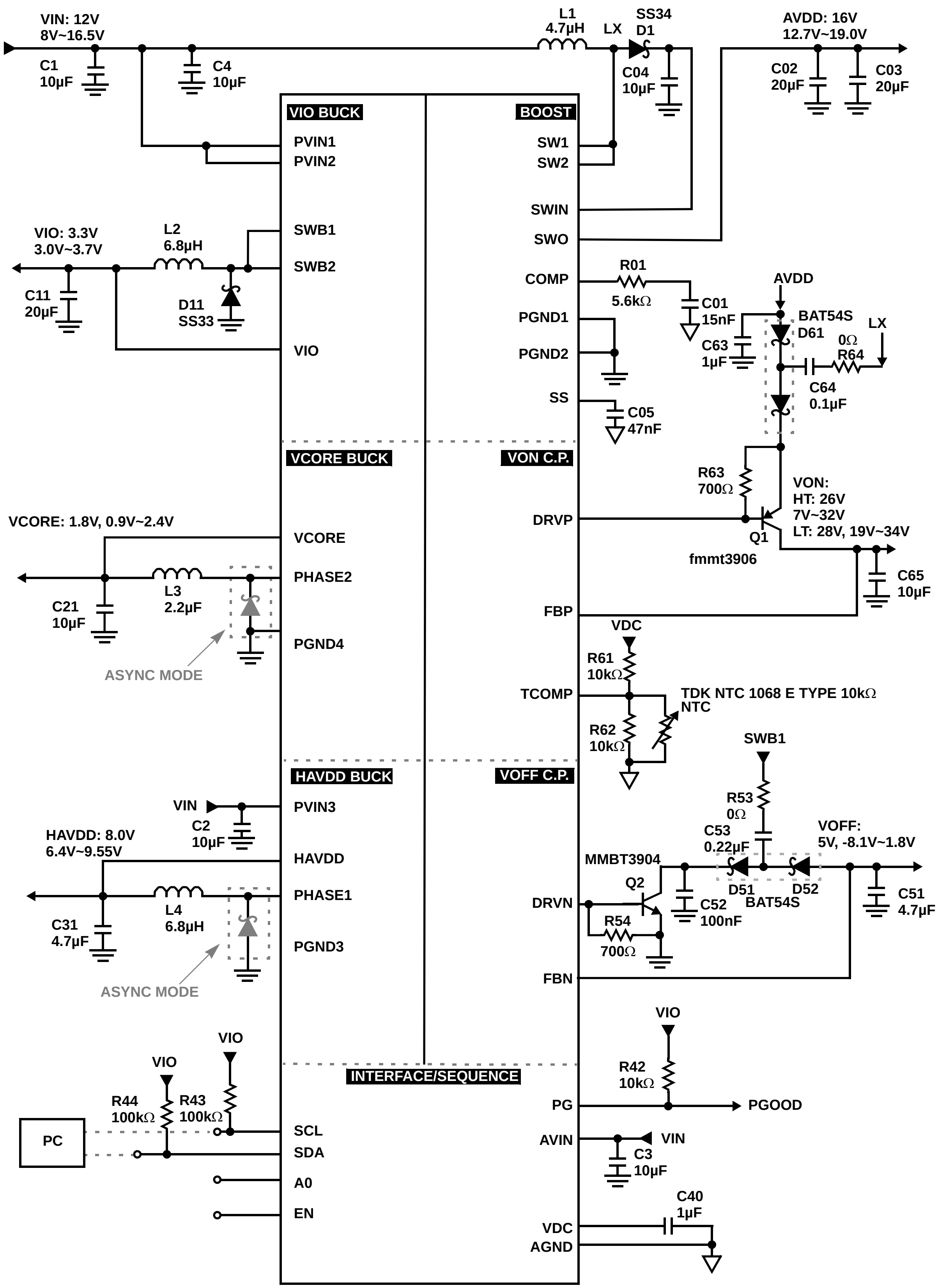
- LCD TV

Pin Configuration

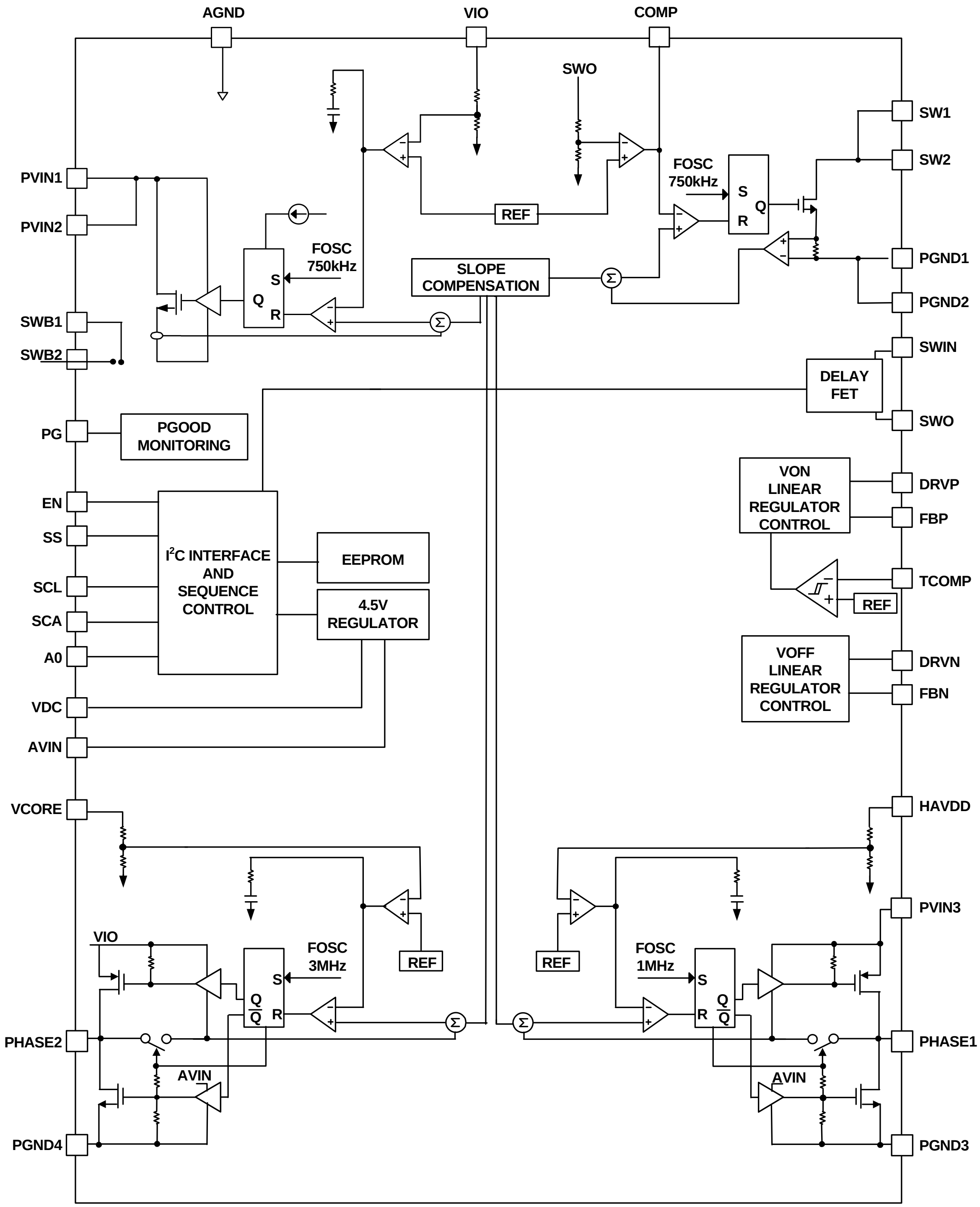
ISL98604
(40 LD 5x5 TQFN)
TOP VIEW



Typical Application Circuit



Block Diagram



Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	EN	IC enable pin; pull high to enable all the outputs.
2	TCOMP	Temperature compensation input, connect NTC resistor in the resistor ladder from VDC to GND to set the curve of V_{ON} vs temperature.
3	VDC	Internal linear regulator output, connected to external 1µF capacitor close to the pin.
4	AGND	Analog ground pin.
5	AVIN	Internal regulator supply pin; connect to external 10µF capacitor close to the pin.
6	PVIN3	HAVDD buck power input pin; connect to external 10µF capacitor close to the pin.
7, 19, 23, 25, 34, 37, 40	NC	Not connected.
8	PHASE1	HAVDD buck switch node; connect an inductor to the pin for synchronous mode, or connect a inductor and a Schottky diode to the pin for asynchronous mode.
9	HAVDD	HAVDD buck output feedback input pin.
10	PGND3	HAVDD buck Power ground.
11	SS	AVDD boost and HAVDD buck soft-start timing capacitor connection for step-up.
12	COMP	AVDD boost compensation pin; connect a 5.6kΩ resistor and 15nF capacitor in series to the pin.
13, 14	PGND2, 1	AVDD boost power ground.
15, 16	SW2, 1	AVDD boost switch node connection.
17	SWIN	AVDD delay FET input, connect a 10µF capacitor close to the pin.
18	SWO	AVDD delay FET output, connect a 22µF capacitors close to the pin.
20	DRVP	Positive charge pump LDO transistor driver, connect the base of an external PNP bipolar to the pin.
21	FBP	Positive charge pump output feedback input pin.
22	FBN	Negative charge pump output feedback input pin.
24	DRVN	Negative charge pump LDO transistor driver, connect the base of an external NPN bipolar to the pin.
26	PG	Power good output.
27	A0	IIC slave address select pin.
28	SCL	IIC clock pin.
29	SDA	IIC data pin.
30	VCORE	VCORE buck output feedback input pin.
31	PGND4	VCORE buck power ground.
32	PHASE2	VCORE buck switch node, connect an inductor to the pin for synchronous mode, or connect a inductor and a Schottky diode to the pin for asynchronous mode.
33	VIO	VIO buck output feedback input pin.
35, 36	SWB1, 2	VIO asynchronous buck switch node connection.
38, 39	PVIN2, 1	VIO buck and VCORE buck power input pin; connect to external 10µF capacitor close to the pin.
-	PAD	Thermal Pad.

Ordering Information (Note 1)

PART NUMBER (Notes 2, 3, 4)	PART MARKING	AVDD BOOST (V)	HAVDD BUCK (V)	VIO BUCK (V)	VCORE BUCK (V)	V_{ON} LT (V)	V_{ON} HT (V)	V_{OFF} (V)	DLY1 (ms)	DLY2 (ms)	DLY3 (ms)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL98604IRTZ	ISL9860 4IRZ	16	8.0	3.3	1.0	28	26	-5	10	30	30	-40 to +85	40 Ld 5x5 TQFN	L40.5x5D
ISL98604IRTZ-EVZ	Evaluation Board													

NOTES:

1. For availability and lead time of devices with voltage and power-on timing combinations not listed in the table, please contact Intersil Marketing via email at Consumer-All@intersil.com.
2. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL98604. For more information on MSL please see techbrief TB363.

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Absolute Maximum Ratings (T_A = +25°C)

DRVP to AGND and PGND . . . . -0.3V to +45V
FBP to AGND and PGND . . . . -0.3V to +36V
FBN to AGND and PGND . . . . +0.3V to -10V
SW1, SW2, SWI, and SWO . . . . -0.3V to +24V
PVIN1, PVIN2, AVIN, SWB1, SWB2, PHASE1, PHASE2, HAVDD, and EN to AGND and PGND. . . . . -0.3V to +18.6V
DRVN, VDC, VCORE, SS, PGOOD, SCL, SDA, and A0 to AGND and PGND . . . . -0.3V to +5.5V
Voltage between AGND and PGND. . . . . ±0.5V
All other pins to GND, AGND and PGND . . . . -0.5V to +5.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2.5kV
Machine Model (Tested per JESD22-A115-A). 200V
Charged Device Model (Tested per JESD22-C101). 750V
Latch Up (Tested per JESD-78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5x5 TQFN Package (Notes 5, 6)	32	2.4

Maximum Junction Temperature (Plastic Package) . . . .+150°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . . -40°C to +85°C
Supply Voltage . . . . 8.0V to 16.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = 12V, EN = VDC, AVDD = 16V, V_{ON} = 28V, V_{OFF} = -5V, HAVDD = 8.0V, VIO = 3.3V, VCORE = 1.0V. **Boldface limits apply over the operating temperature range, T_A = -40°C to +85°C, unless otherwise noted.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SUPPLY PINS						
P_{VIN} +SUP	Supply Voltage		**8**	12	**16.5**	V
IV_{IN} +SUP	Supply Current when Disabled	EN = 0V		1.25		mA
IV_{IN} +SUP	Supply Current when Enabled	EN = VDC, no loading on all channels		8		mA
IEN	Enable Input Bias Current	EN = 0		0.01	**0.1**	µA
		EN = VDC		10	**15**	µA
V_{LDO}	Internal LDO Output Voltage			4.5		V
AVDD BOOST						
V_{AVDD}	Output Voltage Range		**1.14*VIN**	16	**19.0**	V
ACC_{AVDD}	Output Voltage Accuracy	AVDD = 16V, I_{LOAD} = 100mA	**-2**		**2**	%
I_{SWPL_AVDD}	Switch Peak Current Limit	Boost Peak Current limit	**3.5**	4	**4.5**	A
EFF_{AVDD}	Peak Efficiency			93		%
I_{SWLK_AVDD}	Switch Leakage Current				**22**	µA
$r_{DS(ON)\_AVDD}$	Switch ON-Resistance	T_A = +25°C, I_{SW} = 500mA		0.125	0.19	Ω
DV_{AVDD}/DV_{IN}	Line Regulation	9.5V < PVIN < 13.5V, I_{LOAD} = 200mA,		0.08		%
DV_{AVDD}/DI_{OUT}	Load Regulation	100mA < I_{LOAD} < 500mA		0.5		%
D_{MAX_AVDD}	Maximum Duty Cycle	F_{OSC} = 750kHz	**82**	87		%
D_{MIN_AVDD}	Minimum Duty Cycle	F_{OSC} = 750kHz		12	**16**	%
F_{OSC_AVDD}	Oscillator Frequency	Internal OSC	**675**	750	**825**	kHz
AVDD DELAY SWITCH						
$r_{DS(ON)\_DLY}$	Switch ON-Resistance			0.15	**0.24**	Ω

Electrical Specifications V_{IN} = 12V, EN = VDC, AVDD = 16V, V_{ON} = 28V, V_{OFF} = -5V, HAVDD = 8.0V, VIO = 3.3V, VCORE = 1.0V. **Boldface limits apply over the operating temperature range, T_A = -40°C to +85°C, unless otherwise noted.** (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
I_{SWPL_DLY}	Switch Peak Current Limit		**2.3**	3.1	**3.8**	A
FET timeout	Delay FET Fault Timeout	I_{SWO} > I_{DLY}		1		ms
I_{SWPL_Immed}	Switch High Current Limit, Immediate Shut Down Once Triggered			6.0		A
I_{SWLK_DLY}	Leakage Current When Disabled	V_{IN} = 16.5V, V_{SWIN} = 19V, V_{SWO} = 0V, EN = 0V		5	**20**	µA
HAVDD SYNC BUCK						
V_{HAVDD}	Output Voltage Range	Internal feedback	**6.4**	8	**9.55**	V
ACC_{HAVDD}	Output voltage accuracy	HAVDD = 8V	**-1.6**		**1.6**	%
I_{SWPL_HAVDD}	Switching Peak Current Limit		**1**			A
I_{SWRL_HAVDD}	Lower Switch Reverse Current Limit		**0.65**	0.9	**1.15**	A
EFF_{HAVDD}	Peak Efficiency			93		%
$r_{DS(ON)\_U\_HAVDD}$	Upper Switch ON-Resistance	T_A = +25°C , I_{SW} = 500mA		0.3	0.37	Ω
$r_{DS(ON)\_L\_HAVDD}$	Lower Switch ON-Resistance	T_A = +25°C , I_{SW} = 500mA		0.3	0.37	Ω
I_{FB_HAVDD}	Feedback Input Current			11		µA
DV_{HAVDD}/DV_{IN}	Line Regulation	9.5V < PV_{IN} < 13.5V, I_{LOAD} = 200mA		0.3		%
DV_{HAVDD}/DI_{OUT}	Load Regulation	200mA < I_{LOAD} < 1000mA		0.3		%
I_{SWLK_HAVDD}	Switch Leakage Current	T_A = +25°C		5	20	µA
DMAX_HAVDD	Maximum Duty Cycle	F_{OSC} = 750kHz	**85**	90		%
D_{MIN_HAVDD}	Minimum Duty Cycle	F_{OSC} = 750kHz		15		%
F_{OSC_HAVDD}	Oscillator Frequency	Internal OSC	**675**	750	**825**	kHz
VIO BUCK						
V_{IO}	Output Voltage Range	Internal feedback	**3.0**	3.3	**3.7**	V
ACC_{VIO}	Output Voltage Accuracy	V_{IO} = 3.3V	**-2.25**		**2.25**	%
I_{VIO}	Output Current	Internal feedback		0.7		A
I_{SWPL_VIO}	Switch Peak Current Limit	Current limit	**2**			A
EFF_{VIO}	Peak Efficiency	See graphs and “Applications Information” on page 15 for component recommendations		86		%
$r_{DS(ON)\_VIO}$	Switch On-Resistance	T_A = +25°C, I_{SW} = 500mA		0.200	0.300	Ω
DV_{VIO}/DV_{IN}	Line Regulation	9.5V < PV_{IN} < 13.5V, I_{LOAD} = 200mA		0.3		%
DV_{VIO}/DI_{OUT}	Load Regulation	200mA < I_{LOAD} < 1000mA		0.3		%
I_{FB_VIO}	Feedback Input Current			2.5	**100**	nA
I_{SWLK_VIO}	Switch Leakage Current	T_A = +25°C		5	20	µA
D_{MAX_VIO}	Maximum Duty Cycle	F_{OSC} = 750kHz	**85**	86		%
D_{MIN_VIO}	Minimum Duty Cycle	F_{OSC} = 750kHz		10	**15.5**	%
F_{OSC_VIO}	Oscillator Frequency	Internal OSC	**675**	750	**825**	kHz
VCORE BUCK						
V_{CORE}	Output Voltage Range	Internal feedback	**0.9**	1.0	**2.4**	V
ACC_{VCORE}	Output Voltage Accuracy	V_{CORE} = 1.0V	**-2.5**		**2.5**	%

Electrical Specifications

V_{IN} = 12V, EN = VDC, AVDD = 16V, V_{ON} = 28V, V_{OFF} = -5V, HAVDD = 8.0V, VIO = 3.3V, VCORE = 1.0V. **Boldface limits apply over the operating temperature range, T_A = -40°C to +85°C, unless otherwise noted. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
I_{CORE}	Output Current			0.5		A
I_{SWPL_VCORE}	Switch Peak Current Limit	Current limit	**1**			A
EFF_{VCORE}	Peak Efficiency	See graphs and “Applications Information” on page 15 for component recommendations		86		%
$r_{DS(ON)\_U\_VCORE}$	Upper Switch ON-Resistance	T_A = +25°C , I_{SW} = 500mA		0.18		Ω
$r_{DS(ON)\_L\_VCORE}$	Lower Switch ON-Resistance	T_A = +25°C , I_{SW} = 500mA		0.18		Ω
DV_{VCORE}/DV_{IN}	Line Regulation of VCORE Buck	9.5V < PV_{IN} < 13.5V, I_{LOAD} = 200mA		0.1		%
DV_{VCORE}/DI_{OUT}	Load Regulation of VCORE Buck	200mA < I_{LOAD} < 500mA		0.3		%
I_{FB_VCORE}	Feedback Input Current	V_{VCORE} = 1.8V		5		µA
I_{SWLK_VCORE}	Switch leakage current			3	**10**	µA
D_{MAX_VCORE}	Maximum Duty Cycle	F_{OSC} = 3MHz	**85**	90		%
D_{MIN_VCORE}	Minimum Duty Cycle	F_{OSC} = 3MHz		8		%
F_{OSC_VCORE}	Oscillator Frequency	Internal OSC	**1.32**	1.50	**1.68**	MHz
V_{ON} LDO						
V_{VON}	Output Voltage Range	Low temperature	**19**	28	**34**	V
		High temperature	**17**	26	**32**	V
ACC_{VON}	Output Voltage Accuracy	V_{ON} = 28V	**-2.1**		**2.1**	%
DV_{ON}/DI_{OUT}	Load Regulation	I_{DRVP} = 60µA to 120µA with MMBT3906 PNP, related resistors are shown in the application circuit		0.64		%
DV_{ON}/DV_{IN}	Line Regulation	I_{DRVP} = 100µA, V_{IN} = 9.5V to 14V		0.5		%
I_{DRVP}	Positive Source Current (Max)	V_{FBP} = 1.15V, V_{DRVN} = 10V	**3**	6		mA
I_{LEAK_DRVP}	DRVP Off Leakage Current	V_{FBP} = 1.40V, V_{DRVN} = 30V		0.1	**10**	µA
V_{TCOMP_TH}(NOTE 2)	Threshold Voltage in Temp. Compensation			1.265		V
V_{TCOMP_HYST}	Hysteresis Voltage in Temp. Compensation	V_{REF} = 1.265V		20		mV
V_{OFF} LDO						
V_{VOFF}	Output Voltage Range		**-8.1**	-5	**-1.8**	V
ACC_{VOFF}	Output Voltage Accuracy	V_{OFF} = -5V	**-3.75**		**3.75**	%
I_{FBN}	LDO Input Bias Current	V_{FBN} = -5V		11		µA
DV_{OFF}/DI_{OUT}	Load Regulation	I_{DRVN} = 60µA to 120µA with MMBT3904 NPN, related resistors are shown in the application circuit, I_{OUT} = 200mA		2.7		%
I_{DRVN}	Negative Source Current	V_{FBN} = 0.6V, V_{DRVN} = -10V	**3**	5		mA
I_{LEAK_DRVN}	DRVN Off Leakage Current	V_{FBN} = 0.5V, V_{DRVN} = -6V		0.1	**10**	µA
LOGIC INPUTS						
V_{HI}	Logic “HIGH”	SCL, SDA, A0	**1.85**			V
		EN	**1.6**			V
V_{LO}	Logic “LOW”	SCL, SDA, A0			**0.85**	V
		EN			**0.675**	V

Electrical Specifications V_{IN} = 12V, EN = VDC, AVDD = 16V, V_{ON} = 28V, V_{OFF} = -5V, HAVDD = 8.0V, VIO = 3.3V, VCORE = 1.0V. **Boldface limits apply over the operating temperature range, T_A = -40°C to +85°C, unless otherwise noted. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
I_{LG_PD}	Logic Pin Pull-Down Current	V_{LG} > V_{LO}			**25**	µA
I^2C						
f_{SCL} (Note 8)	SCL Frequency				**400**	kHz
t_{IN} (Note 8)	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than max spec is suppressed			**50**	ns
t_{AA} (Note 8)	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of VO_LDO, until SDA exits the 30% to 70% of VO_LDO window			**900**	ns
t_{BUF} (Note 8)	Time the Bus Must Be Free before the Start of a New Transmission	SDA crossing 70% of VO_LDO during a STOP condition, to SDA crossing 70% of VO_LDO during the following START condition	**1300**			ns
t_{LOW} (Note 8)	Clock LOW Time	Measured at the 30% of VO_LDO crossing	**1300**			ns
t_{HIGH} (Note 8)	Clock HIGH Time	Measured at the 70% of VO_LDO crossing	**600**			ns
$t_{SU:STA}$ (Note 8)	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of VO_LDO	**600**			ns
$t_{HD:STA}$ (Note 8)	START Condition Hold Time	SDA falling edge crossing 30% of VO_LDO to SCL falling edge crossing 70% of VO_LDO	**600**			ns
$t_{SU:DAT}$ (Note 8)	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge cross 30% of V_{CC}	**100**			ns
$t_{HD:DAT}$ (Note 8)	Input Data Hold Time	From SCL falling edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	**0**		**900**	ns
$t_{SU:STO}$ (Note 8)	Stop Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge cross 30% of V_{CC}	**600**			ns
$t_{HD:STO}$ (Note 8)	Stop Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}	**600**			ns
t_{DH} (Note 8)	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	**0**			ns
t_R (Note 8)	SDA and SCL Rise Time	Depend on Load			**1000**	ns
$t_{SU:A}$ (Note 8)	nWR Condition Setup Time	From nWR rising/falling edge crossing 70/30% of V_{CC}, to SDA falling edge cross 30% of V_{CC} (START)	**600**			ns
$t_{HD:A}$ (Note 8)	nWR Data Hold Time	From SDA rising edge crossing 70% of V_{CC} (STOP) to nWR rising/falling edge crossing 70/30% of V_{CC} window	**800**			ns
t_F (Note 8)	SDA and SCL Fall Time				**300**	ns
Cb (Note 8)	I^2C Bus Capacitive Load				**400**	pF
C_{SDA} (Note 8)	Capacitance on SDA			5		pF
C_{SCL} (Note 8)	Capacitance on SCL	nWR = 0		5		pF
		nWR = 1		5		pF
t_{WP} (Note 8)	Non-volatile Write Cycle Time			12	**20**	ms
EEPROM						
t_{EEPROM}	EEPROM Programming Time	T_A = +25°C		90		ms
R_{EEPROM}	EEPROM Memory Retention	T_A = +25°C		88		kHrs

Electrical Specifications

V_{IN} = 12V, EN = VDC, AVDD = 16V, V_{ON} = 28V, V_{OFF} = -5V, HAVDD = 8.0V, VIO = 3.3V, VCORE = 1.0V. **Boldface limits apply over the operating temperature range, T_A = -40°C to +85°C, unless otherwise noted. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
C_{EEPROM}	EEPROM Read/Write Cycles	T_A = +25°C		1		kCyc
FAULT DETECTION THRESHOLD						
OVP	Overvoltage Protection Off Threshold to Shutdown IC			20.5		V
V_{UVLO}	Undervoltage Lock Out Threshold	PV_{IN} rising	**7.2**	7.5	**7.9**	V
		PV_{IN} falling	**6.0**	6.3	**6.6**	V
T_{OFF}	Thermal Shutdown All Channels	Temperature rising		140		°C
START-UP AND SOFT-START						
I_{SS_AVDD}	Soft-Start Current	C_{SS} = 47nF		6		µA
t_{SS_HAVDD}	Boost and HAVDD Buck Soft-Start Time	C_{SS} = 47nF		10		ms
t_{SS_VON}	Positive Charge Pump Soft-Start Period			6.4		ms
t_{SS_VOFF}	Negative Charge Pump Soft-Start Period	t_{SS_VOFF} = -1.6*V_{OFF}-15	**1.6**		**9**	ms
t_{DLY1}	Delay Time from VIO to /RST Start	From 90% of VIO	**0**	10		ms
t_{DLY2}	Delay Time from V_{OFF} to AVDD Start	From 90% of V_{OFF}	**0**	30		ms
t_{DLY3}	Delay Time from AVDD to V_{ON} Start	From 90% of AVDD	**0**	30		ms
POWER GOOD BLOCK						
V_{PGOOD}	PGOOD Output Low Voltage	IPGOOD = 1mA		0.007	**0.025**	V
I_{PGLEAK}	PGOOD Leakage Current	VPGOOD = 3V			**0.05**	µA

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Limits established by design or characterization but not production tested.

Typical Performance Curves

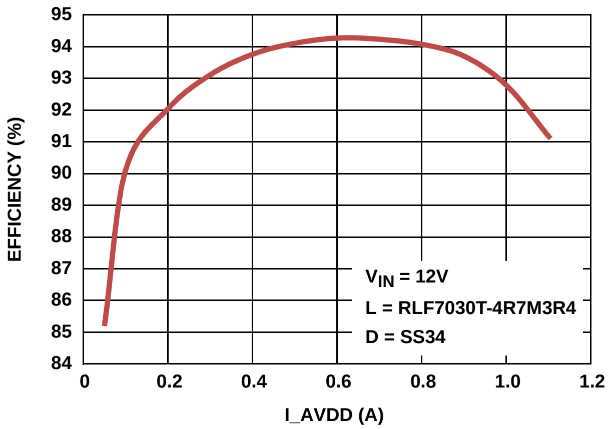


FIGURE 1. AVDD BOOST EFFICIENCY

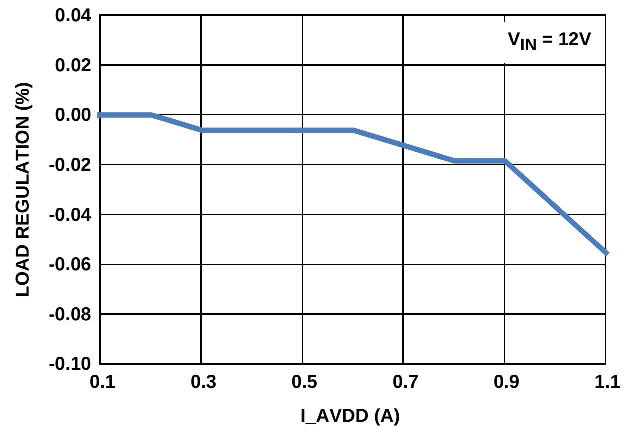


FIGURE 2. AVDD BOOST LOAD REGULATION

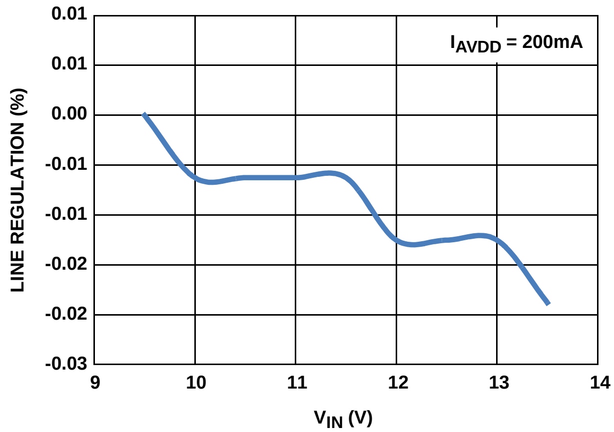


FIGURE 3. AVDD BOOST LINE REGULATION

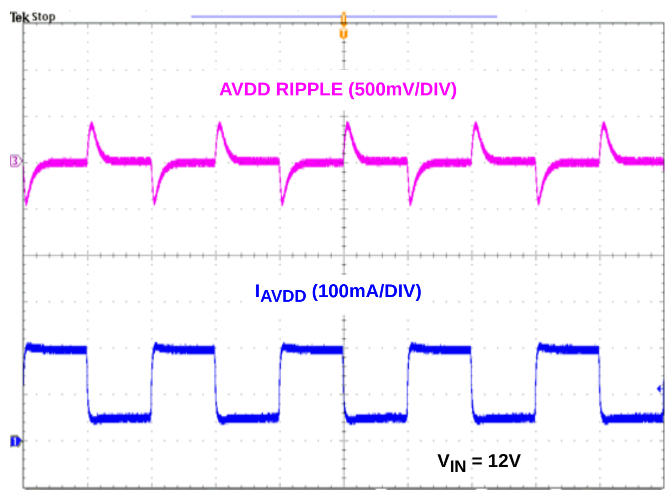


FIGURE 4. AVDD BOOST TRANSIENT RESPONSE

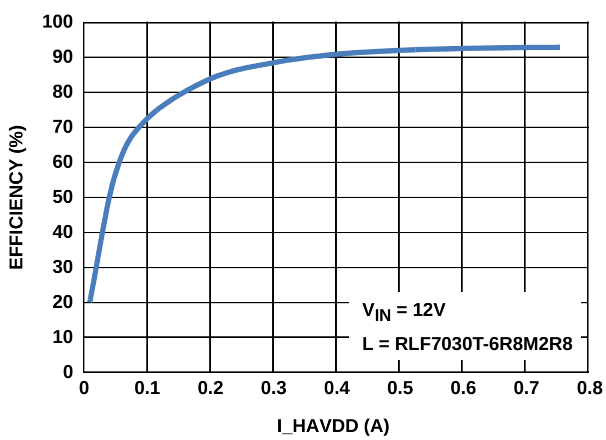


FIGURE 5. HAVDDBUCK EFFICIENCY

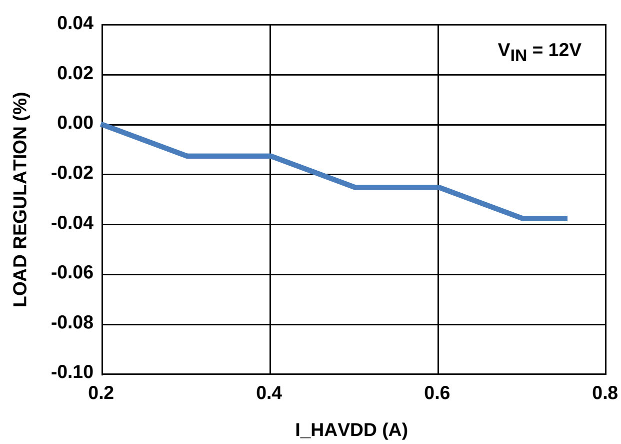


FIGURE 6. HAVDD BUCK REGULATION

Typical Performance Curves (Continued)

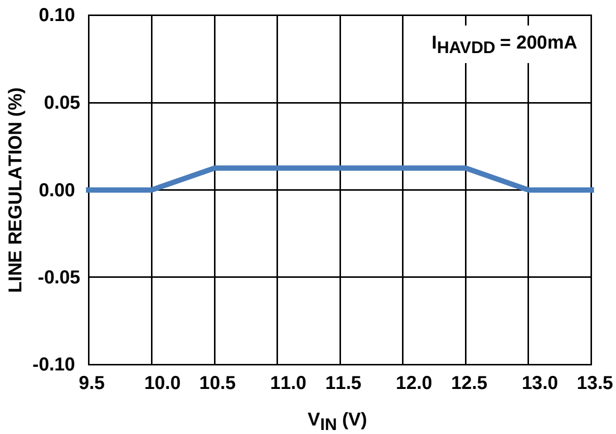


FIGURE 7. HAVDD BUCK LINE REGULATION

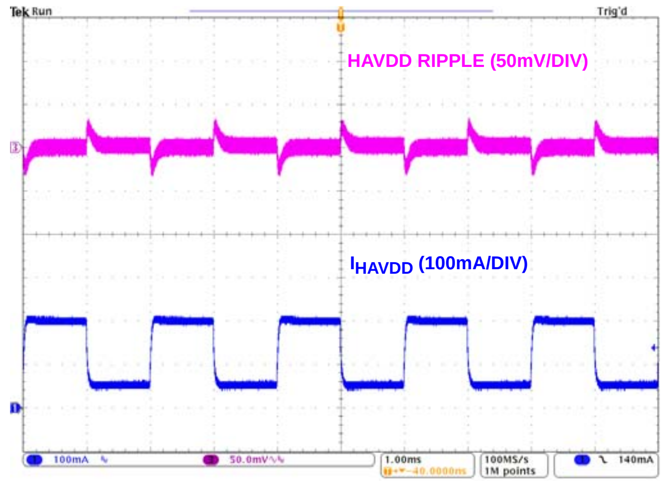


FIGURE 8. HAVDD BUCK TRANSIENT RESPONSE

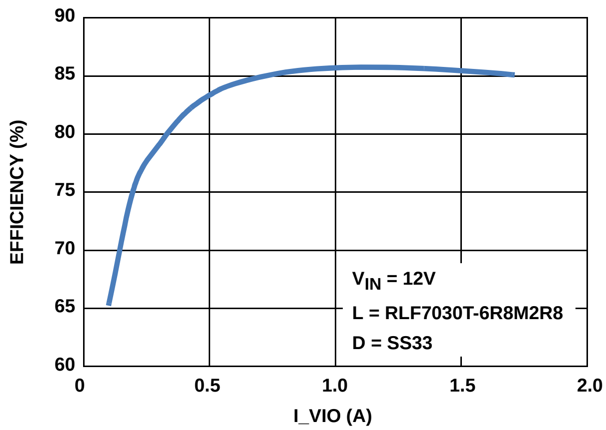


FIGURE 9. VIO BUCK EFFICIENCY

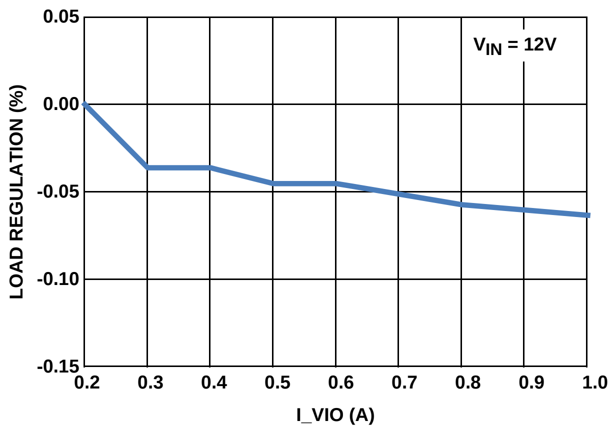


FIGURE 10. VIO BUCK LOAD REGULATION

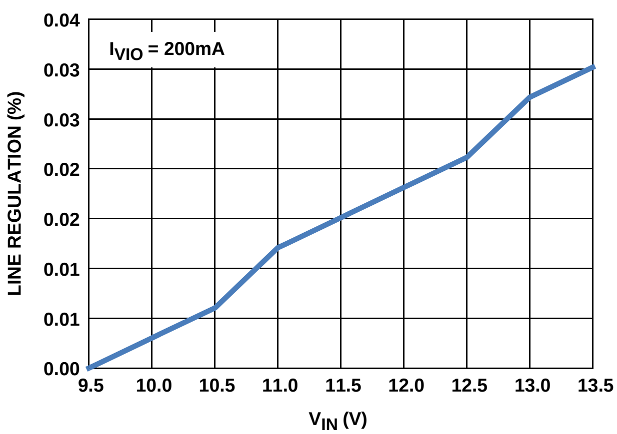


FIGURE 11. VIO BUCK LINE REGULATION

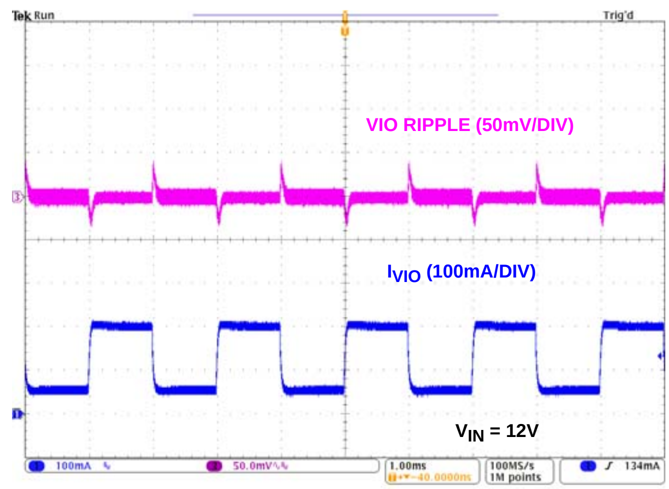


FIGURE 12. VIO BUCK TRANSIENT RESPONSE

Test Circuits and Waveforms

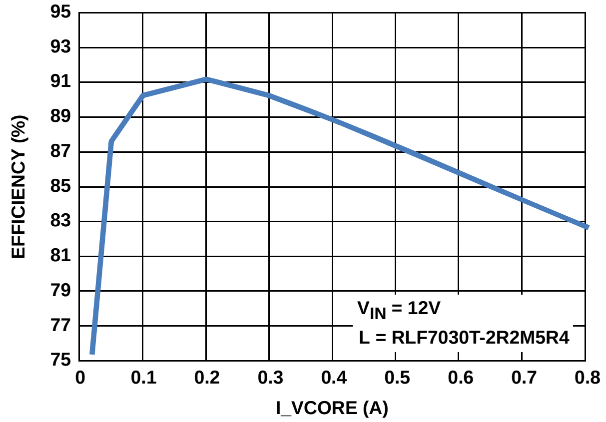


FIGURE 13. VCORE BUCK EFFICIENCY

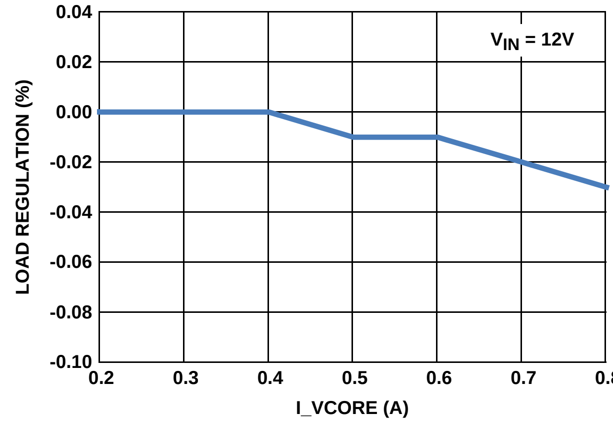


FIGURE 14. VCORE BUCK LOAD REGULATION

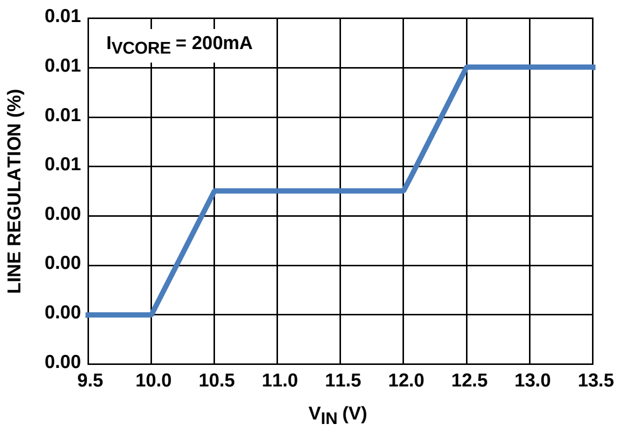


FIGURE 15. VCORE BUCK LINE REGULATION

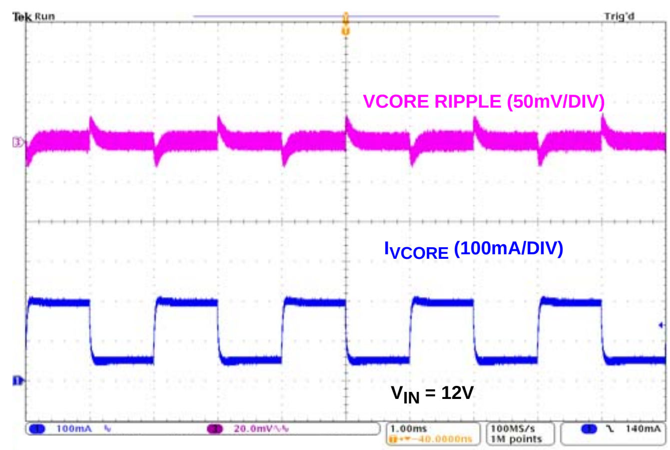


FIGURE 16. VCORE BUCK TRANSIENT RESPONSE

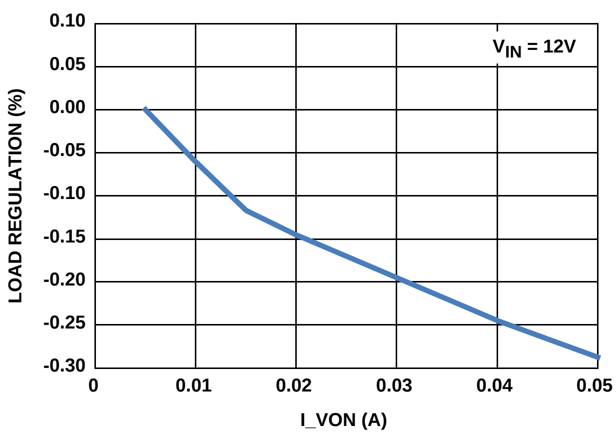


FIGURE 17. V_{ON} LOAD REGULATION

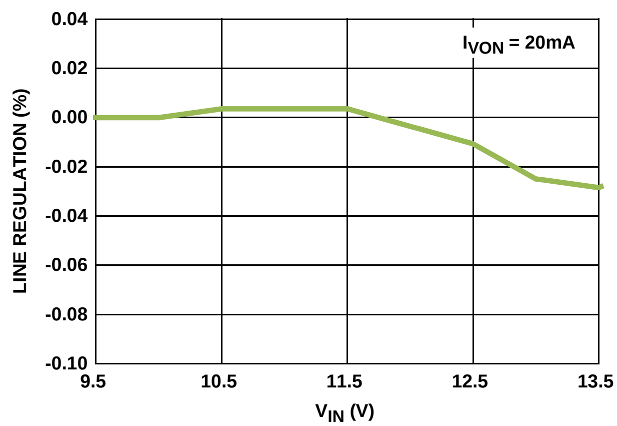


FIGURE 18. V_{ON} LINE REGULATION

Test Circuits and Waveforms (Continued)

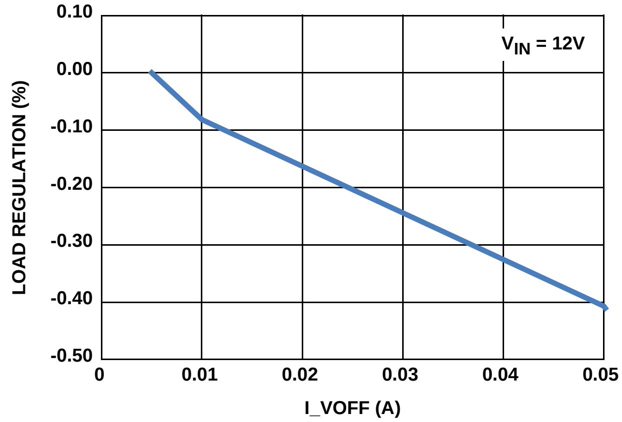


FIGURE 19. V_{OFF} LOAD REGULATION

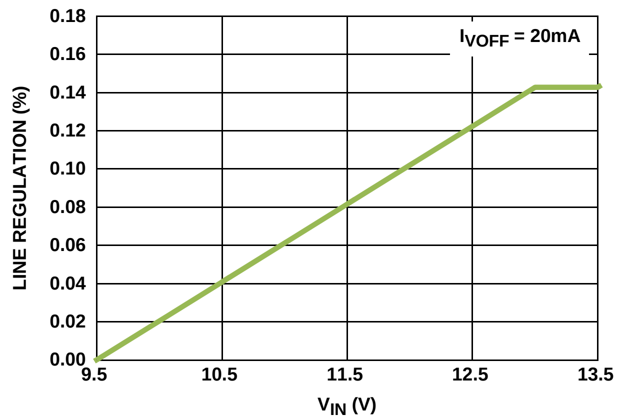


FIGURE 20. V_{OFF} LINE REGULATION

Applications Information

The ISL98604 provides a complete power solution for TFT LCD applications. The system consists of one boost converter to generate A_{VDD} voltage for column drivers, one asynchronous buck converter to provide voltage to logic circuit in the LCD panel, two synchronous bucks for core voltage and HAVDD, LDO controllers for V_{ON} and V_{OFF} charge pump outputs, and A_{VDD} delay FET. With the high output current capability, this part is ideal for LCD TV and monitor panel application.

Boost Converter

OPERATION

The AVDD boost converter is a current mode PWM converter operating at a fixed switching frequency (750kHz). It can operate in both discontinuous conduction mode (DCM) at light loads and continuous mode (CCM). In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{V_{boost}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

where D is the duty cycle of the switching MOSFET.

The boost converter uses a summing amplifier architecture for voltage feedback, current feedback, and slope compensation. A comparator looks at the peak inductor current cycle-by-cycle and terminates the PWM cycle if the current limit is triggered. Since this comparison is cycle based, the PWM output will be released after the peak current goes below the current limit threshold.

The current through the MOSFET is limited to 4A peak. This restricts the maximum output current (average) based on Equation 2:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 2)}$$

Where DI_L is peak to peak inductor ripple current, and is set by Equation 3. f_S is the switching frequency (750kHz).

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 3)}$$

ISL98604 uses internal feedback resistor divider to divide the output voltage down to the nominal reference voltage. The boost converter output voltage is programmable through I^2C control, which will be described in more detail in section "I^2C Control" on page 20.

INPUT CAPACITOR

An input capacitor is used to suppress the voltage ripple injected into the boost converter. A ceramic capacitor with low ESR should be chosen to minimize the ripple. The voltage rating of input capacitor should be larger than the maximum input voltage. Some capacitors are recommended in Table 1.

TABLE 1. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1206	TDK	C3216X7R1E106K
22µF/25V	1206	Murata	GRM31CR61E226KE15L

BOOST INDUCTOR

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. The selection of inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR) and size. Values of 3.3µH to 10µH are recommended to match the internal slope compensation as well as to maintain a good transient response performance. The inductor must be able to handle the average and peak currents shown in Equations 4 and 5:

$$I_{LAVG} = \frac{I_O}{(1-D)xEff} \quad \text{(EQ. 4)}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 5)}$$

Where Eff is the efficiency of the boost converter; 90% can be used in calculation as approximation.

Some inductors are recommended in Table 2.

TABLE 2. BOOST INDUCTOR RECOMMENDATION

INDUCTANCE	DCR (mΩ)	DIMENSIONS (mm)	VENDOR	PART NUMBER
4.7µH/ $3.4A_{PEAK}$	31	7.3x6.8x3.2	TDK	RLF7030T-4R7M3R4
4.7µH/ $4.5A_{PEAK}$	44.1	4.0x4.0x3.1	Coilcraft	XAL4030-472MEB
4.3µH/ $6.4A_{PEAK}$	11.2	12.9x12.9x4	SUMIDA	CDEP12D38NP-4R3M

RECTIFIER DIODE

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode must be higher than the maximum output voltage. Also the average/peak current rating of the selected Schottky diode must meet the output current and peak inductor current requirements. Table 3 shows some recommendations for boost converter diodes.

TABLE 3. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
SS34	40V/3A	DO-214	Fairchild
PMEG3030	30V/3A	SOD128	NXP

OUTPUT CAPACITOR

The output capacitors smooths the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_s} \qquad \text{(EQ. 6)}$$

The conservation of charge principle also indicates that, during the boost switch Off period, the output capacitor is charged with the inductor ripple current, minus a relatively small output current in boost topology. As a result, the user must select an output capacitor with low ESR and adequate input ripple current capability.

Table 4 shows some recommendations of output capacitors.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in Equation 6 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

TABLE 4. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/50V	1206	TDK	C3216X5R1H106K
22µF/25V	1210	Murata	GRM32ER71E226KE15L

COMPENSATION

The boost converter of ISL98604 can be compensated by a RC network connected from the COMP pin to ground. The resistance sets the high -frequency integrator gain for fast transient response and the capacitance sets the integrator zero to ensure loop stability. On the demo board 5.6k and 15nF RC network is used. Stability can be examined by repeatedly changing the load between 100mA and a max level that is likely to be used in the application. The A_{VDD} voltage should be examined with an oscilloscope set to AC and observe the amount of ringing when the load current changes.

SOFT-START

The soft-start is provided by an internal current source to charge the external soft-start capacitor. The ISL98604 ramps up the current limit from 0A up to the full value, as the voltage at the SS pin ramps up from 0.8V. Hence, the soft-start time is 2.9ms when the soft-start capacitor is 22nF, 6.3ms for 47nF and 13.3ms for 100nF.

AVDD DELAY SWITCH

ISL98604 integrates a disconnect switch for the AVDD boost output to disconnect V_{IN} from AVDD when the EN input is low or when DLY2 is not completed. When EN is taken high and DLY2 timing is finished, the integrated FET is turned on to connect power to the display. The AVDD delay switch circuitry constantly monitors both the current flowing through the switch and the voltage at SWOUT. The delay switch has two current limits: a low current limit and a high current limit. If the current flowing through delay switch is higher than the delay switch low current limit, the IC faults out after 1ms; if the delay switch high current limit is reached, the IC faults out immediately.

HAVDD Synchronous Buck Converter

OPERATION

HAVDD synchronous buck converter is a step down converter with a fixed switching frequency (750kHz) supplying voltage bias for gamma buffer in the LCD system. The ISL98604 integrates two MOSFETs to reduce external component count, save cost, and improve efficiency. In continuous current mode, the relationship between input voltage and output voltage is as shown in Equation 7:

$$\frac{HVDD}{V_{IN}} = D \qquad \text{(EQ. 7)}$$

where D is the duty cycle of the upper switching MOSFET. Because D is always less than 1, the output voltage of the HAVDD buck converter is lower than the input voltage.

The peak current limit of HAVDD buck converter is set to 0.9A, which restricts the maximum output current based on Equation 8:

$$I_{HAVDDMAX} = 0.9 - \frac{\Delta I_{P-P}}{2} \qquad \text{(EQ. 8)}$$

Where ΔI_{P-P} is the ripple current in the buck inductor as shown in Equation 9:

$$\Delta I_{P-P} = \frac{HAVDD}{L \cdot f_s} \cdot (1 - D) \qquad \text{(EQ. 9)}$$

Where L is the buck inductance, f_S is the switching frequency of HADD buck inductor (750kHz).

ISL98604 uses internal feedback resistor divider to divide the output HAVDD voltage down to the nominal reference voltage. The HAVDD voltage is programmable through I^2C control, which will be described in more detail in section "I^2C Control" on page 20.

INPUT CAPACITOR

Selection of input capacitance is important for input voltage ripple. A ceramic capacitor should be used because of its small ESR. Another important criteria when selecting input capacitor is that it should be able to support the maximum AC RMS current which occurs at D = 0.5 and maximum output current.

$$I_{ACRMS} = \sqrt{D \cdot (1 - D)} \cdot I_{HAVDD} \quad \text{(EQ. 10)}$$

Where I_{HAVDD} is the output current of the buck converter. Table 5 shows recommendations for input capacitors.

TABLE 5. HAVDD BUCK CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1206	TDK	C3216X7R1E106K
22µF/25V	1206	Murata	GRM31CR61E226KE15L

HAVDD BUCK INDUCTOR

The inductance is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. Increasing the inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to load transients. Taking all the factors into consideration, a 3.3µH to 10µH inductor range is recommended for the HAVDD buck converter. Besides the inductance, the DC resistance and the saturation current are also factors that need to be considered when choosing a buck inductor. Low DC resistance can help maintain high efficiency. Saturation current rating should be higher than the peak inductor current in the application. Table 5 shows some recommendations for the HAVDD buck inductor.

TABLE 6. HAVDD BUCK INDUCTOR RECOMMENDATION

INDUCTANCE	DCR (mΩ)	DIMENSIONS (mm)	VENDOR	PART NUMBER
6.8µH/ $3.6A_{PEAK}$	74.1	4.0x4.0x3.1	Coilcraft	XAL4030-682MEB
6.8µH/ $2.8A_{PEAK}$	45	7.3x6.8x3.2	TDK	RLF7030T-6R8M2R8

OUTPUT CAPACITOR

The output ripple and transient response typically drives the selection of an output capacitor. A 10µF or a 22µF ceramic capacitor is recommended (see Table 7).

TABLE 7. HAVDD BUCK OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
22µF/16V	0805	TDK	C2012X5R1C226K
10µF/25V	0805	TDK	C2012X5R1E106M

VIO Buck Converter

OPERATION

VIO buck converter is an asynchronous step down converter with a fixed switching frequency (750kHz) supplying power to the logic circuit of the LCD system. In continuous current mode, the relationship between input voltage and output voltage, is as shown in Equation 11.

$$\frac{VIO}{V_{IN}} = D \quad \text{(EQ. 11)}$$

where D is the duty cycle of the switching MOSFET.

The peak current limit of VIO buck converter is set to 2A, which restricts the maximum output current based on Equation 12:

$$I_{VIOMAX} = 2 - \frac{\Delta I_{P-P}}{2} \quad \text{(EQ. 12)}$$

Where ΔI_{P-P} is the ripple current in the buck inductor as shown in Equation 13:

$$\Delta I_{P-P} = \frac{VIO}{L \cdot f_S} \cdot (1 - D) \quad \text{(EQ. 13)}$$

Where L is the buck inductance, f_S is the switching frequency of VIO buck inductor.

ISL98604 uses internal feedback resistor divider to divide the output VIO voltage down to the nominal reference voltage. The VIO voltage is programmable through I^2C control, which will be described in more detail in section "I^2C Control" on page 20.

INPUT CAPACITOR

Selection of input capacitance is important for input voltage ripple. A ceramic capacitor should be used because of its small ESR. Another important criteria when selecting input capacitor is that it should be able to support the maximum AC RMS current, which occurs at D = 0.5 and maximum output current.

$$I_{ACRMS} = \sqrt{D \cdot (1 - D)} \cdot I_{VIO} \quad \text{(EQ. 14)}$$

Where I_{VIO} is the output current of the VIO buck converter. Table 8 shows recommendations for input capacitors.

TABLE 8. VIO BUCK CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/25V	1206	TDK	C3216X7R1E106K
22µF/25V	1206	Murata	GRM31CR61E226KE15L

VIO BUCK INDUCTOR

The inductance is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. Increasing the inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to load transients. Taking all the factors into consideration, a 3.3µH to 10µH inductor range is recommended for the VIO buck converter. Besides the inductance, the DC resistance and the saturation current are also factors that need to be considered when choosing a buck inductor. Low DC resistance can help maintain high efficiency. Saturation current rating should be higher than the peak inductor current in the application. Table 9 shows some recommendations for the VIO buck inductor.

TABLE 9. VIO BUCK INDUCTOR RECOMMENDATION

INDUCTANCE	DCR (mΩ)	DIMENSIONS (mm)	VENDOR	PART NUMBER
6.8µH/ $3.6A_{PEAK}$	74.1	4.0x4.0x3.1	Coilcraft	XAL4030-682MEB
6.8µH/ $2.8A_{PEAK}$	45	7.3x6.8x3.2	TDK	RLF7030T-6R8M2R8

VIO BUCK DIODE

A Schottky diode is recommended for its fast recovery time and low forward voltage. The reverse voltage rating should be higher than the maximum input voltage. The peak current rating should be higher than the current limit of the VIO switch, and the average current rating should be higher than the value given by Equation 15.

$$I_{AVG} = (1 - D)^{*}I_{VIO} \quad \text{(EQ. 15)}$$

Where I_{VIO} is the output current of the VIO buck converter. Table 10 shows diode recommendations..

TABLE 10. VIO BUCK DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	VENDOR
PMEG2020EJ	20V/2A	SOD323F	NXP Semiconductors
SS22	20V/2A	SMB	Fairchild Semiconductor

OUTPUT CAPACITOR

The output ripple and transient response typically drives the selection of output capacitor. 10µF or 22µF ceramic capacitors (Table 11) are recommended.

TABLE 11. VIO BUCK OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/10V	0805	TDK	C2012X7R1A106K
10µF/10V	0805	Murata	GRM21BR71A106KE51L
22µF/10V	0805	TDK	C2012X5R1A226M

VCORE Buck Converter

OPERATION

VCORE buck converter is a synchronous step-down converter with a fixed switching frequency (1.5MHz) to generate voltage and supply current to the core circuit of the LCD system. In continuous current mode, the relationship between input voltage and output voltage is as shown in Equation 16.

$$\frac{VCORE}{V_{IN}} = D \quad \text{(EQ. 16)}$$

where D is the duty cycle of the upper MOSFET and V_{IN} of the VCORE buck converter is the output voltage of the VIO buck converter.

The peak current limit of the VCORE buck converter is set to 1A, which restricts the maximum output current based on Equation 17:

$$I_{VCOREMAX} = 1 - \frac{\Delta I_{P\text{-}P}}{2} \quad \text{(EQ. 17)}$$

Where $\Delta I_{P\text{-}P}$ is the ripple current in the buck inductor, as shown in Equation 18:

$$\Delta I_{P\text{-}P} = \frac{VCORE}{L \cdot f_S} \cdot (1 - D) \quad \text{(EQ. 18)}$$

Where L is the buck inductance and f_S is the switching frequency of the VCORE buck inductor.

The ISL98604 uses internal feedback resistor divider to divide the output VCORE voltage down to the nominal reference voltage. The VCORE voltage is programmable through I^2C control, which will be described in more detail in section "I^2C Control" on page 20.

INPUT CAPACITOR

The input of the VCORE buck converter is internally connected to the output of VIO buck converter. Therefore, the output capacitors of the VIO buck converter also plays the role of input capacitor of the VCORE buck converter. Please refer to the "Output Capacitor" section of the "VIO Buck Converter" on page 17 for selection of input capacitors for the VCORE buck converter.

VCORE BUCK INDUCTOR

The inductance is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. Increasing the inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to load transients. Besides the inductance, the DC resistance and the saturation current are also factors that need to be considered when choosing a buck inductor. Low DC resistance can help maintain high efficiency. Saturation current rating should be higher than the peak inductor current in the application. Taking all the factors into consideration, 2.2µH inductors as shown in Table 12 are recommended for the VCORE buck inductor.

TABLE 12. VCORE BUCK INDUCTOR RECOMMENDATION

INDUCTANCE	DCR (mΩ)	DIMENSIONS (mm)	VENDOR	PART NUMBER
2.2µH/ $1.26A_{PEAK}$	55	3.0x2.5x1.2	TDK	VLF302512MT-2R2M
2.2µH/ $5.6A_{PEAK}$	35.2	4.0x4.0x2.1	Coilcraft	XAL4020-222ME

TABLE 12. VCORE BUCK INDUCTOR RECOMMENDATION

INDUCTANCE	DCR (mΩ)	DIMENSIONS (mm)	VENDOR	PART NUMBER
2.2µH/ $5.5A_{PEAK}$	12	7.3x6.8x3.2	TDK	RLF7030T-2R2M5R4

OUTPUT CAPACITOR

The output ripple and transient response typically drives the selection of output capacitor. 10µF or 22µF ceramic capacitors (Table 13) are recommended.

TABLE 13. VIO BUCK OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	VENDOR	PART NUMBER
10µF/6.3V	0603	MURATA	GRM188R60J106ME47D
10µF/6.3V	0402	TDK	C1005X5R0J106M
22µF/6.3V	0603	TDK	C1608X5R0J226M

V_{ON} Linear-Regulator Controller

The ISL98604 includes two independent linear-regulator controllers for positive output voltage (V_{ON}) and negative voltage (V_{OFF}). The V_{ON} and V_{OFF} linear-regulator controller subcircuit is shown in the “Typical Application Circuit” on page 2.

The V_{ON} power supply is used to power the positive supply of the row driver in the LCD panel. It consists of an external charge pump powered from the switching node (LX) of the boost converter, followed by a low dropout linear regulator (LDO_ON). The LDO_ON regulator uses an external PNP transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 5mA output current, which is sufficient for up to 50mA or more output current under the low dropout condition (forced beta of 10). Typical V_{ON} voltage supported by ISL98604 is programmable from +19V to +34V through I^2C control, which will be described in more detail in section “I^2C Control” on page 20.

V_{OFF} Linear-Regulator Controller and Charge Pump

The V_{OFF} power supply is used to power the negative supply of the row driver in the LCD panel. It consists of an external diode-capacitor charge pump powered from the switching node of the VIO buck converter, followed by a low dropout linear regulator (LDO_OFF). The LDO_OFF regulator uses an external NPN transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 5mA output current, which is sufficient for up to 50mA or more output current under the low dropout condition (forced beta of 10). Typical V_{OFF} voltage supported by ISL98604 is programmable from -8.1V to -1.8V through I^2C control, which will be described in more detail in section “I^2C Control” on page 20.

Calculation of the Linear Regulator Base-Emitter Resistors

For the pass transistor of the linear regulator, DC current gain (Hfe) and unity gain frequency (fT) are usually specified in the datasheet. The pass transistor adds a pole to the loop transfer function at fp = fT/Hfe. Therefore, in order to maintain phase margin at low frequency, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor R_{BE}, which increases the pole frequency to: fp = fT * (1 + Hfe * re/R_{BE})/Hfe, where re = KT/qIc. Therefore, choose the lowest value R_{BE} in the design as long as there is still enough base current (I_B) to support the maximum output current (I_C).

For example, the V_{ON} linear regulator. If a Fairchild MMBT3906 PNP transistor is used as the external pass transistor (Q7 in the application diagram), then for a maximum V_{ON} operating requirement of 50mA, the data sheet indicates Hfe_min = 60. The base-emitter saturation voltage is: Vbe_max = 0.7V.

For the ISL98604, the minimum drive current is: I_DRVP_min = 3mA.

The minimum base-emitter resistor, R_{BP}, can now be calculated as Equation 19:

$$\text{RBP\_min} = \text{VBE\_max}/(\text{I\_DRVP\_min - Ic/Hfe\_min} = ((0.7V)/(3mA - (50mA)/60)) = 325\Omega \quad \text{(EQ. 19)}$$

This is the minimum value that can be used so, we now choose a convenient value greater than this minimum value (e.g., 400W). Larger values may be used to reduce quiescent current, however, regulation may be adversely affected by supply noise if R_{BP} is made too high in value.

V_{ON}/V_{OFF} Charge Pump

Single or multiple stages of charge pumps are needed to generate output voltage higher than V_{BOOST} and negative voltage. The charge pumps can be driven by switching node of the boost converter and VIO buck converter, as shown in “Typical Application Circuit” on page 2.

The number of the charge pump stages can be calculated using Equations 20 and 21.

$$VOFF_{HEADROOM} = N \times V_{IN} - 2 \times N \times V_d - |VOFF| > 0 \quad \text{(EQ. 20)}$$

$$VON_{HEADROOM} = (N+1) \times AVDD - N \times V_d - VON > 0 \quad \text{(EQ. 21)}$$

Where N is the number of the charge pump stages, V_d is the forward voltage drop of one Schottky diode used in the charge pumps. V_d is varied with forward current and ambient temperature, so it should be the maximum value in the diode datasheet according to max forward current and lowest temperature in the application condition.

Once the number of the charge pump stages is determined, the relationship between output voltages and the maximum current that the charge pump can deliver can be calculated using Equations 22 and 23 as follows:

$$V_{OFF} = N \times (-VIN + 2 \times V_d + |I_{VOFF}|/(Freq \times C_{fly})) \quad \text{(EQ. 22)}$$

$$V_{ON} = AVDD + N \times (AVDD - 2 \times V_d - |I_{VON}|/(Freq \times C_{fly})) \quad \text{(EQ. 23)}$$

Where Freq is the switching frequency of the AVDD boost, C_fly is the flying capacitance (C64, C53 in the application diagram). I_{VON} and I_{VOFF} are the loadings of V_{ON} and V_{OFF}.

CHARGE PUMP OUTPUT CAPACITORS

A ceramic capacitor with low ESR is recommended. With ceramic capacitors, the output ripple voltage is dominated by the capacitance value. The capacitance value can be chosen by Equation 24:

$$C_{OUT} \geq \frac{I_{OUT}}{2 \times V_{RIPPLE} \times f_{OSC}} \quad \text{(EQ. 24)}$$

For V_{ON} charge pump, f_{OSC} is the switching frequency of boost converter; for V_{OFF} charge pump, f_{OSC} is the switching frequency of VIO buck converter.

V_{ON} Temperature Compensation

The ISL98604 can output two levels of V_{ON} voltages depending on the temperature. A voltage divider which consists of two resistors (R61 and R62) and a thermistor, as shown in the application diagram connected to TCOMP pin is used to determine the V_{ON} voltage.

Figure 21 shows that the V_{ON} voltage will be VON_LT when the TCOMP voltage is above the compensation threshold voltage. If the TCOMP voltage is below the compensation threshold voltage, the V_{ON} voltage will be VON_HT. There is a 20mV hysteresis between the threshold when TCOMP voltage rises and the threshold when TCOMP voltage falls. R61, R62, and thermistor values are selected to set the V_{ON} voltage at desired temperature. VON_LT and VON_HT are programmable through I^2C control, which will be described in more detail in section "I^2C Control" on page 20.

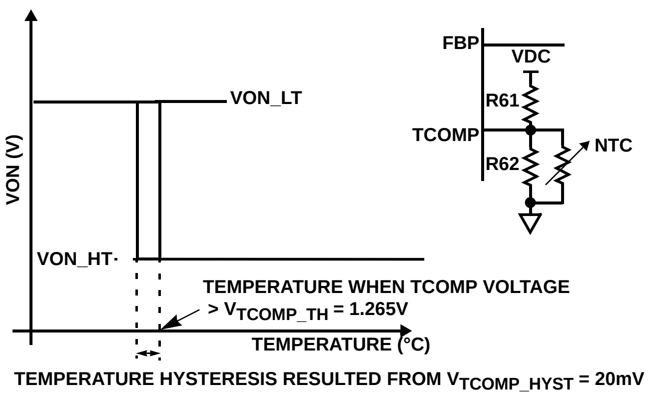


FIGURE 21. V_{ON} TEMPERATURE COMPENSATION

I^2C Control

The ISL98604 supports all rail outputs with fully programmable I^2C control. The programmed output values can be stored into EEPROM during the operation and read out.

The I^2C protocol defines any device that sends data on to the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, ISL98604 operates as a slave device in all applications. The fall and rise time of SDA and SCL signal should be in the range listed in Table 14. The capacitive load on the I^2C bus is also specified in Table 14.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

TABLE 14. I^2C INTERFACE SPECIFICATION

PARAMETER	MIN	TYP	MAX	UNITS
SDA and SCL Rise Time			1000	ns
SDA and SCL Fall Time			300	ns
I^2C Bus Capacitive Load			400	pF

PROTOCOL CONVENTIONS

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 22). On power-up, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. ISL98604 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 22). All I^2C interface must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is high (see Figure 22). An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 23).

WRITE OPERATION

To write into a DAC register (DR), it requires a START condition from the Master, followed by 7-bit device address ($010000A_0$), R/W bit (=0 when writing), a valid DAC register address Byte (01h-09h), a data byte, and a STOP condition. After each of the three bytes, the ISL98604 responds with an ACK. At this time, if the data byte is to be written only to volatile registers, the device enters its standby state.

Example: Writing 21h to register address 01h (HAVDD)

To write data in the DAC registers into EEPROM, it requires a START condition from the Master, followed by 7-bit device address, R/W bit (=0 when writing), Control Register (CR) address byte (FFh), a data byte of 80h to write data in DRs to EEPROM and a STOP condition. After each of the three bytes, ISL98604 responds with an ACK. If the Data Byte is to be written to EEPROM, ISL98604 begins its internal write cycle, which takes 25ms to finish. During the internal EEPROM write cycle, the device ignores transitions at the SDA and SCL pins and the SDA output is at high impedance state. When the internal EEPROM write cycle is completed, the ISL98604 enters its standby state.

Example: Writing current data in DRs into EEPROM.

READ OPERATION

To read from the DAC register (DR), it first requires to write 00 into the Control Register (CR) (FFh) to specify that the data is read from DR. Then it sends desired DR address to be read (00h-09h). Finally, it reads data from DR, which requires a START condition from Master, followed by 7-bit device address ($010000A_0$), R/W bit (= 1 when reading); the second byte contains the data read from the specified DR. Note that the Master will not acknowledge this byte. Finally, the last Master sends STOP condition.

Example: Reading data from DR address 06h (V_{OFF}).

To read from EEPROM first, it first requires to write 01 into the Control Register (CR) (FFh) to specify that the data is read from EEPROM. Then it sends the desired DR address to be read (00h-09h). Finally, it reads data from DR, which requires a START condition from Master, followed by 7-bit device address (010000A_0), R/W bit (=1 when reading); the second byte contains the data read from EEPROM. Note that the Master will not acknowledge this byte. Finally, the last Master sends STOP condition.

Example: Reading data from EEPROM address 06h (V_{OFF}).

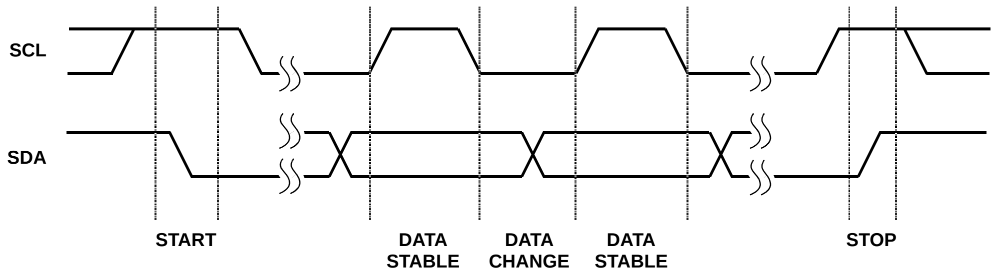


FIGURE 22. VALID DATA CHANGES, START, AND STOP CONDITION

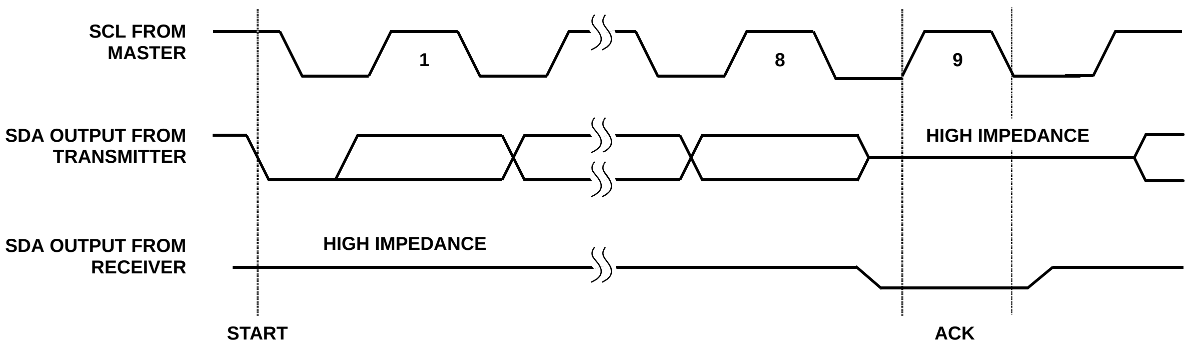


FIGURE 23. ACKNOWLEDGE RESPONSE FROM RECEIVER

REGISTER MAP AND REGISTER VALUES

Table 15 shows the address of the DAC registers and their default values. Table 16 shows the data format of each register. Table 17 shows the parameters corresponding to different register values.

TABLE 15. MEMORY MAP OF DAC REGISTER AND EEPROM

REGISTER	ADDRESS	DATA (VOLATILE/ NON-VOLATILE)	FACTORY DEFAULT (POWER-UP)
AVDD	00h	6-bit Non-volatile	21h
HAVDD	01h	6-bit Non-volatile	20h
VIO	02h	3-bit Non-volatile	03h
VCORE	03h	4-bit Non-volatile	01h
VON_LT	04h	4-bit Non-volatile	09h
VON_HT	05h	4-bit Non-volatile	09h
V_{OFF}	06h	6-bit Non-volatile	20h
DLY1	07h	3-bit Non-volatile	01h
DLY2	08h	3-bit Non-volatile	03h
DLY3	09h	3-bit Non-volatile	03h
CR	FFh	Volatile	00h

TABLE 16. DATA FORMAT OF DAC REGISTER AND EEPROM

AVDD (Default Data: 21h)

MSB							LSB
R	R	1	0	0	0	0	1

HAVDD (Default Data: 20h)

MSB							LSB
R	R	1	0	0	0	0	0

VIO (Default Data: 03h)

MSB							LSB
R	R	R	R	R	0	1	1

VCORE (Default Data: 01h)

MSB							LSB
R	R	R	R	0	0	0	1

VON_LT (Default Data: 09h)

MSB							LSB
R	R	R	R	1	0	0	1

VON_HT (Default Data: 09h)

MSB							LSB
R	R	R	R	1	0	0	1

V_{OFF} (Default Data: 20h)

MSB							LSB
R	R	1	0	0	0	0	0

DLY1 (Default Data: 01h)

MSB							LSB
R	R	R	R	R	0	0	1

DLY2 (Default Data: 03h)

MSB							LSB
R	R	R	R	R	0	1	1

DLY3 (Default Data: 03h)

MSB							LSB
R	R	R	R	R	0	1	1

Control Register (Default Data: 00h)

MSB							LSB
Write EEPROM Data	R	R	R	R	R	R	Read EEPROM or DR data

R: Reserved
<Contol Register Data>
0h: Read DAC register data only
01h: ead EEPROM data only
80h Write all DAC Register data to EEPROM

TABLE 17. PARAMETER VALUES CORRESPONDING TO REGISTER VALUES

ADDRESS		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h
STEP	HEX	AVDD (V)	HAVDD (V)	VIO (V)	VCORE (V)	VON_LT (V)	VON_HT (V)	VOFF (V)	DLY1 (ms)	DLY2 (ms)	DLY3 (ms)
0	00h	12.7	6.40	3.0	0.9	19	17	-1.8	0	0	0
1	01h	12.8	6.45	3.1	1.0	20	18	-1.9	10	10	10
2	02h	12.9	6.50	3.2	1.1	21	19	-2.0	20	20	20
3	03h	13.0	6.55	3.3	1.2	22	20	-2.1	30	30	30
4	04h	13.1	6.60	3.4	1.3	23	21	-2.2	40	40	40
5	05h	13.2	6.65	3.5	1.4	24	22	-2.3	50	50	50
6	06h	13.3	6.70	3.6	1.5	25	23	-2.4	60	60	60
7	07h	13.4	6.75	3.7	1.6	26	24	-2.5	70	70	70
8	08h	13.5	6.80		1.7	27	25	-2.6			
9	09h	13.6	6.85		1.8	28	26	-2.7			
10	0Ah	13.7	6.90		1.9	29	27	-2.8			
11	0Bh	13.8	6.95		2.0	30	28	-2.9			
12	0Ch	13.9	7.00		2.1	31	29	-3.0			
13	0Dh	14.0	7.05		2.2	32	30	-3.1			
14	0Eh	14.1	7.10		2.3	33	31	-3.2			
15	0Fh	14.2	7.15		2.4	34	32	-3.3			
16	10h	14.3	7.20					-3.4			
17	11h	14.4	7.25					-3.5			
18	12h	14.5	7.30					-3.6			
19	13h	14.6	7.35					-3.7			
20	14h	14.7	7.40					-3.8			
21	15h	14.8	7.45					-3.9			
22	16h	14.9	7.50					-4.0			
23	17h	15.0	7.55					-4.1			
24	18h	15.1	7.60					-4.2			
25	19h	15.2	7.65					-4.3			
26	1Ah	15.3	7.70					-4.4			
27	1Bh	15.4	7.75					-4.5			
28	1Ch	15.5	7.80					-4.6			
29	1Dh	15.6	7.85					-4.7			
30	1Eh	15.7	7.90					-4.8			
31	1Fh	15.8	7.95					-4.9			
32	20h	15.9	8.00					-5.0			
33	21h	16.0	8.05					-5.1			
34	22h	16.1	8.10					-5.2			
35	23h	16.2	8.15					-5.3			
36	24h	16.3	8.20					-5.4			
37	25h	16.4	8.25					-5.5			

TABLE 17. PARAMETER VALUES CORRESPONDING TO REGISTER VALUES (Continued)

ADDRESS		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h
STEP	HEX	AVDD (V)	HAVDD (V)	VIO (V)	VCORE (V)	VON_LT (V)	VON_HT (V)	VOFF (V)	DLY1 (ms)	DLY2 (ms)	DLY3 (ms)
38	26h	16.5	8.30					-5.6			
39	27h	16.6	8.35					-5.7			
40	28h	16.7	8.40					-5.8			
41	29h	16.8	8.45					-5.9			
42	2Ah	16.9	8.50					-6.0			
43	2Bh	17.0	8.55					-6.1			
44	2Ch	17.1	8.60					-6.2			
45	2Dh	17.2	8.65					-6.3			
46	2Eh	17.3	8.70					-6.4			
47	2Fh	17.4	8.75					-6.5			
48	30h	17.5	8.80					-6.6			
49	31h	17.6	8.85					-6.7			
50	32h	17.7	8.90					-6.8			
51	33h	17.8	8.95					-6.9			
52	34h	17.9	9.00					-7.0			
53	35h	18.0	9.05					-7.1			
54	36h	18.1	9.10					-7.2			
55	37h	18.2	9.15					-7.3			
56	38h	18.3	9.20					-7.4			
57	39h	18.4	9.25					-7.5			
58	3Ah	18.5	9.30					-7.6			
59	3Bh	18.6	9.35					-7.7			
60	3Ch	18.7	9.40					-7.8			
61	3Dh	18.8	9.45					-7.9			
62	3Eh	18.9	9.50					-8.0			
63	3Fh	19.0	9.55					-8.1			

NOTE: Shaded numbers are the factory default at power-up.

PROTECTIONS

The ISL98604 integrates overcurrent protection (OCP), overvoltage protection (OVP), and over-temperature protection (OTP). The protection threshold and the reaction of the chip are listed in Table 18.

TABLE 18. ISL98604 PROTECTION TABLE

CATEGORY	CHANNEL	TRIP LEVEL (TYP)	CONTINUED FAUTL TIME TO SHUTDOWN	CHIP REACTION	RE-ENABLE MECHANISM
OCP	AVDD	Switch peak current higher than 4A	NA	Terminate PWM	NA
	AVDD delay FET	IDS current higher than 3.1A during operation	1ms	Shut down whole IC	Power Cycle
		IDS current higher than 6A at start-up and normal operation	Immediately	Shut down whole IC	Power Cycle
	HAVDD	Switch peak current higher than 1A or lower switch peak current higher than 0.9A	NA	Terminate PWM	NA
	VIO	Switch peak current higher than 2A	NA	Terminate PWM	NA
	VCORE	Switch peak current higher than 1A	NA	Terminate PWM	NA
OVP	AVDD	Higher than 20.5V on SWI pin	Immediately	Shut down whole IC	Power Cycle
OTP	Junction Temp	Temperature higher than +140°C	Immediately	Shut down whole IC	Power Cycle

Start-Up Sequence

When VIN rising exceeds UVLO and EN is high, VIO and VCORE start-up. When VIO and VCORE reach 90% of the their target values, after a delay time of DLY1, PGOOD rises up and VOFF soft-starts; when VOFF reaches 90% of its target value, after a delay time of DLY2, AVDD and HAVDD start to rise up. The soft-start time of AVDD and HAVDD depends on the capacitance on the soft-start pin. When AVDD and HAVDD reach 90% of their target values, after a delay time of DLY3, V_{ON} starts to rise up. DLY1, DLY2 and DLY3 are programmable through I^2C control, which is described in section "I^2C Control" on page 20. The detailed start-up sequence is shown in Figure 24.

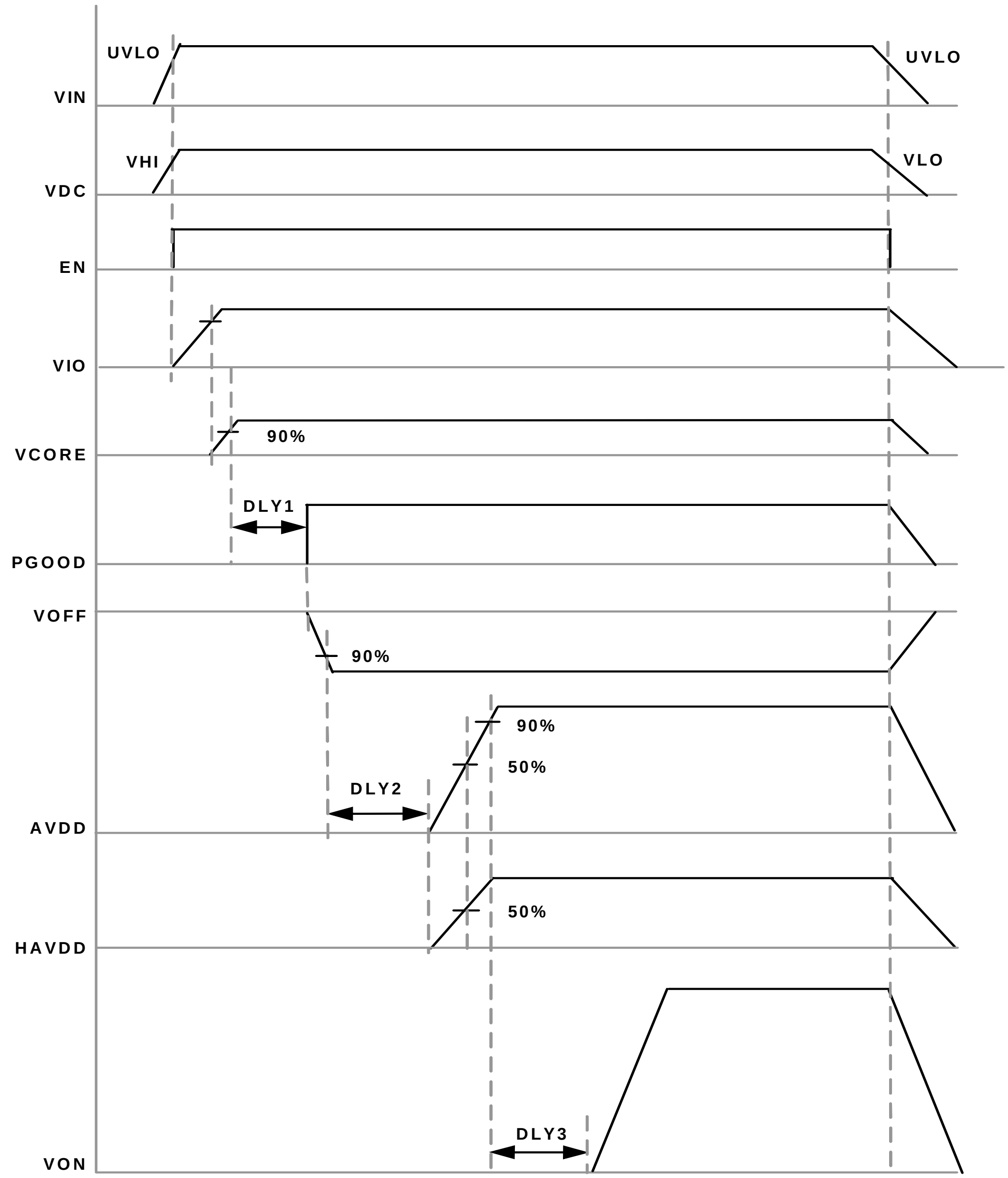
Layout Recommendation

PCB layout is critical especially at high switching frequency. The device's performance, including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout.

There are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{DC} and V_{REF} bypass capacitors close to the pins.
3. Reduce the loop with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from the LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at the ISL98604 exposed die plate area.
6. The exposed die plate, on the underside of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. Minimize feedback input track lengths to avoid switching noise pick-up.

A demo board is available to illustrate the proper layout implementation.



NOTES:

9. VIO and VCORE start when EN is enabled and 90% rising point will occur at the same time. The timing gap between VIO and VCORE at 90% rising point will be less than 3ms.
10. PGOOD and V_{OFF} will be triggered after VIO and VCORE rise and not before delay time DLY1.
11. AVDD and HAVDD start-up after delay time DLY2. Both are synchronized at 50% rising point.
12. V_{ON} will be triggered after AVDD and HAVDD rise and not before delay time DLY3.

FIGURE 24. ISL98604 START-UP SEQUENCE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 17, 2012	FN7687.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL98604

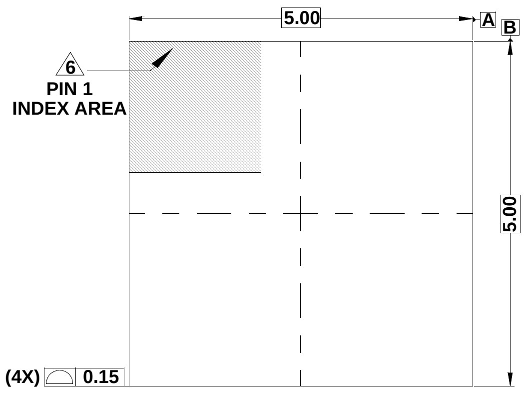
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

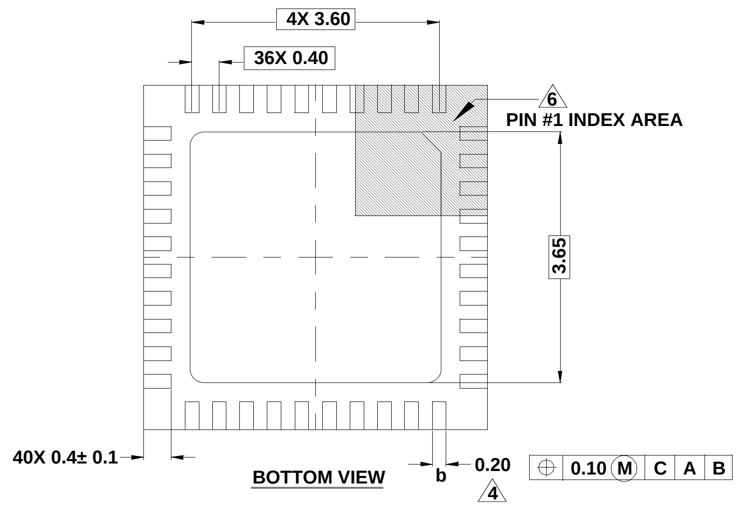
Package Outline Drawing

L40.5x5D

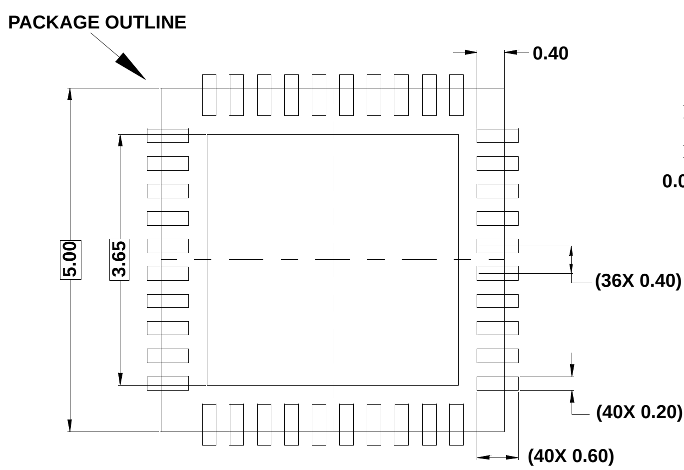
40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 9/10



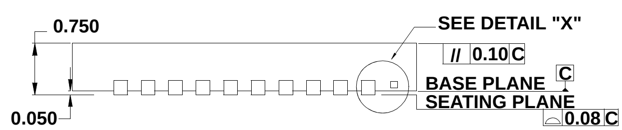
TOP VIEW



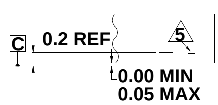
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1