High Performance 1A Linear Regulator with Programmable Current Limiting

ISL80101A

The ISL80101A is a low dropout voltage, single output LDO with programmable current limiting. This LDO operates from input voltages of 2.2V to 6V, and is capable of providing output voltages of 0.8V to 5V. Other custom voltage options are available upon request.

A sub-micron BiCMOS process is utilized for this product family to deliver the best in class analog performance and overall value. The programmable current limiting improves system reliability of end applications. An external capacitor on the soft-start pin provides an adjustable soft-starting ramp. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode.

This CMOS LDO will consume significantly lower quiescent current as a function of load compared to bipolar LDOs, which translates into higher efficiency and packages with smaller footprints. Quiescent current is modestly compromised to achieve a very fast load transient response.

Table 1 shows the differences between the ISL80101A and others in its family:

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

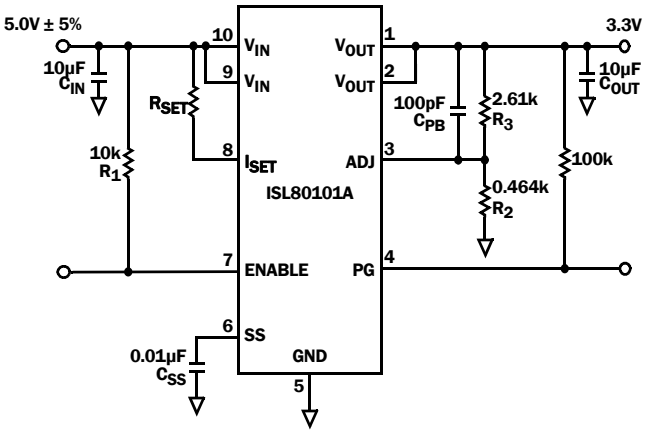
PART NUMBER	PROGRAMMABLE I_{LIMIT}	I_{LIMIT} (DEFAULT)	ADJ or FIXED V_{OUT}
ISL80101-ADJ	No	1.75A	ADJ
ISL80101	No	1.75A	1.8V, 2.5V, 3.3V, 5.0V
ISL80101A	Yes	1.62A	ADJ
ISL80121-5	Yes	0.75A	5.0V

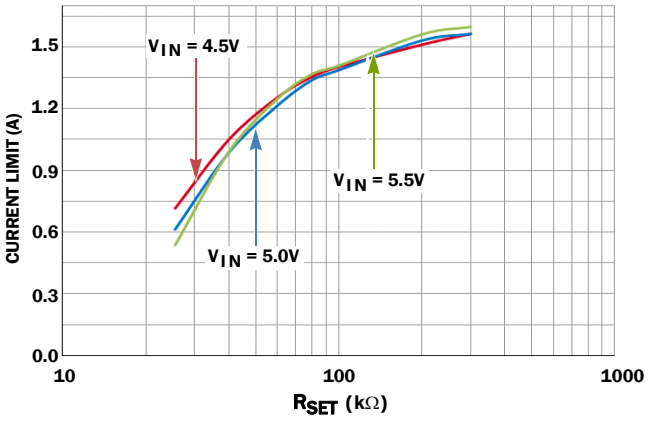
Features

- ±2% V_{ADJ} Accuracy Guaranteed Over Line, Load and T_J = -40°C to +125°C
- Very Low 212mV Dropout Voltage at V_{IN} = 4.5V
- High Accuracy Current Limit Programmable up to 1.75A
- Very Fast Transient Response
- 100µV_{RMS} Output Noise
- Power-Good Output
- Programmable Soft-Start
- Over-Temperature Protection
- Small 10 Ld DFN Package

Applications

- Telecommunications and Networking
- Medical Equipment
- Instrumentation Systems
- USB Devices
- Gaming
- Routers and Switchers

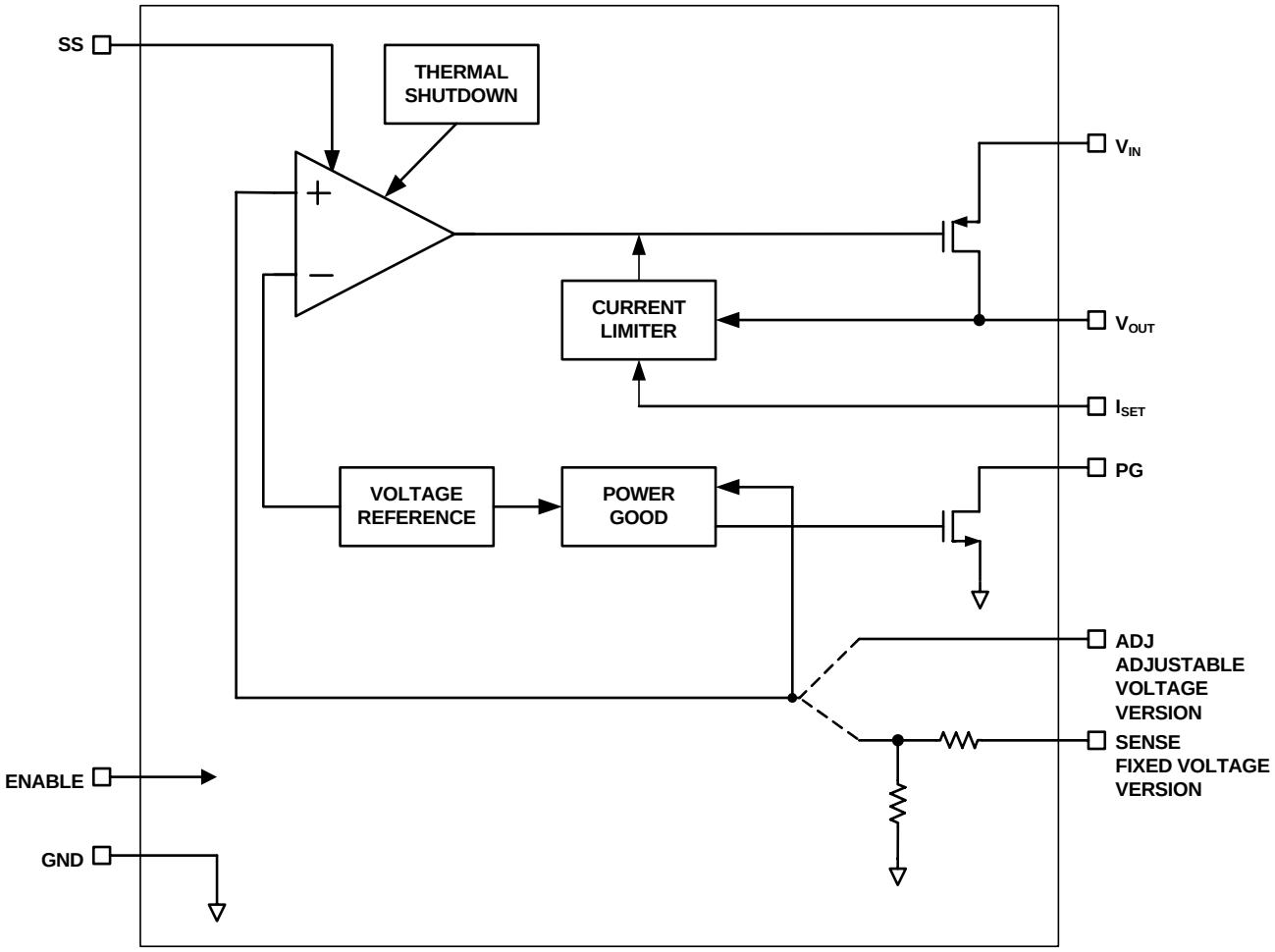




$$I_{LIMIT} = 1.62 - \frac{2.9x(2xV_{IN} - 1)}{R_{SET}(k\Omega)}$$

FIGURE 1. TYPICAL APPLICATION

Block Diagram



Ordering Information

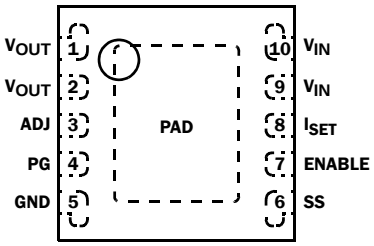
PART NUMBER (Notes 1, 2, 4)	PART MARKING	V_{OUT} VOLTAGE (Note 3)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL80101AIRAJZ	DZAC	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. The 1.5V, 3.3V and 5V fixed output voltages will be released in the future. Please contact Intersil Marketing for more details.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL80101A. For more information on MSL please see techbrief TB363.

Pin Configurations

ISL80101A
(10 LD 3X3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	V_{OUT}	Output voltage. A minimum 10uF X5R/X7R output capacitor is required for stability. See “External Capacitor Requirements” on page 8 for more details.
3	ADJ	LDO output feedback input. To adjust the output voltage, connect this pin to a resistive voltage divider from the V_{OUT} to GND.
4	PG	V_{OUT} in regulation signal. Logic low indicates V_{OUT} is not in regulation, and must be grounded if not used.
5	GND	Ground.
6	SS	External capacitor adjusts in-rush current.
7	ENABLE	V_{IN}-independent chip enable. TTL and CMOS compatible.
8	I_{SET}	Current limit setting. Current limit is 1.62A when this pin is left floating. This default value can be increased by tying R_{SET} to GND, or decreased by tying R_{SET} to V_{IN}. See “Programmable Current Limit” on page 7 for more details.
9, 10	V_{IN}	Input supply. A minimum of 10µF X5R/X7R input capacitor is required for stability. See “External Capacitor Requirements” on page 8 for more details.
-	EPAD	EPAD at ground potential. Soldering it directly to GND plane is required for thermal considerations. See “Power Dissipation and Thermals” on page 9 for more details.

Absolute Maximum Ratings (Note 7)

V_{IN} Relative to GND ..... -0.3V to +6.5V
V_{OUT} Relative to GND ..... -0.3V to +6.5V
PG, ENABLE, SENSE, SS, I_{SET}
Relative to GND ..... -0.3V to +6.5V
ESD Rating
Human Body Model (Tested per JEDEC) 2.5kV
Machine Model (Tested per JEDEC) 250V
Latch Up (Tested per JEDEC) ..... ±100mA @ +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 5, 6).	48	7

Maximum Junction Temperature (Plastic Package) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Pb-Free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions (Note 8)

Junction Temperature Range (T_J) ..... -40°C to +125°C
V_{IN} Relative to GND ..... 2.2V to 6V
V_{OUT} Range ..... 800mV to 5V
PG, ENABLE, SENSE, SS, I_{SET} Relative to GND ..... 0V to 6V
PG Sink Current 10mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%
8. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 3.3V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$
Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 7 and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
DC CHARACTERISTICS						
DC ADJ Pin Voltage Accuracy	V_{ADJ}	$V_{OUT} + 0.4V < V_{IN} < 6V$; $0A < I_{LOAD} < 1A$	**490**	500	**510**	mV
DC Input Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{OUT} + 0.4V < V_{IN} < 6.0V$, $V_{OUT} = 5.0V$		0.2	**1**	%
DC Output Load Regulation	ΔV_{OUT}	$0A < I_{LOAD} < 1A$	**-1**			%
Feedback Input Current		$V_{ADJ} = 0.5V$		0.01	1	µA
Ground Pin Current	I_Q	$I_{LOAD} = 0A$, $2.2V < V_{IN} < 6V$		3	**5**	mA
		$I_{LOAD} = 1A$, $2.2V < V_{IN} < 6V$		5	**7**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE = 0.2V, $V_{IN} = 6V$		0.2	**12**	µA
Dropout Voltage (Note 10)	V_{DO}	$I_{LOAD} = 1A$, $V_{IN} = 4.5V$, $V_{SENSE} = 0V$		90	**212**	mV
Output Current Limit	I_{LIMIT}	$V_{OUT} = 2V$, $4.5V < V_{IN} < 5.5V$, I_{SET} is floating		1.62		A
		$V_{OUT} = 2V$, $V_{IN} = 5.0V$, $R_{SET} = 25.5k\Omega$	0.540	0.640	0.740	A
Thermal Shutdown Temperature	TSD	$V_{OUT} + 0.4V < V_{IN} < 6V$		160		°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	$V_{OUT} + 0.4V < V_{IN} < 6V$		30		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, $I_{LOAD} = 1A$; $V_{IN} = 5.0V$		48		dB
		f = 120Hz, $I_{LOAD} = 1A$; $V_{IN} = 5.0V$		48		dB
Output Noise Voltage		$I_{LOAD} = 10mA$, BW = 300Hz < f < 300kHz		100		μV_{RMS}
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold	$V_{EN(HIGH)}$	$2.2V < V_{IN} < 6V$	**0.3**	0.8	**1.0**	V

Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 3.3V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$
Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Functional Description" on page 7 and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines established limits. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Hysteresis (Rising Threshold)	$V_{EN(HYS)}$	$2.2V < V_{IN} < 6V$	**10**	80	**200**	mV
ENABLE Pin Turn-on Delay	t_{EN}	$C_{OUT} = 10\mu F$, $I_{LOAD} = 1A$		80		µs
ENABLE Pin Leakage Current		$V_{IN} = 6V$, ENABLE = 3V			**1**	µA
SOFT START CHARACTERISTICS						
Reset Pull-Down Current	I_{PD}	$V_{IN} = 5.4V$, ENABLE = 0V, SS = 1V	**0.5**	1	**1.3**	mA
Soft Start Charge Current	I_{CHG}		**-3.3**	-2	**-0.8**	µA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			**75**	84	**92**	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		$I_{SINK} = 500\mu A$		47	**100**	mV
PG Flag Leakage Current		$V_{IN} = 6V$, PG = 6V		0.05	**1**	µA

NOTES:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
10. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the output is below its nominal regulation.

Typical Operating Performance

Unless otherwise noted: V_{IN} = 5V, V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

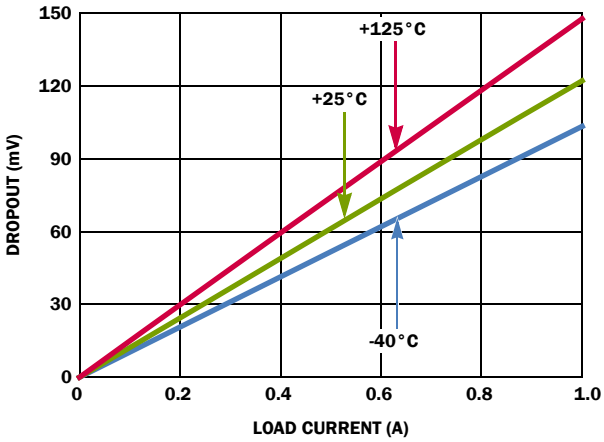


FIGURE 2. DROPOUT vs LOAD

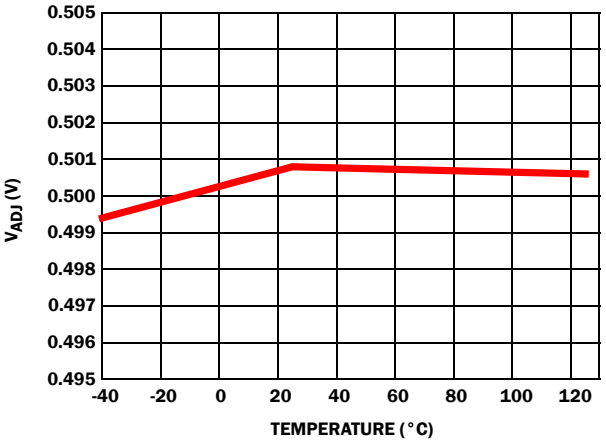


FIGURE 3. V_{ADJ} vs TEMPERATURE

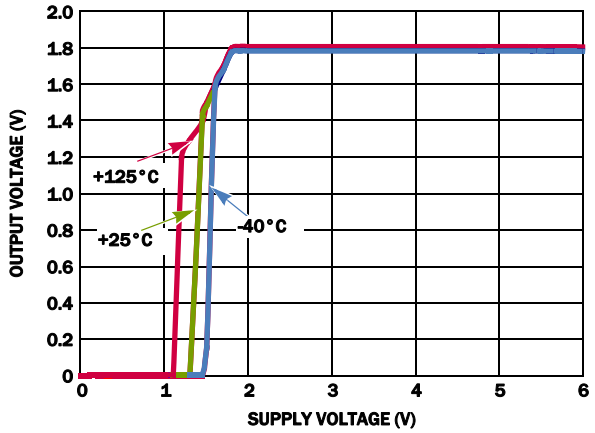


FIGURE 4. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

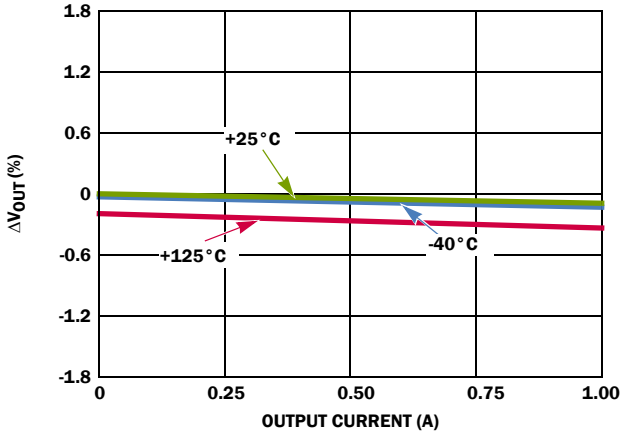


FIGURE 5. OUTPUT VOLTAGE vs OUTPUT CURRENT

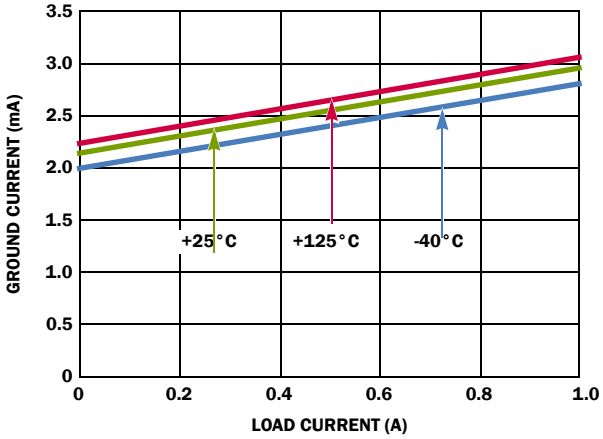


FIGURE 6. GROUND CURRENT vs LOAD CURRENT

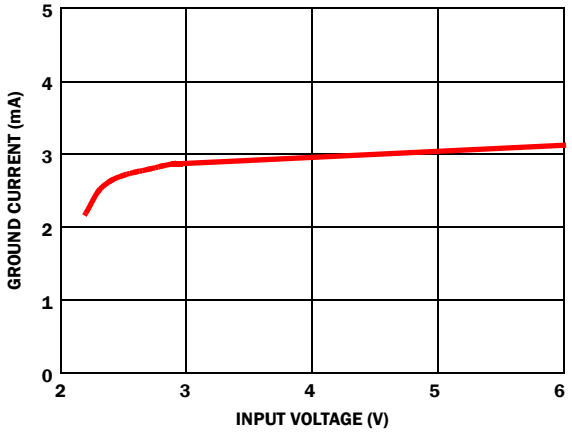


FIGURE 7. GROUND CURRENT vs SUPPLY VOLTAGE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 5V, V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

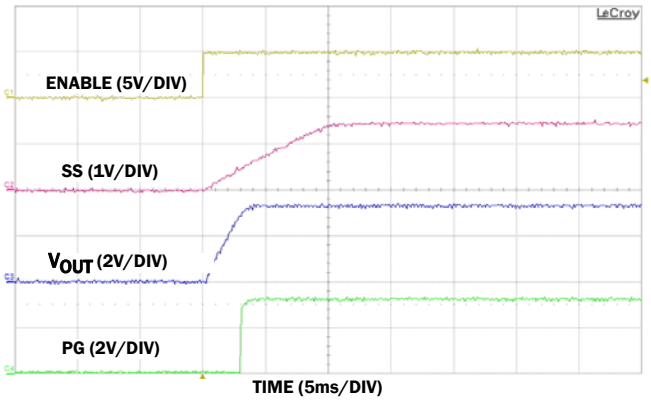


FIGURE 8. ENABLE START-UP

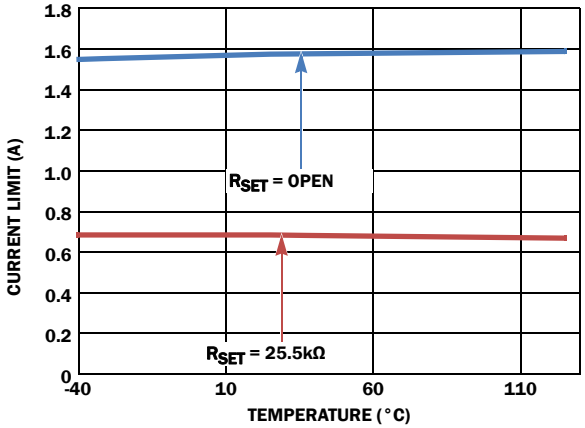


FIGURE 9. CURRENT LIMIT vs TEMPERATURE

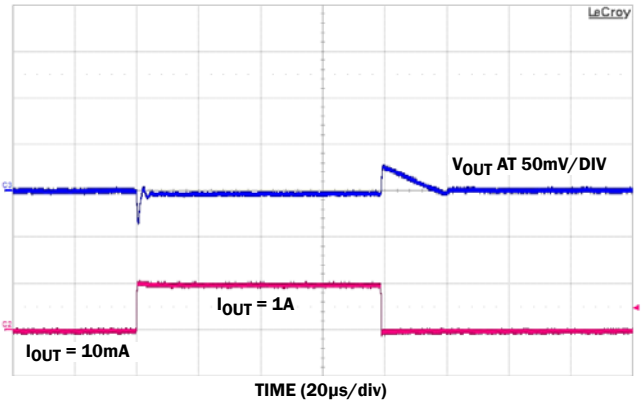


FIGURE 10. LOAD TRANSIENT RESPONSE

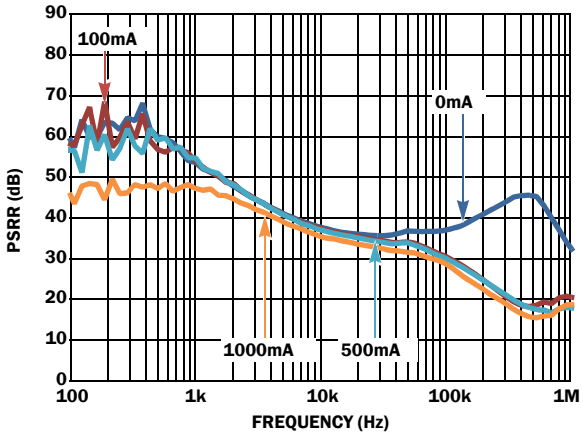


FIGURE 11. PSRR vs FREQUENCY

Functional Description

Input Voltage Requirements

ISL80101A is capable of delivering output voltages from 0.8V to 5.0V. Due to the nature of an LDO, V_{IN} must be some margin higher than V_{OUT} plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The generous dropout specification of this family of LDOs allows applications to design for a level of efficiency that can accommodate profiles smaller than the TO220/263.

Programmable Current Limit

The ISL80101A protects against overcurrent due to short-circuit and overload conditions applied to the output. When this happens, the LDO performs as a constant current source. If the short-circuit or overload condition is removed, the output returns to normal voltage regulation operation.

The current limit is set at 1.62A by default when the I_{SET} pin is left floating.

This limit can be increased by tying a resistor R_{SET} from the I_{SET} pin to ground. The current limit is determined by R_{SET} as shown in Equation 1. Do not short this pin to ground. Increasing the current limit past 1.75A may cause damage to the part and is highly discouraged.

$$I_{LIMIT} = 1.62 + \frac{2.9}{R_{SET}(k\Omega)} \quad \text{(EQ. 1)}$$

The current limit can be decreased from the 1.62A default by tying R_{SET} from the I_{SET} pin to V_{IN}. The current limit is then determined by both R_{SET} and V_{IN} following Equation 2.

$$I_{LIMIT} = 1.62 - \frac{2.9 \times (2 \times V_{IN} - 1)}{R_{SET}(k\Omega)} \quad \text{(EQ. 2)}$$

Figure 12 shows the relationship between R_{SET} and the current limit when R_{SET} is tied from the I_{SET} pin to V_{IN} for various V_{IN} values.

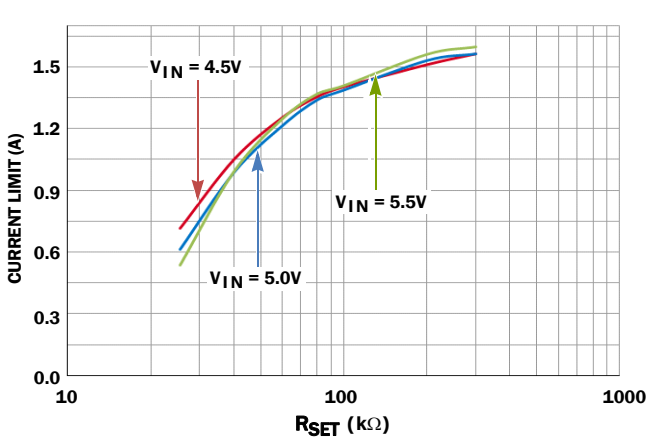


FIGURE 12. CURRENT LIMIT vs RSET AT DIFFERENT V_{IN}

Enable Operation

The ENABLE turn-on threshold is typically 800mV with 80mV of hysteresis. An internal pull-up or pull-down resistor to change these values is available upon request. As a result, this pin must not be left floating, and should be tied to V_{IN} if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the ENABLE pin. The ENABLE pin may be connected directly to V_{IN} for applications with outputs that are always on.

Power-Good Operation

PG is a logic output that indicates the status of V_{OUT}, current limit tripping, and V_{IN}. The PG flag is an open-drain NMOS that can sink up to 10mA during a fault condition. The PG pin requires an external pull-up resistor typically connected to the V_{OUT} pin. The PG pin should not be pulled up to a voltage source greater than V_{IN}. PG goes low when the output voltage drops below 84% of the nominal output voltage, the current limit faults, or the input voltage is too low. PG functions during shutdown, but not during thermal shutdown. For applications not using this feature, connect this pin to ground.

Soft-Start Operation

The soft-start circuit controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS pin to ground. An internal 2µA current source charges up this C_{SS} and the feedback reference voltage is clamped to the voltage across it. The start-up time is set by Equation 3.

$$T_{start} = \frac{(C_{SS} \times 0.5)}{2\mu A} \quad \text{(EQ. 3)}$$

Equation 4 determines the C_{SS} required for a specific start-up in-rush current, where V_{OUT} is the output voltage, C_{OUT} is the total capacitance on the output and I_{INRUSH} is the desired in-rush current.

$$C_{SS} = \frac{(V_{OUT} \times C_{OUT} \times 2\mu A))}{I_{INRUSH} \times 0.5V} \quad \text{(EQ. 4)}$$

The external capacitor is always discharged to ground at the beginning of start-up or enabling.

Table 2 shows the recommended C_{PB}, R_3 and R_2 for different output voltage and ceramic C_{OUT}.

Output Voltage Selection

An external resistor divider is used to scale the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.8V and 5V. An external resistor divider, R_2 and R_3, is used to set the output voltage as shown in Equations 5 and 6. Please see Table 2 on page 9 for recommended values of R_2 and R_3.

$$V_{OUT} = 0.5V \times \left(\frac{R_3}{R_2} + 1\right) \quad \text{(EQ. 5)}$$

$$R_3 = R_2 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad \text{(EQ. 6)}$$

External Capacitor Requirements

External capacitors are required for proper operation. Careful attention must be paid to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The ISL80101A applies state-of-the-art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming a minimum of 10µF X5R/X7R is used for local bypass on V_{OUT}. This output capacitor must be connected to the V_{OUT} and GND pins of the LDO with PCB traces no longer than 0.5cm.

There is a growing trend to use very-low ESR multilayer ceramic capacitors (MLCC) because they can support fast load transients and also bypass very high frequency noise from other sources. However, the effective capacitance of MLCCs drops with applied voltage, age, and temperature. X7R and X5R dielectric ceramic capacitors are strongly recommended as they typically maintain a capacitance range within ±20% of nominal voltage over full operating ratings of temperature and voltage.

Additional capacitors of any value in ceramic, POSCAP, alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

Phase Boost Capacitor

A small phase boost capacitor, C_{PB}, can be placed across the top resistor, R_3, in the feedback resistor divider network in order to place a zero at:

$$F_z = \frac{1}{2\pi \times R_3 \times C_{PB}} \quad \text{(EQ. 7)}$$

This zero increases the crossover frequency of the LDO and provides additional phase resulting in faster load transient response.

It is also important to note that the LDO stability and load transient are affected by the type of output capacitor used. For optimal result, empirical tuning is suggested for each specific application.

TABLE 2. RECOMMENDED C_{PB} FOR DIFFERENT V_{OUT} AND C_{OUT}

V_{OUT} (V)	R_3 (kΩ)	R_2 (kΩ)	C_{OUT} (µF)	C_{PB} (pF)
5.0	2.61	0.287	10	100
3.3	2.61	0.464	10	100
2.5	2.61	0.649	10	82
1.8	2.61	1.0	10	82
1.5	2.61	1.3	10	68
1.5	2.61	1.3	22	150
1.2	2.61	1.87	22	120
1.2	2.61	1.87	47	270
1.0	2.61	2.61	47	220
0.8	2.61	4.32	47	220

INPUT CAPACITOR

For proper operation, a minimum capacitance of 10µF X5R/X7R is required at the input. This ceramic input capacitor must be connected to the V_{IN} and GND pins of the LDO with PCB traces no longer than 0.5cm.

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions (Note 8)" on page 4. The power dissipation can be calculated by using Equation 8:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 8)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable power dissipation, as shown in Equation 9:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 9)}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, ensure that the power dissipation P_D, calculated from Equation 8, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heat-sink. The EPAD of this package must be soldered to the copper plane (GND plane). Figure 13 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

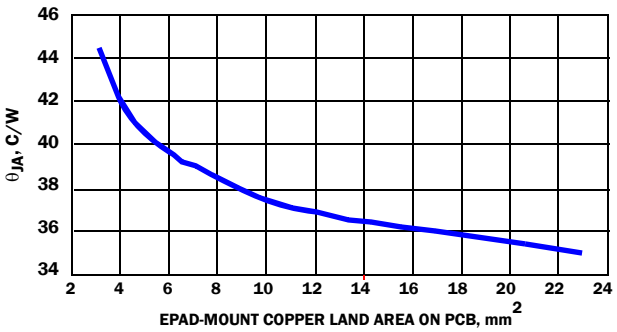


FIGURE 13. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

The power level and the thermal impedance of the package (+48°C/W for DFN) determine when the junction temperature exceeds the thermal shutdown temperature. In the event that the die temperature exceeds around +160°C, the output of the LDO will shut down until the die temperature cools down to about +130°C.

General PowerPAD Design Considerations

Figure 14 shows the recommended use of vias on the thermal pad to remove heat from the IC. This typical array populates the thermal pad footprint with vias spaced three times the radius distance from the center of each via. Small via size is advisable, but not to the extent that solder reflow becomes difficult.

All vias should be connected to the pad potential, with low thermal resistance for efficient heat transfer. Complete connection of the plated-through hole to each plane is important. It is not recommended to use "thermal relief" patterns to connect the vias.

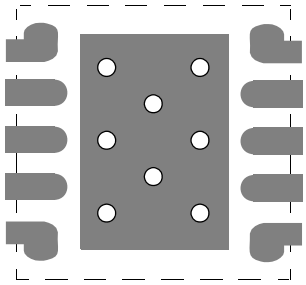


FIGURE 14. PCB VIA PATTERN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
9/19/11	FN7712.3	Table 1 on page 1 updated to include more information on Intersil's 1A LDO portfolio. Added standard MSL Note to “Ordering Information” (Note 4)
2/2/11	FN7712.2	1. On page 1, “Features” a."±1.8% Vout Accuracy Guaranteed..." changed to "±2% Vadj Accuracy Guaranteed..." 2. Figure 1 on page 1 a."Typical Applications" changed to "Typical Application" b."82pF" for Cpb changed to "100pF" 3. On page 3, Pin Number 8 a. On "Description" of ISET, change 2nd sentence from "Current limit is 0.75mA when..." to "Current limit is 1.62A when..." 4. On page 4, “Electrical Specifications” a."DC Input Line Regulation" given own line, added symbol, and changed test conditions b. “Feedback Input Current”, added typical "0.01" and max "1" with units "µA" 5. On page 5, “Electrical Specifications” a. “PG PIN CHARACTERISTICS” “VOUT PG Flag Threshold”, Typical "85" changed to "84" %Vout 7. On page 7, “Programmable Current Limit” a. Equation 1 changed to "Ilimit=1.62+..." b. Equation 2 changed to "Ilimit=1.62-..." 8. Added "The current limit can be decreased from the 0.75A default..." changed to "The current limit can be decreased from the 1.62A default..." on page 7, between Equation 1 and Equation 2 9. On page 7, beginning of last paragraph a. "Figure 11 shows the relationship..." changed to "Figure 12 shows the relationship..." 10. “External Capacitor Requirements” on page 8: a. "The ISL80121-5 applies..." changed to "The ISL80101A applies... 11. On page 4, “Electrical Specifications”, “DC CHARACTERISTICS”, “Output Current Limit” a. "VOUT = 2V, VIN = 5.5V, RSET = 25.5k " changed to ""VOUT = 2V, VIN = 5.0V, RSET = 25.5k " 12. On page 4, “Electrical Specifications”, “AC CHARACTERISTICS”, “Input Supply Ripple Rejection” a. "58db" typical changed to "48" b. "62dB" typical changed to "48" 13. On page 8, revised Figure 12. Updated same graphic on page 1 14. Throughout: All "VIN" changed to "V_{IN}" 15. Throughout: All "VOUT" changed to "V_{OUT}" 16. Throughout: All "RSET" changed to "R_{SET}" 17. Throughout: All "ISET" changed to "I_{SET}" 18. Throughout: All "EN" and "enable" changed to "ENABLE" 19. Throughout: All "PGOOD" changed to "PG" 20. “Block Diagram” on page 2, subscripted pin names for V_{IN}, V_{OUT}, I_{SET}. Changed PGOOD to PG 21. On page 3, EPAD Description a. "directly to GND plane is optional." Changed to "directly to GND plane is required for thermal considerations. See “Power Dissipation and Thermals” on page 9 for more details." 22. On page 1, in paragraph 2, "The programmable current limiting improves system reliability of applications" changed to "The programmable current limiting improves system reliability of end applications." 23. On page 1, “Features”, "Programmable Soft-starting" changed to "Programmable Soft-Start" 24. On page 4, “Electrical Specifications”, “DC CHARACTERISTICS”, "DC Output Voltage Accuracy" changed to “DC ADJ Pin Voltage Accuracy” 25. On page 5, Notes 10 and 11 deleted (they were not referenced in the spec table). 26. “Output Voltage Selection” on page 8, "An external resistor divider, R2 and R3, is used to set the output voltage as shown in Equation 5. The recommended value for R3 is 500Ω to 1kΩ. R2 is then chosen according to Equation 6." changed to "An external resistor divider, R2 and R3, is used to set the output voltage as shown in Equations 5 and 6. Please see Table 2 on page 9 for recommended values of R2 and R3." 29. Added “General PowerPAD Design Considerations” on page 9 30. Revised Figure 8
12/6/10	FN7712.1	Modified “Block Diagram” on page 2. In “Ground Pin Current” on page 4 Test Conditions: -Changed 1st line from "V_{OUT} + 0.4V < V_{IN} < 5V, VSENSE = 0V" to "I_{LOAD} = 0A, 2.2V < V_{IN} <6V" -Changed 2nd line from "V_{OUT} + 0.4V < V_{IN} < 6V, VSENSE = 0V" to "I_{LOAD} = 1A, 2.2V < V_{IN} <6V" Figure 2 “DROPOUT vs LOAD” on page 6: -Switched colors on 25°C and 125°C.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
11/29/10	FN7712.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL80101A

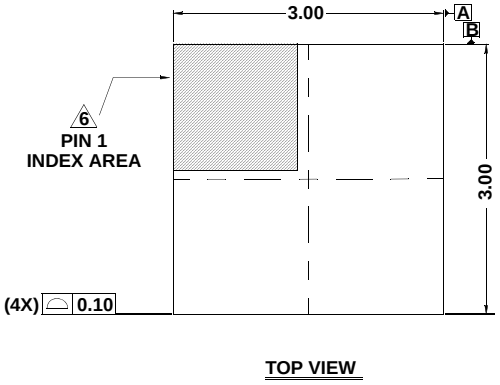
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

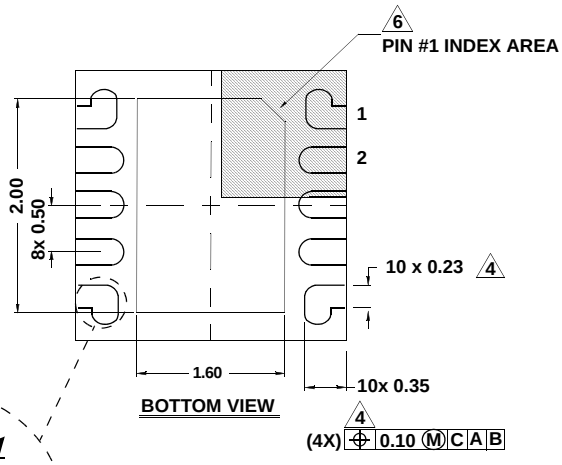
Package Outline Drawing

L10.3x3

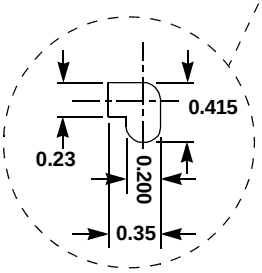
10 LEAD DUAL FLAT PACKAGE (DFN)
Rev 6, 09/09

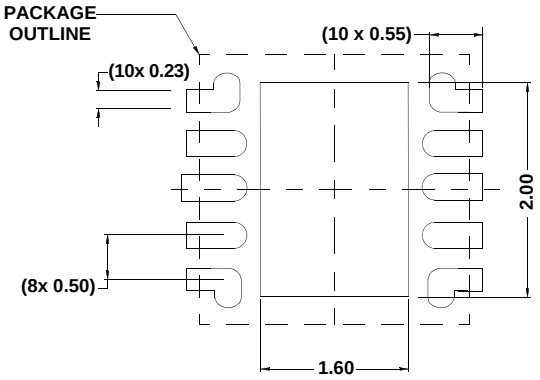


TOP VIEW

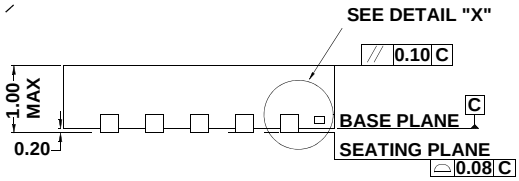


BOTTOM VIEW

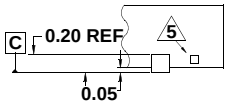




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.