HMC747LC3C

14 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

Typical Applications

The HMC747LC3C is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 14 Gbps
- Digital Logic Systems up to 14 GHz

Features

Supports High Data Rates: up to 14 Gbps

Differential & Single-Ended Operation

Fast Rise and Fall Times: 22 / 20 ps

Low Power Consumption: 264 mW typ.

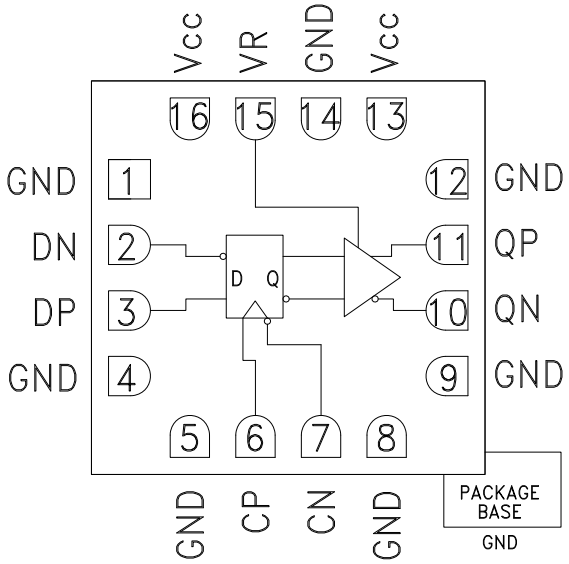
Programmable Differential
Output Voltage Swing: 700 - 1300 mV

Propagation Delay: 105 ps

Single Supply: +3.3 V

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC747LC3C is a D-Type Flip-Flop designed to support data transmission rates of up to 14 Gbps, and clock frequencies as high as 14 GHz. During normal operation, data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications.

All differential inputs to the HMC747LC3C are CML and terminated on-chip with 50 ohms to the positive supply, Vcc, and may be AC or DC coupled. The differential CML outputs are source terminated to 50 ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 ohm Vcc-terminated system, while DC blocking capacitors may be used if the terminating system is 50 ohms to ground. The HMC747LC3C also features an output level control pin, VR, which allows for loss compensation or signal-level optimazation. the HMC747LC3C operates from a single 3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vcc = 3.3 V, VR = 3.3 V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		3.0	3.3	3.6	V
Power Supply Current			80		mA
Maximum Data Rate			14		Gbps
Maximum Clock Rate			14		GHz
Input Voltage Range		Vcc - 1.5		Vcc + 0.5	V
Input Differential Range		0.1		2	Vp-p
Input Return Loss	Frequency <14 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			3.29		V

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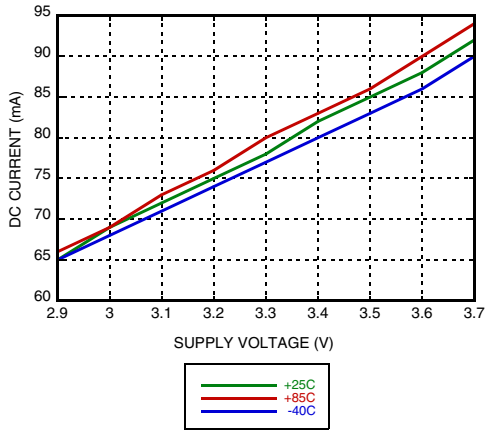
Electrical Specifications (continued)

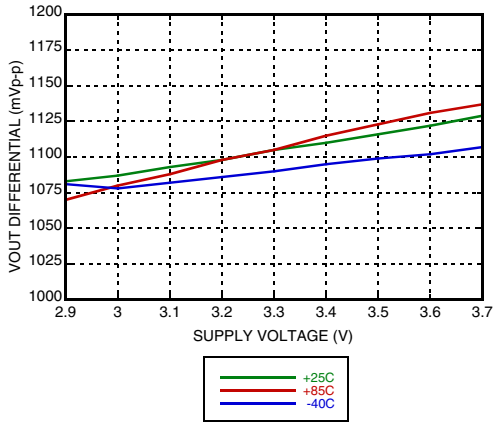
Parameter	Conditions	Min.	Typ.	Max	Units
Output Low Voltage			2.74		V
Output Rise / Fall Time	Differential, 20% - 80%		22 / 20		ps
Output Return Loss	Frequency <13 GHz		10		dB
Random Jitter Jr	rms			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		2		ps, p-p
Propagation Delay Clock to Data, td			105		ps
Clock Phase Margin	13 GHz		320		deg
Set Up & Hold Time, t_{SH}			6		ps
VR Pin Current	VR = 3.3 V		2		mA
VR Pin Current	VR = 3.7 V			3.5	mA

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 13 GHz, 2^{15}-1 PRBS input, and a single-ended output

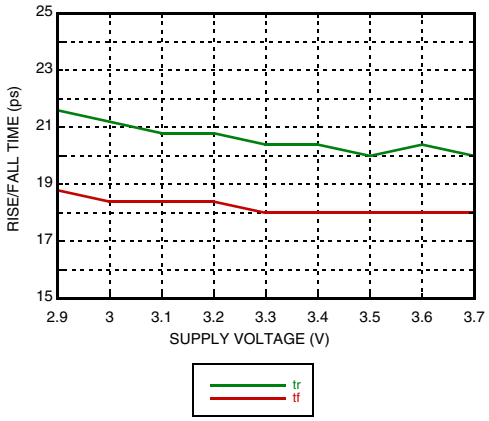
DC Current vs. Supply Voltage [1][2]



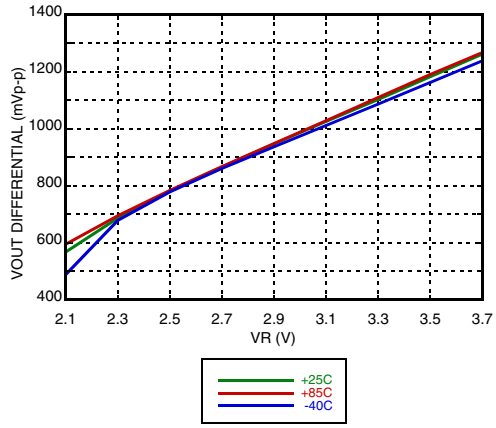
Output Differential Voltage vs. Supply Voltage [1][2]



Rise / Fall Time vs. Supply Voltage [1][2]



Output Differential Voltage vs. VR [1][2]



[1] VR = 3.3 V [2] Frequency = 13 GHz [3] Vcc = 3.3 V

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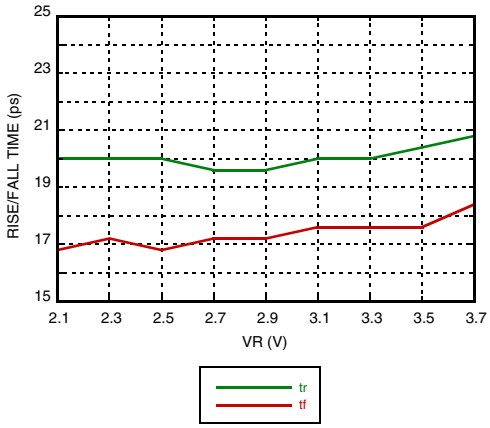
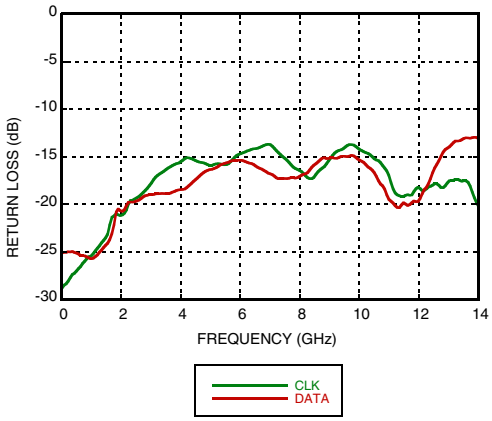
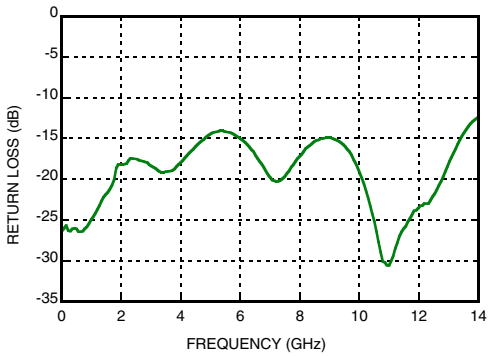
Rise / Fall Time vs. VR [1][2]



Input Return Loss vs. Frequency

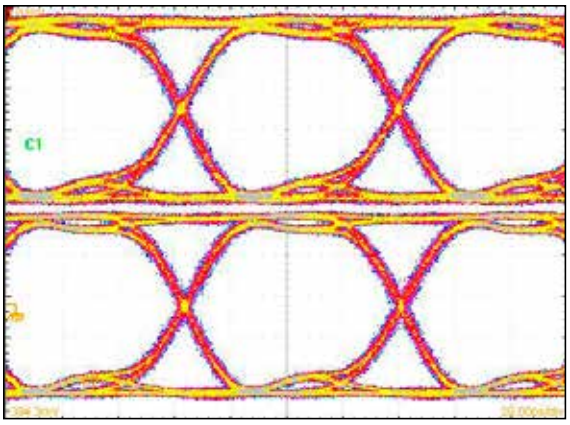


Output Return Loss vs. Frequency



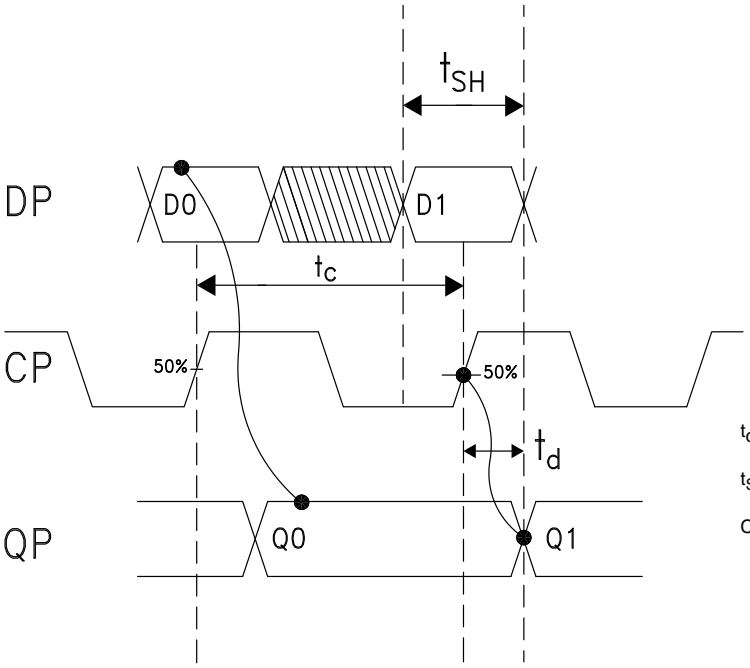
[1] Vcc = 3.3 V [2] Frequency = 13 GHz

Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 13 Gbps PN code.
Both output channels shown.
Device is AC coupled to scope.

Timing Diagram



$t_c = \frac{1}{f_{clock}}$

t_{SH} = Setup and Hold Time

CPM = Clock Phase Margin = $360° \frac{t_c - t_{SH}}{t_c}$

Truth Table

Input		Outputs
D	C	Q
L	L -> H	L
H	L -> H	H
Notes: D = DP - DN C = CP - CN Q = QP - QN	H - Positive voltage level L - Negative voltage level	

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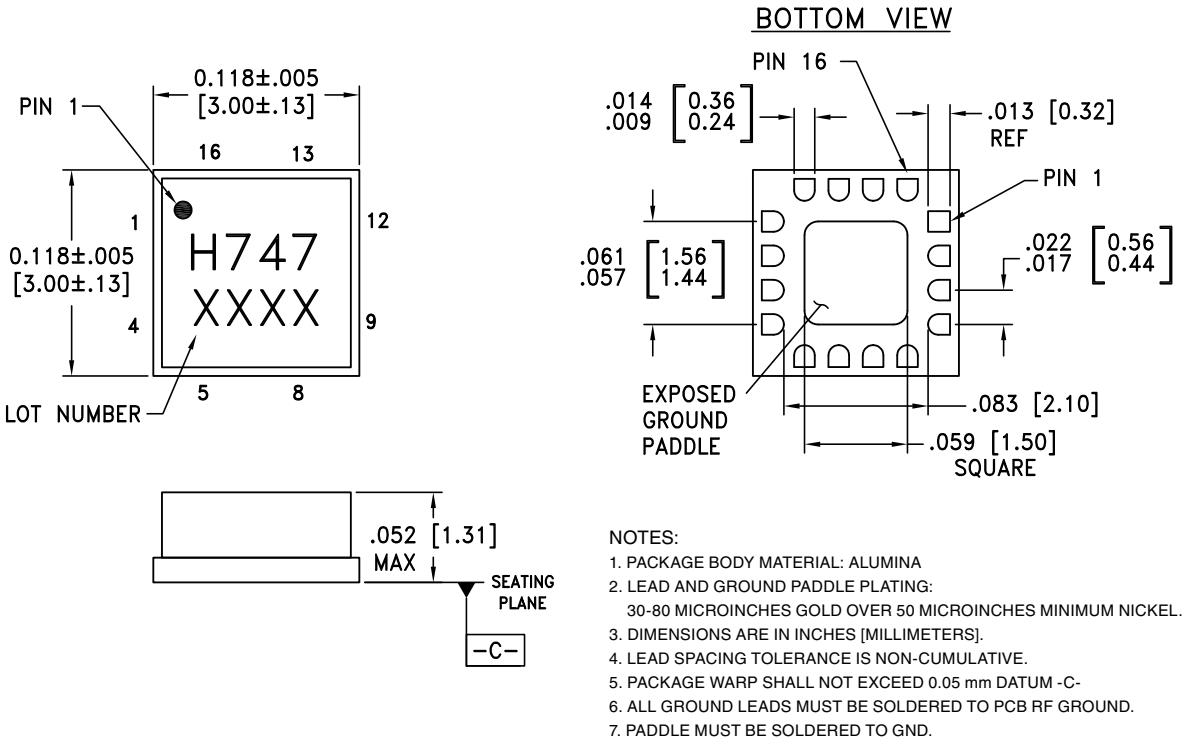
Absolute Maximum Ratings

Power Supply Voltage (Vcc)	Vcc -0.5 V to 3.75 V
Input Signals	Vcc - 2.0 V to Vcc + 0.5 V
Output Signals	Vcc - 1.5 V to Vcc + 0.5 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

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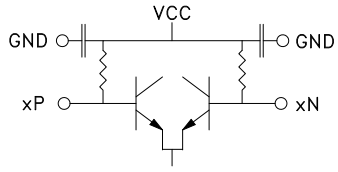
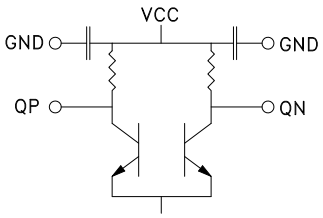
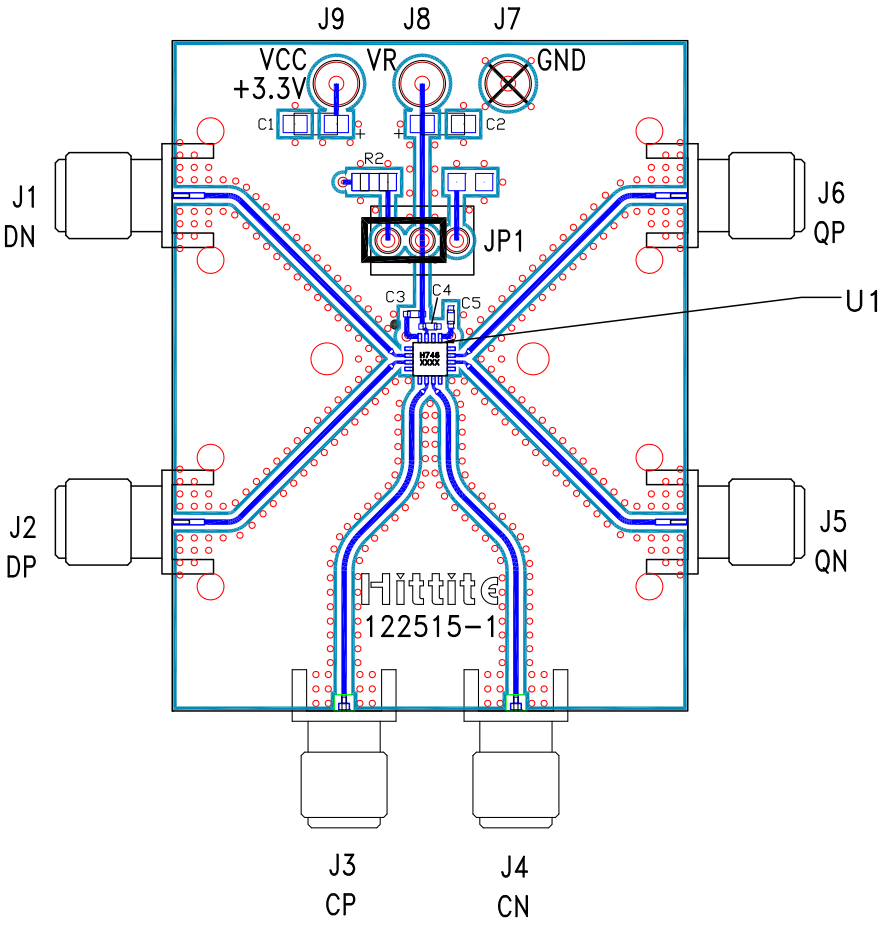
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3 6, 7	DN, DP CP, CN	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
10, 11	QN, QP	Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply.s	
13, 16	Vcc	Positive Supply	
14, Package Base	GND	Supply Ground	
15	VR	Output level control. Output level may be adjusted by applying a voltage to VR per "Output Differential vs. VR" plot.	

Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC747LC3C [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J9	DC Pin
JP1	Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF Capacitor, 0402 Pkg.
R2	10 Ohm Resistor, 0603 Pkg.
U1	HMC747LC3C High Speed Logic, D-Type Flip-Flop
PCB [2]	122515 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package gro-und leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to Vcc for normal operation.

Application Circuit