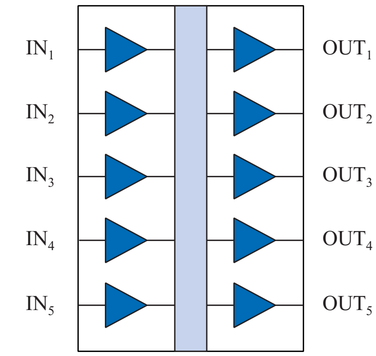
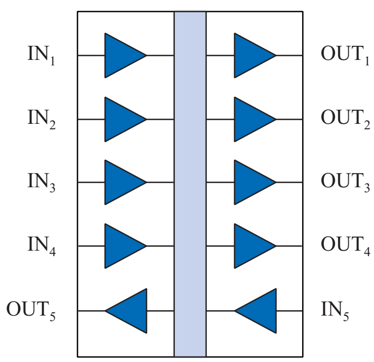
IL260/IL261/IL262

High Speed Five-Channel Digital Isolators

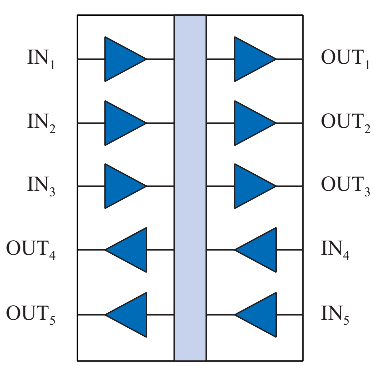
Functional Diagrams



IL260



IL261



IL262

Features

- High Speed: 110 Mbps
- 1.2 mA/channel typical quiescent current
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- −40°C to +85°C operating temperature
- 1000 V_{RMS}/1500 V_{DC} high voltage endurance
- 44000 year barrier life
- Excellent magnetic immunity
- 2 ns typical pulse width distortion
- 100 ps typical pulse jitter
- 4 ns typical propagation delay skew
- 10 ns typical propagation delay
- 2 ns channel-to-channel skew
- 0.15", 0.3", and True 8™ mm 16-pin SOIC packages
- UL 1577 recognized; IEC 60747-5-5 (VDE 0884) certifed

Applications

- ADCs and DACs
- Multiplexed data transmission
- Board-to-board communication
- Peripheral interfaces
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

NVE's IL260-Series five-channel high-speed digital isolators are CMOS devices manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator. The unique fifth channel can be is used to distribute isolated clocks or handshake signals to multiple delta-sigma A/D converters. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

Typical transient immunity of 50 kV/µs is unsurpassed. Performance is specified over the temperature range of −40°C to +85°C without derating.

Parts are available in an ultraminiature 0.15" 16-pin SOIC package, a JEDEC-standard 0.3"-wide package, or NVE's exclusive True 8™ 16-pin SOIC package for true 8 millimeter creepage. In the 0.15" packages, the five-channel devices provide the highest channel density available.

*U.S. Patent number 5,831,426; 6,300,617 and others.

REV. Q

Absolute Maximum Ratings[1]

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55		150	°C	
Ambient Operating Temperature	T_A	−40		85	°C	
Supply Voltage	V_{DD1},V_{DD2}	−0.5		7	V	
Input Voltage	V_I	−0.5		V_{DD} + 0.5	V	
Output Voltage	V_O	−0.5		V_{DD} + 0.5	V	
Output Current Drive	I_O	−10		10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	−40		85	°C	
Supply Voltage	V_{DD1},V_{DD2}	3.0		5.5	V	3.3/5.0 V Operation
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	0.15" SOIC 0.3" SOIC		4.0 8.03	 8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)			0.012	0.013		mm	
Leakage Current[5]				0.2		μA_{RMS}	240 V_{RMS}
Barrier Resistance[5]		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance[5]		C_{IO}		5		pF	f = 1 MHz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC DC	V_{IO}	1000 1500			V_{RMS} V_{DC}	At maximum operating temperature
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Safety and Approvals

IEC 60747-5-5 (VDE 0884) (File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Transient overvoltage (V_{IOTM}) and surge voltage (V_{IOSM}) 4000 V_{PK}
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)
Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-3	SOIC	150 V_{RMS}
None	Wide-body SOIC/True 8™	300 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)
Each part tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

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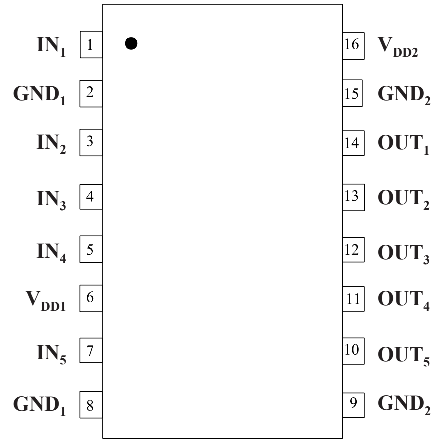
IL260 Pin Connections

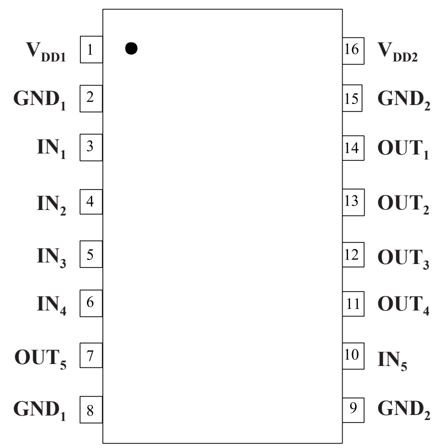
1	IN_1	Input 1
2	GND_1	Ground*
3	IN_2	Input 2
4	IN_3	Input 3
5	IN_4	Input 4
6	V_{DD1}	Supply Voltage 1
7	IN_5	Input 5
8	GND_1	Ground*
9	GND_2	Ground*
10	OUT_5	Output 5
11	OUT_4	Output 4
12	OUT_3	Output 3
13	OUT_2	Output 2
14	OUT_1	Output 1
15	GND_2	Ground*
16	V_{DD2}	Supply Voltage 2



IL260

IL261 Pin Connections

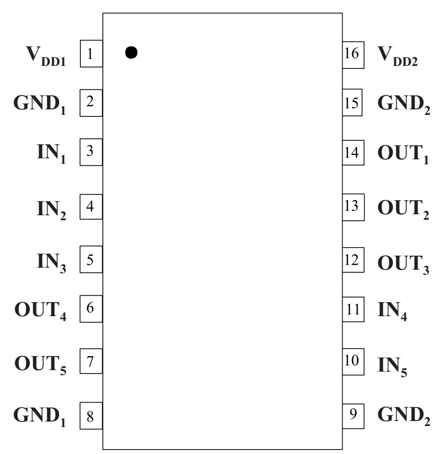
1	V_{DD1}	Supply Voltage 1
2	GND_1	Ground*
3	IN_1	Input 1
4	IN_2	Input 2
5	IN_3	Input 3
6	IN_4	Input 4
7	OUT_5	Output 5
8	GND_1	Ground*
9	GND_2	Ground*
10	IN_5	Input 5
11	OUT_4	Output 4
12	OUT_3	Output 3
13	OUT_2	Output 2
14	OUT_1	Output 1
15	GND_2	Ground*
16	V_{DD2}	Supply Voltage 2



IL261

IL262 Pin Connections

1	V_{DD1}	Supply Voltage 1
2	GND_1	Ground*
3	IN_1	Input 1
4	IN_2	Input 2
5	IN_3	Input 3
6	OUT_4	Output 4
7	OUT_5	Output 5
8	GND_1	Ground*
9	GND_2	Ground*
10	IN_5	Input 5
11	IN_4	Input 4
12	OUT_3	Output 3
13	OUT_2	Output 2
14	OUT_1	Output 1
15	GND_2	Ground*
16	V_{DD2}	Supply Voltage 2



IL262

***NOTE:** Pins 2 and 8 are internally connected, as are pins 9 and 15.

3.3 Volt Electrical Specifications (T_{min} to T_{max})						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Current IL260	I_{DD1}		300	400	µA	
Input Quiescent Current IL261	I_{DD1}		1.2	1.75	mA	
Input Quiescent Current IL262	I_{DD1}		2.4	3.5	mA	
Output Quiescent Current IL260	I_{DD2}		6	8.75	mA	
Output Quiescent Current IL261	I_{DD2}		4.8	7	mA	
Output Quiescent Current IL262	I_{DD2}		4.8	7	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD}−0.1	V_{DD}		V	I_O = −20 µA, V_I=V_{IH}
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, V_I=V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I=V_{IL}
			0.5	0.8		I_O = 4 mA, V_I=V_{IL}

Switching Specifications (V_{DD} = 3.3 V)						
Maximum Data Rate		100	110		Mbps	C_L = 15 pF
Minimum Pulse Width[7]	PW	10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	C_L = 15 pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$[2]	PWD		2	3	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)[4]	$\lvert CM_H \rvert$,$\lvert CM_L \rvert$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
Channel-to-Channel Skew			2	3	ns	C_L = 15 pF
Dynamic Power Consumption[6]			140	240	µA/Mbps	per channel

Magnetic Field Immunity[8] (V_{DD2} = 3V, 3V$<V_{DD1}<$5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	1800	2000		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

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5 Volt Electrical Specifications (T_{min} to T_{max})							
Parameters		**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Current	IL260	I_{DD1}		350	500	µA	
	IL261			1.8	2.5	mA	
	IL262			3.6	5	mA	
Output Quiescent Current	IL260	I_{DD2}		9	12.5	mA	
	IL261			7.2	10	mA	
	IL262			7.2	10	mA	
Logic Input Current		I_i	−10		10	µA	
Logic High Output Voltage		V_{OH}	V_{DD}−0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
			0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage		V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
				0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 5 V)						
Maximum Data Rate		100	110		Mbps	C_L = 15 pF
Minimum Pulse Width(7)	PW	10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Pulse Width Distortion $\|t_{PHL}-t_{PLH}\|$(2)	PWD		2	3	ns	C_L = 15 pF
Pulse Jitter(10)	t_J		100		ps	C_L = 15 pF
Propagation Delay Skew(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	30	50		kV/µs	V_{CM} = 1500 V_{DC}, $t_{TRANSIENT}$ = 25 ns
Channel-to-Channel Skew			2	3	ns	C_L = 15 pF
Dynamic Power Consumption(6)			200	340	µA/Mbps	per channel

Magnetic Field Immunity(8) (V_{DD2} = 5V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	4000	4500		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 6.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 6).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

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Application Information

Electrostatic Discharge Sensitivity
This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility
IsoLoop Isolators have the lowest EMC footprint of any isolation technology. There are no internal clocks or carriers. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

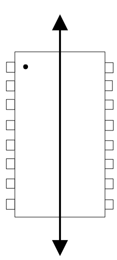
These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1
- Residential, Commercial & Light Industrial
- Methods EN55022, EN55014

EN50082-2: Industrial Environment
- Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

ENV50204
- Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

Dynamic Power Consumption
IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Power Supply Decoupling
Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both GND_1 and GND_2 are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the V_{DD} pins.

Maintaining Creepage
Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Signal Status on Start-up and Shut Down
To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Data Transmission Rates
The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$PWD\% = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

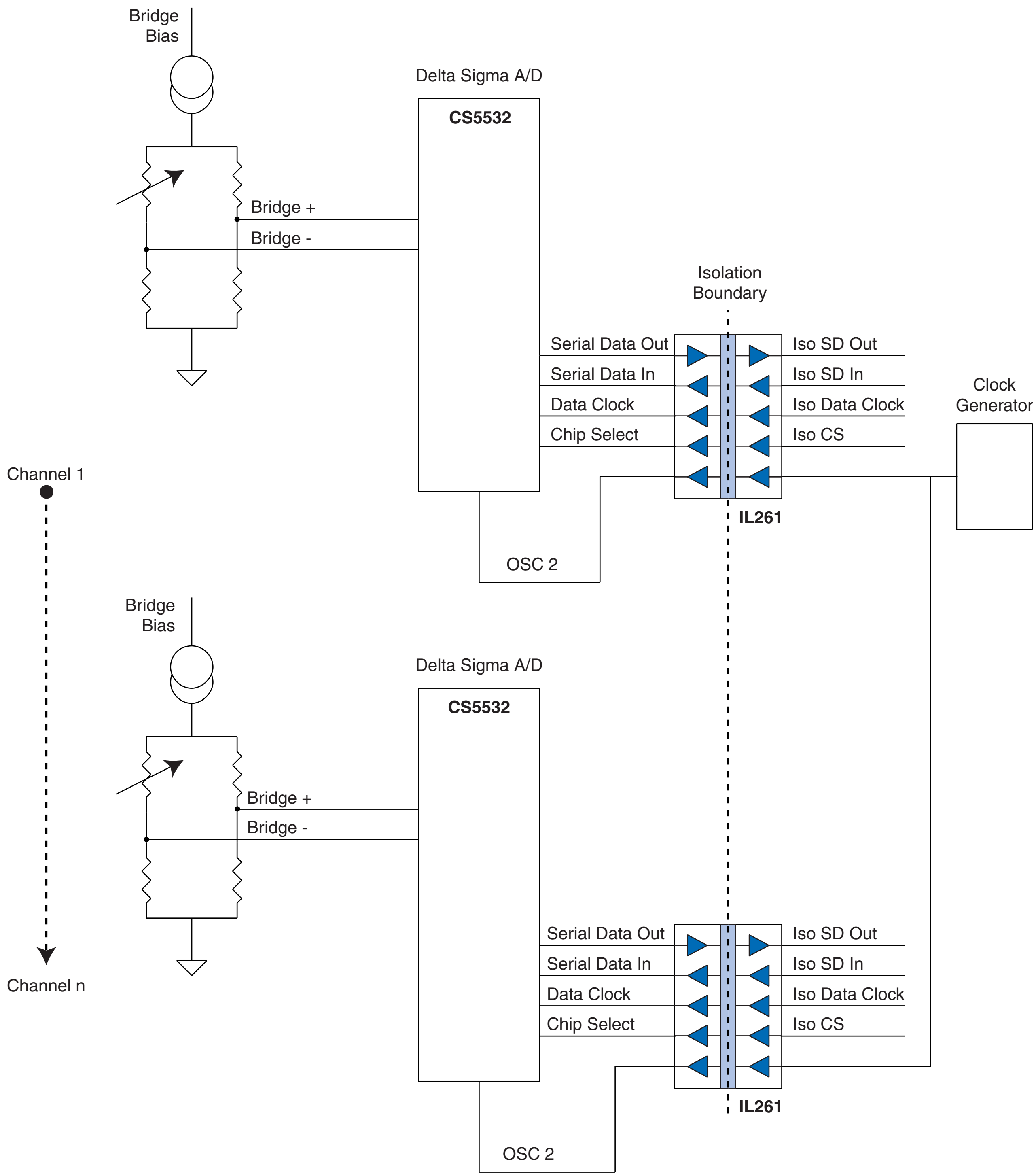
$$PWD\% = \frac{3\text{ ns}}{80\text{ ns}} \times 100\% = 3.75\%$$

This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in IL260-Series Isolators is only 3 ns, which is **ten times** better than any optocoupler. IL260-Series Isolators have a maximum propagation delay skew of 6 ns, which is **five times** better than any optocoupler.

Application Diagram—Multi-Channel Delta-Sigma A/D Converter

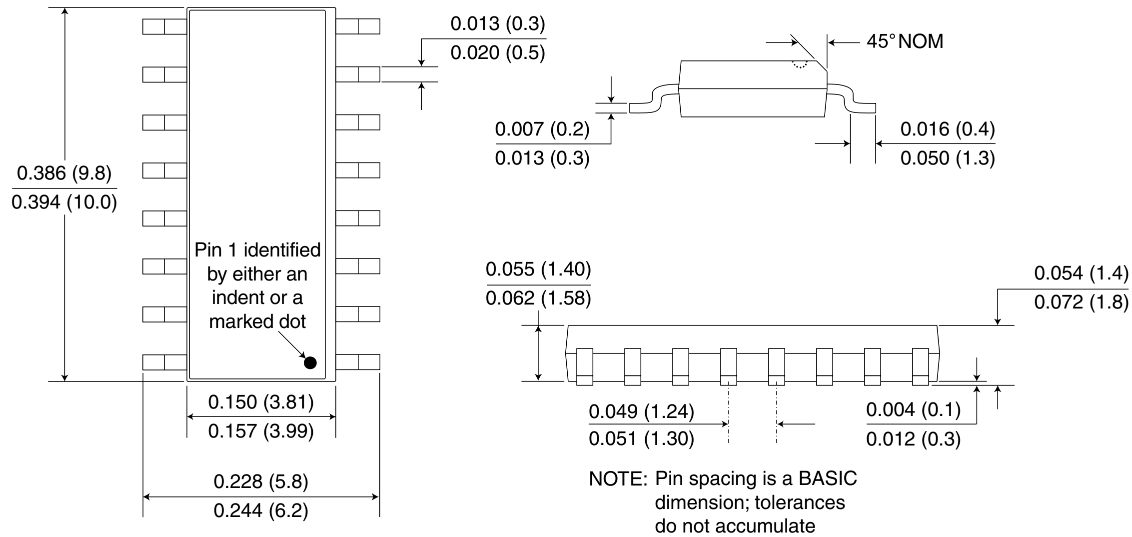
In a typical single-channel delta-sigma ADC, the system clock is located on the isolated side of the system and only four channels of isolation are required. With multiple ADCs configured in a channel-to-channel isolation configuration, however, clock jitter and edge placement accuracy of the system clock must be matched between ADCs. The best solution is to use a single clock on the system side and distribute the clock to each ADC. The five-channel IL261 is ideal, with the fifth channel used to distribute a single, isolated clock to multiple ADCs as shown below:



Package Drawings

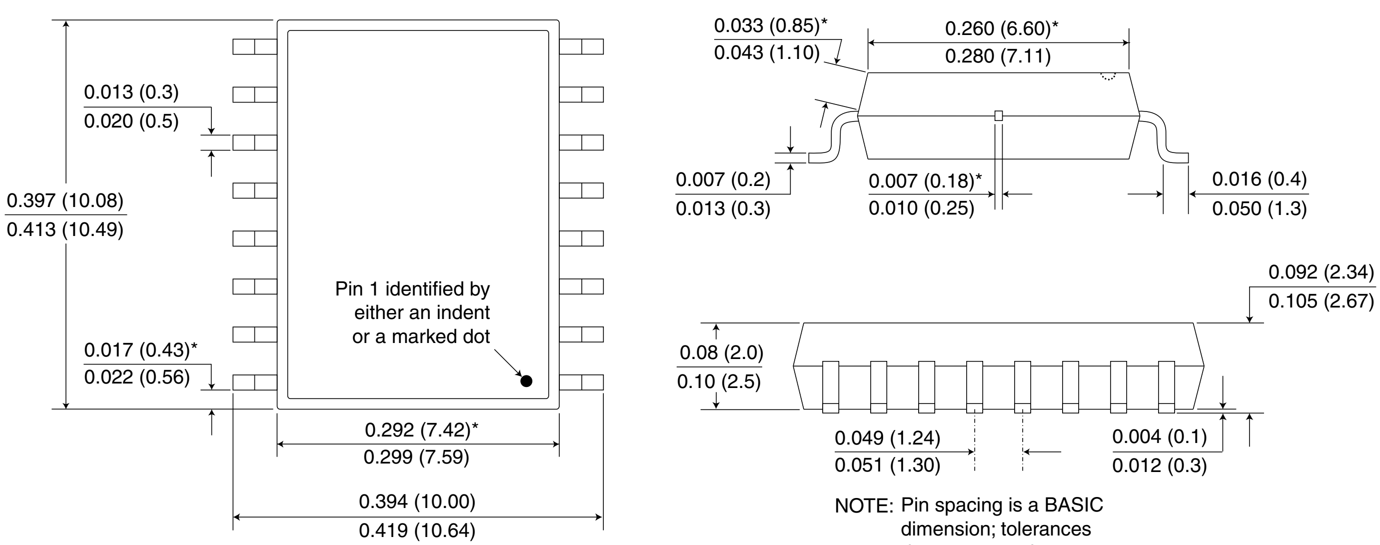
0.15" 16-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Package (no suffix)

Dimensions in inches (mm); scale = approx. 5X

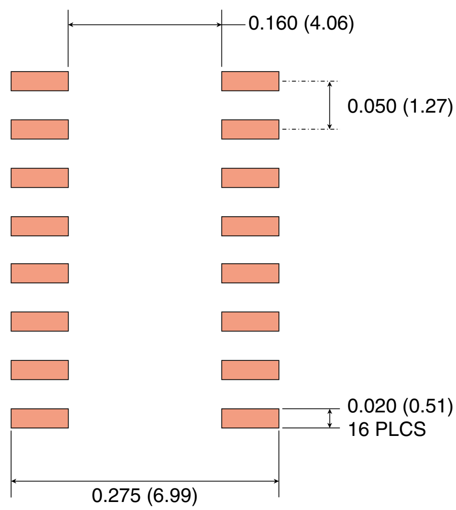


*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

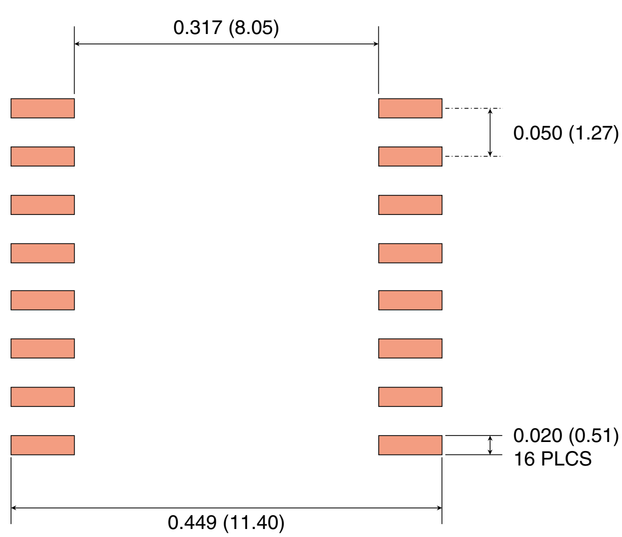
0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information and Valid Part Numbers

IL 260 - 3 E TR13

Bulk Package
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
Blank = 80/20 Tin/Lead Plating
E = RoHS Compliant

Package Type
Blank = 0.3" 16-pin SOIC
-3 = 0.15" 16-pin SOIC

Base Part Number
260 = 5 Drive Channels
261 = 4 Drive Channels, 1 Receive Channel
262 = 3 Drive Channels, 2 Receive Channel

Product Family
IL = Isolators

Valid Part Numbers

IL260
IL260E
IL260-3
IL260-3E
IL261
IL261E
IL261-3
IL261-3E
IL262
IL262E
IL262-3
IL262-3E

All IL260-Series part types are available on tape and reel.

RoHS COMPLIANT

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Revision History

ISB-DS-001-IL260/1-Q
November 2013

Change

- IEC 60747-5-5 (VDE 0884) certification.

ISB-DS-001-IL260/1-P
October 2013

Change

- Tighter quiescent current specifications.
- Upgraded from MSL 2 to MSL 1.

ISB-DS-001-IL260/1-O

Change

- Increased transient immunity specifications based on additional data.
- Added VDE 0884 pending.
- Added high voltage endurance specifications.
- Increased magnetic immunity specifications.
- Updated package drawings.
- Added recommended solder pad layouts.

ISB-DS-001-IL260/1-N

Change

- Detailed isolation and barrier specifications.
- Cosmetic changes.

ISB-DS-001-IL260/1-M

Change

- Tightened typical output quiescent supply specs.

ISB-DS-001-IL260/1/2-L

Change

- Update terms and conditions.

ISB-DS-001-IL260/1/2-K

Change

- Added clarification of internal ground connections.

ISB-DS-001-IL260/1/2-J

Change

- Relaxed Vdd1 quiescent current specification to 500µA.

ISB-DS-001-IL260/1/2-I

Change

- Added typical jitter specification at 5V.

ISB-DS-001-IL260/1/2-H

Change

- Added EMC details.

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Datasheet Limitations
The information and data provided in datasheets shall define the specification of the product as agreed between NVE and its customer, unless NVE and customer have explicitly agreed otherwise in writing. All specifications are based on NVE test protocols. In no event however, shall an agreement be valid in which the NVE product is deemed to offer functions and qualities beyond those described in the datasheet.

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