Analog Output Current Shunt and Voltage Instantaneous Power Monitor

Check for Samples: INA223

FEATURES

- **Wide Common-Mode Range: 0 V to 26 V**
- **±100 µV Offset (Max, Gain = 300 V/V)**
- **Accuracy**
  - **±0.25% Shunt Voltage Gain Error (Max)**
  - **±0.15% Bus Voltage Gain Error (Max)**
  - **1.25% Power Error (Max)**
  - **0.3 µV/°C Offset Drift (Max)**
  - **50 ppm/°C Gain Drift (Max)**
- **Programmable Gains**
  - **Current Shunt Voltage Gains: 20, 128, 300**
  - **Bus Voltage Attenuations: 1/10, 1/5, 2/5**
- **Monitors/Measures/Reports:**
  - **Instantaneous Power**
  - **Bus Voltage**
  - **Load Current**
- **Quiescent Current: 250 µA (Max)**
- **Shutdown Current: 1 µA (Max)**

APPLICATIONS

- **Notebook Computers**
- **Cell Phones**
- **Telecom Equipment**
- **Power Management**

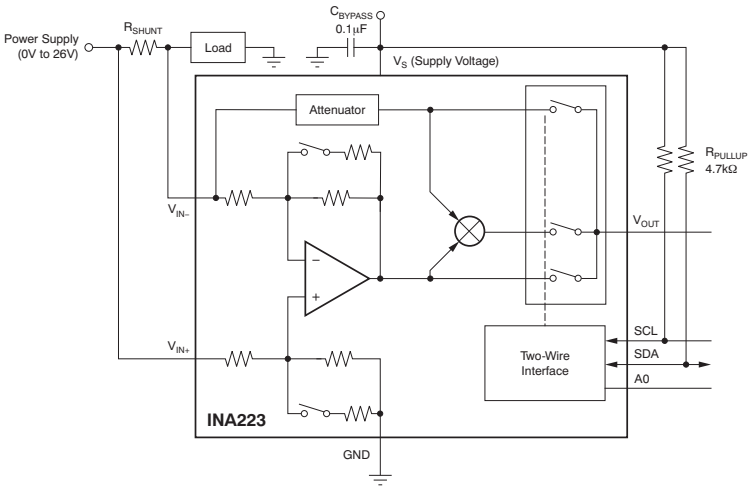
DESCRIPTION

The INA223 is a voltage-output device that monitors the current, bus voltage, and power of a supply line by sensing a voltage drop across a shunt at common-mode voltages from 0 V to 26 V. The common-mode voltage range is independent of the supply voltage. The low offset of the Zerø-Drift architecture enables current sensing with maximum drops across the shunt as low as 10 mV, full-scale.

The INA223 includes a two-wire interface used for adjusting the configuration settings of the device. The interface is used to control the signal (current shunt voltage, bus voltage, or power) that is directed to the device output. Multiple gain and attenuation settings can be programmed through the two-wire interface to allow for application-specific configurations. The programmable gain feature also allows the device to be operated over a much wider dynamic current load range without having to switch the sensing element used.

A shutdown feature is available to disable the device and effectively disconnect it from the shunt resistor and supply voltage, thus reducing the drain on the battery.

The INA223 operates from a single +2.7-V to +5.5-V supply, drawing a maximum supply current of 250 µA. It is specified over the extended temperature range of –40°C to +105°C, and is offered in an SON-10 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA223	SON-10	DSK	P223

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		INA223	UNIT
Supply voltage		+6	V
Analog inputs, V_{IN}+, V_{IN}– (2)	Differential (V_{IN}+) – (V_{IN}–)	–26 to +26	V
	Common-mode(3)	(GND – 0.3) to +26	V
Input current into any pin(3)		5	mA
Operating temperature		–55 to +150	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
Electrostatic discharge (ESD)ratings	Human body model (HBM)	2500	V
	Charged-device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{IN}+ and V_{IN}– are the voltages at the +IN and –IN pins, respectively.
(3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{SENSE} = (V_{IN}+) – (V_{IN}–) = 10 mV, V_S = 3.3 V, and V_{IN}+ = 12 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA223 MIN	INA223 TYP	INA223 MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	T_A = –40°C to +105°C	0		26	V
CMR	Common-mode rejection	T_A = –40°C to +105°C, V_{IN}+ = 0 V to +26 V, V_{SENSE} = 0 mV, Current shunt voltage gain = 20 V/V	92	106		dB
		T_A = –40°C to +105°C, V_{IN}+ = 0 V to +26 V, V_{SENSE} = 0 mV, Current shunt voltage gain = 128 V/V, 300V/V	100	120		dB
V_{OS}	Shunt offset voltage, RTI(1)	Current shunt voltage gain = 20 V/V		±75	±300	µV
		Current shunt voltage gain = 128 V/V		±20	±150	µV
		Current shunt voltage gain = 300 V/V		±15	±100	µV
dV_{OS}/dT	vs temperature	T_A = –40°C to +105°C, current shunt voltage gain = 20 V/V		0.6	1	µV/°C
		T_A = –40°C to +105°C, current shunt voltage gain = 128 V/V, 300V/V		0.1	0.3	
PSR	vs power supply	V_S = +2.7 V to +5.5 V, current shunt voltage gain = 20 V/V		±15	±50	µV/V
		V_S = +2.7 V to +5.5 V, current shunt voltage gain = 128 V/V		±5	±25	µV/V
		V_S = +2.7 V to +5.5 V, current shunt voltage gain = 300 V/V		±2.5	±15	µV/V
V_{OS}	Bus offset voltage, RTI(1)	Bus voltage gain = 0.1 V/V		±2.5	±20	mV
		Bus voltage gain = 0.2 V/V		±2.5	±15	mV
		Bus voltage gain = 0.4 V/V		±1.5	±10	mV
dV_{OS}/dT	vs temperature	T_A = –40°C to +105°C, bus voltage gain = 0.1 V/V		15	40	µV/°C
		T_A = –40°C to +105°C, bus voltage gain = 0.2 V/V, 0.4 V/V		10	30	µV/°C
PSR	vs power supply	V_S = +2.7 V to +5.5 V		±9	±15	mV/V
I_B	Input bias current	Enabled, V_{IN}+, V_{IN}–	15	18	25	µA
		Disabled, V_{IN}+, V_{IN}–		1	1.5	µA
	Input impedance, differential			2.5		kΩ
OUTPUT						
G_{SV}	Current shunt voltage gain			20, 128, 300		V/V
	Current shunt voltage gain error	T_A = –40°C to +105°C, V_{SENSE} = 10 mV to 155 mV, current shunt voltage gain = 20 V/V		±0.05%	±0.25%	
		T_A = –40°C to +105°C, V_{SENSE} = 1.5 mV to 24 mV, current shunt voltage gain = 128 V/V		±0.05%	±0.5%	
		T_A = –40°C to +105°C, V_{SENSE} = 1 mV to 9 mV, current shunt voltage gain = 300 V/V		±0.2%	±1%	
	vs temperature	T_A = –40°C to +105°C, current shunt voltage gain = 20 V/V			50	ppm/°C
		T_A = –40°C to +105°C, current shunt voltage gain = 128 V/V			75	ppm/°C
		T_A = –40°C to +105°C, current shunt voltage gain = 300 V/V			125	ppm/°C
	Nonlinearity error	V_{SENSE} = 1 mV to 10 mV		±0.01%		
G_{BV}	Bus voltage gain			0.1, 0.2, 0.4		V/V
	Bus voltage gain error	T_A = –40°C to +105°C, bus voltage gain = 0.1 V/V, V_{CM} = 0.5V to 26V		±0.05%	±0.2%	
		T_A = –40°C to +105°C, bus voltage gain = 0.2 V/V, V_{CM} = 0.5 V to 12 V		±0.025%	±0.15%	
		T_A = –40°C to +105°C, bus voltage gain = 0.4V/V, V_{CM} = 0.5 V to 6 V		±0.025%	±0.15%	
	vs temperature	T_A = –40°C to +105°C			5	ppm/°C
	Nonlinearity error			±0.01%		

(1) RTI = referred-to-input.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{SENSE} = (V_{IN}+) – (V_{IN}–) = 10 mV, V_S = 3.3 V, and V_{IN}+ = 12 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA223			UNIT
			MIN	TYP	MAX	
	Power measurement error	Current shunt voltage gain = 20 V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V		±0.35	±1.25	%FSR
		Current shunt voltage gain = 20 V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V T_A = –40°C to +105°C			±2	%FSR
		Current shunt voltage gain = 128 V/V, 300V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V		±0.35	±1.5	%FSR
		Current shunt voltage gain = 128 V/V, 300V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V; T_A = –40°C to +105°C			±2.25	%FSR
	Output impedance			4		Ω
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT(2)						
	Swing to VS power-supply rail	T_A = –40°C to +105°C, R_L = 10 kΩ to GND		VS – 0.015	VS – 0.035	V
	Swing to GND	T_A = –40°C to +105°C, R_L = 10 kΩ to GND		V_{GND} + 2.5	V_{GND} + 10	mV
FREQUENCY RESPONSE						
GBW	Bandwidth	Gain = 300, C_{LOAD} = 10 pF		10		kHz
		Gain = 128, C_{LOAD} = 10 pF		20		kHz
		Gain = 20, C_{LOAD} = 10 pF		25		kHz
SR	Slew rate			0.25		V/µs
NOISE, RTI(1)						
	Voltage noise density	0.1 Hz to 10 Hz, current shunt voltage gain = 20 V/V		235		nV/√Hz
		0.1 Hz to 10 Hz, current shunt voltage gain = 300 V/V		54		nV/√Hz
DIGITAL INPUTS (SDA as Input, SCL, A0)						
	Input capacitance			3		pF
V_{IH}	High-level input voltage		0.7(V_S)		6	V
V_{IL}	Low-level input voltage		–0.3		0.3(V_S)	V
	Leakage input current			0.1	1	µA
	Hysteresis			500		mV

(2) See Typical Characteristic curve, *Output Swing vs Output Current* (Figure 22).

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{SENSE} = (V_{IN}+) – (V_{IN}–) = 10 mV, V_S = 3.3 V, and V_{IN}+ = 12 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA223 MIN	INA223 TYP	INA223 MAX	UNIT
POWER SUPPLY						
V_S	Operating range	T_A = –40°C to +105°C	+2.7		+5.5	V
I_Q	Quiescent current	Enabled		200	250	µA
		Disabled		0.1	1	µA
	Power-on reset threshold			2		V
TEMPERATURE						
	Specified range		–40		+105	°C

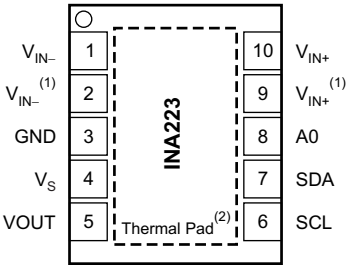
THERMAL INFORMATION

THERMAL METRIC(1)		INA223 DSK (SON) 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	47.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	57.9	
θ_{JB}	Junction-to-board thermal resistance	21.5	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	21.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	4.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

DSK PACKAGE
SON-10
(TOP VIEW)



(1) See *Application Information* section for a description of how to connect input pins to the shunt resistor.

(2) Must be connected to ground.

PIN DESCRIPTIONS

PIN		ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
NAME	NUMBER		
A0	8	Digital input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 6 shows pin settings and corresponding address.
GND	3	Analog	Ground
SCL	6	Digital input	Serial bus clock line
SDA	7	Digital I/O	Serial bus data line
V_{IN+}	9	Analog input	Connect to supply side of shunt resistor. This pin can also be connected directly to pin 10.
V_{IN+}	10	Analog input	Connect to supply side of shunt resistor
V_{IN-}	1	Analog input	Connect to load side of shunt resistor
V_{IN-}	2	Analog input	Connect to load side of shunt resistor. This pin can also be connected directly to pin 1.
VOUT	5	Analog output	Output signal selected by multiplexer
V_S	4	Analog	Power supply (2.7 V to 5.5 V)

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V unless otherwise noted.

SHUNT OFFSET VOLTAGE (G = 20 V/V) PRODUCTION DISTRIBUTION

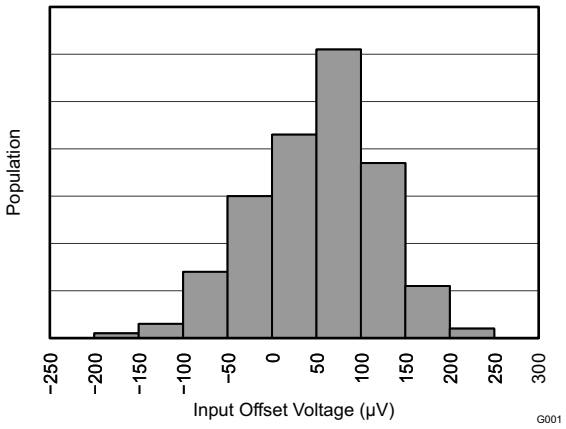


Figure 1.

SHUNT OFFSET VOLTAGE (G = 128 V/V) PRODUCTION DISTRIBUTION

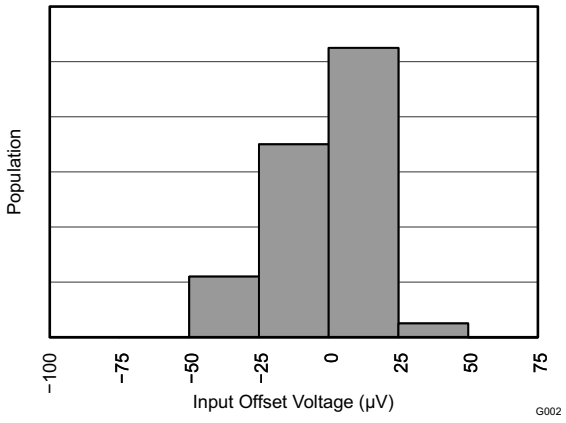


Figure 2.

SHUNT OFFSET VOLTAGE (G = 300 V/V) PRODUCTION DISTRIBUTION

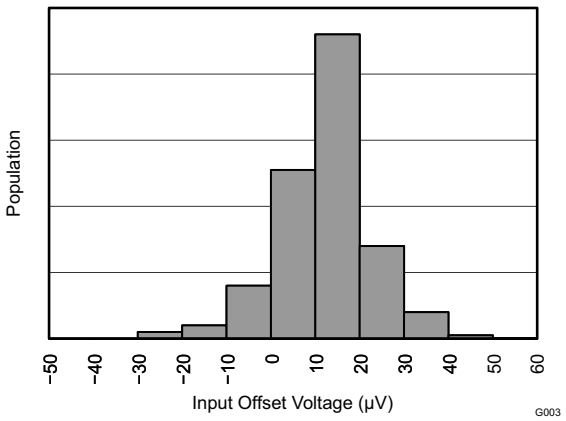


Figure 3.

SHUNT OFFSET VOLTAGE vs TEMPERATURE

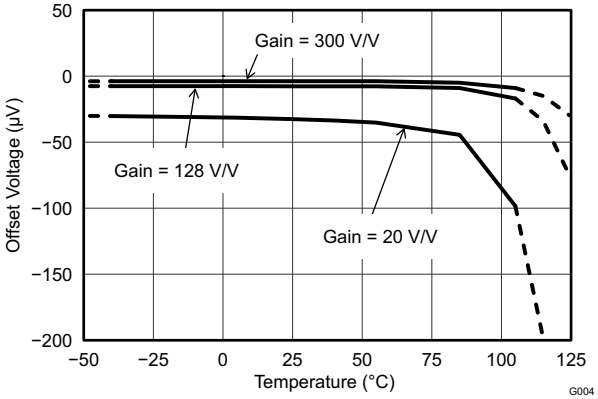


Figure 4.

SHUNT INPUT CMRR (G = 20 V/V) PRODUCTION DISTRIBUTION

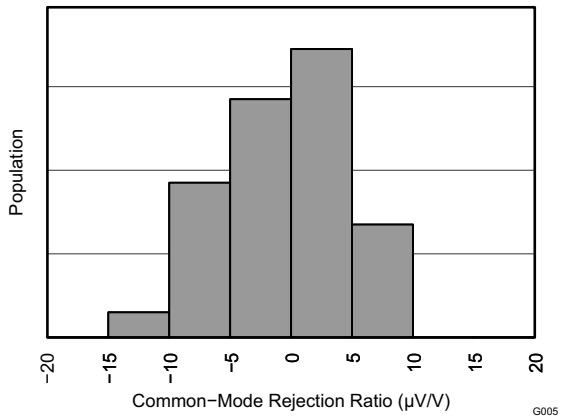


Figure 5.

SHUNT INPUT CMRR (G = 128 V/V and 300 V/V) PRODUCTION DISTRIBUTION

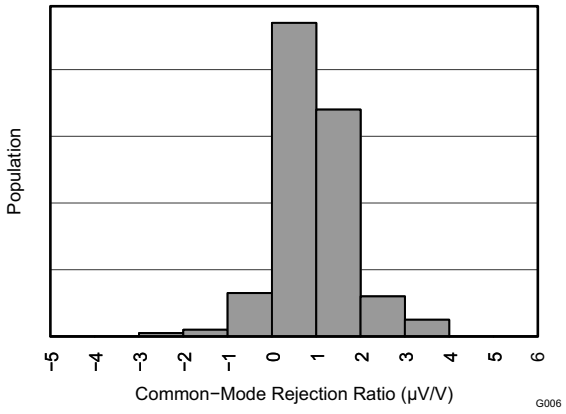


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V unless otherwise noted.

SHUNT INPUT CMRR vs TEMPERATURE

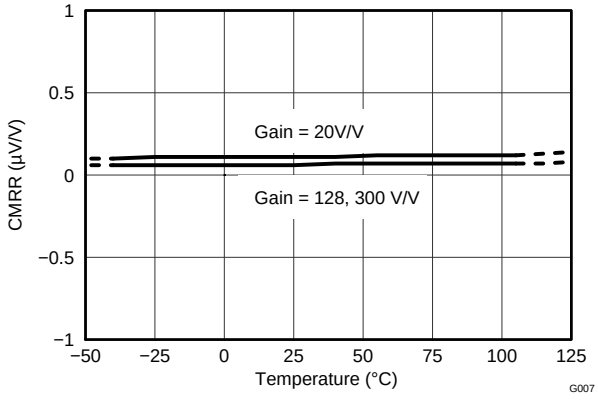


Figure 7.

SHUNT GAIN ERROR (G = 20 V/V and 128 V/V) PRODUCTION DISTRIBUTION

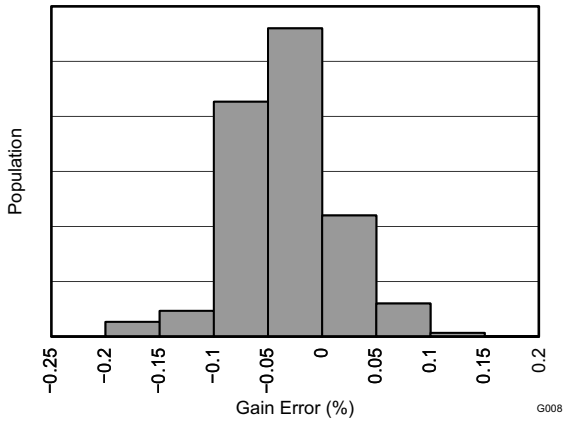


Figure 8.

SHUNT GAIN ERROR (G = 300 V/V) PRODUCTION DISTRIBUTION

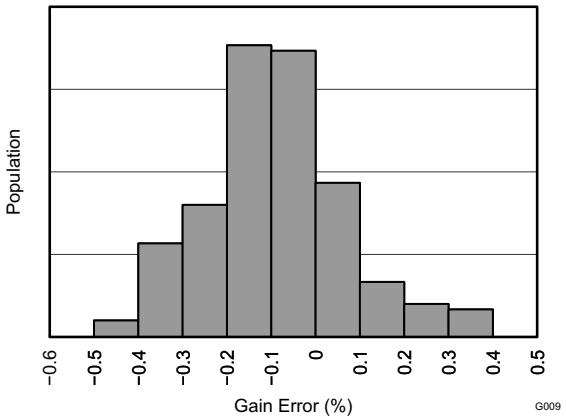


Figure 9.

SHUNT GAIN ERROR vs TEMPERATURE

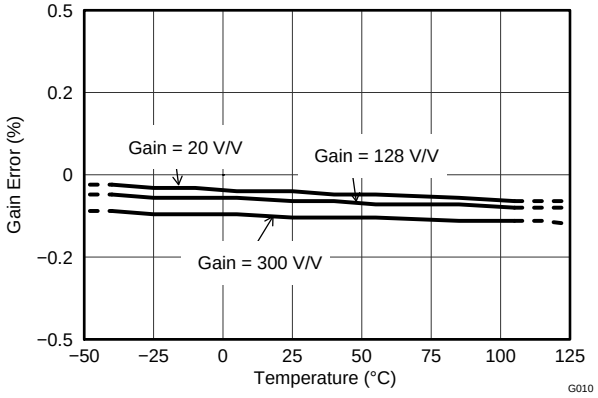


Figure 10.

BUS OFFSET VOLTAGE (G = 0.1 V/V and 0.2 V/V) PRODUCTION DISTRIBUTION

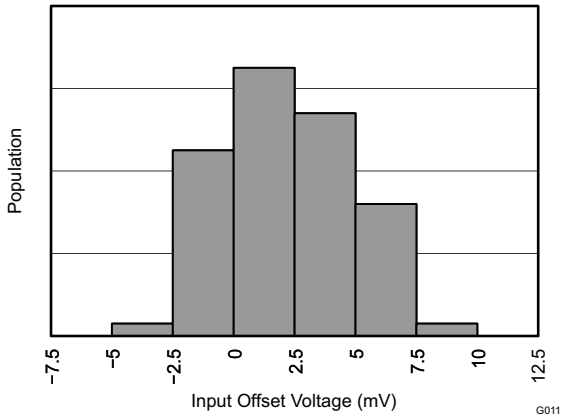


Figure 11.

BUS OFFSET VOLTAGE (G = 0.4 V/V) PRODUCTION DISTRIBUTION

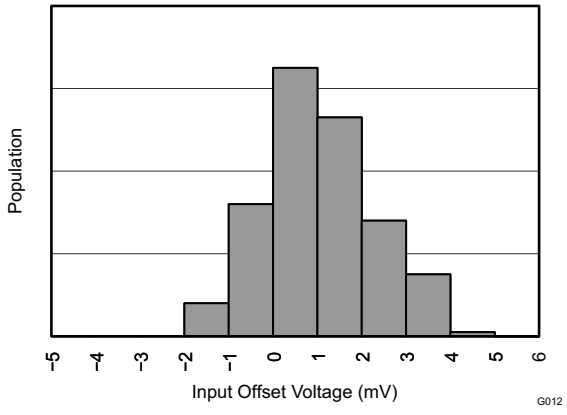


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V unless otherwise noted.

BUS OFFSET VOLTAGE vs TEMPERATURE

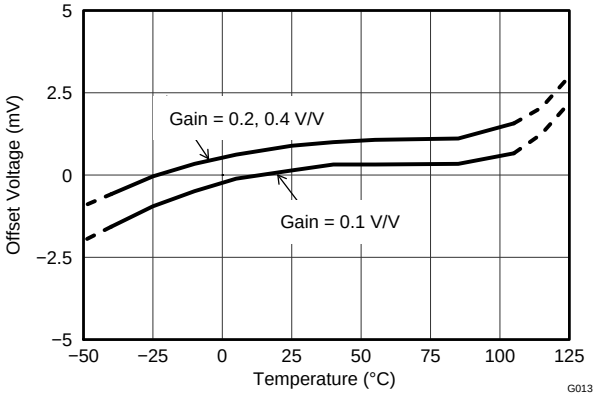


Figure 13.

BUS GAIN ERROR (G = 0.1 V/V) PRODUCTION DISTRIBUTION

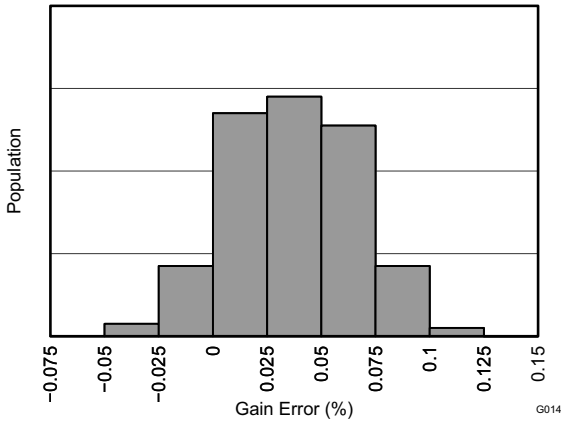


Figure 14.

BUS GAIN ERROR (G = 0.2 V/V and 0.4 V/V) PRODUCTION DISTRIBUTION

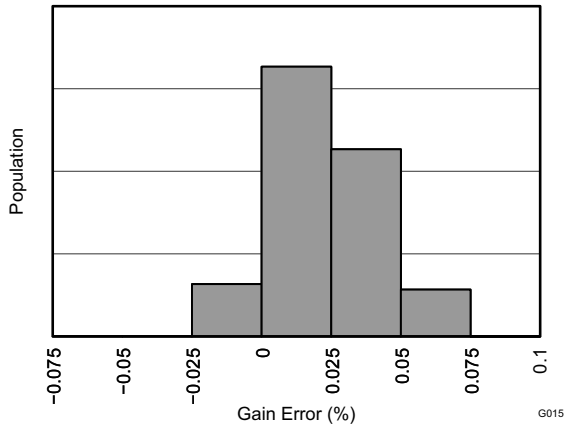


Figure 15.

BUS GAIN ERROR vs TEMPERATURE

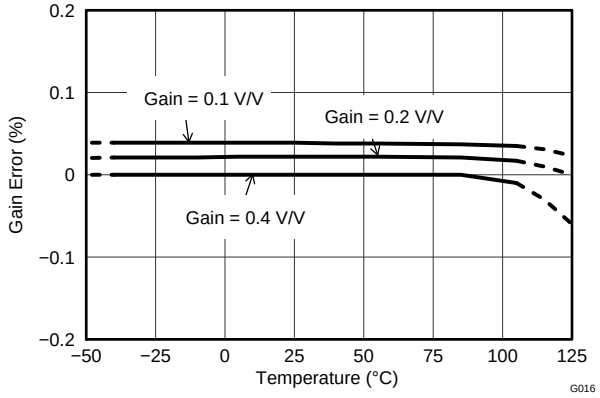


Figure 16.

POWER GAIN ERROR PRODUCTION DISTRIBUTION

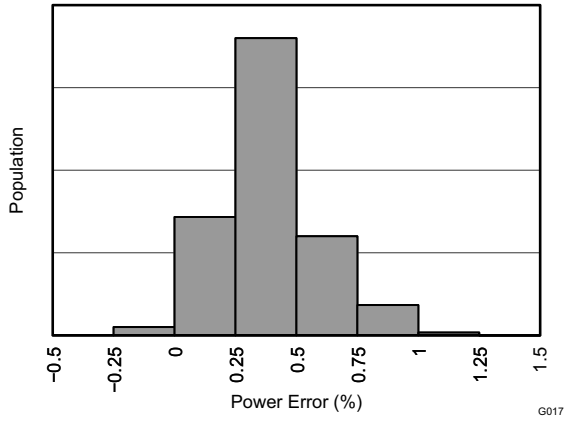


Figure 17.

POWER GAIN vs TEMPERATURE

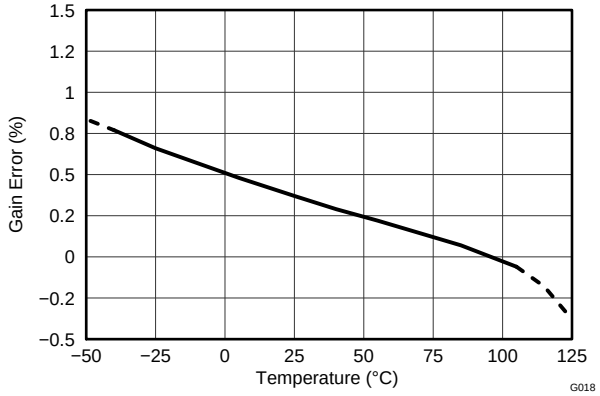


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V unless otherwise noted.

SHUNT INPUT CMR vs FREQUENCY

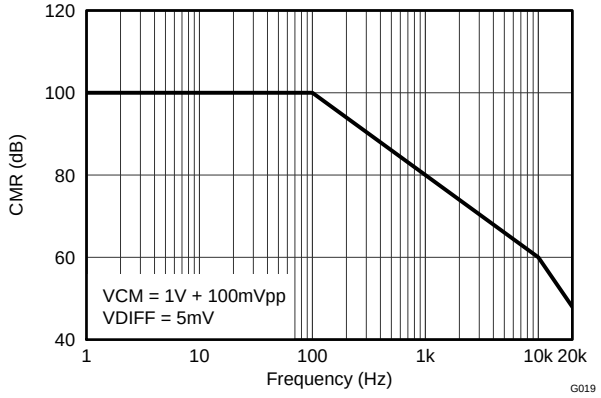


Figure 19.

GAIN vs FREQUENCY

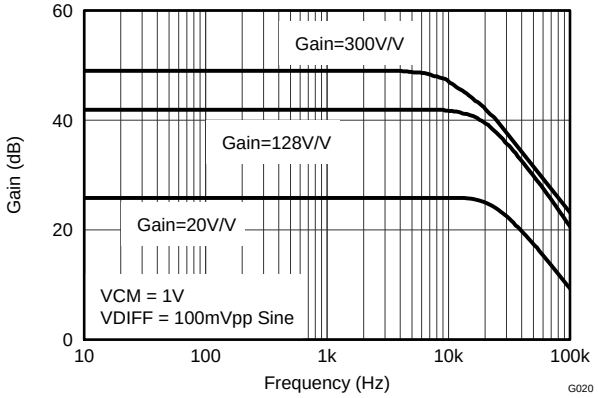


Figure 20.

PSRR vs FREQUENCY

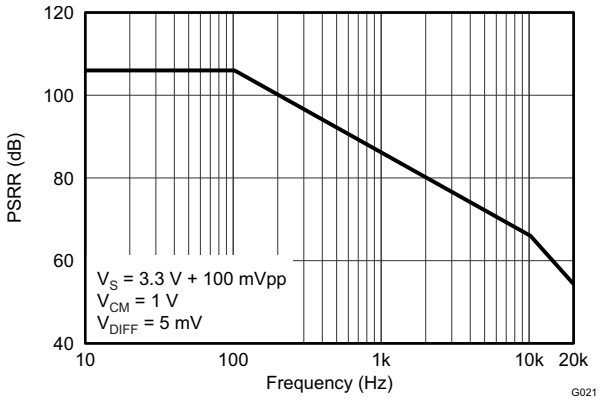


Figure 21.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

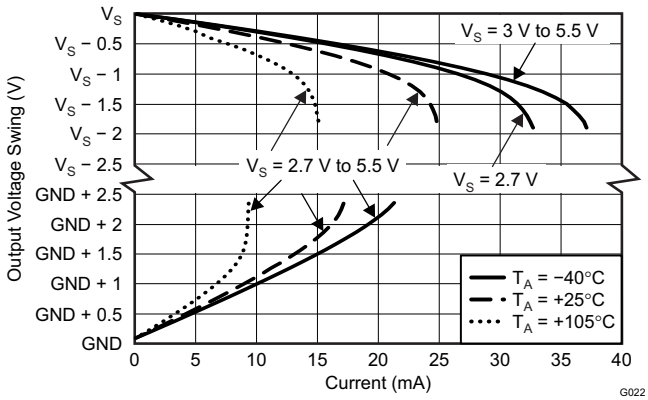


Figure 22.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE, ENABLED

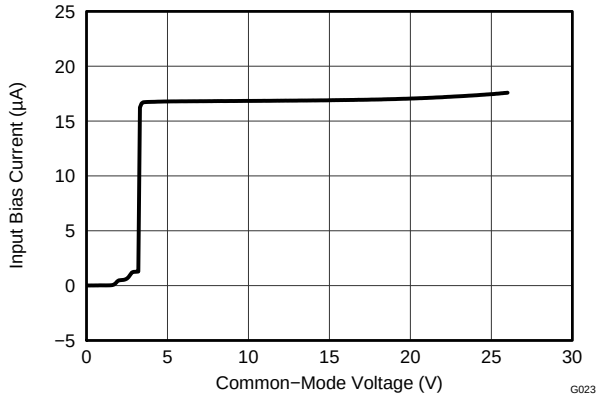


Figure 23.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE, DISABLED

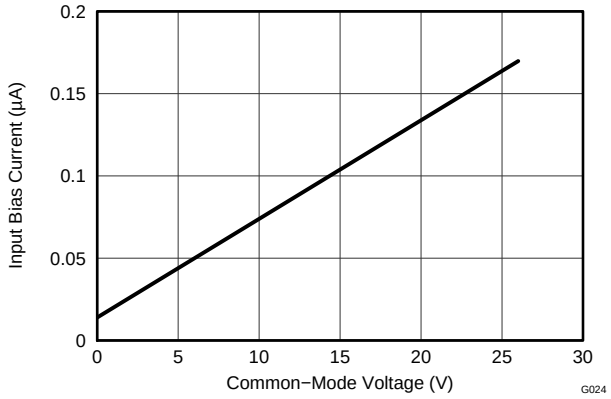


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE

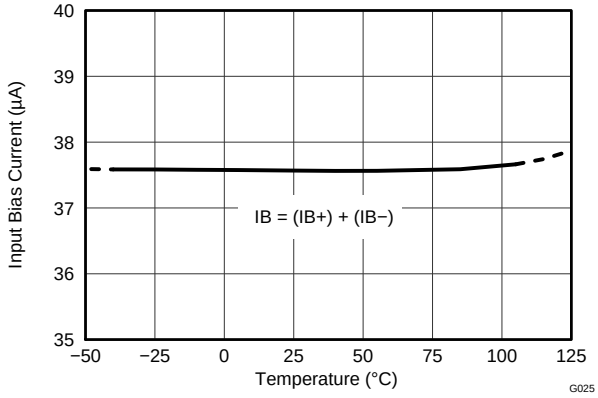


Figure 25.

QUIESCENT CURRENT vs TEMPERATURE

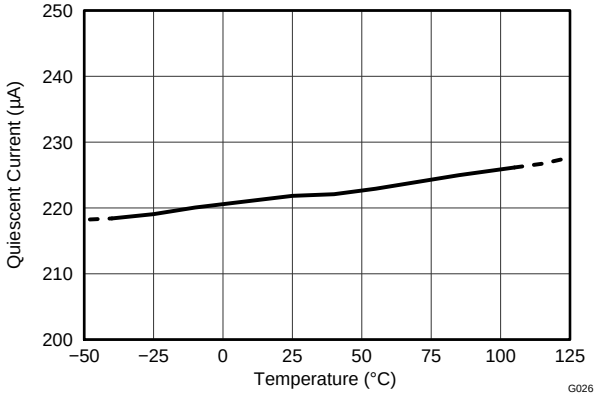


Figure 26.

INPUT REFERRED VOLTAGE NOISE vs FREQUENCY

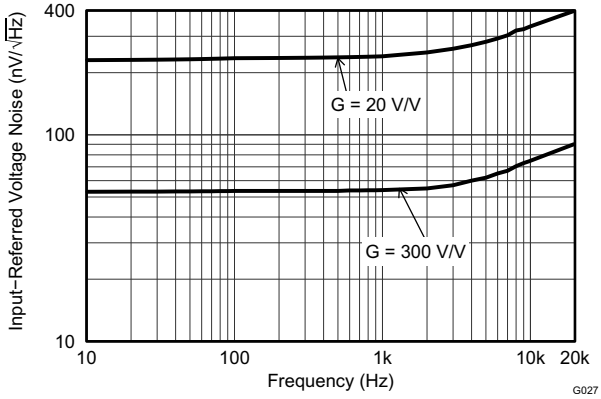


Figure 27.

0.1-Hz TO 10-Hz VOLTAGE NOISE

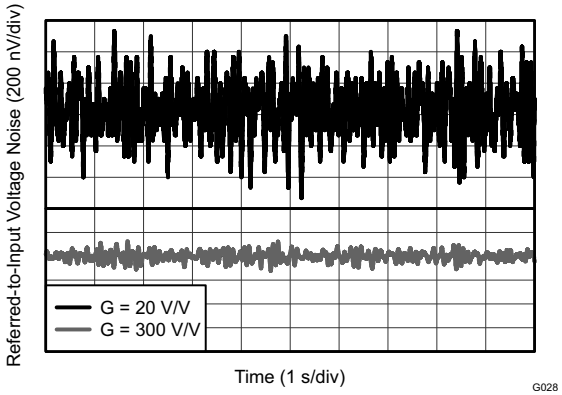


Figure 28.

SHUNT INPUT STEP RESPONSE GAIN = 20 V/V

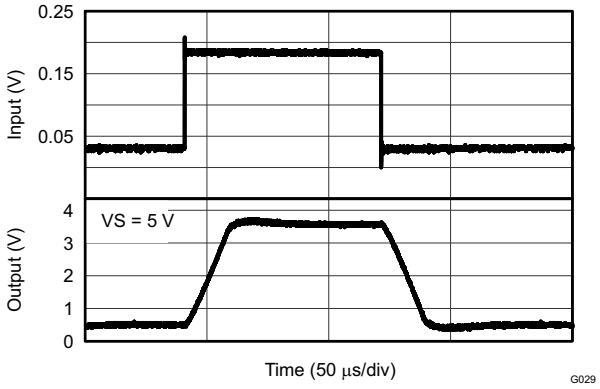


Figure 29.

SHUNT INPUT STEP RESPONSE GAIN = 128 V/V

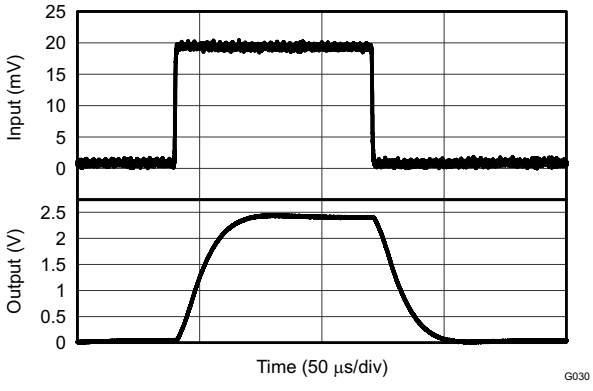


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V unless otherwise noted.

SHUNT INPUT STEP RESPONSE
GAIN = 300 V/V

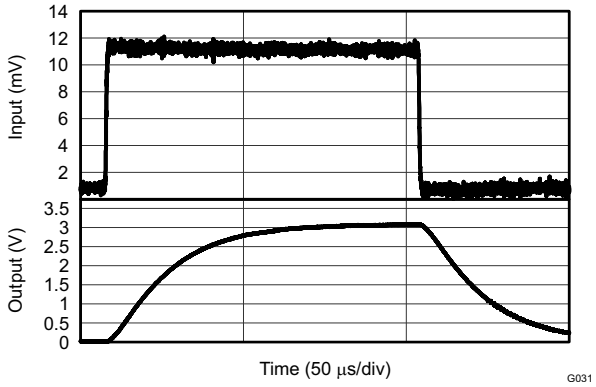


Figure 31.

INPUT OVERLOAD
RECOVERY

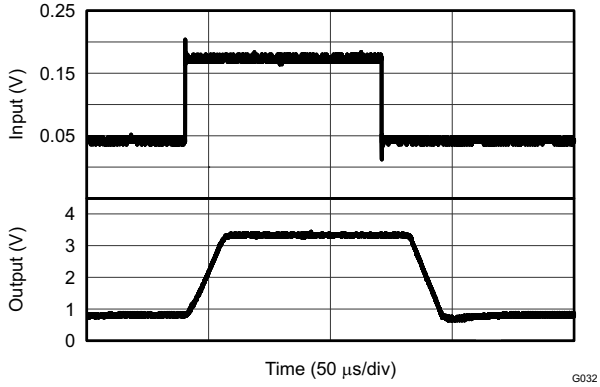


Figure 32.

APPLICATION INFORMATION

The INA223 is an analog output current shunt monitor that incorporates an analog multiplier to provide instantaneous power measurement. The INA223 features a two-wire and SMBus-compatible interface allowing the configuration settings of the device to be adjusted and changed as needed, based on the specific application requirements. The configuration options include the selection of the desired signal to be available at the output pin, switching between multiple current shunt voltage gains and bus voltage attenuation factors, as well as being able to place the device into a disabled state.

INA223 TYPICAL APPLICATION

Figure 33 shows the typical application circuit for the INA223. The input pins, V_{IN+} and $V_{IN–}$, should be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistance. A power-supply bypass capacitor is required for stability. Use a 0.1-µF ceramic capacitor for supply bypassing, placed as close as possible between the supply and ground pins.

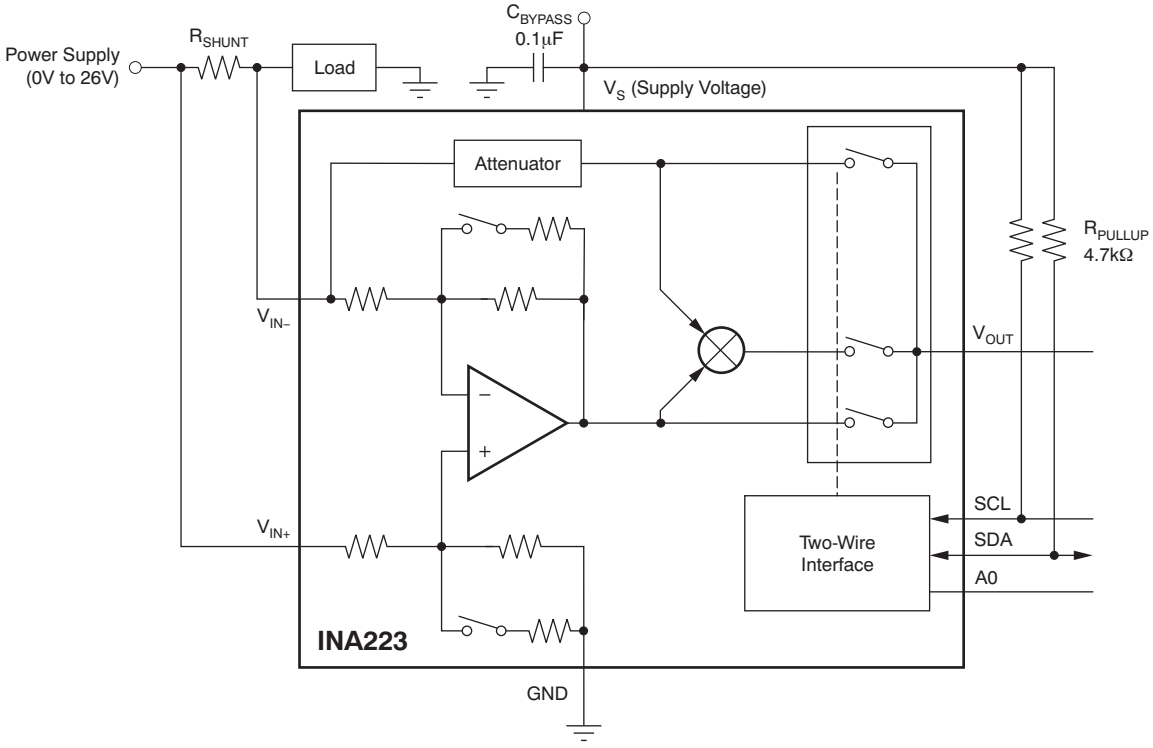


Figure 33. Typical Application

BASIC FUNCTIONS

The INA223 can be configured to monitor and report the differential voltage developed across a shunt resistor, the power supply bus voltage, or the power being delivered to the load. Through the two-wire interface, the output multiplexer (mux) can be configured to provide a proportional output signal to any one of these input signals at the output pin, VOUT. The digital interface can also be used to switch between different current shunt voltage gains, bus voltage attenuation settings, as well as place the device into a disabled mode. The multiple settings available for the current shunt voltage gains and bus voltage attenuation factors allow the INA223 to operate over a wider input signal range than a single fixed-setting device would allow.

Shunt Voltage

The INA223 has three available current shunt voltage gain options that can be selected using the two-wire interface. This allows for optimization of the output signal to maximize the available dynamic range. This flexibility provides a benefit over a fixed-gain current shunt monitor. A fixed-gain current shunt monitor has a finite range of current that can be monitored based on the limitations of the output stage of the device.

For example, in a typical application using a fixed-gain current shunt monitor, the shunt resistor is selected to achieve the maximum allowable full-scale output based on the maximum expected current to be monitored and the fixed gain value of the current shunt monitor. One limitation to a fixed gain approach is in the minimum current level that can be monitored. The minimum current than can be monitored is based on the ability of the output stage of the current shunt monitor to swing to ground. This minimum current level is calculated based on the maximum swing to ground specification (50 mV for the INA223), which is then divided by the fixed gain of the device. This calculation provides the minimum differential voltage that can be monitored and then divided by the shunt resistor to determine the minimum current that can be monitored. After the monitored current drops below this level, further decreases in the monitored current can no longer be detected at the output. The ability to switch the current shunt voltage gain to a higher gain setting brings the output level above this saturation point and enables lower currents to be monitored, thus extending the dynamic range of the device.

Bus Voltage Range

The INA223 monitors bus voltages that can range from 0 V to 26 V. This voltage must be internally divided down to interface with the analog multiplier and output stage circuitry. The supply voltage for the INA223 can range from 2.7 V to 5.5 V; therefore, the bus voltage must be divided down so that it does not exceed the supply voltage. If this divider ratio or attenuation factor results in an internal voltage that exceeds the supply voltage, the measurement circuitry is saturated. The device will not be damaged, but the measurement result at the output will be invalid. Having multiple attenuation factors (0.1 V/V, 0.2 V/V, 0.4 V/V) allows for the optimization of the output range based on the specific common-mode voltage present. Having multiple values that can be selected provides a helpful advantage over a single fixed-attenuation device, given the wide common-mode range of the INA223. With a single attenuation factor, the maximum common-mode voltage (26 V) must be divided down to less than the minimum supply voltage (2.7 V). A bus voltage less than 26 V results in a significantly smaller output range. The ability to switch between different attenuation settings allows the device to be configured to maximize the dynamic output range at multiple common-mode voltage levels. Additionally, because the power calculation is based on the bus voltage measurement, the larger the corresponding representation of the common-mode voltage, the more accurate the power calculation.

Output Range

The power calculation has two inputs: the current shunt voltage measurement, as well as the bus voltage measurement. Both of these measurements must be valid (within the linear range of the device) to achieve a valid power calculation. Set the gain setting for the current shunt voltage and attenuation setting for the bus voltage to allow each of these two measurements to remain within the linear range of the device, based on the input conditions. Saturating one of these two measurements may not result in the output being saturated based on the internal scaling of the analog multiplier; therefore, care should be taken to ensure that the two inputs to the multiplier are valid.

Shutting Down the INA223

The INA223 includes a shutdown feature that is programmed through the serial interface. Setting the Enable bit in the Configuration Register to '0' places the INA223 into a disabled state. While in the disabled state, the input bias currents and device quiescent current drop below 1 µA, thus reducing the power consumption of the system when this device is not in use. The device is placed back into the active mode by setting the Enable bit high. The time required for the INA223 output to be valid after enabling the device to come out of the shutdown state is typically 40 µs.

In addition to responding to the Enable bit, the INA223 also responds to an Enable and Disable General Call as described in the GENERAL CALL section.

CONFIGURATION REGISTER

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	—	—	—	—	—	—	—	—	EN	OUT1	OUT0	GSV1	GSV0	GBV1	GBV0
POR VALUE	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1

EN **Enable/Disable Mode**

Bit 6 Setting this bit to '0' places the device into a disabled mode.

This mode drops the input bias current to 1 μA for each of the analog inputs and reduces the quiescent current to 1 μA.

OUT **Output Mode**

Bits 4, 5 Controls the setting of the output mux to select the signal that is available at the output pin. There are two different mode settings for selecting power at the output pin. The Supply Power output mode sets the bus voltage measurement to be taken at the V_{IN+} pin to calculate the power provided by the power supply. The Load Power output mode sets the bus voltage measurement to be taken at the V_{IN-} pin to calculate the power consumed by the load. Refer to Table 1.

Table 1. Output Mode Settings(1)

OUT1	OUT0	
D5	D4	OUTPUT MODE
0	0	Bus Voltage Measurement
0	1	Shunt Voltage Measurement
1	0	Supply Power
1	1	Load Power

(1) Shaded cells indicate default value.

GSV **Current Shunt Voltage Gain**

Bits 2, 3 Sets the gain for the current shunt voltage measurement. Table 2 summarizes the gain settings.

Table 2. Current Shunt Voltage Gain Settings(1)

GSV1	GSV0	
D3	D2	CURRENT SHUNT VOLTAGE GAIN
0	0	20 V/V
0	1	128 V/V
1	0	300 V/V

(1) Shaded cells indicate default value.

GBV **Bus Voltage Gain**

Bits 0, 1 Sets the gain for the bus voltage measurement. Refer to Table 3.

Table 3. Bus Voltage Gain Settings(1)

GBV1	GBV0	
D1	D0	BUS VOLTAGE GAIN
0	0	2/5 V/V
0	1	1/5 V/V
1	0	1/10 V/V

(1) Shaded cells indicate default value.

OUTPUT

The signal available at the output pin is selected by the output mode setting programmed in the Configuration Register. The default setting for the output mux is the Supply Power mode. For the power value to be valid, both the shunt voltage measurement and the bus voltage measurement must both be valid (within the linear range of the device).

Power Calculation

The output voltage for the two power output modes is calculated as shown in Equation 1. To convert the output voltage to the corresponding power representation, the output voltage must be divided by the product of the power gain shown in Table 4 and the value of the shunt resistor.

$$V_{OUT} = (V_{CM})(V_{SENSE})(POWER_{GAIN}) \quad (1)$$

$$POWER = \frac{V_{OUT}}{(POWER_{GAIN})(R_{SHUNT})} \quad (2)$$

Table 4. $Power_{GAIN}$ Values

GBV	GSV	$POWER_{GAIN}$
0.1 V/V	20 V/V	0.667
0.1 V/V	128 V/V	4.267
0.1 V/V	300 V/V	10
0.2 V/V	20 V/V	1.333
0.2 V/V	128 V/V	8.533
0.2 V/V	300 V/V	20
0.4 V/V	20 V/V	2.667
0.4 V/V	128 V/V	17.067
0.4 V/V	300 V/V	40

Power Calculation Example

The following example is based on Figure 34. In this example the system consists of a load current of 5 A and a common-mode voltage of 12 V. This 5-A current flowing through the 1-mΩ shunt resistor develops a differential voltage of 5 mV across the INA223 input pins. With the 3.3-V supply voltage shown here, a practical full-scale target for the output voltage is 3 V.

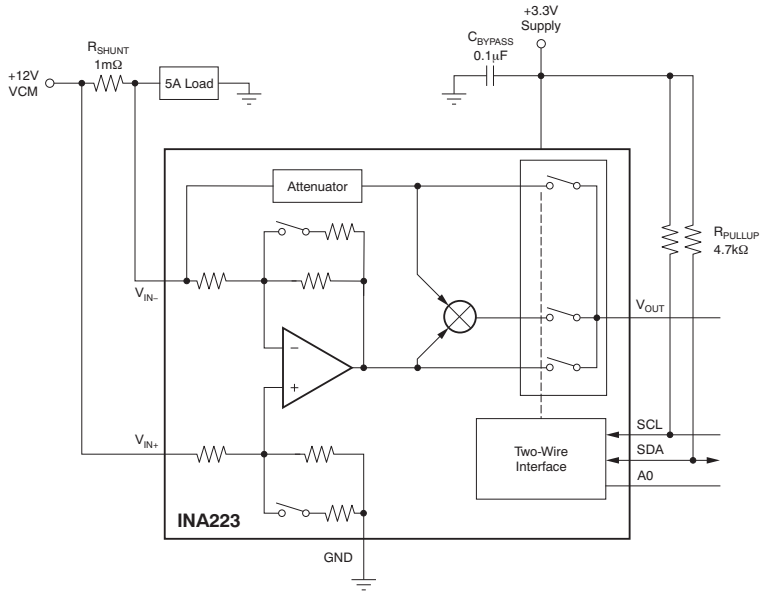


Figure 34. Example Circuit

Current Shunt Voltage Measurement Mode

Based on the 5-mV differential voltage present at the input and the device set to Current Shunt Voltage mode, a current shunt voltage gain setting of 300 V/V is selected resulting in an output voltage of 1.5 V. A current shunt voltage gain setting less than 300 V/V could also be used in this example. The drawback of a lower gain setting is a smaller dynamic range present at the output as well as a less accurate input for the power measurement in the Power Output mode. A larger shunt resistor (2 mΩ) could also be used to increase the full-scale drop to result. One drawback of increasing the impedance of the shunt resistor is the increased power dissipation requirement the component must be able to accommodate. A higher-accuracy power measurement is obtained with the largest possible input from the current shunt voltage, while remaining within the linear range of the device.

Bus Voltage Measurement Mode

Assuming the same 3-V target as previously discussed, and with the device set to Bus Voltage mode, an attenuation factor of 0.2 V/V results in an output voltage of 2.4 V. An attenuation factor of 0.1 V/V could also be used, but results in a lower dynamic output range. An attenuation factor of 0.4 V/V cannot be used in this example because it results in an internal voltage of 4.8 V, exceeding the supply voltage of 3.3 V.

Power Modes

For the power output modes, the current shunt voltage and bus voltage measurements are multiplied by the Power Gain factor to yield a voltage output representing the calculated power. In this example, the 5 mV developed across the shunt resistor is multiplied by the 12-V bus voltage. This product is then multiplied by the Power Gain factor of 20 (GSV = 300 V/V, GBV = 0.2 V/V; See Table 4), and results in a 1.2-V output voltage representation of the power. Using Equation 2 and the corresponding Power Gain of 20, the power being consumed by the load is calculated to be 60 W. This corresponds to the original 5-A load current and 12-V common-mode voltage conditions.

Bus Voltage Measurement Location for Power Output Modes

For the power output mode, the bus voltage can be measured either at the V_{IN+} (supply side) or at the $V_{IN–}$ (load side) pins when the current shunt voltage gain setting is 20. When the current shunt voltage gain setting is 128 or 300, this measurement assumes a relatively small differential voltage is being developed across the sense resistor. With a small drop across the sense resistor, the voltages at V_{IN+} and $V_{IN–}$ are very close to one another, making the shunt voltage impact on the bus voltage measurement much less critical. When the device set to a gain of 20, it implies that a greater differential voltage is being developed across the sense resistor, causing the voltages at the V_{IN+} and $V_{IN–}$ pins to be noticeably different. The power calculation can be configured to measure the bus voltage either at V_{IN+} (Supply Power) or at $V_{IN–}$ (Load Power). If the power being supplied by the power supply is of interest, the Supply Power mode should be selected as the output mode setting. If the power being consumed by the load is of interest, the Load Power mode should be selected as the output mode setting. Note that the bus voltage measurement location is only available for the power calculation. For the Bus Voltage output mode, the bus voltage is always measured at the V_{IN+} pin.

Input Filtering

An obvious and straightforward location for filtering is at the output of the INA223. However, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA223. Figure 35 shows a filter placed at the inputs pins.

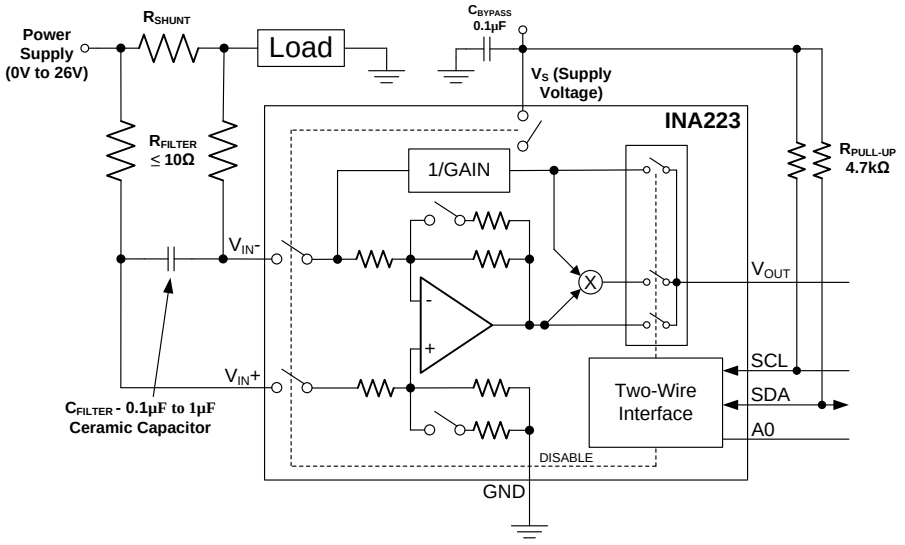


Figure 35. Input Filter

The addition of external series resistance, though, creates an additional error that is not present under normal operating conditions. An internal bias network at the input pins creates a mismatch in input bias currents when a differential voltage is applied to the device's input pins. This results in a mismatch of voltage drops on the input lines due to the mismatch of input bias currents flowing through the additional external series filter resistors. This creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. The result is a reduced differential voltage at the device input pins relative to the expected shunt voltage created by the load current flowing through the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on the operation of the device.

The amount of variance in the differential voltage present directly at the input pins relative to the voltage developed at the shunt resistor is based both on values of external series resistance as well as the internal input resistors (R_{INT}), which is based on the shunt voltage gain setting as shown in Table 5. The reduction of the shunt voltage reaching the device input pins appears as a gain error when looking at the output voltage relative to the shunt voltage. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 3.

$$\text{Gain Error Factor} = \frac{(1250 \cdot R_{INT})}{(1250 \cdot R_S) + (1250 \cdot R_{INT}) + (R_S \cdot R_{INT})} \quad (3)$$

Where

- R_{INT} is the internal input resistance.
- R_S is the external series resistance.

With the adjustment factor equation including the device internal input resistance, this factor will vary with each gain setting.

Table 5. Internal Resistance Values

GAIN SETTING	R_{INT}
20	600 kΩ
128	93 kΩ
300	40 kΩ

Using The INA223 with Common-Mode Transients Above 26 V

The INA223 is designed for a maximum common-mode voltage of 26 V. In applications that may be subjected to transients above 26 V, the INA223 inputs must be protected. Figure 36 is the recommended method for protecting the INA223 to these transients. Use only zener diodes or zener-type transient absorbers (also known as a TransZorb™). Most other types of transient absorbers have an unacceptable time delay. The input resistors shown in Figure 36 should be kept as small as possible (less than 10 Ω) to limit the effects this resistance has on the gain, as discussed in the Input Filtering section.

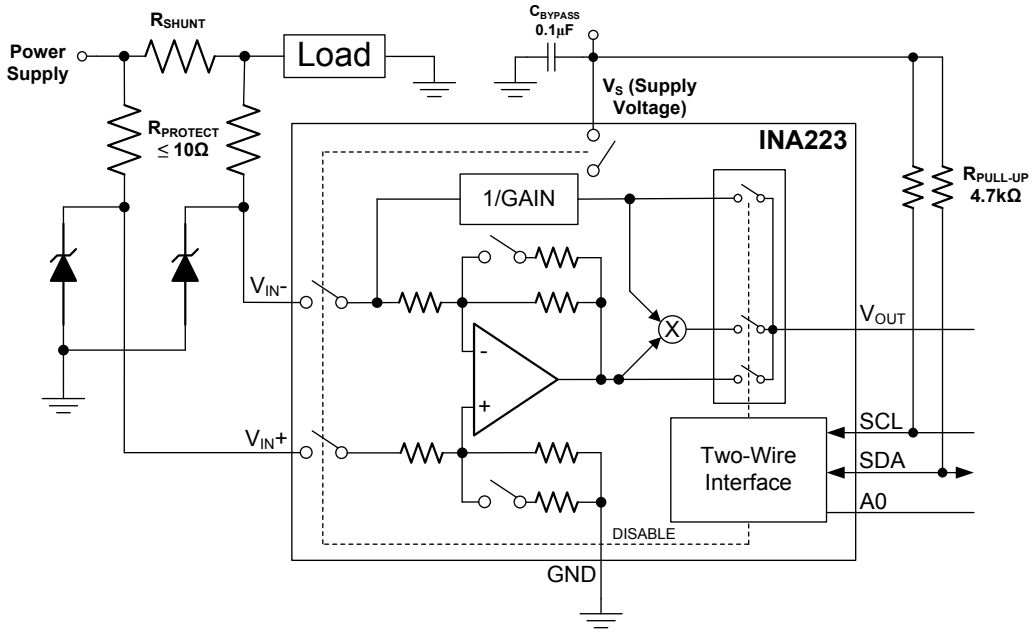


Figure 36. INA223 Transient Protection

Low-Side Current Sensing

The bus voltage of the INA223 is measured internally at the V_{IN+} pin, making it a high-side-only power monitor. However, the INA223 can be used for low-side current sensing, as shown in Figure 37 (as the common-mode voltage ranges from 0 V to 26 V).

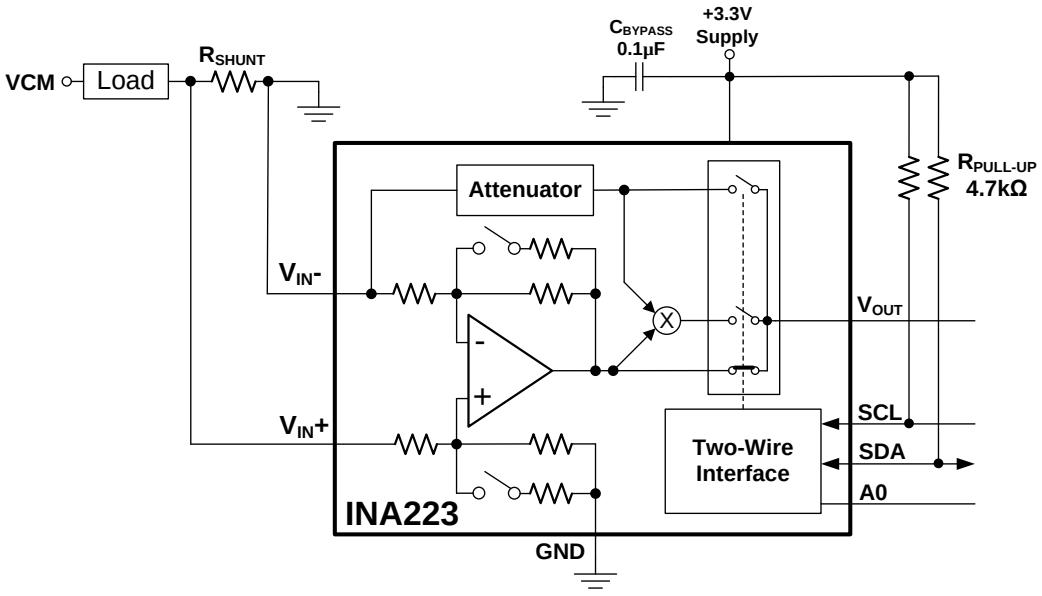
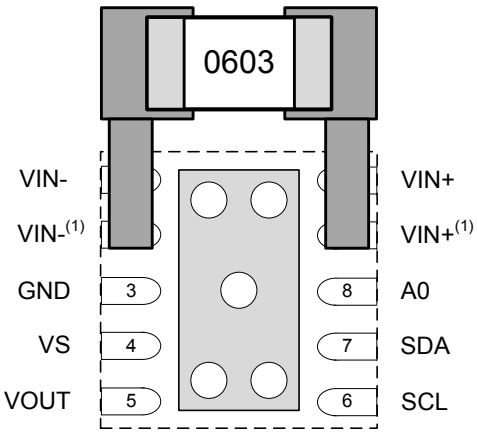


Figure 37. Low-Side Sensing with INA223

INA223 Recommended Layout

The recommended layout is shown in Figure 38. Pins 2 and 9 should be connected directly to Pins 1 and 10, respectively. The shunt resistor should be placed as closely to the input pins, VIN+ and VIN-, to minimize any parasitics or added resistance. Use a four-wire, or kelvin, connection to the shunt to achieve the most accurate measurement across the shunt.



(1) See *Application Information* section for a description of how to connect input pins to the shunt resistor.

Figure 38. INA223 Recommended Layout

BUS OVERVIEW

The INA223 is compatible with both two-wire and SMBus interfaces. These protocols are essentially compatible with one another. The two-wire interface is used throughout this data sheet as the primary example, with the SMBus protocol specified only when a difference between the two systems is considered.

Two bidirectional lines, SCL and SDA, connect the INA223 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates *start* and *stop* conditions.

To address a specific device, the master initiates a *start* condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a *start* or *stop* condition.

After all data have been transferred, the master generates a *stop* condition, indicated by pulling SDA from low to high while SCL is high. The INA223 includes a 28-ms timeout on its interface to prevent locking up the bus.

Serial Bus Address

To communicate with the INA223, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit that indicates the intent of executing a read or write operation.

The INA223 has one address pin, A0. Table 6 describes the pin logic levels for each of the four possible addresses. The state of the A0 pin is sampled on every bus communication and should be set before any activity on the interface occurs. The address pins are read at the start of each communication event.

Table 6. INA223 Address Pins and Slave Addresses

A0	ADDRESS
GND	1000000
V_S	1000001
SDA	1000010
SCL	1000011

Serial Interface

The INA223 operates only as a slave device on both the two-wire bus and SMBus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The INA223 supports the transmission protocol for fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted most significant byte first.

GENERAL CALL

The INA223 responds to three unique two-wire general call commands. A response occurs to a general call address (0000000) if the eighth bit is '0'. The device acknowledges the general call address and responds to commands based on the second byte. The three commands that the INA223 responds to are:

- General Call Reset (06h)
- General Call Enable (81h)
- General Call Disable (82h)

The INA223 responds to the General Call Reset by resetting all of the Configuration Registers settings to the respective default power-on values. The INA223 responds to a General Call Enable or General Call Disable by entering into or exiting from a disabled state. The INA223 can also be enabled and disabled by setting or clearing the enable/disable mode (EN) bit in the Configuration Register. The General Call Enable and General Call Disable commands allow for a single command to place multiple connected INA223 devices into either an enabled or disabled state.

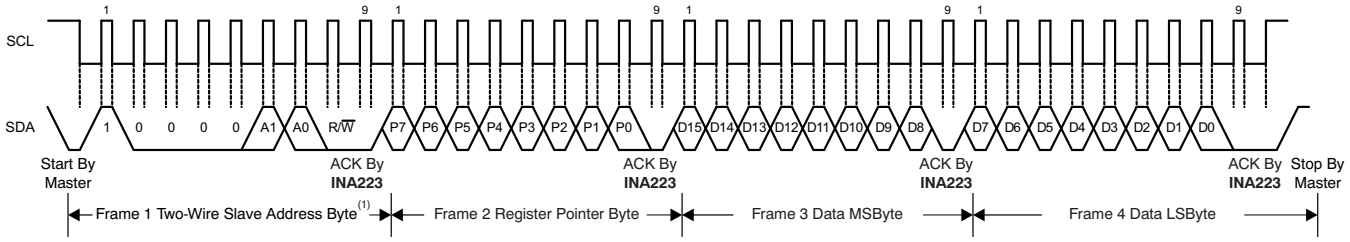
WRITING TO AND READING FROM THE INA223

The INA223 has a single configuration register. This register is used to configure the INA223 based on how the device is to be used. This register can also be read to determine the register contents and the current device configuration.

Writing to the Configuration Register in the INA223 begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit low. The INA223 then acknowledges receipt of a valid address. The next two bytes are written to the register addressed by the register pointer. The INA223 acknowledges receipt of each data byte. The master may terminate data transfer by generating a *start* or *stop* condition.

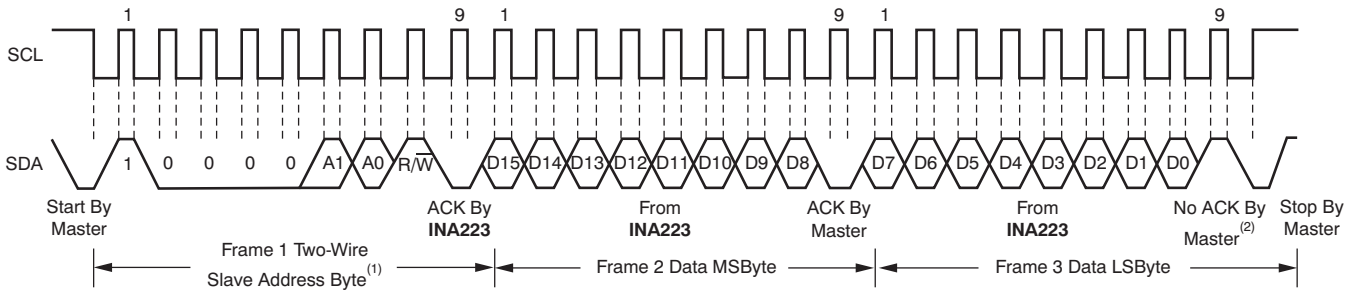
When reading the Configuration Register in the INA223, the communication sequence begins the same with the first byte being transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit high. The INA223 then acknowledges receipt of a valid address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an acknowledge bit from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a not-acknowledge bit after receiving any data byte, or by generating a *start* or *stop* condition.

Figure 39 and Figure 40 show read and write operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the Slave Address Byte is determined by the setting of the A0 pin. Refer to Table 1.

Figure 39. Timing Diagram for Write Word Format



(1) The value of the Slave Address Byte is determined by the setting of the A0 pin. Refer to Table 1.

(2) ACK by master can also be sent.

Figure 40. Timing Diagram for Read Word Format

High-Speed Two-Wire Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a *start* condition followed by a valid serial byte containing high-speed (HS) master code *00001XXX*. This transmission is made in either fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The INA223 does not acknowledge the HS master code, but recognizes it and switches its internal filters to support 3.4-MHz operation.

The master then generates a repeated *start* condition (a *repeated start* condition has the same timing as the *start* condition). After this *repeated start* condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 MHz are allowed. Instead of using a *stop* condition, *repeated start* conditions should be used to secure the bus in HS-mode. A *stop* condition ends the HS-mode and switches all the internal filters of the INA223 to support the F/S mode. Figure 41 illustrates the bus timing. Corresponding definitions are listed in Table 7.

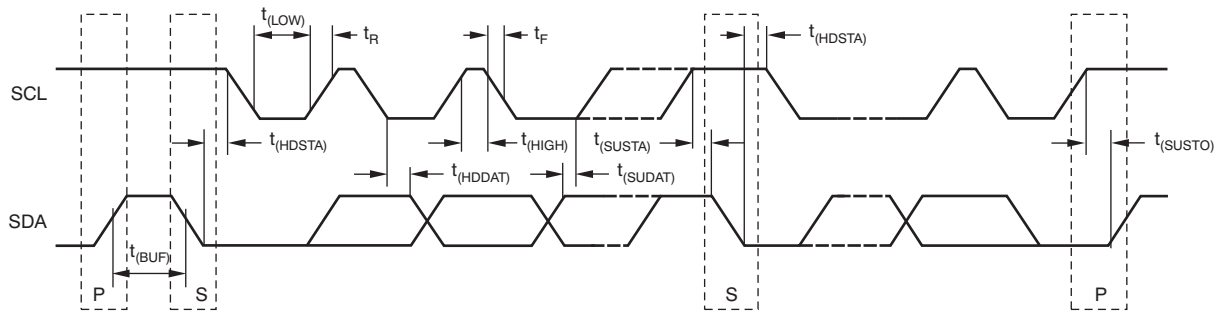


Figure 41. Bus Timing Diagram

Table 7. Bus Timing Diagram Definitions

SYMBOL	DESCRIPTION	FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	3.4	MHz
$t_{(BUF)}$	Bus free time between *stop* and *start* conditions	600		160		ns
$t_{(HDSTA)}$	Hold time after *repeated start* condition. After this period, the first clock is generated.	100		100		ns
$t_{(SUSTA)}$	*Repeated start* condition setup time	100		100		ns
$t_{(SUSTO)}$	*Stop* condition setup time	100		100		ns
$t_{(HDDAT)}$	Data hold time	15		15		ns
$t_{(SUDAT)}$	Data setup time	100		10		ns
$t_{(LOW)}$	SCL clock low period	1300		160		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
t_F	Clock/Data fall time		300		160	ns
t_R	Clock/Data rise time		300		160	ns
	Clock/Data rise time for SCLK ≤ 100 kHz		1000			ns

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
INA223AIDSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
INA223AIDSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

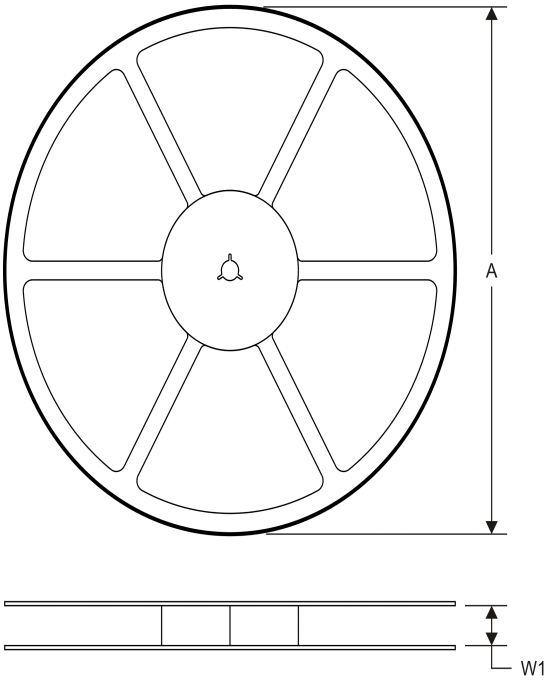
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

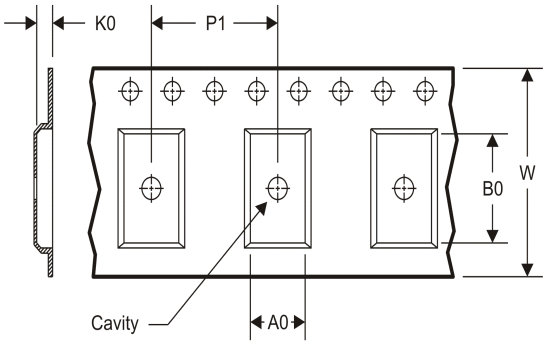
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



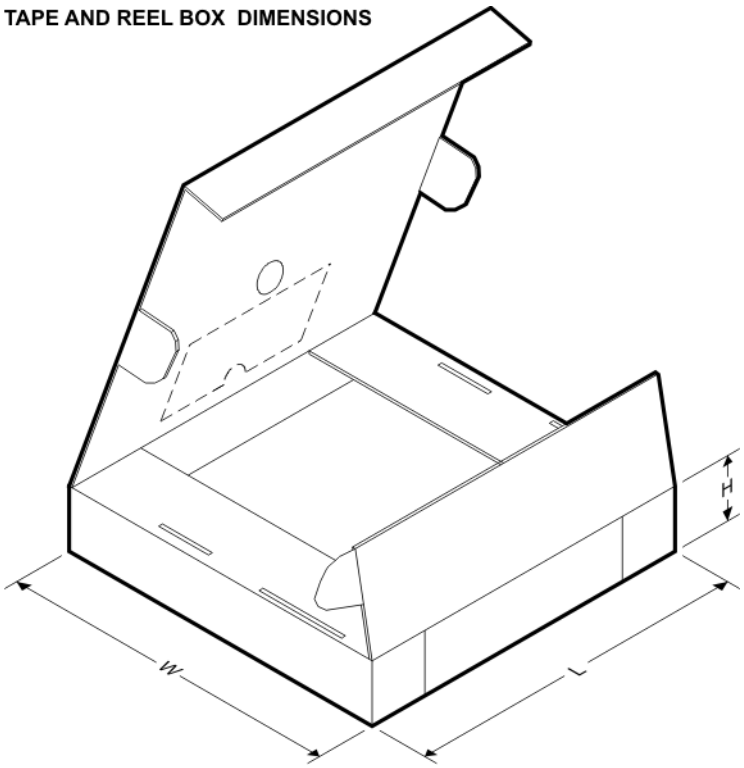
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA223AIDSKR	SON	DSK	10	3000	330.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
INA223AIDSKT	SON	DSK	10	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

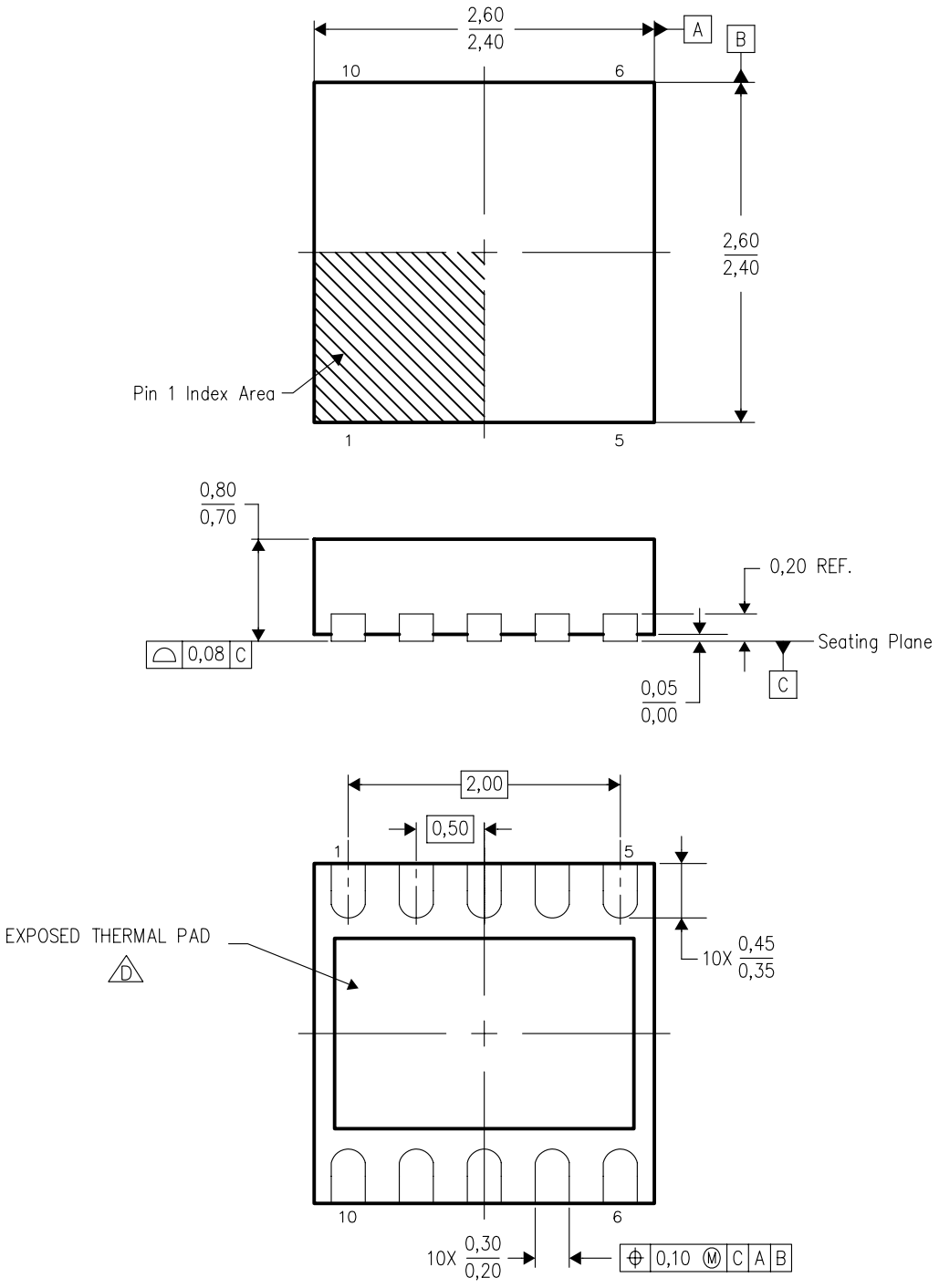
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA223AIDSKR	SON	DSK	10	3000	367.0	367.0	35.0
INA223AIDSKT	SON	DSK	10	250	210.0	185.0	35.0

DSK (S–PDSO–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

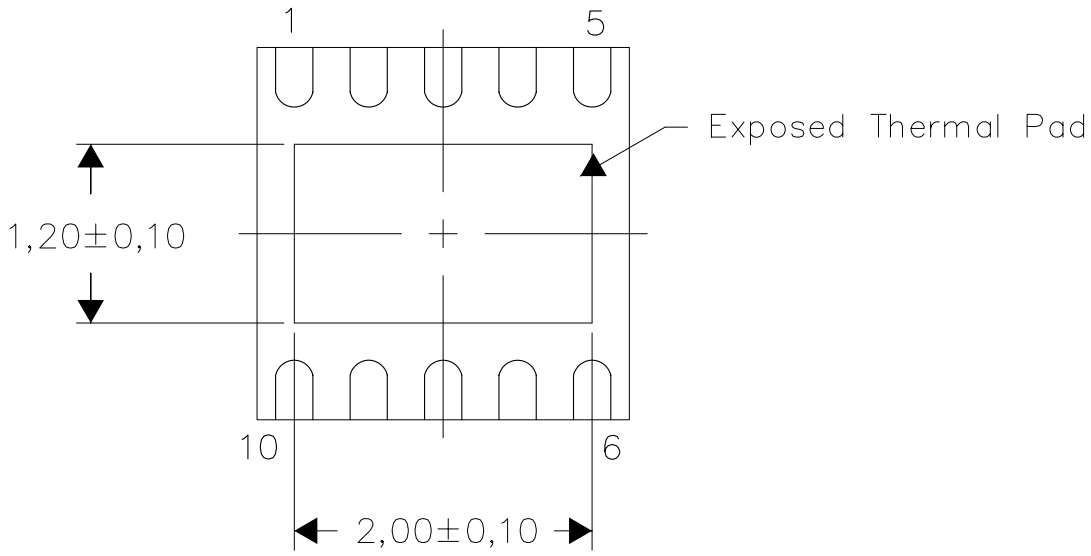
DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



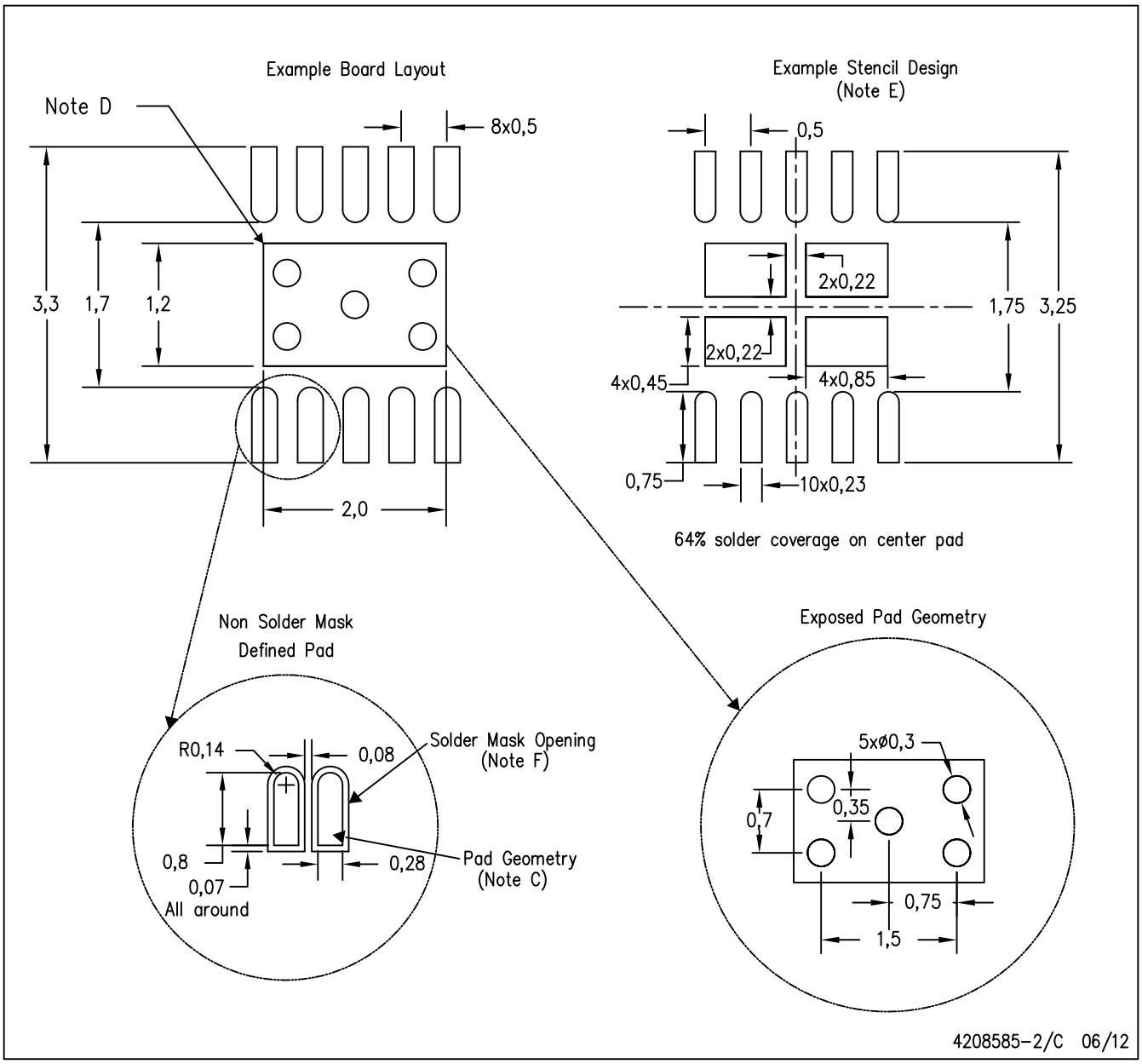
Bottom View

Exposed Thermal Pad Dimensions

4208579–2/D 10/10

NOTE: A. All linear dimensions are in millimeters

DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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