

## FEATURES

- Peak efficiency up to 95% at 1.2V
- Integrated driver, control MOSFET, synchronous MOSFET and Schottky diode
- Input voltage (VIN) operating range up to 15V
- Output voltage range from 0.25V up to 3.3
- Output current capability of 60A DC
- Operation up to 1.0MHz
- Integrated current sense amplifier
- VCC under voltage lockout
- Thermal flag
- Body-Braking™ load transient support
- Diode-emulation high efficiency mode
- Compatible with 3.3V PWM logic and VCC tolerant
- Compliant with Intel DrMOS V4.0
- PCB footprint compatible with IR3576
- Enhanced top side cooling through exposed pad
- Small 6mm x 6mm x 0.65mm PQFN package
- Lead free RoHS compliant package

## APPLICATIONS

- Voltage Regulators for CPUs, GPUs, and DDR memory arrays
- High current, low profile DC-DC converters

## DESCRIPTION

The IR3575 exposed-top integrated PowIRstage® is a synchronous buck gate driver co-packed with a control MOSFET and a synchronous MOSFET with integrated Schottky diode. It is optimized internally for PCB layout, heat transfer and driver/MOSFET timing. Custom designed gate driver and MOSFET combination enables higher efficiency at lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

Up to 1.0MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency. The IR3575's superior efficiency enables smallest size and lower solution cost. The IR3575 PCB footprint is compatible with the IR3576 (50A).

Integrated current sense amplifier achieves superior current sense accuracy and signal to noise ratio vs. best-in-class controller based Inductor DCR sense methods.

The IR3575 incorporates the Body-Braking™ feature which enables reduction of output capacitors and is activated quickly. Synchronous diode emulation mode in the IR3575 removes the zero-current detection burden from the PWM controller and increases system light-load efficiency.

The IR3575 is optimized specifically for CPU core power delivery in server applications. The ability to meet the stringent requirements of the server market also makes the IR3575 ideally suited to powering GPU and DDR memory designs and other high current applications.

## BASIC APPLICATION

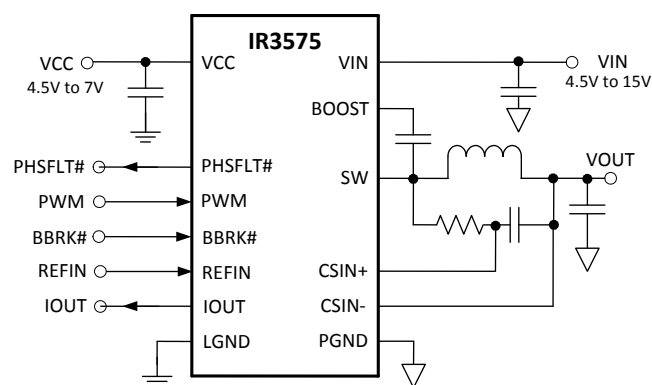


Figure 1: IR3575 Basic Application Circuit

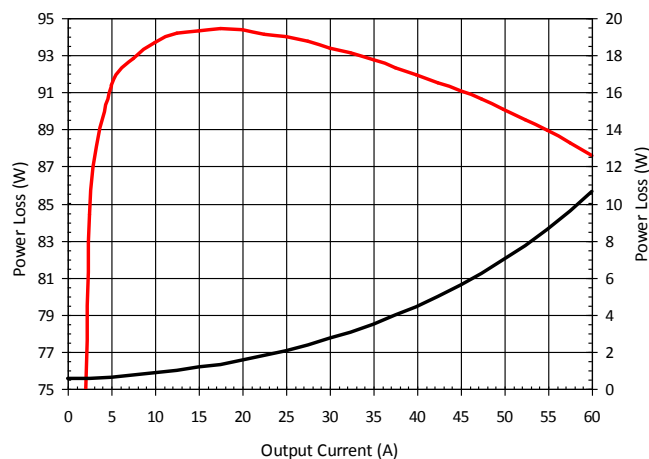


Figure 2: Typical IR3575 Efficiency & Power Loss (See Note 2 on Page 8)

## PINOUT DIAGRAM

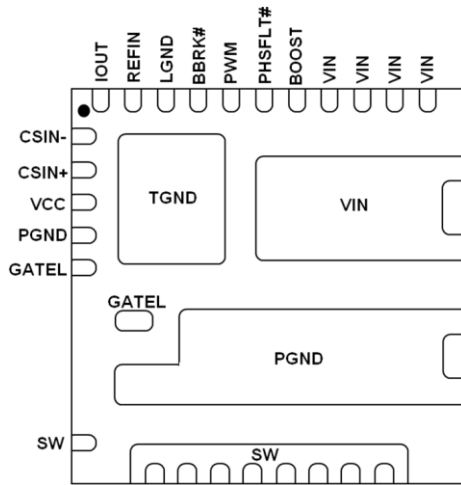


Figure 3: IR3575 Pin Diagram, Top View

## ORDERING INFORMATION

| Package                    | Tape & Reel Qty | Part Number  |
|----------------------------|-----------------|--------------|
| PQFN, 32 Lead<br>6mm x 6mm | 3000            | IR3575MTRPBF |

## TYPICAL APPLICATION DIAGRAM

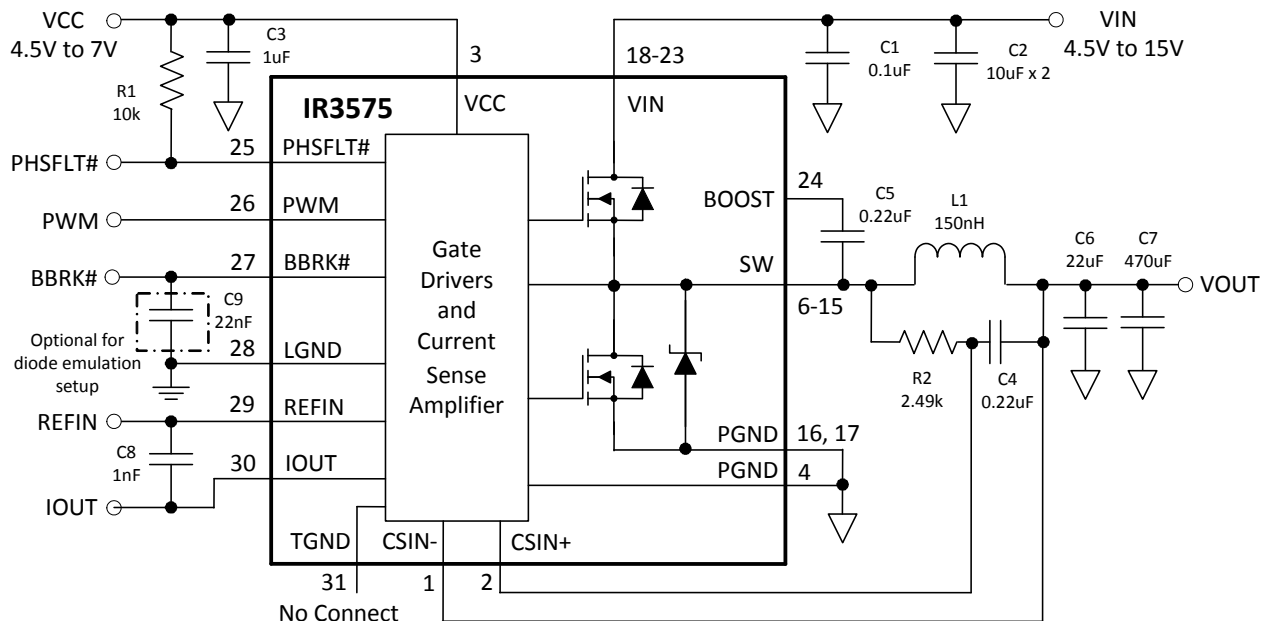


Figure 4: Application Circuit with Current Sense Amplifier

## TYPICAL APPLICATION DIAGRAM (CONTINUED)

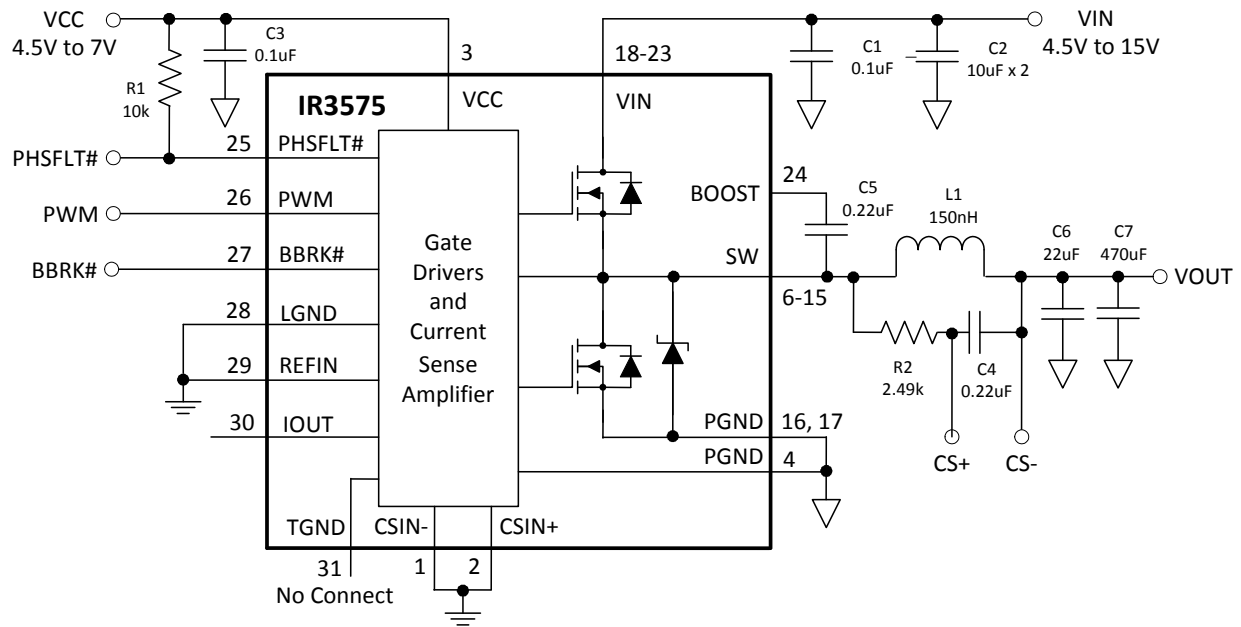


Figure 5: Application Circuit without Current Sense Amplifier

## FUNCTIONAL BLOCK DIAGRAM

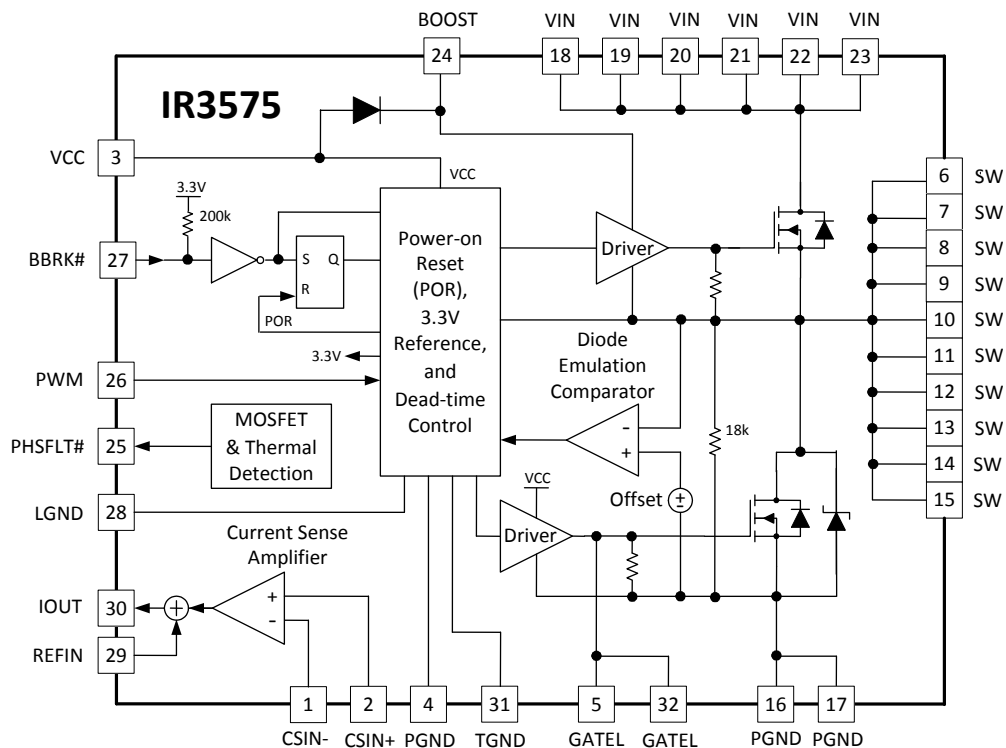


Figure 6: IR3575 Functional Block Diagram

## PIN DESCRIPTIONS

| PIN #       | PIN NAME | PIN DESCRIPTION                                                                                                                                                                                                                                                                                                                                                          |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1           | CSIN-    | Inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.                                                                                                                                                                                                                                                              |
| 2           | CSIN+    | Non-Inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.                                                                                                                                                                                                                                                          |
| 3           | VCC      | Bias voltage for control logic. Connect a minimum 1uF cap between VCC and PGND (pin 4) if current sense amplifier is used. Connect a minimum 0.1uF cap between VCC and PGND (pin 4) if current sense amplifier is not used.                                                                                                                                              |
| 4, 16, 17   | PGND     | Power ground of MOSFET driver and the synchronous MOSFET. MOSFET driver signal is referenced to this pin.                                                                                                                                                                                                                                                                |
| 5, 32       | GATEL    | Low-side MOSFET driver pins that can be connected to a test point in order to observe the waveform.                                                                                                                                                                                                                                                                      |
| 6 – 15      | SW       | Switch node of synchronous buck converter.                                                                                                                                                                                                                                                                                                                               |
| 18 – 23     | VIN      | High current input voltage connection. Recommended operating range is 4.5V to 15V. Connect at least two 10uF 1206 ceramic capacitors and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to VIN pins and PGND pins (16-17). The 0.1uF 0402 capacitor should be on the same side of the PCB as the IR3575.                                      |
| 24          | BOOST    | Bootstrap capacitor connection. The bootstrap capacitor provides the charge to turn on the control MOSFET. Connect a minimum 0.22uF capacitor from BOOST to SW pin. Place the capacitor as close to BOOST pin as possible and minimize the parasitic inductance of the connection from the capacitor to SW pin.                                                          |
| 25          | PHSFLT#  | Open drain output of the phase fault circuits. Connect to an external pull-up resistor. Output is low when a MOSFET fault or over temperature condition is detected.                                                                                                                                                                                                     |
| 26          | PWM      | 3.3V logic level tri-state PWM input and 7V tolerant. “High” turns the control MOSFET on, and “Low” turns the synchronous MOSFET on. “Tri-state” turns both MOSFETs off in Body-Braking® mode. In diode emulation mode, “Tri-state” activates internal diode emulation control. See “PWM Tri-state Input” Section for further details about the PWM Tri-State functions. |
| 27          | BBRK#    | 3.3V logic level input and 7V tolerant with internal weak pull-up to 3.3V. Logic low disables both MOSFETs. Pull up to VCC if Body-Braking® is not used. Pulling BBRK# low at least 20ns after VCC passes its UVLO threshold selects internal diode emulation control. See “Body-Braking® Mode” Section for further details.                                             |
| 28          | LGND     | Signal ground. Driver control logic, analog circuits and IC substrate are referenced to this pin.                                                                                                                                                                                                                                                                        |
| 29          | REFIN    | Reference voltage input from the PWM controller. IOUT signal is referenced to the voltage on this pin. Connect to LGND if the current sense amplifier is not used.                                                                                                                                                                                                       |
| 30          | IOUT     | Current output signal. Voltage on this pin is equal to $V(\text{REFIN}) + 32.5 * [V(\text{CSIN+}) - V(\text{CSIN-})]$ . Float this pin if the current sense amplifier is not used.                                                                                                                                                                                       |
| 31          | TGND     | This pin is connected to internal power and signal ground of the driver. For best performance of the current sense amplifier, TGND must be electrically isolated from Power Ground (PGND) and Signal Ground (LGND) in the PCB layout.                                                                                                                                    |
| Exposed Pad | SW       | Exposed pad on top side of the package. Connect to a heat sink through insulated thermal material to improve the thermal performance of the package.                                                                                                                                                                                                                     |

## ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

| PIN Number | PIN NAME           | V <sub>MAX</sub> | V <sub>MIN</sub>          | I <sub>SOURCE</sub>       | I <sub>SINK</sub>         |
|------------|--------------------|------------------|---------------------------|---------------------------|---------------------------|
| 1          | CSIN-              | VCC + 0.3V       | -0.3V                     | 1mA                       | 1mA                       |
| 2          | CSIN+              | VCC + 0.3V       | -0.3V                     | 1mA                       | 1mA                       |
| 3          | VCC                | 8V               | -0.3V                     | NA                        | 5A for 100ns,<br>200mA DC |
| 4          | PGND               | 0.3V             | -0.3V                     | 15mA                      | 15mA                      |
| 5, 32      | GATEL              | VCC + 0.3V       | -3V for 20ns,<br>-0.3V DC | 1A for 100ns,<br>200mA DC | 1A for 100ns,<br>200mA DC |
| 6-15       | SW <sup>2</sup>    | 25V              | -5V for 20ns,<br>-0.3V DC | 65A RMS                   | 30A RMS                   |
| 16, 17     | PGND               | NA               | NA                        | 30A RMS                   | 65A RMS                   |
| 18-23      | VIN <sup>2</sup>   | 25V              | -0.3V                     | 5A RMS                    | 25A RMS                   |
| 24         | BOOST <sup>1</sup> | 33V              | -0.3V                     | 1A for 100ns,<br>100mA DC | 5A for 100ns,<br>100mA DC |
| 25         | PHSFLT#            | VCC + 0.3V       | -0.3V                     | 1mA                       | 20mA                      |
| 26         | PWM                | VCC + 0.3V       | -0.3V                     | 1mA                       | 1mA                       |
| 27         | BBRK#              | VCC + 0.3V       | -0.3V                     | 1mA                       | 1mA                       |
| 28         | LGND               | 0.3V             | -0.3V                     | 15mA                      | 15mA                      |
| 29         | REFIN              | 3.5V             | -0.3V                     | 1mA                       | 1mA                       |
| 30         | IOUT               | VCC + 0.3V       | -0.3V                     | 5mA                       | 5mA                       |
| 31         | TGND               | 0.3V             | -0.3V                     | NA                        | NA                        |

**Note:**

1. Maximum BOOST – SW = 8V.
2. Maximum VIN – SW = 25V.
3. All the maximum voltage ratings are referenced to PGND (Pins 16 and 17).

| THERMAL INFORMATION                                                 |                             |
|---------------------------------------------------------------------|-----------------------------|
| Thermal Resistance, Junction to Top ( $\theta_{JC\_TOP}$ )          | 0.5 °C/W                    |
| Thermal Resistance, Junction to PCB (pin 17) ( $\theta_{JC\_PCB}$ ) | 1.7 °C/W                    |
| Thermal Resistance ( $\theta_{JA}$ ) <sup>1</sup>                   | 19.1 °C/W                   |
| Maximum Operating Junction Temperature                              | -40 to 150°C                |
| Maximum Storage Temperature Range                                   | -65°C to 150°C              |
| ESD rating                                                          | HBM Class 1C JEDEC Standard |
| MSL Rating                                                          | 3                           |
| Reflow Temperature                                                  | 260°C                       |

**Note:**

1. Thermal Resistance ( $\theta_{JA}$ ) is measured with the component mounted on a high effective thermal conductivity test board in free air. Refer to International Rectifier Application Note AN-994 for details.

## ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

### RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

| PARAMETER                                  | SYMBOL          | MIN  | MAX       | UNIT |
|--------------------------------------------|-----------------|------|-----------|------|
| Recommended VIN Range                      | VIN             | 4.5  | 15        | V    |
| Recommended VCC Range                      | VCC             | 4.5  | 7         | V    |
| Recommended REFIN Range                    | REFIN           | 0.25 | VCC - 2.5 | V    |
| Recommended Switching Frequency            | f <sub>sw</sub> | 200  | 1000      | kHz  |
| Recommended Operating Junction Temperature | T <sub>J</sub>  | -40  | 125       | °C   |

## ELECTRICAL CHARACTERISTICS

| PARAMETER                                | SYMBOL                   | CONDITIONS                                         | MIN  | TYP  | MAX  | UNIT |
|------------------------------------------|--------------------------|----------------------------------------------------|------|------|------|------|
| Efficiency                               |                          |                                                    |      |      |      |      |
| IR3575 Peak Efficiency <sup>Note 1</sup> | $\eta$                   | Note 2. See Figure 2.                              |      | 94.5 |      | %    |
|                                          |                          | Note 3. See Figure 7.                              |      | 93.5 |      | %    |
| PWM Comparator                           |                          |                                                    |      |      |      |      |
| PWM Input High Threshold                 | V <sub>PWM_HIGH</sub>    | PWM Tri-state to High                              | 2.5  |      |      | V    |
| PWM Input Low Threshold                  | V <sub>PWM_LOW</sub>     | PWM Tri-state to Low                               |      |      | 0.8  | V    |
| PWM Tri-state Float Voltage              | V <sub>PWM_TRI</sub>     | PWM Floating                                       | 1.2  | 1.65 | 2.1  | V    |
| Hysteresis                               | V <sub>PWM_HYS</sub>     | Active to Tri-state or Tri-state to Active, Note 1 | 65   | 76   | 100  | mV   |
| Tri-state Propagation Delay              | t <sub>PWM_DELAY</sub>   | PWM Tri-state to Low transition to GATEL >1V       |      | 38   |      | ns   |
|                                          |                          | PWM Tri-state to High transition to GATEH >1V      |      | 18   |      | ns   |
| PWM Sink Impedance                       | R <sub>PWM_SINK</sub>    |                                                    | 3.67 | 5.1  | 8.70 | kΩ   |
| PWM Source Impedance                     | R <sub>PWM_SOURCE</sub>  |                                                    | 3.67 | 5.1  | 8.70 | kΩ   |
| Internal Pull up Voltage                 | V <sub>PWM_PULLUP</sub>  | VCC > UVLO                                         |      | 3.3  |      | V    |
| Minimum Pulse Width                      | t <sub>PWM_MIN</sub>     | Note 1                                             |      | 41   | 58   | ns   |
| Current Sense Amplifier                  |                          |                                                    |      |      |      |      |
| CSIN+/- Bias Current                     | I <sub>CSIN_BIAS</sub>   |                                                    | -100 | 0    | 100  | nA   |
| CSIN+/- Bias Current Mismatch            | I <sub>CSIN_BIASMM</sub> |                                                    | -50  | 0    | 50   | nA   |
| Calibrated Input Offset Voltage          | V <sub>CSIN_OFFSET</sub> | Self-calibrated offset, 0.5V ≤ V(REFIN) ≤ 2.25V    |      | ±450 |      | μV   |
| Gain                                     | G <sub>CS</sub>          | 0.5V ≤ V(REFIN) ≤ 2.25V                            | 30.0 | 32.5 | 35.0 | V/V  |
| Unity Gain Bandwidth                     | f <sub>BW</sub>          | C(IOUT) = 10pF. Measure at IOUT. Note 1            | 4.8  | 6.8  | 8.8  | MHz  |

| PARAMETER                              | SYMBOL               | CONDITIONS                             | MIN  | TYP  | MAX     | UNIT         |
|----------------------------------------|----------------------|----------------------------------------|------|------|---------|--------------|
| Slew Rate                              | $S_R$                |                                        |      | 6    |         | V/ $\mu$ s   |
| Differential Input Range               | $V_{D\_IN}$          | $0.8V \leq V(REFIN) \leq 2.25V$ ,      | -10  |      | 25      | mV           |
| Common Mode Input Range                | $V_{C\_IN}$          |                                        | 0    |      | VCC-2.5 | V            |
| Output Impedance (IOUT)                | $R_{CS\_OUT}$        |                                        |      | 62   | 200     | $\Omega$     |
| IOUT Sink Current                      | $I_{CS\_SINK}$       | Driving external 3 k $\Omega$          | 0.5  | 0.8  | 1.1     | mA           |
| <b>Diode Emulation Mode Comparator</b> |                      |                                        |      |      |         |              |
| Input Offset Voltage                   | $V_{IN\_OFFSET}$     | Note 3                                 | -12  | -3   | 3       | mV           |
| Leading Edge Blanking Time             | $t_{BLANK}$          | $V(GATEL) > 1V$ Starts Timer           | 50   | 150  | 200     | ns           |
| Negative Current Time-Out              | $t_{NC\_TOUT}$       | PWM = Tri-State,<br>$V(SW) \leq -10mV$ | 12   | 28   | 46      | $\mu$ s      |
| <b>Digital Input – BBRK#</b>           |                      |                                        |      |      |         |              |
| Input voltage high                     | $V_{BBRK\#\_IH}$     |                                        | 2.0  |      |         | V            |
| Input voltage low                      | $V_{BBRK\#\_IL}$     |                                        |      |      | 0.8     | V            |
| Internal Pull Up Resistance            | $R_{BBRK\#\_PULLUP}$ | VCC > UVLO                             | 69   | 200  | 338     | k $\Omega$   |
| Internal Pull Up Voltage               | $V_{BBRK\#\_PULLUP}$ | VCC > UVLO                             |      | 3.3  |         | V            |
| <b>Digital Output – PHSFLT#</b>        |                      |                                        |      |      |         |              |
| Output voltage high                    | $V_{PHASFLT\#\_OH}$  |                                        |      |      | VCC     | V            |
| Output voltage low                     | $V_{PHASFLT\#\_OL}$  | 4mA                                    |      | 150  | 300     | mV           |
| Input current                          | $I_{PHASFLT\#\_IN}$  | $V(PHSFLT\#) = 5.5V$                   |      | 0    | 1       | $\mu$ A      |
| <b>Phase Fault Detection</b>           |                      |                                        |      |      |         |              |
| Control MOSFET Short Threshold         | $V_{CM\_SHORT}$      | Measure from SW to PGND                |      | 3.3  |         | V            |
| Synchronous MOSFET Short Threshold     | $V_{SM\_SHORT}$      | Measure from SW to PGND                | 150  | 200  | 250     | mV           |
| Synchronous MOSFET Open Threshold      | $V_{SM\_OPEN}$       | Measure from SW to PGND                | -250 | -200 | -150    | mV           |
| Propagation Delay                      | $t_{PROP}$           | PWM High to Low Cycles                 |      | 15   |         | Cycle        |
| <b>Thermal Flag</b>                    |                      |                                        |      |      |         |              |
| Rising Threshold                       | $T_{RISE}$           | PHSFLT# Drives Low,<br>Note 1          |      | 160  |         | $^{\circ}$ C |
| Falling Threshold                      | $T_{FALL}$           | Note 1                                 |      | 135  |         | $^{\circ}$ C |
| <b>Bootstrap Diode</b>                 |                      |                                        |      |      |         |              |
| Forward Voltage                        | $V_{FWD}$            | $I(BOOST) = 30mA$ , VCC = 6.8V         | 360  | 520  | 920     | mV           |
| <b>VCC Under Voltage Lockout</b>       |                      |                                        |      |      |         |              |
| Start Threshold                        | $V_{VCC\_START}$     |                                        | 3.3  | 3.7  | 4.1     | V            |
| Stop Threshold                         | $V_{VCC\_STOP}$      |                                        | 3.0  | 3.4  | 3.8     | V            |
| Hysteresis                             | $V_{VCC\_HYS}$       |                                        | 0.2  | 0.3  | 0.4     | V            |
| <b>General</b>                         |                      |                                        |      |      |         |              |

| PARAMETER                  | SYMBOL             | CONDITIONS                           | MIN  | TYP | MAX | UNIT |
|----------------------------|--------------------|--------------------------------------|------|-----|-----|------|
| VCC Supply Current         | $I_{VCC}$          | VCC = 4.5V to 7V                     | 4    | 8   | 12  | mA   |
| VIN Supply Leakage Current | $I_{VIN}$          | VIN = 20V, 125°C, V(PWM) = Tri-State |      |     | 1   | μA   |
| BOOST Supply Current       | $I_{BOOST}$        | 4.75V < V(BOOST)-V(SW) < 8V          | 0.5  | 1.5 | 3.0 | mA   |
| REFIN Bias Current         | $I_{REFIN}$        |                                      | -1.5 | 0   | 1   | μA   |
| SW Floating Voltage        | $V_{SW\_FLOAT}$    | V(PWM) = Tri-State                   |      | 0.2 | 0.4 | V    |
| SW Pull Down Resistance    | $R_{SW\_PULLDOWN}$ | BBRK# is Low or VCC = 0V             |      | 18  |     | kΩ   |

#### Notes

1. Guaranteed by design but not tested in production
2.  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW} = 300kHz$ ,  $L=210nH$  (0.2mΩ),  $VCC=6.8V$ ,  $C_{IN}=47\mu F \times 4$ ,  $C_{OUT}=470\mu F \times 3$ , 400LFM airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.
3.  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW} = 400kHz$ ,  $L=150nH$  (0.29mΩ),  $VCC=7V$ ,  $C_{IN}=47\mu F \times 4$ ,  $C_{OUT}=470\mu F \times 3$ , no airflow, no heat sink, 25°C ambient temperature, and 8-layer PCB of 3.7" (L) x 2.6" (W). PWM controller loss and inductor loss are not included.

## TYPICAL OPERATING CHARACTERISTICS

Circuit of Figure 32,  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW} = 400kHz$ ,  $L=150nH$  ( $0.29m\Omega$ ),  $V_{CC}=7V$ ,  $T_{AMBIENT} = 25^{\circ}C$ , no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

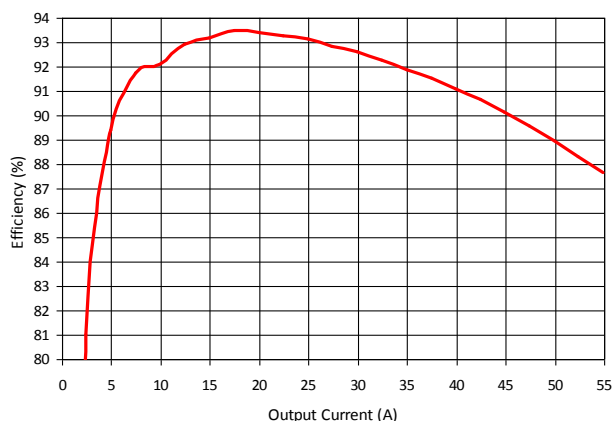


Figure 7: Typical IR3575 Efficiency

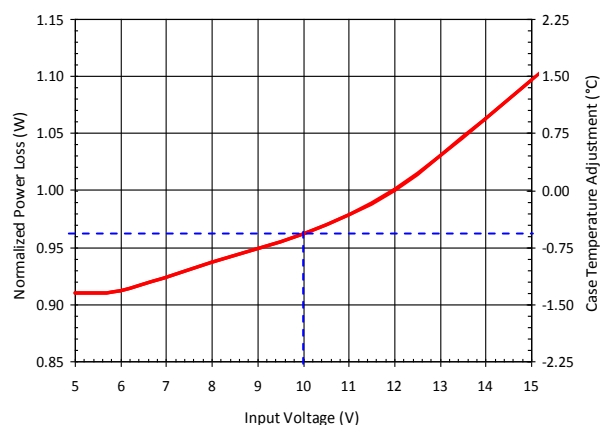


Figure 10: Normalized Power Loss vs. Input Voltage

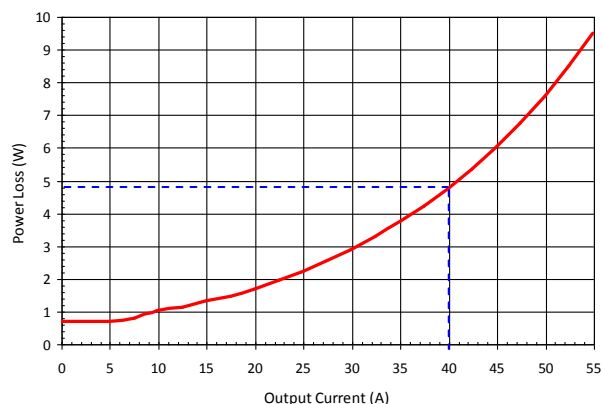


Figure 8: Typical IR3575 Power Loss

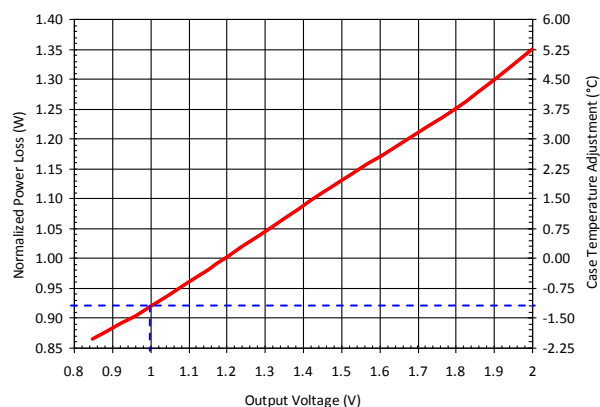


Figure 11: Normalized Power Loss vs. Output Voltage

(To be added)

Figure 9: Safe Operating Area,  $T_{CASE} \leq 125^{\circ}C$

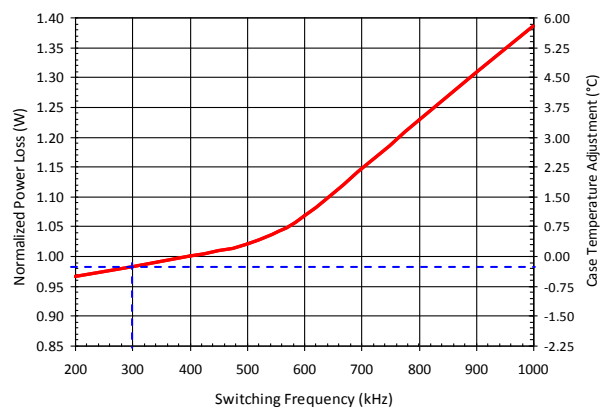


Figure 12: Normalized Power Loss vs. Switching Frequency

## TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32,  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW} = 400kHz$ ,  $L=150nH$  ( $0.29m\Omega$ ),  $V_{CC}=7V$ ,  $T_{AMBIENT} = 25^{\circ}C$ , no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

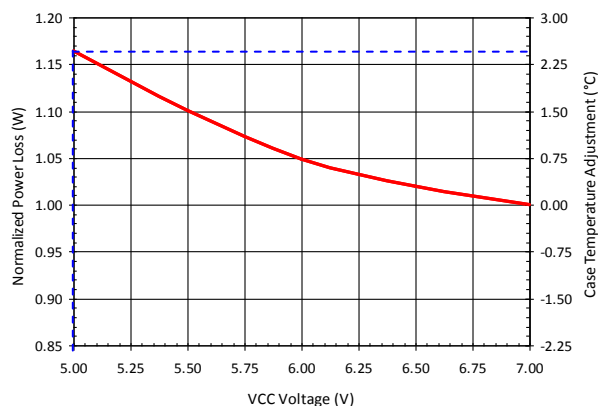


Figure 13: Normalized Power Loss vs. VCC Voltage

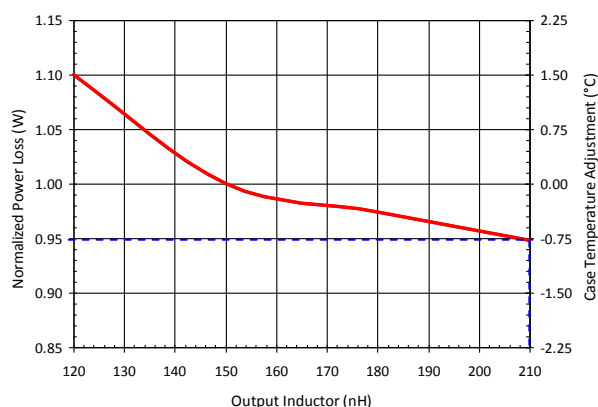


Figure 14: Power Loss vs. Output Inductor

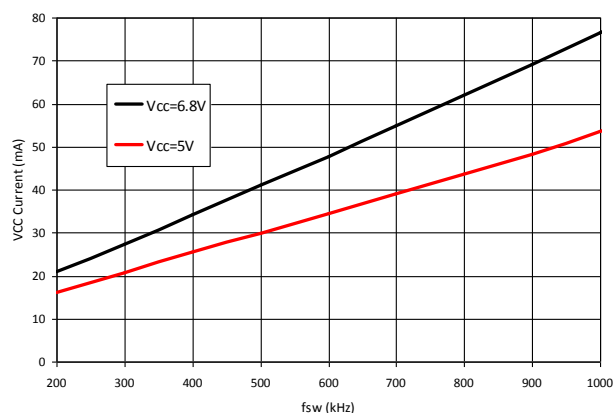


Figure 15: VCC Current vs. Switching Frequency

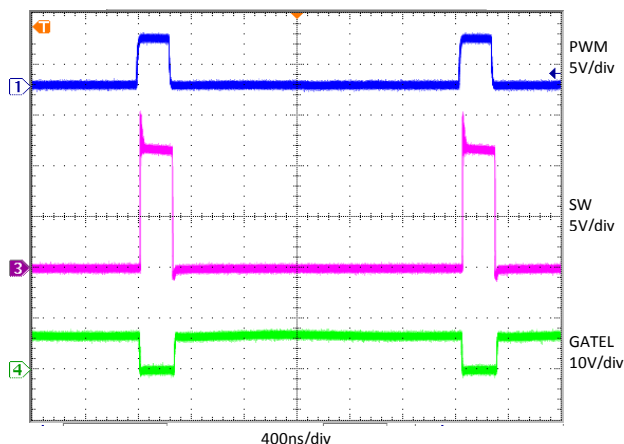


Figure 16: Switching Waveform,  $I_{OUT} = 0A$

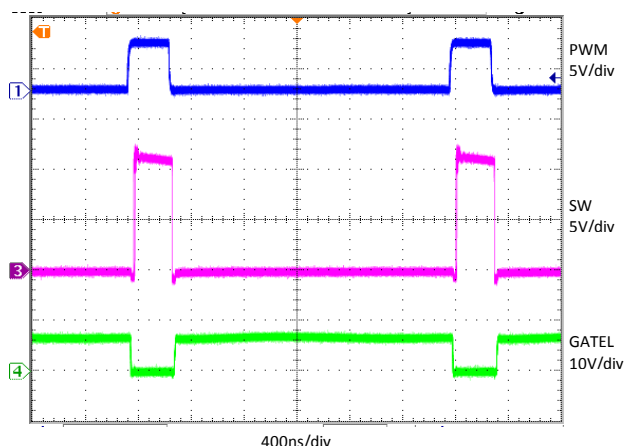


Figure 17: Switching Waveform,  $I_{OUT} = 50A$

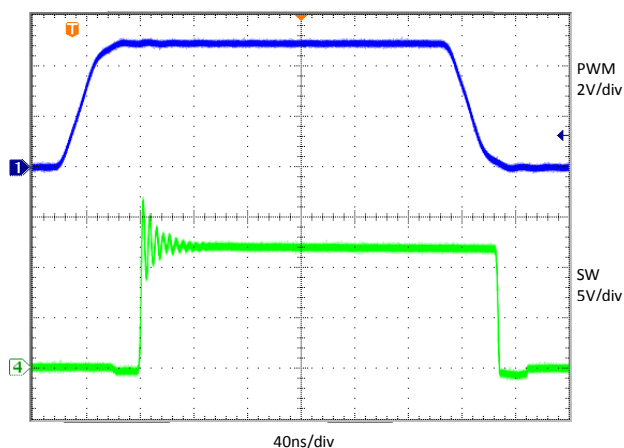


Figure 18: PWM to SW Delays,  $I_{OUT} = 10A$

## TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32,  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW} = 400kHz$ ,  $L=150nH$  (0.29mΩ),  $V_{CC}=7V$ ,  $T_{AMBIENT} = 25^{\circ}C$ , no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

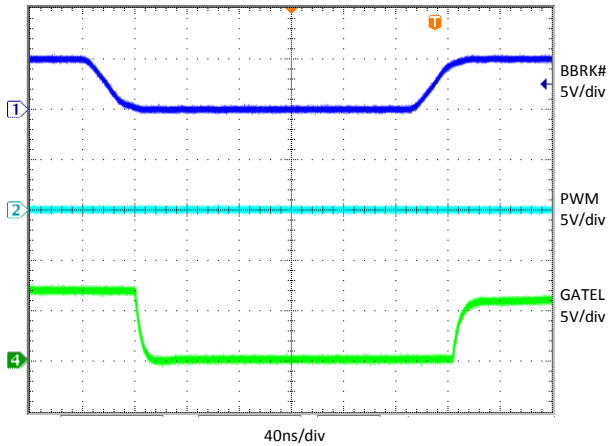


Figure 19: Body-Braking™ Delays

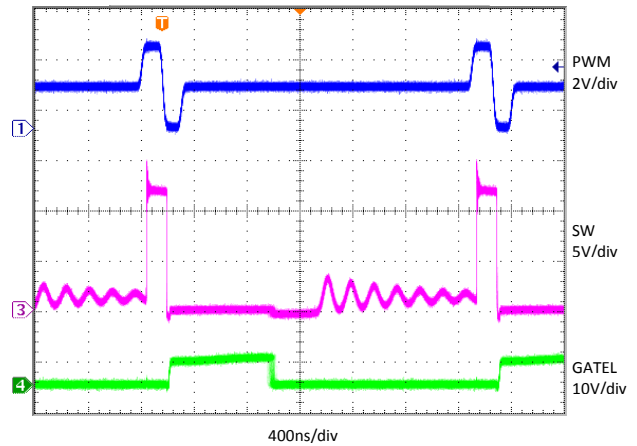


Figure 22: Diode Emulation Mode,  $I_{OUT} = 3A$

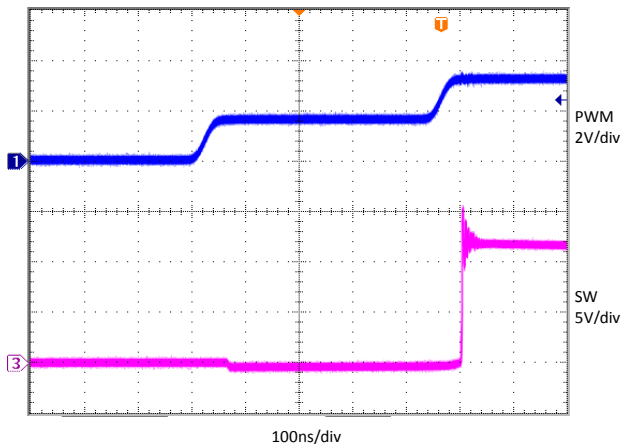


Figure 20: PWM Tri-state Delays,  $I_{OUT} = 10A$

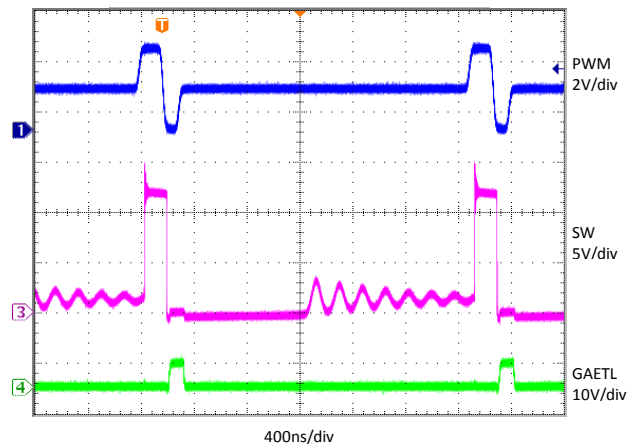


Figure 23: Body-Braking™ Mode,  $I_{OUT} = 3A$

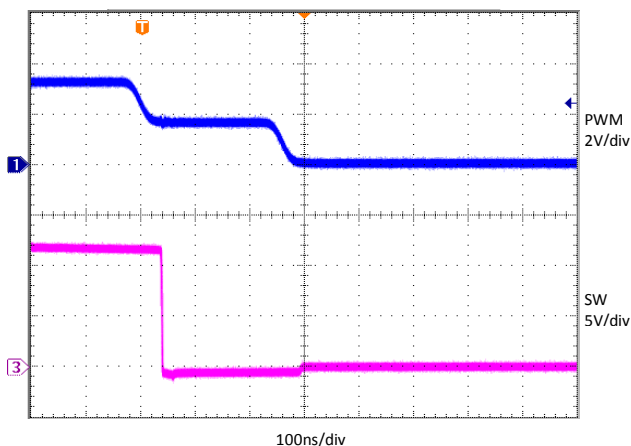


Figure 21: PWM Tri-state Delays,  $I_{OUT} = 10A$

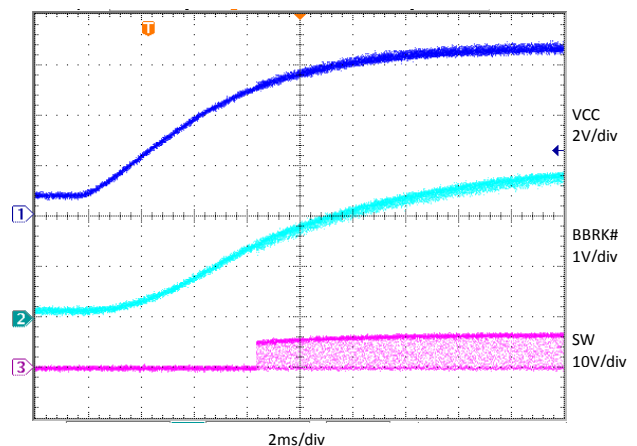


Figure 24: Diode Emulation Setup through BBRK# Capacitor

## TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Circuit of Figure 32,  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW} = 400kHz$ ,  $L=150nH$  (0.29mΩ),  $V_{CC}=7V$ ,  $T_{AMBIENT} = 25^{\circ}C$ , no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

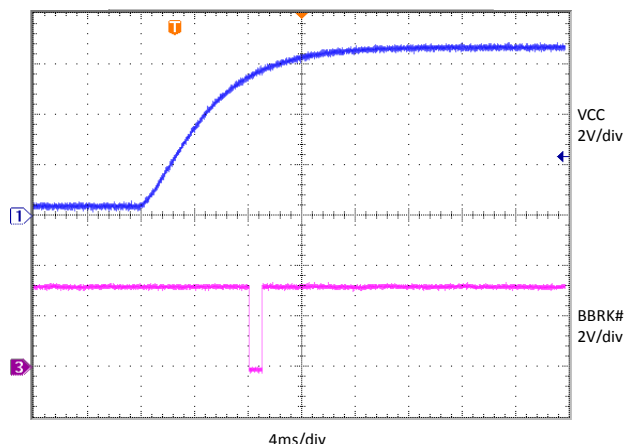


Figure 25: Diode Emulation Setup through BBRK# Input

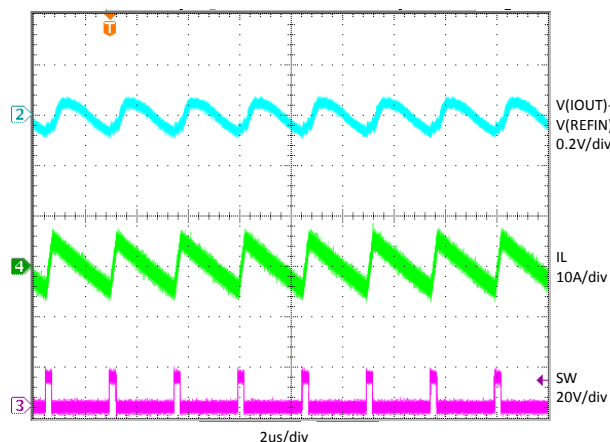


Figure 28: Current Sense Amplifier Output,  $I_{OUT} = 0A$

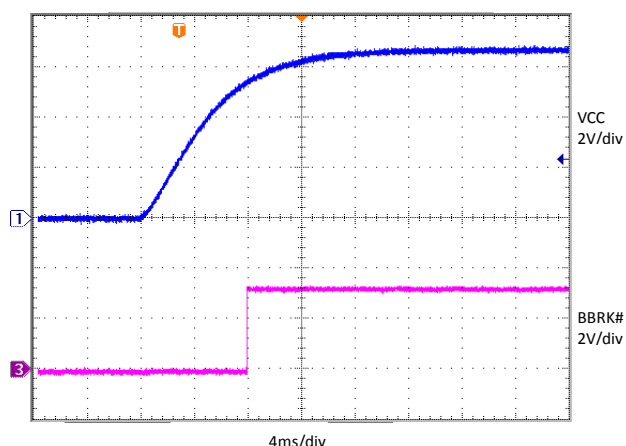


Figure 26: Diode Emulation Setup through BBRK# Input

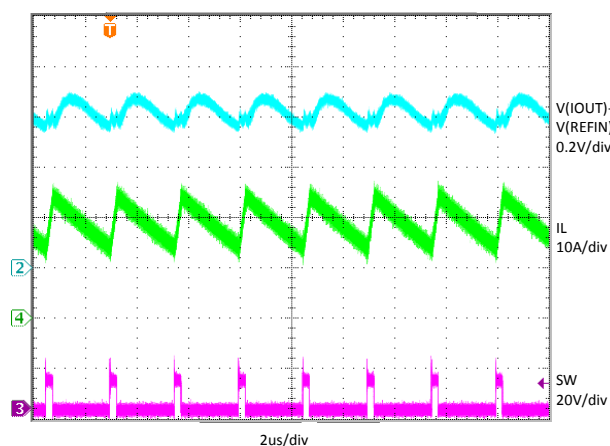


Figure 29: Current Sense Amplifier Output,  $I_{OUT} = 20A$

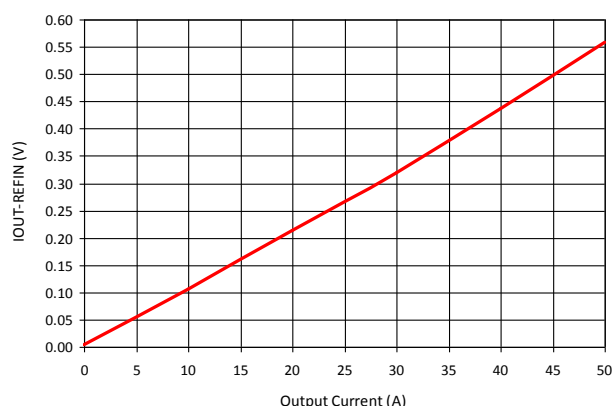


Figure 27: Current Sense Amplifier Output vs. Current

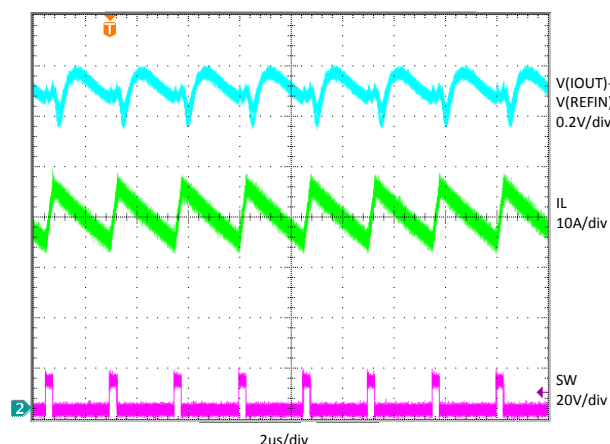


Figure 30: Current Sense Amplifier Output,  $I_{OUT} = 40A$

## THEORY OF OPERATION

### DESCRIPTION

The IR3575 exposed-top PowIRstage® is a synchronous buck driver with co-packed MOSFETs with integrated Schottky diode, which provides system designers with ease of use and flexibility required in cutting edge CPU, GPU and DDR memory power delivery designs and other high-current low-profile applications.

The IR3575 is designed to work with a PWM controller. It incorporates a continuously self-calibrated current sense amplifier, optimized for use with inductor DCR sensing. The current sense amplifier provides signal gain and noise immunity, supplying multiphase systems with a superior design toolbox for programmed impedance designs.

The IR3575 provides a phase fault signal capable of detecting open or shorted MOSFETs, or an over-temperature condition in the vicinity of the power stage.

The IR3575 accepts an active low Body-Braking® input which disables both MOSFETs to enhance transient performance or provide a high impedance output.

The IR3575 provides diode emulation feature which avoids negative current in the synchronous MOSFET and improves light load efficiency.

The IR3575 PWM input is compatible with 3.3V logic signal and 7V tolerant. It accepts 3-level PWM input signals with tri-state.

### PWM TRI-STATE INPUT

The IR3575 PWM accepts 3-level input signals. When PWM input is high, the synchronous MOSFET is turned off and the control MOSFET is turned on. When PWM input is low, control MOSFET is turned off and synchronous MOSFET is turned on. Figures 16-18 show the PWM input and the corresponding SW and GATEL output of the IR3575. If PWM pin is floated, the built-in resistors pull the PWM pin into a tri-state region centered around 1.65V.

When PWM input is in tri-state, two operation modes can be selected by controlling BBRK# input. If the BBRK# input is always high, the default operation mode is Body-Braking®, in which both MOSFETs will be turned off when the PWM input is in tri-state. If the BBRK# input has been pulled low for at least 20ns after the VCC passes its UVLO threshold during power up, the diode emulation mode is

set. PWM input in tri-state will activate a synchronous diode emulation feature allowing designers to maximize system efficiency at light loads without compromising transient performance.

### BODY-BRAKING® MODE

International Rectifier's Body-Braking® is a operation mode in which two MOSFETs are turned off. When the synchronous MOSFET is off, the higher voltage across the Schottky diode in parallel helps discharging the inductor current faster, which reduces the output voltage overshoot. The Body-Braking® can be used either to enhance transient response of the converter after load release or to provide a high impedance output.

There are two ways to place the IR3575 in Body-Braking® mode, either controlling the BBRK# pin directly or through a PWM tri-state signal. Both control signals are usually from the PWM controller.

Pulling BBRK# low forces the IR3575 into Body-Braking® mode rapidly, which is usually used to enhance converter transient response after load release, as shown in Figure 19. Releasing BBRK# forces the IR3575 out of Body-Braking® mode quickly.

The BBRK# low turns off both MOSFETs and therefore can also be used to disable/enable a converter.

If the BBRK# input is always high, the Body-Braking® is activated when the PWM input enters the tri-state region, as shown in Figures 20 and 21. Comparing to pulling down the BBRK# pin directly, the Body-Braking® response to PWM tri-state signal is slower due to the hold-off time created by the PWM pin parasitic capacitor with the pull-up and pull-down resistors of PWM pin. For better performance, no more than 100pF parasitic capacitive load should be present on the PWM line of IR3575.

### SYNCHRONOUS DIODE EMULATION MODE

An additional feature of the IR3575 is the synchronous diode emulation mode. This function enables increased efficiency by preventing negative inductor current from flowing in the synchronous MOSFET.

As shown in Figure 22, when the PWM input enters the tri-state region the control MOSFET is turned off first, and the synchronous MOSFET is initially turned on and then is turned off when the output current reaches zero. If the sensed output current does not reach zero within a set amount of time the gate driver will assume that the output

is de-biased and turn off the synchronous MOSFET, allowing the switch node to float.

This is in contrast to the Body-Braking® mode shown in Figure 23, where GATEL follows PWM input. The Schottky diode in parallel with the synchronous MOSFET conducts for a longer period of time and therefore lowers the light load efficiency.

The zero current detection circuit in the IR3575 is independent of the current sense amplifier and therefore still functions even if the current sense amplifier is not used. As shown in Figure 6, an offset is added to the diode emulation comparator so that a slightly positive output current in the inductor and synchronous MOSFET is treated as zero current to accommodate propagation delays, preventing any negative current flowing in the synchronous MOSFET. This causes the Schottky diode in parallel with the synchronous MOSFET to conduct before the inductor current actually reaches zero, and the conduction time increases with inductance of the output inductor.

To set the IR3575 in diode emulation mode, the BBRK# pin must be toggled low at least once after the VCC passes its UVLO threshold during power up. One simple way is to use the internal BBRK# pull-up resistor (200kΩ typical) with an external capacitor from BBRK# pin to LGND, as shown in Figure 4. To ensure the diode emulation mode is properly set, the BBRK# voltage should be lower than 0.8V when the VCC voltage passes its UVLO threshold (3.3V minimum and 3.7V typical), as shown in Figure 24. A digital signal from the PWM controller can also be used to set the diode emulation mode. The BBRK# signal can either be pulled low for at least 20ns after the VCC passes its UVLO threshold, as shown in Figure 25, or be pulled low before VCC power up and then released after the VCC passes its UVLO threshold, as shown in Figure 26.

Once the diode emulation mode is set, it cannot be reset until the VCC power is recycled.

## PHASE FAULT AND THERMAL FLAG OUTPUT

The phase fault circuit looks at the switch node with respect to ground to determine whether there is a defective MOSFET in the phase. The output of the phase fault signal is high during normal operation and is pulled low when there is a fault. Each driver monitors the MOSFET it drives. If the switch node is less than a certain voltage above ground when the PWM signal goes low or if the switch node is a certain voltage above ground when the PWM signal rises, this gives a fault signal. If there are a

number of consecutive faults the phase fault signal is asserted.

Thermal flag circuit monitors the temperature of the IR3575. If the temperature goes above a threshold (160°C typical) the PHSFLT# pin is pulled low after a maximum delay of 100μs.

The PHSFLT# pin can be pulled low by either the phase fault circuit or the thermal flag circuit. The phase fault signal could be used to turn off the AC/DC converter or blow a fuse to disconnect the DC/DC converter input from the supply.

If PHSFLT# is not used it can be floated or connected to LGND.

## LOSSLESS AVERAGE INDUCTOR CURRENT SENSING

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 31.

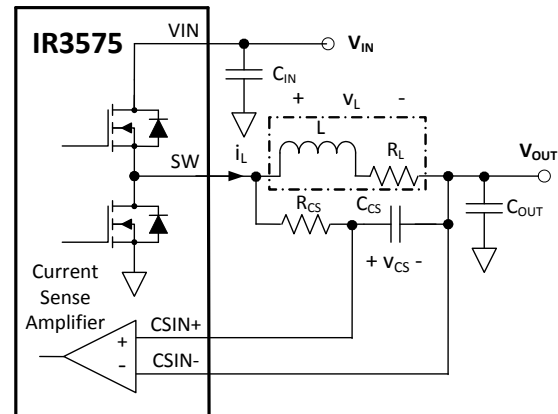


Figure 31: Inductor current sensing

The equation of the current sensing network is as follows.

$$v_{CS}(s) = v_L(s) \frac{1}{1 + sR_{CS}C_{CS}} = i_L(s)R_L \frac{1 + s\frac{L}{R_L}}{1 + sR_{CS}C_{CS}}$$

$$= i_L(s)R_L \text{ when } L/R_L = R_{CS}C_{CS}$$

Usually the resistor  $R_{CS}$  and capacitor  $C_{CS}$  are chosen so that the time constant of  $R_{CS}$  and  $C_{CS}$  equals the inductor time



If any of the application condition, i.e. input voltage, output voltage, switching frequency, VCC MOSFET driver voltage or inductance, is different from those of Figure 8, a set of normalized power loss curves should be used. Obtain the normalizing factors from Figure 10 to Figure 14 for the new application conditions; multiply these factors by the power loss obtained from Figure 8 for the required load current.

As an example, the power loss calculation procedures under different conditions,  $V_{IN}=10V$ ,  $V_{OUT}=1V$ ,  $f_{SW} = 300kHz$ ,  $VCC=5V$ ,  $L=210nH$ ,  $VCC=5V$ ,  $I_{OUT}=40A$ ,  $T_{AMBIENT} = 25^{\circ}C$ , no heat sink, and no air flow, are as follows.

- 1) Determine the power loss at 40A under the default test conditions of  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW} = 400kHz$ ,  $L=150nH$ ,  $VCC=7V$ ,  $T_{AMBIENT} = 25^{\circ}C$ , no heat sink, and no air flow. It is 4.8W from Figure 8.
- 2) Determine the input voltage normalizing factor with  $V_{IN}=10V$ , which is 0.96 based on the dashed lines in Figure 10.
- 3) Determine the output voltage normalizing factor with  $V_{OUT}=1V$ , which is 0.92 based on the dashed lines in Figure 11.
- 4) Determine the switching frequency normalizing factor with  $f_{SW} = 300kHz$ , which is 0.98 based on the dashed lines in Figure 12.
- 5) Determine the VCC MOSFET drive voltage normalizing factor with  $VCC=5V$ , which is 1.16 based on the dashed lines in Figure 13.
- 6) Determine the inductance normalizing factor with  $L=210nH$ , which is 0.95 based on the dashed lines in Figure 14.
- 7) Multiply the power loss under the default conditions by the five normalizing factors to obtain the power loss under the new conditions, which is  $4.8W \times 0.96 \times 0.92 \times 0.98 \times 1.16 \times 0.95 = 4.58W$ .

## SAFE OPERATING AREA

Figure 9 shows the IR3575 safe operating area with the case temperature controlled at or below  $125^{\circ}C$ . The test conditions are  $V_{IN}=12V$ ,  $V_{OUT}=1.2V$ ,  $f_{SW}=400kHz$ ,  $L=150nH$  (0.29mΩ),  $VCC=7V$ ,  $T_{AMBIENT} = 0^{\circ}C$  to  $90^{\circ}C$ , no heat sink, and Airflow = 0LFM / 100LFM / 200LFM / 400LFM.

If any of the application condition, i.e. input voltage, output voltage, switching frequency, VCC MOSFET driver voltage, or inductance is different from those of Figure 9, a set of IR3575 case temperature adjustment curves should be used. Obtain the temperature deltas from Figure 10 to Figure 14 for the new application conditions; sum these deltas and then subtract from the IR3575 case temperature obtained from Figure 9 for the required load current.

- 8) From Figure 9, determine the highest ambient temperature at the required load current under the default conditions, which is  $77^{\circ}C$  at 40A with 0LFM airflow and the IR3575 case temperature of  $125^{\circ}C$ .
- 9) Determine the case temperature with  $V_{IN}=10V$ , which is  $-0.6^{\circ}$  based on the dashed lines in Figure 10.
- 10) Determine the case temperature with  $V_{OUT}=1V$ , which is  $-1.2^{\circ}$  based on the dashed lines in Figure 11.
- 11) Determine the case temperature with  $f_{SW} = 300kHz$ , which is  $-0.3^{\circ}$  based on the dashed lines in Figure 12.
- 12) Determine the case temperature with  $VCC = 5V$ , which is  $+2.4^{\circ}$  based on the dashed lines in Figure 13.
- 13) Determine the case temperature with  $L=210nH$ , which is  $-0.8^{\circ}$  based on the dashed lines in Figure 14.
- 14) Sum the case temperature adjustment from 9) to 13),  $-0.6^{\circ} -1.2^{\circ} -0.3^{\circ} +2.4^{\circ} -0.8^{\circ} = -0.5^{\circ}$ . Deduct the delta from the highest ambient temperature in step 8),  $77^{\circ}C - (-0.5^{\circ}C) = 77.5^{\circ}C$ .

## INDUCTOR CURRENT SENSING CAPACITOR $C_{CS}$ AND RESISTOR $R_{CS}$

If the IR3575 is used with inductor DCR sensing, care must be taken in the printed circuit board layout to make a Kelvin connection across the inductor DCR. The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor  $R_{CS}$  and capacitor  $C_{CS}$  in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor  $C_{CS}$  represents the inductor current.

Measure the inductance  $L$  and the inductor DC resistance  $R_L$ . Pre-select the capacitor  $C_{CS}$  and calculate  $R_{CS}$  as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}}$$

### INPUT CAPACITORS $C_{VIN}$

At least two 10uF 1206 ceramic capacitors and one 0.1uF 0402 ceramic capacitor are recommended for decoupling the VIN to PGND connection. The 0.1uF 0402 capacitor should be on the same side of the PCB as the IR3575 and next to the VIN and PGND pins. Adding additional capacitance and use of capacitors with lower ESR and mounted with low inductance routing will improve efficiency and reduce overall system noise, especially in single-phase designs or during high current operation.

### BOOTSTRAP CAPACITOR $C_{BOOST}$

A minimum of 0.22uF 0402 capacitor is required for the bootstrap circuit. A high temperature 0.22uF or greater value 0402 capacitor is recommended. It should be mounted on the same side of the PCB as the IR3575 and as close as possible to the BOOST pin. A low inductance routing of the SW pin connection to the other terminal of the bootstrap capacitor is strongly recommended.

### VCC DECOUPLING CAPACITOR $C_{VCC}$

A 0.1uF to 1uF ceramic decoupling capacitor is required at the VCC pin. It should be mounted on the same side of the PCB as the IR3575 and as close as possible to the VCC and PGND (pin 4). Low inductance routing between the VCC capacitor and the IR3575 pins is strongly recommended.

### BODY-BRAKING® FEATURE

The BBRK# pin should be pulled up to VCC if the feature is not used by the PWM controller. Use of a small value resistor or a direct connection to VCC is recommended.

### MOUNTING OF HEAT SINKS

Care should be taken in the mounting of heat sinks so as not to short-circuit nearby components. The VCC and Bootstrap capacitors are typically mounted on the same side of the PCB as the IR3575. The mounting height of these capacitors must be considered when selecting their package sizes.

### HIGH OUTPUT VOLTAGE DESIGN CONSIDERATIONS

The IR3575 is capable of creating output voltages above the 3.3V recommended maximum output voltage as there are no restrictions inside the IR3575 on the duty cycle applied to the PWM pin. However if the current sense feature is required, the common mode range of the

current sense amplifier inputs must be considered. A violation of the current sense input common mode range may cause unexpected IR3575 behavior. Also the output current rating of the device will be reduced as the duty cycle increases. In very high duty cycle applications sufficient time must be provided for replenishment of the Bootstrap capacitor for the control MOSFET drive.

### LAYOUT EXAMPLE

Contact International Rectifier for a layout example suitable for your specific application.

## METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be  $\geq 0.2\text{mm}$  to prevent shorting.
- Lead land length should be equal to maximum part lead length  $+0.15 - 0.3\text{ mm}$  outboard extension and  $0$  to  $+0.05\text{mm}$  inboard extension. The outboard extension ensures a large and visible toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width.
- Only  $0.30\text{mm}$  diameter via shall be placed in the area of the power pad lands and connected to power planes to minimize the noise effect on the IC and to improve thermal performance.

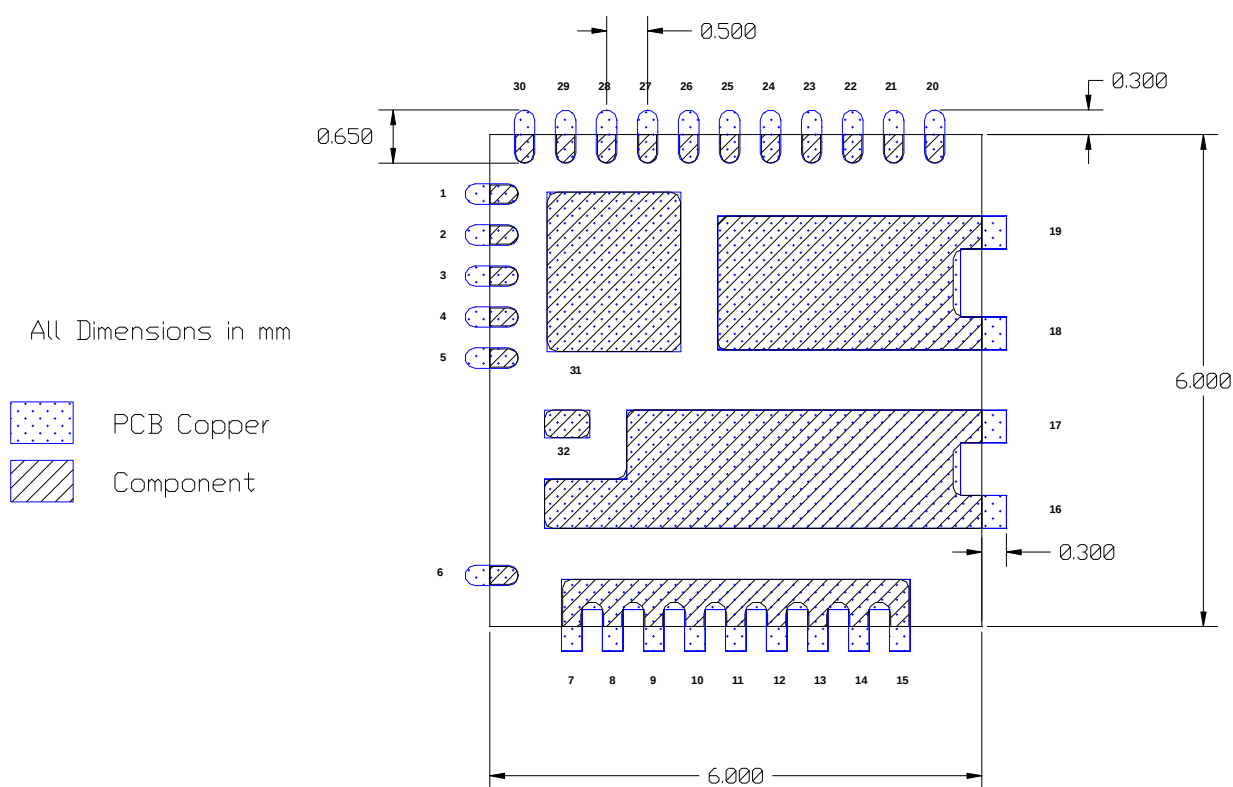
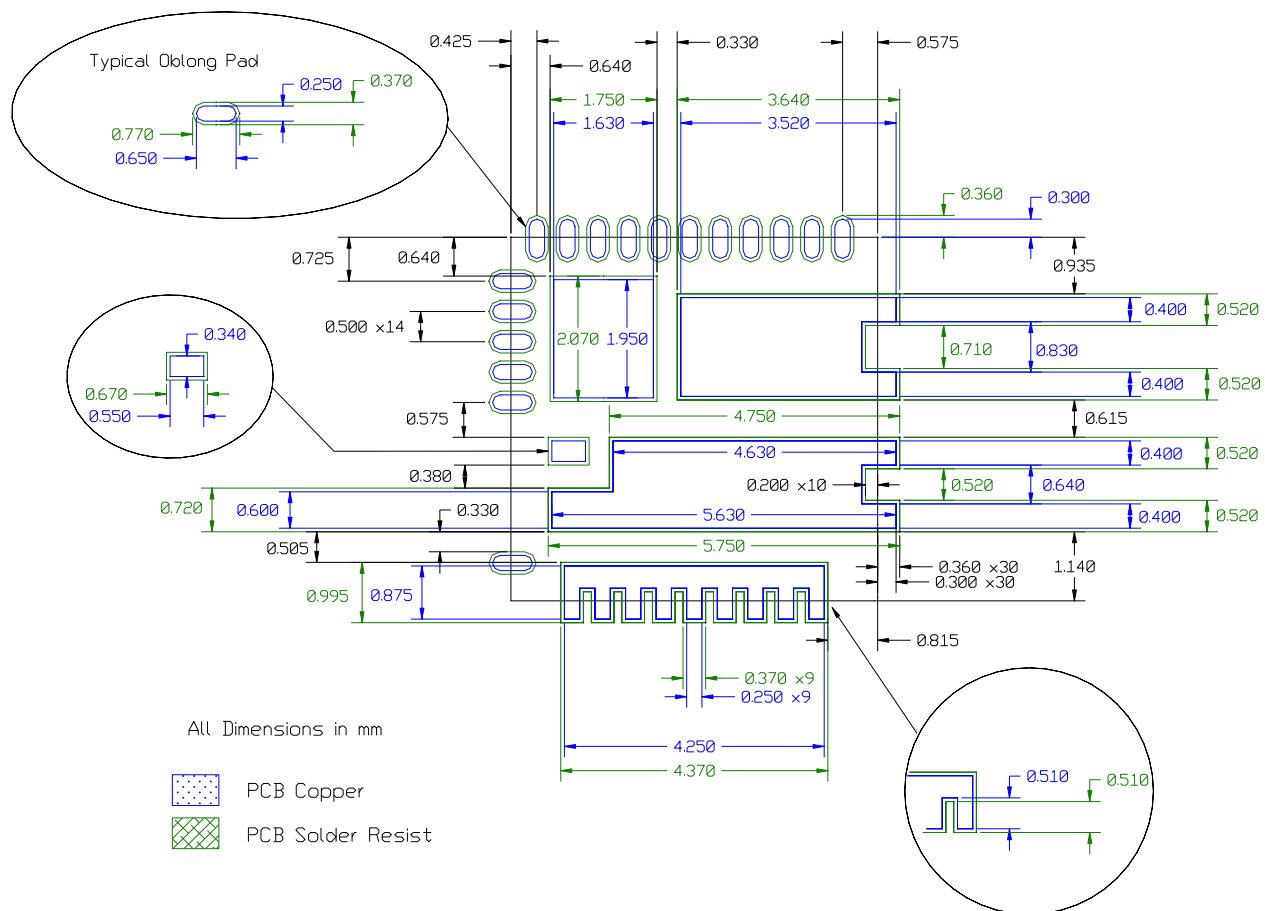


Figure 33: Metal and component placement

\* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

## SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the low power signal lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm typical.

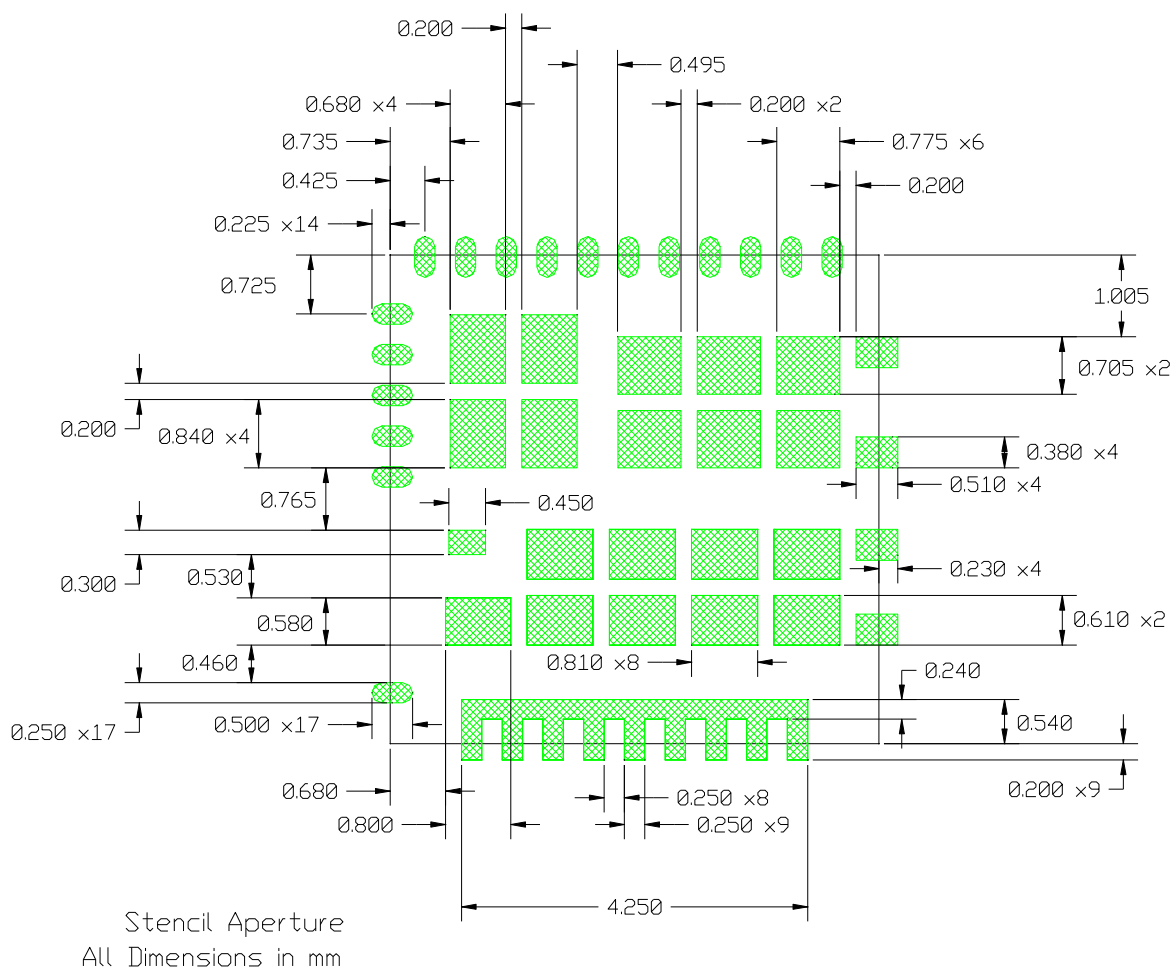


**Figure 34: Solder resist**

\* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

## STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 65% to 75% of the area of the lead lands depending on stencil thickness. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The low power signal stencil lead land apertures should therefore be shortened in length to keep area ratio of 65% to 75% while centered on lead land.
- The power pads VIN, PGND, TGND and SW, land pad apertures should be approximately 65% to 75% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open. Solder paste on large pads is broken down into small sections with a minimum gap of 0.2mm between allowing for out-gassing during solder reflow.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



### Figure 35: Stencil design

\* Contact International Rectifier to receive an electronic PCB Library file in Cadence Allegro or CAD DXF/DWG format.

## MARKING INFORMATION

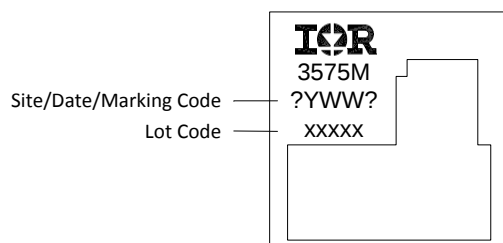
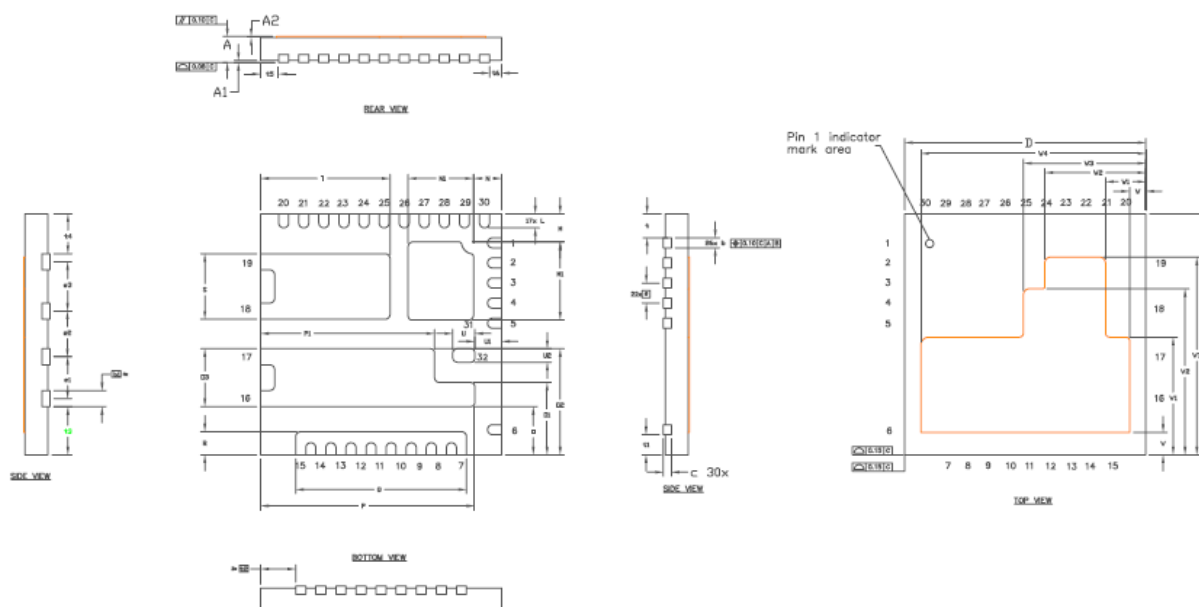


Figure 36: PQFN 6mm x 6mm

## PACKAGE INFORMATION



| DIM | MILLIMETERS |       | INCHES      |       |
|-----|-------------|-------|-------------|-------|
|     | MIN         | MAX   | MIN         | MAX   |
| A   | 0.55        | 0.75  | .0217       | .0295 |
| A1  | 0.000       | 0.050 | .0000       | .0020 |
| A2  | 0.000       | 0.050 | .0000       | .0020 |
| b   | 0.20        | 0.30  | .0079       | .0118 |
| b1  | 0.350       | 0.450 | .0138       | .0177 |
| c   | 0.203 REF.  |       | .0080 REF.  |       |
| D   | 6.000 BASIC |       | .2362 BASIC |       |
| E   | 6.000 BASIC |       | .2362 BASIC |       |
| e   | 0.500 BASIC |       | .0197 BASIC |       |
| e1  | 1.041 BASIC |       | .0410 BASIC |       |
| e2  | 1.134 BASIC |       | .0446 BASIC |       |
| e3  | 1.230 BASIC |       | .0484 BASIC |       |
| t   | 0.600 BASIC |       | .0236 BASIC |       |
| t1  | 0.500 BASIC |       | .0197 BASIC |       |
| t2  | 0.875 BASIC |       | .0344 BASIC |       |
| t3  | 1.200 BASIC |       | .0472 BASIC |       |
| t4  | 0.996 BASIC |       | .0392 BASIC |       |
| t5  | 0.450 BASIC |       | .0177 BASIC |       |
| t6  | 0.300 BASIC |       | .0118 BASIC |       |

| DIM | MILLIMETERS |       | INCHES |       |
|-----|-------------|-------|--------|-------|
|     | MIN         | MAX   | MIN    | MAX   |
| L   | 0.300       | 0.400 | .0118  | .0157 |
| M   | 0.650       | 0.750 | .0256  | .0295 |
| M1  | 1.896       | 1.996 | .0747  | .0786 |
| N   | 0.650       | 0.750 | .0256  | .0295 |
| N1  | 1.577       | 1.677 | .0621  | .0660 |
| O   | 1.150       | 1.250 | .0453  | .0492 |
| O1  | 1.750       | 1.850 | .0689  | .0728 |
| O2  | 2.591       | 2.691 | .1020  | .1060 |
| O3  | 1.391       | 1.491 | .0548  | .0587 |
| P   | 5.281       | 5.381 | .2079  | .2119 |
| P1  | 4.281       | 4.381 | .1685  | .1725 |
| Q   | 4.200       | 4.300 | .1654  | .1693 |
| R   | 0.525       | 0.625 | .0207  | .0246 |
| S   | 1.580       | 1.680 | .0622  | .0661 |
| T   | 3.173       | 3.273 | .1249  | .1289 |
| U   | 0.500       | 0.600 | .0197  | .0236 |
| U1  | 0.619       | 0.719 | .0244  | .0283 |
| U2  | 0.287       | 0.387 | .0130  | .0152 |
| V   | 0.506       | 0.606 | .0199  | .0239 |
| V1  | 2.879       | 2.979 | .1133  | .1173 |
| V2  | 4.085       | 4.185 | .1608  | .1648 |
| V3  | 4.872       | 4.972 | .1918  | .1957 |
| W   | 0.350       | 0.450 | .0138  | .0177 |
| W1  | 0.951       | 1.051 | .0374  | .0414 |
| W2  | 2.463       | 2.563 | .0970  | .1009 |
| W3  | 2.995       | 3.095 | .1179  | .1219 |
| W4  | 5.550       | 5.650 | .2185  | .2224 |

Figure 37: PQFN 6mm x 6mm

Data and specifications subject to change without notice.  
This product will be designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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