Low-Power Dual Channel Digital Isolator

Check for Samples: ISO7420FCC

FEATURES

- **Signaling Rate: 50 Mbps (5V Supplies)**
- **Output is Low in Default Mode**
- **Integrated Noise Filter on the Input pins**
- **Low Power Consumption: Typical I_{CC} per Channel**
  - **1.8 mA at 1 Mbps, 3.9 mA at 25 Mbps (5V Supplies)**
  - **1.4 mA at 1 Mbps, 2.6 mA at 25 Mbps (3.3V Supplies)**
- **Low Propagation Delay: 20 ns Typical (5V Supplies)**
- **Channel-to-Channel Output Skew: 2ns Maximum**
- **3.3 V / 5 V Level Translation**
- **Wide T_A Range Specified: –40°C to 125°C**
- **60 KV/µs Transient Immunity, Typical (5V Supplies)**
- **Low Emissions**
- **Isolation Barrier Life: > 25 Years**
- **Operates from 2.7V to 5.5V Supply Levels**
- **Narrow Body SOIC-8 Package**

APPLICATIONS

- **Opto-Coupler Replacement in:**
  - **Industrial FieldBus**
    - **ProfiBus**
    - **ModBus**
    - **DeviceNet™ Data Buses**
  - **Servo Control Interface**
  - **Motor Control**
  - **Power Supplies**
  - **Battery Packs**

SAFETY AND REGULATORY APPROVALS

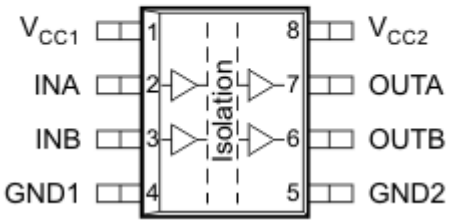
- **3 KV_{RMS} / 4242 V_{PK} Isolation per DIN EN 60747-5-2 (VDE 0884 Part 2)**
- **2.5 KV_{RMS} Isolation for 1 minute per UL 1577**
- **CSA Component Acceptance Notice #5A**
- **IEC 60950-1 and IEC 61010-1 End Equipment Standards**
- **All Agencies Approvals Pending**

DESCRIPTION

ISO7420FCC provides galvanic isolation up to 2500 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. This device has two isolated channels. Each channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies,this device prevents noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix F indicates low-output option in fail-safe conditions (see Table 1). This device has integrated noise filter for harsh environments where short noise pulses may be present at the device input pins.

These devices have TTL input thresholds and operate from 2.7V to 5.5V supplies. All inputs are 5V tolerant when supplied from a 2.7V or 3.3V supply.

ISO7420
D Package
(Top View)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	ISO7420FCC		
INA	2	I	Input, channel A
INB	3	I	Input, channel B
GND1	4	–	Ground connection for V_{CC1}
GND2	5	–	Ground connection for V_{CC2}
OUTA	7	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	–	Power supply, V_{CC1}
V_{CC2}	8	–	Power supply, V_{CC2}

Table 1. FUNCTION TABLE

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT INA, INB	OUTPUT OUTA, OUTB
PU	PU	H	H
		L	L
		Open	L (1)
PD	PU	X	L (1)
X	PD	X	Undetermined

(1) In fail-safe condition, output defaults to low level

AVAILABLE OPTIONS

PRODUCT	DATA RATE	DEFAULT OUTPUT	INTEGRATED NOISE FILTER	RATED T_A	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7420FCC	50 Mbps	Low	Yes	–40°C to 125°C	Same	7420FC	ISO7420FCCD (rail)
							ISO7420FCCDR (reel)

ABSOLUTE MAXIMUM RATINGS (1)

					VALUE
V_{CC1} , V_{CC2}	Supply voltage (2)				–0.5 V to 6 V
V_I	Voltage at INA, INB				–0.5 V to 6 V
V_O	Voltage at OUTA, OUTB				–0.5 V to V_{CC} + 0.5 V
I_O	Output current				±15 mA
ESD	Electrostatic discharge	Human-body model	JEDEC Standard 22, Test Method A114-C.01	All pins	±4 kV
		Field-induced charged-device model	JEDEC Standard 22, Test Method C101		±1.5 kV
$T_{J(Max)}$	Maximum junction temperature				150°C
T_{stg}	Storage temperature				-65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.7		5.5	V
I_{OH}	High-level output current (Vcc ≥ 3.0V)		–4			mA
	High-level output current (Vcc < 3.0V)		-2			mA
I_{OL}	Low-level output current				4	mA
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
t_{ui}	Input pulse duration	≥4.5V-Operation	20			ns
		<4.5V-Operation	25			
1 / t_{ui}	Signaling rate	≥4.5V-Operation	0		50	Mbps
		<4.5V-Operation	0		40	
T_J (1)	Junction temperature		–40		136	°C
T_A	Ambient temperature		-40	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Package Thermal Characteristics* table.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CC2} – 0.5	4.8		V
		I_{OH} = –20 µA; see Figure 1.		V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				450		mV
I_{IH}	High-level input current	INx = V_{CC}				10	µA
I_{IL}	Low-level input current	INx = 0 V		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	60		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.5	1.1	mA
I_{CC2}					3	4.6	
I_{CC1}		10 Mbps	C_L = 15pF		1	1.5	
I_{CC2}					4	6	
I_{CC1}		25 Mbps			1.7	2.5	
I_{CC2}					6	8.5	
I_{CC1}		50 Mbps			2.7	4	
I_{CC2}					8.5	12	

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} = 5V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.	10	20	37	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			2.5	5	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time				2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				12	ns
t_r	Output signal rise time	See Figure 1.		2.5		ns
t_f	Output signal fall time			2.5		ns
t_{GS}	Pulse width of glitches suppressed by the input filter			12		ns
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 2.		8		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CC2} – 0.5	3		V
		I_{OH} = –20 µA; see Figure 1.		V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				425		mV
I_{IH}	High-level input current	INx = V_{CC}				10	µA
I_{IL}	Low-level input curre	INx = 0 V		-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.3	0.8	mA
I_{CC2}					2.4	3.3	
I_{CC1}		10 Mbps	C_L = 15pF		0.6	1.2	
I_{CC2}					3.1	4.5	
I_{CC1}		25 Mbps			1	2	
I_{CC2}					4.2	6.1	
I_{CC1}		40 Mbps			1.3	2.3	
I_{CC2}					5.3	7.5	

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} = 3.3 V ± 10%, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.	10	22	40	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				3	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time				2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				19	ns
t_r	Output signal rise time	See Figure 1.		3		ns
t_f	Output signal fall time			3		ns
t_{GS}	Pulse width of glithes suppressed by the input filter			12.5		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		8		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} = 2.7 V, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 1.		V_{CC2} – 0.3	2.5		V
		I_{OH} = –20 µA; see Figure 1.		V_{CC2} – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				350		mV
I_{IH}	High-level input current	INx = V_{CC}				10	µA
I_{IL}	Low-level input current	INx = 0 V		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	35		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15pF		0.15	0.4	mA
I_{CC2}					2.1	3.1	
I_{CC1}		10 Mbps	C_L = 15pF		0.4	0.7	
I_{CC2}					2.7	4	
I_{CC1}		25 Mbps			0.7	1.2	
I_{CC2}					3.6	5	
I_{CC1}		40 Mbps			1	1.7	
I_{CC2}					4.4	6.3	

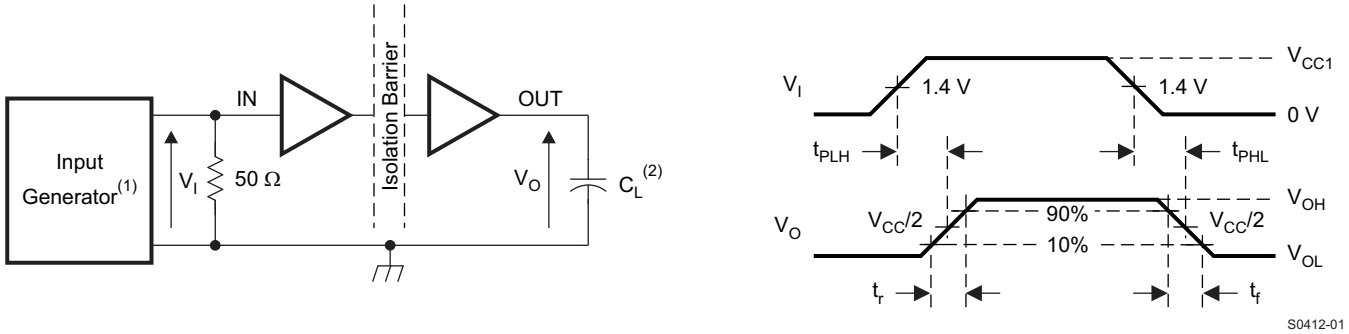
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} = 2.7 V, T_A = -40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.	15	26	45	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				3	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time				2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				22	ns
t_r	Output signal rise time	See Figure 1.		3		ns
t_f	Output signal fall time			3		ns
t_{GS}	Pulse width of glitches suppressed by the input filter			13.5		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		8		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

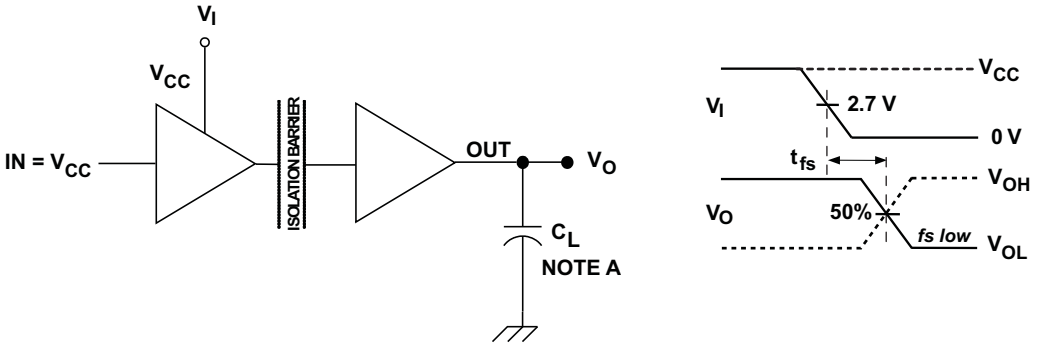
PARAMETER MEASUREMENT INFORMATION



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

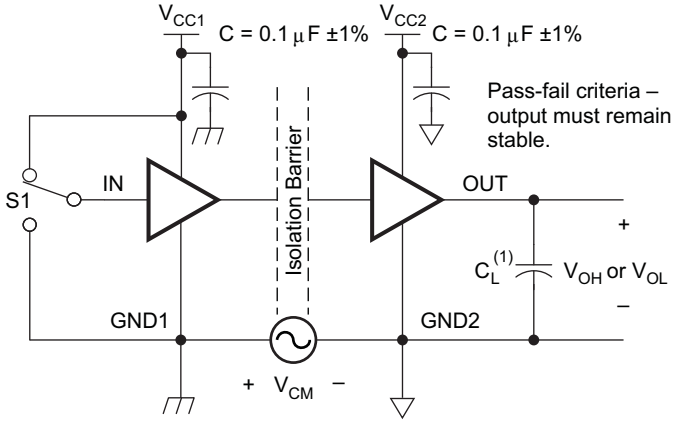
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

IEC Insulation and Safety-Related Specifications for D-8 Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A < 100°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		1		pF
C_I	Input capacitance(2)	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

INSULATION CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		566	V_{PEAK}
V_{PR}	Input-to-output test voltage per DIN EN 60747-5-2	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial Discharge < 5 pC	906	V_{PEAK}
		Method b1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	1062	
		After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	680	
V_{IOTM}	Transient overvoltage per DIN EN 60747-5-2	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	4242	V_{PEAK}
V_{ISO}	Isolation voltage per UL 1577	$V_{TEST} = V_{ISO}$, t = 60 sec (qualification)	2500	V_{RMS}
		V_{TEST} = 1.2 x V_{ISO}, t = 1 sec (100% production)	3000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 2. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III
	Rated mains voltage ≤ 400 V_{RMS}	I–II

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2)	Approved under CSA Component Acceptance Notice #5A	Recognized under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} Maximum Working Voltage, 566 V_{PK}	Basic and Reinforced Insulation per CSA 60950-1 and IEC 60950-1 Reinforced Insulation per CSA 61010-1 and IEC 61010-1	Single / Basic Isolation Voltage, 2500 V_{RMS} (1)
File number: 40016131 (Approval pending)	File number: 220991 (Approval pending)	File number: E181974 (Approval pending)

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 115.1°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			197	mA
		θ_{JA} = 115.1°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			302	
		θ_{JA} = 115.1°C/W, V_I = 2.7 V, T_J = 150°C, T_A = 25°C			402	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

THERMAL METRIC(1)			ISO7420 D PACKAGE (8) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance		115.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance		60.1	
θ_{JB}	Junction-to-board thermal resistance		56.4	
ψ_{JT}	Junction-to-top characterization parameter		17.2	
ψ_{JB}	Junction-to-board characterization parameter		55.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance		N/A	
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 50-Mbps 50% duty-cycle square wave	120	mW

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

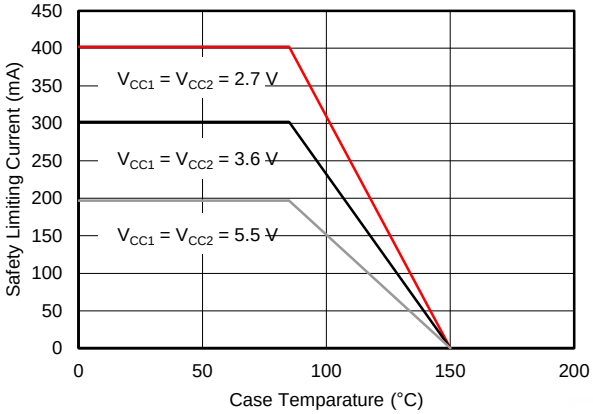


Figure 4. θ_{JC} Thermal Derating Curve per DIN EN 60747-5-2

APPLICATION INFORMATION

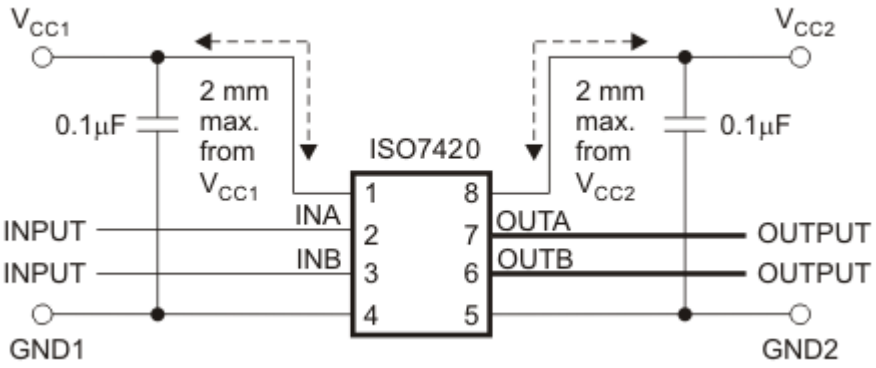


Figure 5. Typical ISO7420FCC Application Circuit

Note: For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide.*

SUPPLY CURRENT EQUATIONS

Maximum Supply Current Equations

(Calculated over recommended operating temperature range and Silicon process variation)

At $V_{CC1} = V_{CC2} = 5V \pm 10\%$
$I_{CC1}(max) = 1.1 + 5.80E\text{-}02 \times f$
$I_{CC2}(max) = 4.6 + 6.55E\text{-}02 \times f + 5.5E\text{-}03 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 3.3V \pm 10\%$
$I_{CC1}(max) = 0.8 + 3.40E\text{-}02 \times f$
$I_{CC2}(max) = 3.3 + 4.60E\text{-}02 \times f + 3.6E\text{-}03 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 2.7V$
$I_{CC1}(max) = 0.4 + 3.20E\text{-}02 \times f$
$I_{CC2}(max) = 3.1 + 3.75E\text{-}02 \times f + 2.7E\text{-}03 \times f \times C_L$

f is data rate of each channel measured in Mbps; C_L is the capacitive load of each channel measured in pF; $I_{CC1}(max)$ and $I_{CC2}(max)$ are measured in mA.

Typical Supply Current Equations

(Calculated for $T_A = 25°C$ and nominal Silicon process material)

At $V_{CC1} = V_{CC2} = 5V$
$I_{CC1}(typ) = 0.5 + 4.40E\text{-}02 \times f$
$I_{CC2}(typ) = 3 + 3.50E\text{-}02 \times f + 5.0E\text{-}03 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 3.3V$
$I_{CC1}(typ) = 0.3 + 2.60E\text{-}02 \times f$
$I_{CC2}(typ) = 2.4 + 2.25E\text{-}02 \times f + 3.3E\text{-}03 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 2.7V$
$I_{CC1}(typ) = 0.15 + 2.10E\text{-}02 \times f$
$I_{CC2}(typ) = 2.1 + 1.75E\text{-}02 \times f + 2.7E\text{-}03 \times f \times C_L$

f is Data Rate of each channel measured in Mbps; C_L is the Capacitive Load of each channel measured in pF; $I_{CC1}(typ)$ and $I_{CC2}(typ)$ are measured in mA.

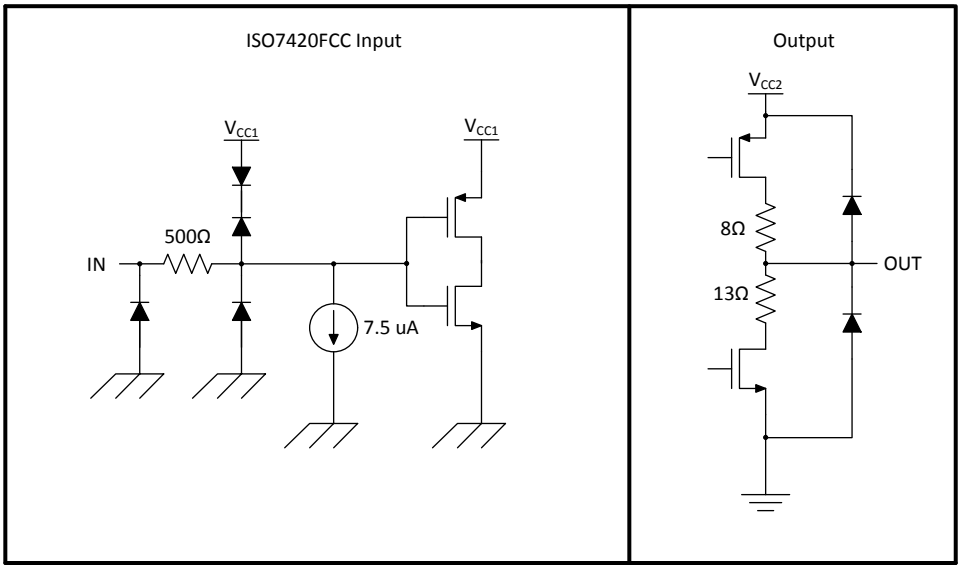


Figure 6. Device I/O Schematics

TYPICAL CHARACTERISTICS

SUPPLY CURRENT PER CHANNEL vs DATA RATE

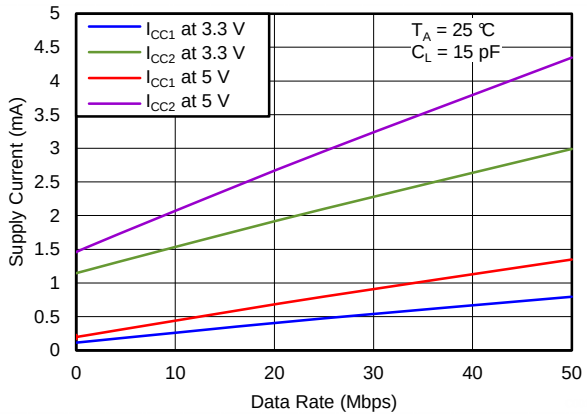


Figure 7.

SUPPLY CURRENT FOR BOTH CHANNELS vs DATA RATE

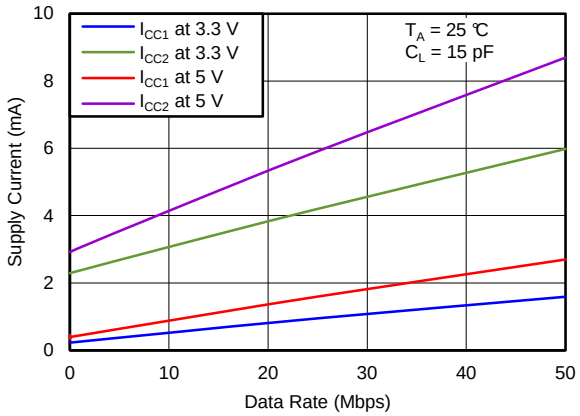


Figure 8.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

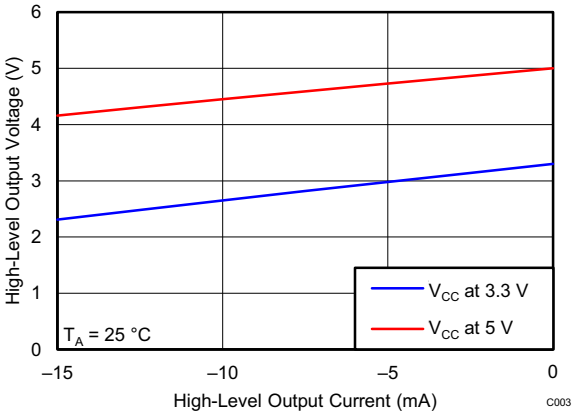


Figure 9.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

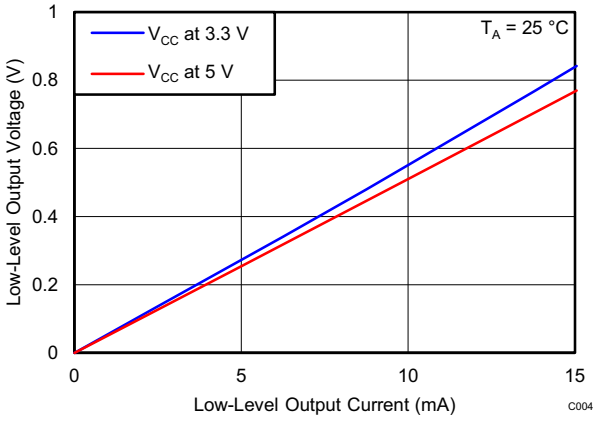


Figure 10.

VCC1 and VCC2 UNDER-VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE

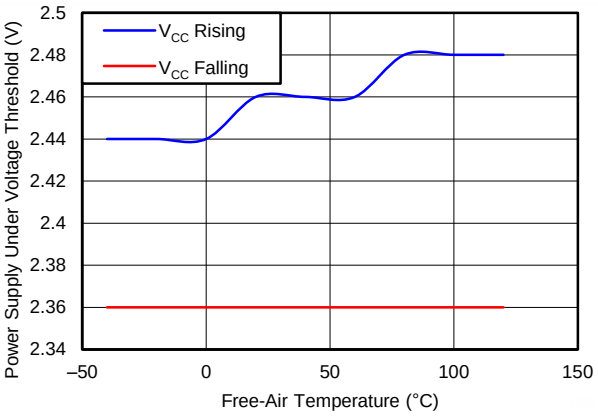


Figure 11.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

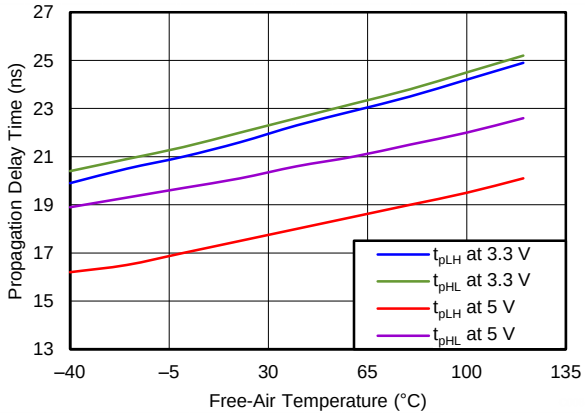


Figure 12.

TYPICAL CHARACTERISTICS (continued)

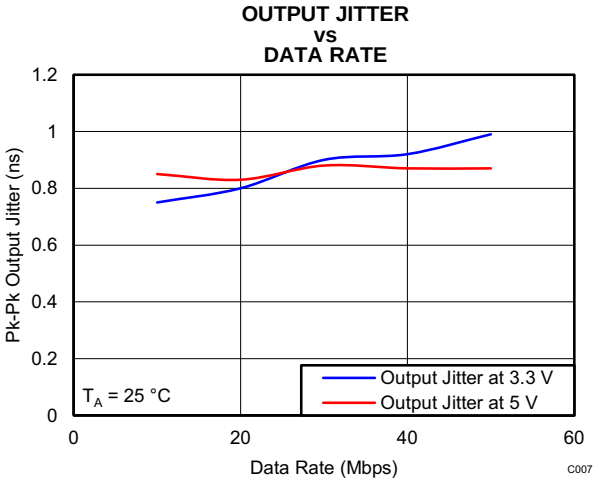


Figure 13.

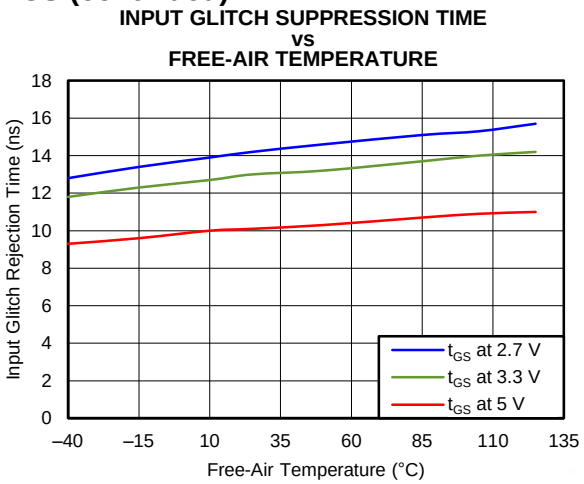


Figure 14.

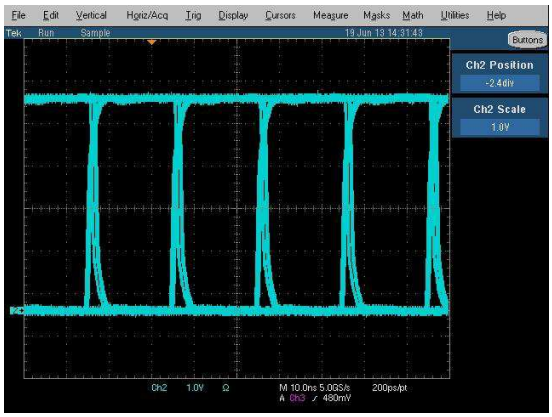


Figure 15. Eye Diagram at 50 Mbps, 5V at 25°C

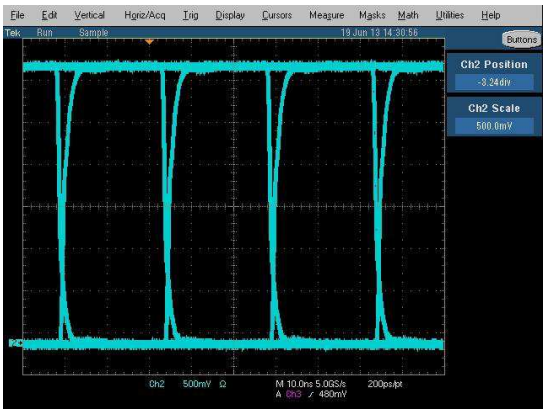


Figure 16. Eye Diagram at 40 Mbps, 3.3V at 25°C

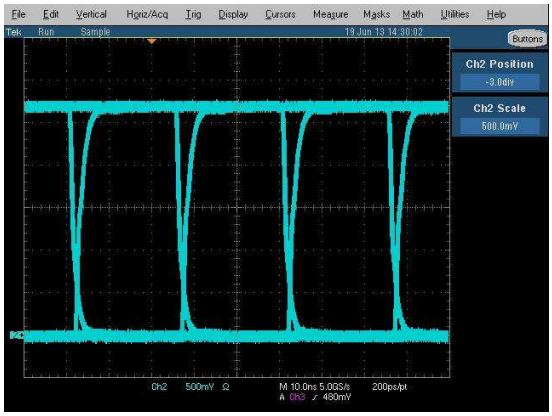


Figure 17. Eye Diagram at 40 Mbps, 2.7V at 25°C

REVISION HISTORY

Changes from Original (June 2013) to Revision A **Page**

- Changed High-level output voltage MIN Value From: V_{CCx} To: V_{CC2} 4
- Changed High-level output voltage MIN Value From: V_{CCx} To: V_{CC2} and removed Note 1 5
- Changed High-level output voltage MIN Value From: V_{CCx} To: V_{CC2} and removed Note 1 6
- Changed Figure 9 X axis values 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7420FCCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7420FC	Samples
ISO7420FCCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7420FC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

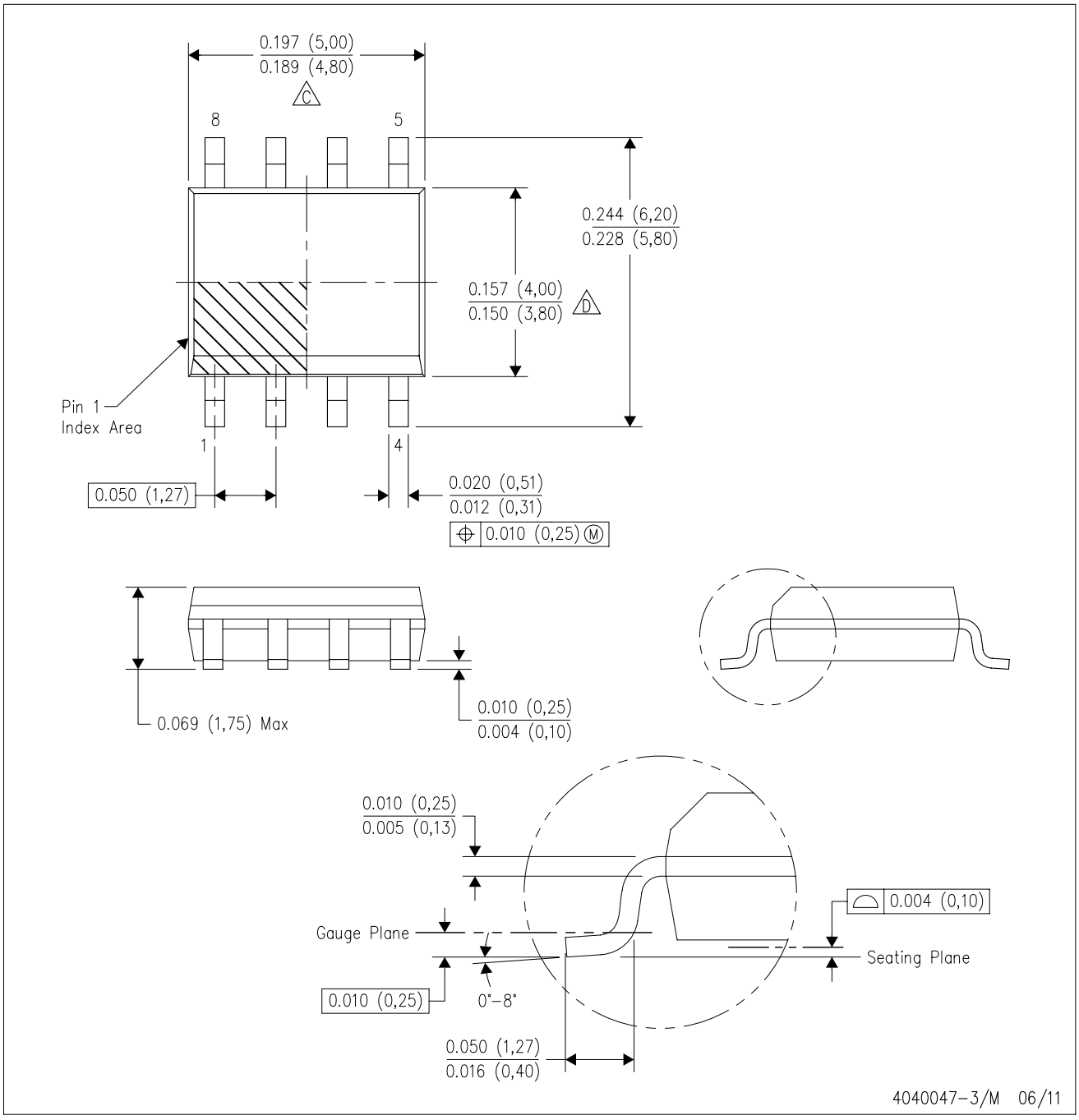
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

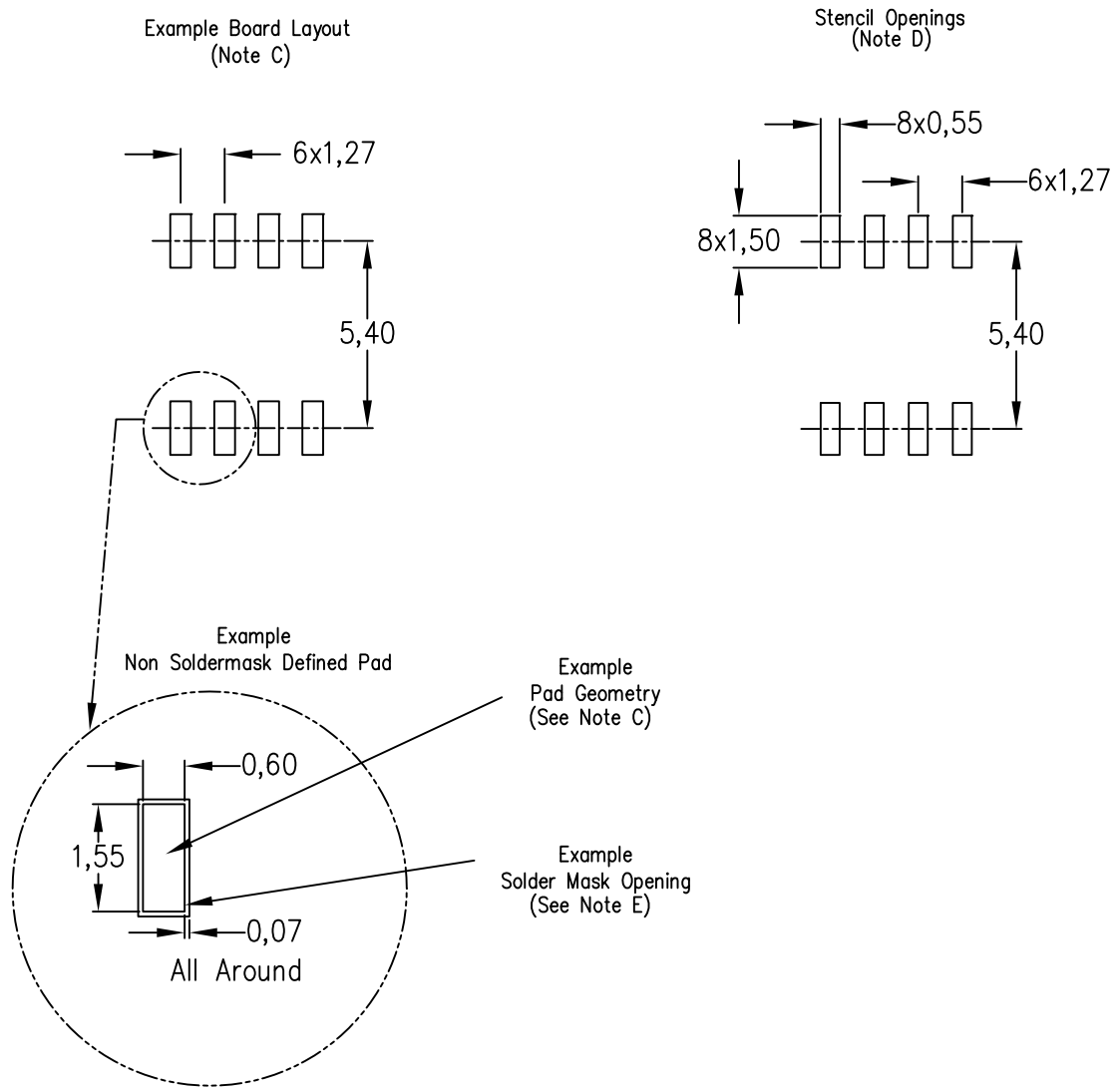
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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