QuickSTART

ispClock5400D Evaluation Board

This document provides a brief introduction and instructions to evaluate and demonstrate key features of the ispClock™ 5400D device on the ispClock5400D Evaluation Board. Please refer to the complete documentation at www.latticesemi.com/5400D_board.

1 Check Kit Contents

The ispClock5400D Evaluation Board package should contain the following items:

- ispClock5400D Evaluation Board pre-loaded with base demo of ispClock5400D features
- ispDOWNLOAD™ Cable with USB PC connection
- International Power Supply Kit
- QuickSTART Guide

Storage and Handling Tips:

Static electricity can shorten the life of electronic components. Please observe these tips to prevent damage that could occur from electro-static discharge:

- Use anti-static precautions such as operating on an anti-static mat and wearing an anti-static wrist-band.
- Store the evaluation board in the pink anti-static packaging foam provided.
- Touch a metal USB housing to equalize voltage potential between you and the board.

2 Connect to the ispClock5400D Evaluation Board

In this step, connect the evaluation board, ispDOWNLOAD Cable and power supply.

1. Plug the ispDOWNLOAD Cable into the USB port on the PC.
2. Plug the labeled flywires of the ispDOWNLOAD Cable to the board's I^2C interface header (J15). SDA=TDO, SDIN=TDI, SCL=TCK, VCC=VCC, GND=GND.
3. Plug the power adaptor to a wall socket and insert the connector into the coaxial Power Jack (J13).
4. Browse to www.latticesemi.com/5400D_board and locate the ispClock5406D Base Applications and download the demo source.
5. Download the ZIP file to your system and unzip it to a location on your PC.
6. Browse to www.latticesemi.com/pac-designer and download the PAC-Designer® Primary Module. Follow the web page instructions to install PAC-Designer.
7. Start PAC-Designer.
8. Choose **File > Open…**
9. Browse to the Base_Demo_CLK5406.PAC file unzipped in Step 5 and choose **Open**.
10. From PAC-Designer, choose **Tools > Design Utilities…**
11. Select **ispClock_5406_I2C_Utility.exe** and click **OK**.

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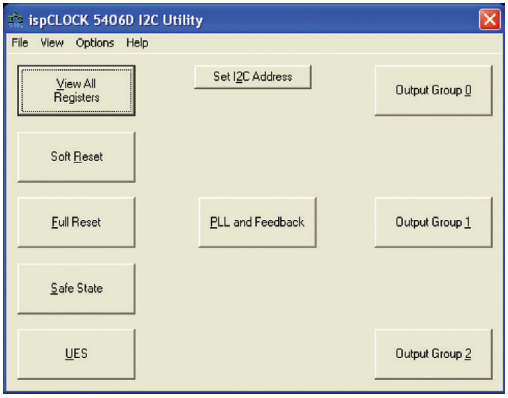
Connect to the ispClock5400D Evaluation Board (Cont.)



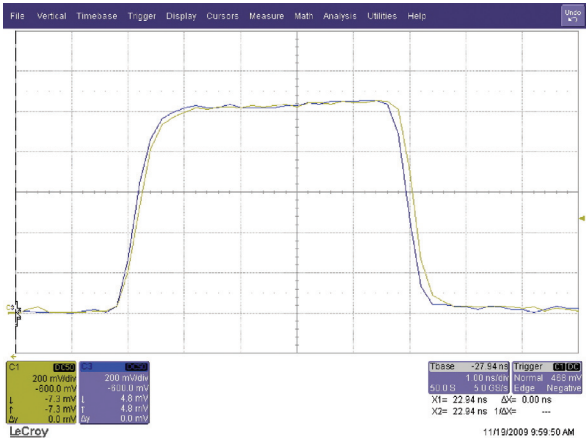
12. Choose **Options > I2C Interface…**
13. Click the **Change…** button until the **Uses PC USB Port** title appears.
14. Uncheck the **Bypass Hardware Checking (Demo Mode)** option.
    Note: If you do not have a high-speed oscilloscope, enable the Demo Mode option.
15. Click the **Settings…** button.
16. From the **Select USB port name…** section, choose **Search for download cable on all USB ports** and click **Connect Now**.
17. Click **OK**.
18. From the Cable and I/O Port Setup dialog, click **OK**.
19. From the ispClock5406D I^2C Utility click the **I2C Address = …** button.
20. Select **7Fh** from the I^2C Address list and click **OK**.

3 Run the ispClock5400D Base Demo

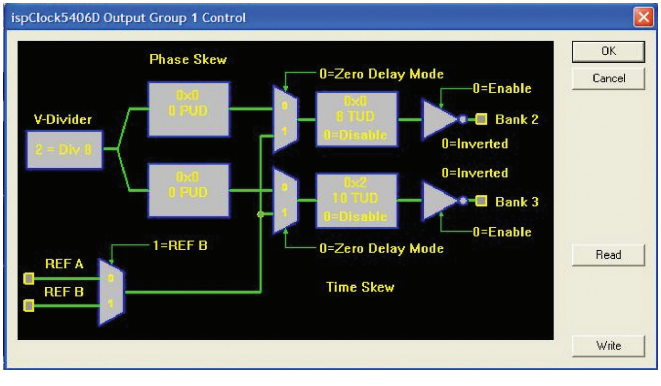
These instructions demonstrate the in-system programmability of the ispClock5406D and highlights its flexibility as a clock distribution IC. The ispClock5400D's I^2C bus interface feature allows you to override many parameters of the device programming and make in-system changes to the phase, time, reference and frequency settings of the device. The feature allows dynamic time/phase skew for testing and margining of the output clocks on every bank output pair.

1. Attach high-speed scope leads to the SMA sockets at BANK0 P, N and BANK2 P, N.
2. Set the scope input channel settings to 50 Ohm termination. The ispClock5406D Base Demo produces an LVDS differential output. The waveforms shown use 3' long RG-316 cables with the SMA connectors. If your test equipment has high-impedance probes or a differential probe, make sure that the LVDS BANK outputs have 100 Ohm termination from BANK_P to BANK_N.
3. Adjust the scope to display BANK0_P and BANK2_P signals only. Overlap the signals to compare the relative skew. Note that a small inherent skew of the outputs plus any set-up delay in cables is about 50 to 80ps.

Run the ispClock5400D Base Demo (Cont.)

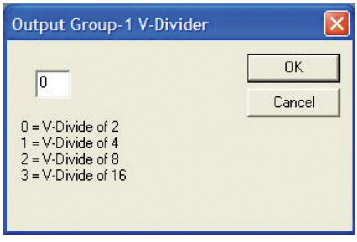


4. From the ispClock5406D I²C Utility click the **Output Group 1** button.



5. Double-click the **TUD** output block for Bank 2 of the schematic.
6. Specify **3** and click **OK**.
7. From the ispClock5406D Output Group 1 Control dialog click the **Write** button. The I²C utility writes the control registers to the ispClock5406D I²C interface and updates the time skew by three steps (18ps x 3 = 54ps).
8. Note the updated scope display. The BANK0_P and BANK2_P outputs are de-skewed.
9. From the ispClock5406D Output Group 1 Control dialog, double-click the **V-Divider** block. The Output Group-1 V-Divider dialog appears.

Run the ispClock5400D Base Demo (Cont.)



10. Enter **0** (0 = V-Divide of 2) into the text entry box and click **OK**.
11. From the ispClock5406D Output Group 1 Control dialog click the **Write** button. The I²C utility writes the control registers to the ispClock5406D I²C interface and updates the V-Divider routing connection between the PLL VCO output (400 MHz) and Output Group 1 to use the $f_{VCO} \div 2$ path. Note the updated scope display. The BANK2_P output frequency has increased to 200 MHz. For more information on I²C control registers, see the ispClock5400D Family Data Sheet.
12. From the ispClock5406D Output Group 1 Control dialog, click the **OK** button.

4 Done!

Congratulations! You have successfully demonstrated the ispClock5400D Evaluation Board. Please refer to the ispClock5400D Evaluation Board User's Guide available on the Lattice website at www.latticesemi.com/5400D_board for the following:

- Running advanced demos
- Details on additional evaluation board features and operation
- Modifying and generating the demo bitstreams from the ispLEVER® project sources
- Schematics
- Gerber PCB layout artwork

Technical Support

If you experience problems running the kit demos or if any kit contents are missing, please email us at techsupport@latticesemi.com or call 1-800-528-8423 (USA) or +1 503-268-8001 (other locations).

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