ispClock

Integrated Universal Fan-out Buffer Offers Programmable Skew and Output Impedance Control

ispClock™– Standard Clock Net Solution

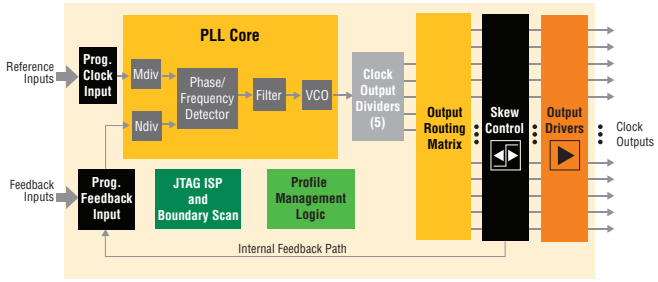
Imagine designing your clock nets without using an assortment of zero delay buffers, fan-out buffers, termination resistors, delay lines and serpentine clock trace layouts! The answer is Lattice's revolutionary ispClock5600A family for complex clock nets and ispClock5300S family for simple clock nets. Lattice's ispClock devices can be programmed in-system to generate multiple clock frequencies, compensate each output for differences in clock trace lengths, precisely match trace impedances and drive clock nets with different signaling requirements – all while meeting stringent skew and jitter standards!

The ispClock architecture is built around a high performance PLL with programmable input, feedback, and output circuitry providing the flexibility to generate up to five different clock frequencies and route them to any of the output pins. The reference input, feedback input and all outputs can be programmed independently to interface with different I/O standards. Each output's skew can be individually and precisely controlled to compensate for differences in board trace lengths or timing requirements of the receiving devices.

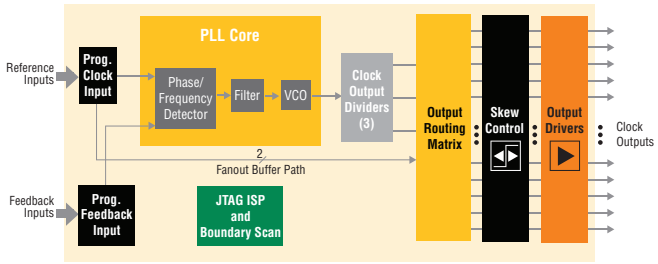
In ispClock5600A devices there are four configuration profiles stored on-chip for dynamically altering output frequencies for power savings, test modes and other purposes.

The ispClock5300S supports implementation of zero delay and non-zero delay fanout buffers in a single device.

ispClock5600A Block Diagram



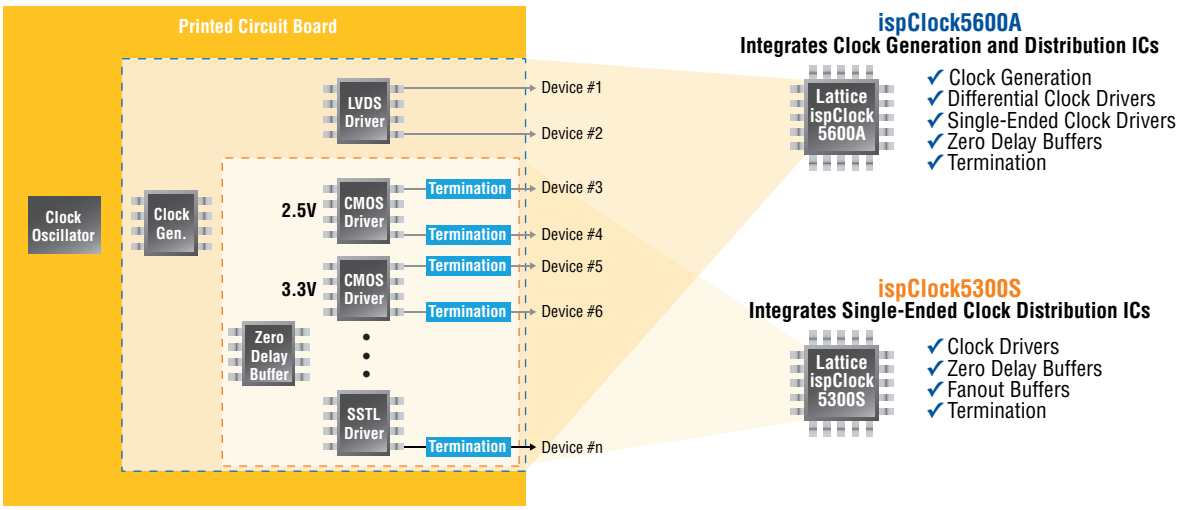
ispClock5300S Block Diagram



Key Features and Benefits

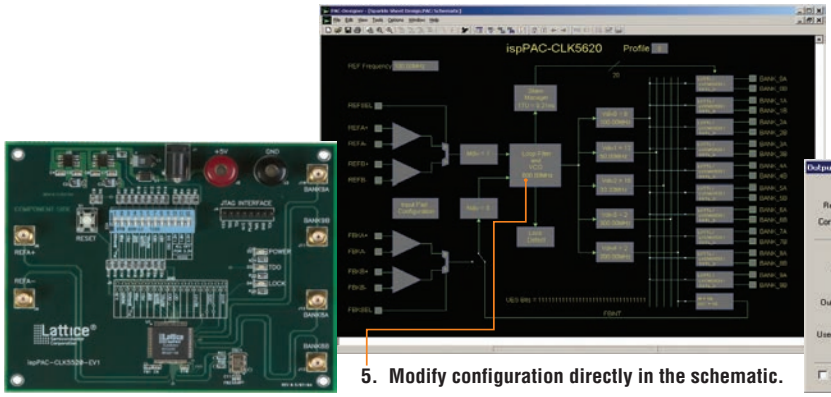
- **Reduced Board Space**
  - A single ispClock device replaces multiple types of clock devices
  - Eliminates need for serpentine traces and termination resistors
- **Improved Clock Net Performance**
  - Low jitter and skew
  - Improved signal integrity
- **Increased Timing Margin**
  - ispClock devices reduce timing uncertainty
- **Reduced Time-to-Market**
  - Windows / PC based design
  - JTAG programming and Boundary Scan

ispClock Integrates Multiple Clock Chips

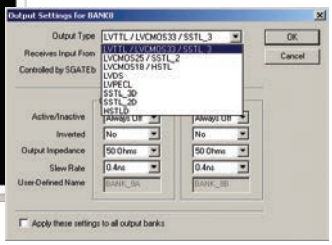


Design Made Simple with PAC-Designer Software

Lattice's PAC-Designer® software, a PC-based software tool, provides simple and intuitive pull-down menus for configuring all programmable features of the device. In addition, design utilities like the Skew Editor, Frequency Calculator and Frequency Synthesizer enable easy configuration of various counters and other options. Configurations can be downloaded into ispClock devices from a PC parallel port.

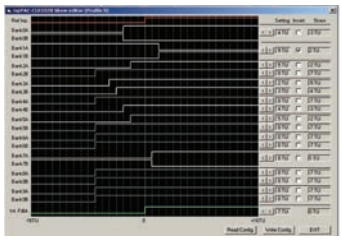


5. Modify configuration directly in the schematic.

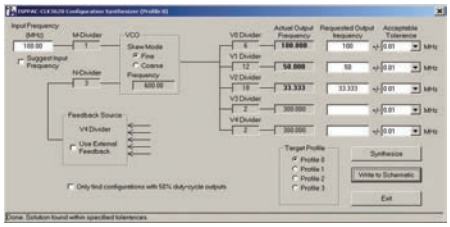


1. Specify I/O interface type.

4. Download design configuration to ispClock5600A for verification.



3. Graphically adjust skew for each clock output.



2. Synthesize M, N & V counters from output frequencies.

ispClock Attributes

Feature	ispClock5600A Family		ispClock5300A Family				
	5610A	5620A	5304S	5308S	5312S	5316S	5320S
Outputs	10	10	4	8	12	16	20
Input & Output Frequency Range	8 to 400MHz		8 to 267MHz (input), 5 to 267MHz (output)				
VCO Operation	320 to 800MHz		160 to 400MHz				
Spread Spectrum Compatibility	Yes		Yes				
Programmable Input Types	LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Diff. SSTL, Diff. HSTL		LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Diff. SSTL, Diff. HSTL				
Programmable Output and Feedback Interface Types	LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Diff. SSTL, Diff. HSTL		LVTTL, LVCMOS, SSTL, HSTL				
Type of PLL Feedback	Internal/External		External				
Maximum Cycle-Cycle Jitter	70ps (peak-peak)		70ps (peak-peak)				
Maximum Period Jitter (RMS)	12ps		12ps				
Maximum Phase Jitter (RMS)	50ps		50ps				
Maximum Static Phase Offset	-100ps to 200ps		-40ps to 100ps				
Frequencies Generated	5		3				
Programmable Skew	156ps to 12ns		156ps to 5ns				
Programmable Termination	40 to 70Ω & 20Ω Setting		40 to 70Ω & 20Ω Setting				

Applications Support
techsupport@latticesemi.com

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