

# ispMACH 4000ZE Pico Development Kit

## Optimize Power, Space, Cost and Flexibility

The ispMACH™ 4000ZE Pico Development Kit is an easy-to-use, low-cost platform for evaluating and designing with ispMACH 4000ZE CPLDs. The kit is based on a 2.5" x 2" evaluation board that features the LC4256ZE device in a lead-free 144-pin csBGA package, a Power Manager II POWR6AT6 for power monitoring, LCD panel, and an expansion header.

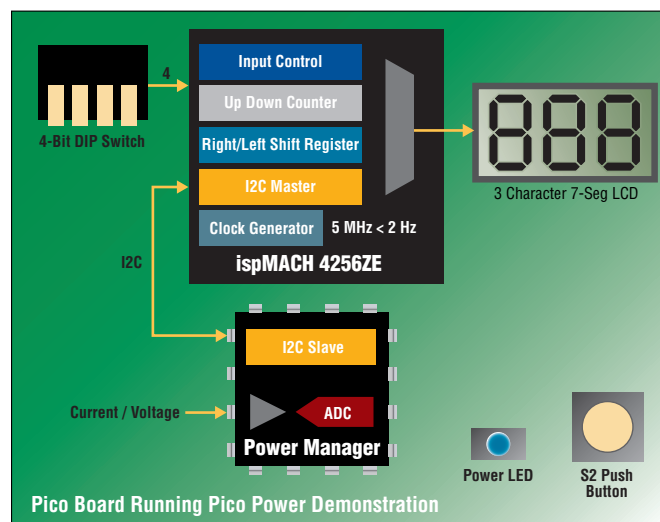
### Flexibility in an Ultra Small Package

The Pico evaluation board is small but packed with features to help evaluate the use of the ispMACH 4000ZE CPLD in the context of battery-powered, handheld application. CPLDs are ideal for glue logic, level shifting between signal standards, and providing additional interfaces for I/O limited microprocessors. On-board power monitoring circuits with the POWR6AT6 device provide a convenient way to monitor power consumption of the CPLD. A USB cable programming interface allows you to modify the CPLD programming from any PC host. And by using ispLEVER® Classic and ispVM™ software you can compile your own designs captured as VHDL, Verilog HDL, or schematics.

### Pico Power Demo

The kit includes demonstration designs pre-programmed into the ispMACH 4256ZE and POWR6AT6 devices which highlight key CPLD applications and power saving measures that will maximize battery life. The CPLD demo design integrates an up/down counter, right/left shift register, and an I<sup>2</sup>C bus master controller which communicates with the POWR6AT6. A 7-seg LCD panel displays demo output using three characters.

### Evaluation Board Diagram



### Key Features

- Pre-programmed Pico Power Demo
- ispMACH 4000ZE Device (LC4256ZE-5MN144C)
- Power Manager II Device (ispPAC-POWR6AT6)
- Button Cell Battery Powered
- 7-Seg LCD Panel
- USB Mini Jack Socket (Program/Power)
- 15x2 Expansion Header Landing for I/O, I<sup>2</sup>C, and JTAG
- Push Button for Input
- 4-bit DIP Switch
- 3.3V and 1.8V Supply Rails
- PicoView User Interface for Windows XP/Vista
- USB connector cable
- QuickSTART Guide
- CE, China RoHS Environmental-Friendly Use Period (EFUP) and Waste Electrical and Electronic Equipment (WEEE) Directives Compliant

### Ordering Information

| Product                             | Description                                                                                                              | Ordering Part # |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------|-----------------|
| ispMACH 4000ZE Pico Development Kit | ispMACH 4000ZE Pico Evaluation Board with LC4256ZE-5MN144C device, USB cable, QuickSTART Guide, and demonstration design | LC4256ZE-P-EVN  |

## Low Power Operation

The Pico evaluation circuit board design and CPLD programming employs several techniques to avoid leakage current paths and stretch battery life including: low speed CPLD clocking using the ispMACH 4256ZE embedded oscillator, oscillator disable when idle, careful use of bus keepers, and gated supply rails.

## High Performance in a Small Footprint

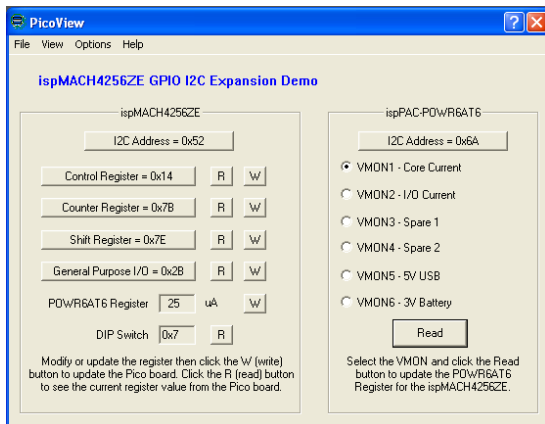
The high-performance ispMACH 4256ZE macrocell architecture is easy to design for and produces very predictable timing results with propagation delay as fast as 5.8ns with the -5 speed grade device provided on-board. The on-board ispMACH 4256ZE is featured in a space-saving 0.5 mm pitch chip, csBGA package which offers a high I/O count in a compact PCB footprint.

## Flexible I/Os

The ispMACH 4000ZE I/O cell supports a variety of output standards and can be configured for open drain operation ideal for switch and LED interfaces. I/Os support input hysteresis for all pins. Each pin supports pull-up, pull-down or a power saving bus keeper control. Programmable slew rate gives you more design options when designing PCB signal traces. The Pico evaluation board provides access to I/O bank pins and supplies for advanced experiments.

## PicoView Software Interface

The Pico Development Kit includes a software interface for Windows XP/Vista and a demonstration design for a general purpose I/O expansion scenario. For this demo, the ispMACH 4256ZE is programmed as an I<sup>2</sup>C slave processing instructions issued by a CPU/MPU. Control registers allow the processor to access counter and shift registers, GPIO, and power measurements.



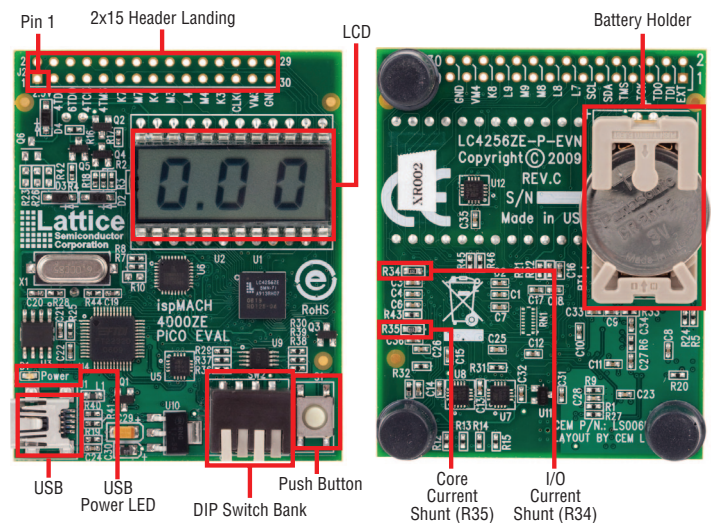
## Applications Support

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## Evaluation Board – Top & Bottom View



## Additional Information

Documentation including reference design source, sub-system descriptions, and schematics are available at [www.latticesemi.com/4000ze-pico-kit](http://www.latticesemi.com/4000ze-pico-kit).

## ispLEVER® Classic Design Tools **FREE**

The downloadable ispLEVER Classic development tools offer a comprehensive design environment for the ispMACH 4000ZE device family. ispLEVER tools include everything you need for design and constraints entry, synthesis, fitting, simulation, project management, and device programming. Synthesis and simulation tools from industry leaders Synopsys and Aldec are included with ispLEVER.

Download ispLEVER Classic at: [www.latticesemi.com/products/designsoftware/isplever/ispleverclassic](http://www.latticesemi.com/products/designsoftware/isplever/ispleverclassic)

## Rich Reference Design Portfolio

Lattice offers an expanding portfolio of IP cores and reference designs targeted for low density control path applications optimized for the ispMACH 4000ZE CPLD architecture. These include:

- 8b/10b Encoder/Decoder
- BSCAN1 - Multiple Scan Port Addressable Buffer
- BSCAN2 - Multiple Scan Port Linker
- Fast Page Mode SDRAM Controller
- HDLC (High Level Data Link Control) Controller
- I<sup>2</sup>C Bus Master
- I<sup>2</sup>C Bus Slave/Peripheral
- I<sup>2</sup>C Bus Controller for Serial EEPROM
- LPC Bus Controller
- SDRAM Controller – Advanced
- SPI Bus Controller
- UART

For more information, go to [www.latticesemi.com/intellectualproperty](http://www.latticesemi.com/intellectualproperty)



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