ispMACH 4000ZE

Low Cost, Small Package, Cool Power

The second generation ispMACH 4000ZE is ideal for ultra low-power, high-volume portable applications. The ispMACH 4000ZE offers standby current as low as 10µA typical. The cost-optimized and feature-rich ispMACH 4000ZE devices offer ultra-small space-saving ucBGA and csBGA packages, a new Power Guard feature that enables ultra-low system power and new system integration capabilities including an on-chip user oscillator and timer.

Built on proven E²CMOS® process technology, ispMACH 4000ZE devices utilize a 1.8V core voltage and support a wide range of 3.3V, 2.5V and 1.8V I/O standards. Plus, ispMACH 4000ZE devices feature 5V tolerant I/Os when using the LVCMOS 3.3, LVTTL, and PCI interfaces.

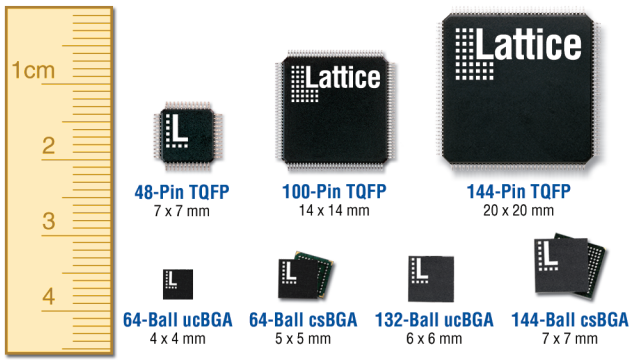
Versions of the ispMACH 4000ZE family support both commercial and industrial temperature grades and are pin compatible with the prior zero power ispMACH 4000Z family in like packages.

The new ispMACH 4000ZE family is fully supported by Lattice's easy-to-use and powerful ispLEVER® Classic design software and a wide range of popular third-party tools.

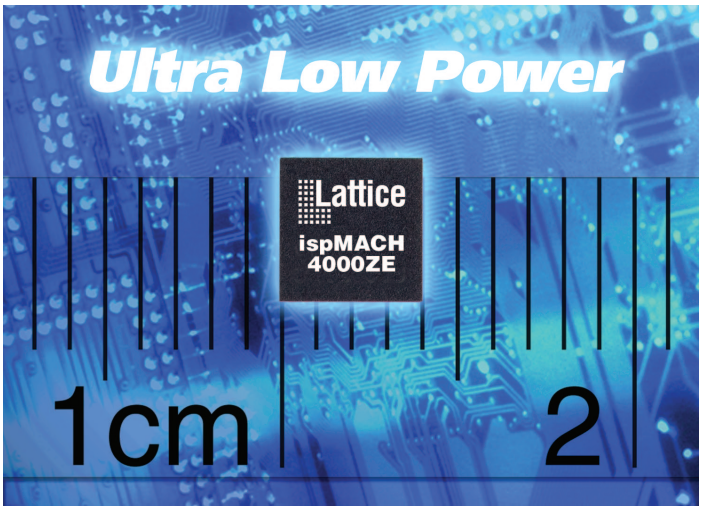
Power Guard

Power Guard lowers standby current in the system by selectively disabling unused input pins. The feature consists of an enabling multiplexer between an I/O pin and input buffer and its associated circuitry inside the device. All I/O pins in a block share a common enable signal or Block Input Enable (BIE) signal. Depending on the device size, there can be from 2 to 16 "blocks" per device. Any I/O pin in the block can be programmed to ignore the BIE signal. The feature can be enabled or disabled on a pin-by-pin basis.

ispMACH 4000ZE Space-Saving Packaging



Packages are shown actual size. Dimensions refer to package body size.



Key Features and Benefits

- **Ultra Low Power**
  - Standby current as low as 10µA typical
  - 1.8V core for low dynamic power
  - Operates down to 1.6V V_{CC}
  - Per pin pull-up, pull-down or bus-keeper control NEW
  - Power Guard with multiple enable signals NEW
- **Ultra Small Footprint**
  - Space-saving packaging as small as 4x4mm (64-ball ucBGA) NEW
- **Easy System Integration**
  - Operation with 3.3V, 2.5V, 1.8V or 1.5V LVCMOS I/O
  - 5V tolerant I/O for LVCMOS 3.3, LVTTL, and PCI interfaces
  - Hot-socketing support
  - Open-drain output option
  - Programmable output slew rate
  - 3.3V PCI compatible
  - I/O pins with fast setup path
  - Input hysteresis NEW
  - IEEE 1149.1 boundary scan testable
  - IEEE 1532 ISC compliant
  - On-chip user oscillator and timer NEW
- **High Performance**
  - 4.4ns t_{PD} pin-to-pin delay
  - 260MHz system performance
- **Broad Device Offering**
  - 32 to 256 macrocells
  - Multiple temperature range support
    – Commercial: 0 to 90°C junction (TJ)
    – Industrial: -40 to 105°C junction (TJ)
- **Eco-Friendly Materials**
  - Lead-free RoHS compliant packages
  - Halogen-free material content

ispMACH 4000ZE Device Selection Guide

Parameter	4032ZE	4064ZE	4128ZE	4256ZE
Macrocells	32	64	128	256
t_{PD} (ns)	4.4	4.7	5.8	5.8
t_{CO} (ns)	3.0	3.2	3.8	3.8
t_S (ns)	2.2	2.5	2.9	2.9
f_{MAX} (MHz)	260	241	200	200
V_{CC} (Volts)	1.8	1.8	1.8	1.8
Typical Standby Current (μA)	10	11	12	13
Packages[1]	**I/Os + Inputs**			
48-pin TQFP (7 x 7 mm)	32 + 4	32 + 4		
64-ball csBGA (5 x 5 mm, 0.5 mm pitch)	32 + 4	48 + 4		
64-ball ucBGA (4 x 4 mm, 0.4 mm pitch)		48 + 4		
100-pin TQFP (14 x 14 mm)		64 + 10	64 + 10	64 + 10
132-ball ucBGA (6 x 6 mm, 0.4 mm pitch)			96 + 4	
144-ball csBGA (7 x 7 mm, 0.5 mm pitch)		64 + 10	96 + 4	108 + 14
144-pin TQFP (20 x 20 mm)			96 + 4	96 + 4

1. Pb-free only.

Pin-by-Pin Controls

The ispMACH 4000ZE provides the following options on a per pin basis:

- Pull Up
- Pull Down
- Bus Keeper
- Or none of the above

These options allow greater flexibility in bus maintenance, while saving power.

Input Hysteresis

ispMACH 4000ZE devices offer an always on per pin hysteresis for each input. This new feature provides improved noise immunity for 3.3V and 2.5V inputs.

On-Chip Oscillator and Timer

An internal oscillator is provided for use in miscellaneous housekeeping functions such as watchdog heartbeats, digital deglitch circuits and control state machines. The oscillator is disabled by default to save power.

ispMACH 4000ZE Pico Development Kit

The ispMACH 4000ZE Pico Development Kit is packed with features to help evaluate the use of the ispMACH 4000ZE CPLD in the context of a battery-powered, handheld application. Build your own design in less than an hour using free reference designs from Lattice. Learn more at www.latticesemi.com/4000ze-pico-kit.

ispMACH 4000ZE Application Areas

- Telematics
- Smart phones
- Paging devices
- Handheld debit and credit card readers
- GPS
- Flat Panel Displays
- Calculators
- Two-way radio
- Industrial instrumentation
- Digital cameras
- Digital video recorders
- Personal audio equipment
- Portable medical equipment
- Automotive applications
- Portable barcode scanners
- Any CPLD application!

Reference Design Portfolio FREE

Lattice offers an expanding portfolio of reference designs targeted for CPLD applications. Optimized for the ispMACH 4000ZE architecture, these designs include popular protocol and connectivity standards such as I^2C and SPI. The reference designs, source code and documentation can be downloaded for free from the Lattice website. For more information, go to www.latticesemi.com/ip.

ispLEVER Classic Design Tools FREE

Lattice's ispLEVER Classic software is a comprehensive design environment for the ispMACH 4000ZE family. The tools include everything you need for design entry, synthesis, fitting, simulation, project management, device programming and more. Synthesis and simulation tools are included. Download ispLEVER Classic at www.latticesemi.com.

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