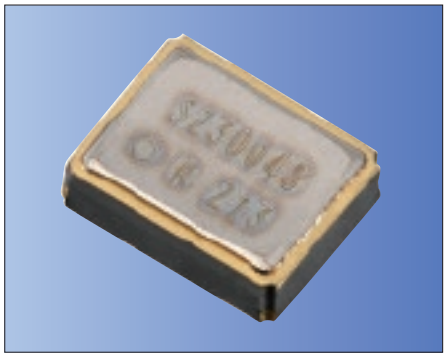
Real Time Clock Modules
Surface Mount Type Digital Temperature Compensated RTC Modules
KR3225Y Series

CMOS/ 3.0V Typ./ 3.2×2.5mm



RoHS Compliant

Features

- Miniature SMD type (3.2×2.5×1.0mm)
- Built-in 32.768kHz D-TCXO
- Excellent frequency stability : ±5.0x10^{-6}/ –40 to +85°C
- Low supply current : 0.6µA typ (V_{DD}=3.0V)
- Temperature compensated voltage range : 2.0V to 5.5V
- Time keeping voltage range : 1.3V to 5.5V
- I^{2}C-BUS interface voltage range : 1.5V to 5.5V
- I^{2}C-BUS serial interface type : 400kHz high speed type
- Frequency selection function : 32.768kHz, 1024Hz, 32Hz, 1Hz
- Voltage detection function : 2.0V temp. compensated voltage detection 1.5V Low Voltage Detection
- Various functions including full calender, alarm and timer

Applications

- High accuracy time references

How to Order

Frequency Tolerance (vs Temp.) : ±3.8×10^{-6}/ –10°C to 60°C

KR3225Y 32768 D G R 30 T xx
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

Frequency Tolerance (vs Temp.) : ±5.0×10^{-6}/ –40°C to 85°C

KR3225Y 32768 E A W 30 T xx
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

① Series
② Output Frequency
③ Frequency Stability

A	No Temp. Compensated
D	±3.8×10^{-6}
E	±5.0×10^{-6}

④ Lower Temperature

A	–40°C
G	–10°C

⑤ Upper Temperature

W	+85°C
R	+60°C

⑥ Supply Voltage

30	3.0V
33	3.3V
50	5.0V

⑦ Initial Frequency Tolerance

A	5±5×10^{-6}	B	0±5×10^{-6}	T	TCXO

⑧ Option Code

Packaging (Tape & Reel 3000pcs/ reel)

Specifications

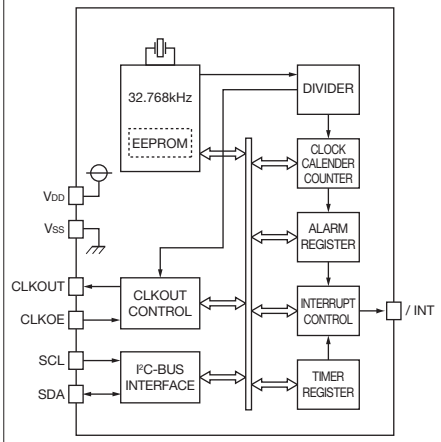
Item	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Nominal Frequency	f_nom		—	32.768	—	kHz
Time Keeping Voltage	V_{DD}	—	1.3	3.0	5.5	V
Temperature Compensation Voltage	V_{TEM}	—	2.0	3.0	5.5	V
Interface Voltage	V_{INT}	—	1.5	3.0	5.5	V
Operationg Temperature Range	T_use	No condensation	–40	+25	+85	°C
Frequency Stability vs. Temp.	fo-Tc	E : Ta=–40 to +85°C	–5.0	—	+5.0	×10^{-6}
Start up Time	t_str	Ta=25°C	—	—	1.0	sec
		Ta=–40 to +85°C	—	—	3.0	sec
Power Supply Current1	$I_{CC}1$	SCL=SDA=/ INT=V_{DD}, CLKOE=V_{SS} CLKOUT Non-operating output V_{DD}=3V	—	0.6	2.0	µA
Power Supply Current2	$I_{CC}2$	SCL=SDA=/ INT=V_{DD}, CLKOE=V_{DD} CLKOUT output 32.768kHz, V_{DD}=3V Output at no load	—	1.5	4.0	µA
		SCL=SDA=/ INT=V_{DD}, CLKOE=V_{DD} CLKOUT output 32.768kHz, V_{DD}=3V CL=15pF	—	2.7	5.5	µA
Low Voltage Detection Voltage	V_{DET}		1.3	1.4	1.5	V

Please contact us for other specifications.

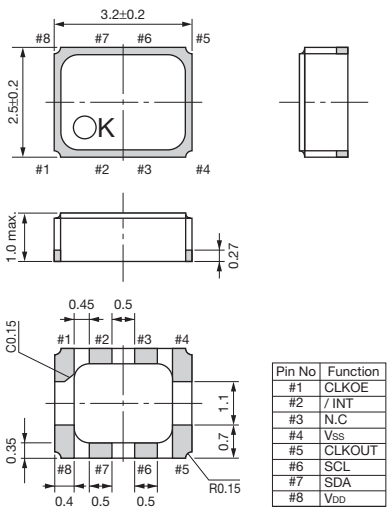
Pin Functions

Pin Name	I/ O	Function
CLKOE	I	Input to control the output mode of the CLKOUT
/ INT	O	Outputs for alarm signals, timer signals, timer update signals and other signals
V_{SS}	—	Pin connected to ground
CLKOUT	O	32.768kHz signal output (CMOS output)
SCL	I	Serial clock input for I^{2}C BUS communications
SDA	I/ O	Serial data input output for I^{2}C BUS communications
V_{DD}	—	This pin is connected to a positive power supply

Block Diagram

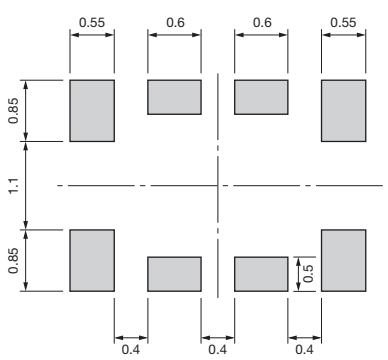


Dimensions (Unit: mm)



Pin No	Function
#1	CLKOE
#2	/ INT
#3	N.C
#4	V_{SS}
#5	CLKOUT
#6	SCL
#7	SDA
#8	V_{DD}

Recommended Land Pattern (Unit: mm)



Note: A capacitor of value 0.01µF between V_{DD} and GND is recommended.

Application Manual

Real Time Clock Module

KR3225Y Series

(I²C)

KYOCERA Crystal Device CORPORATION

Contents

SMALL CERAMIC PACKAGE
I²C-BUS Interface Real-time Clock Module

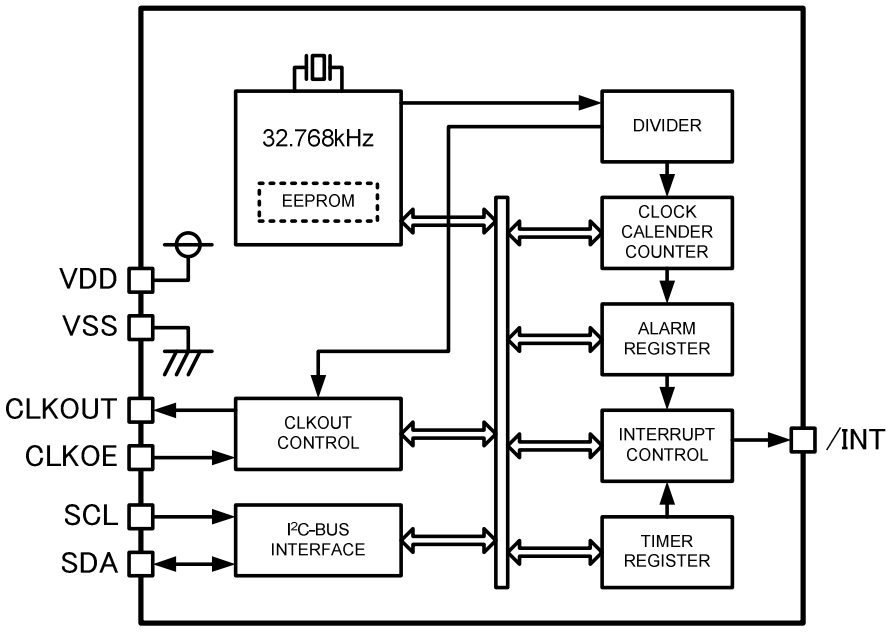
KR3225Y

- **Frequency accuracy : +/-5.0ppm (-40deg.C to +85deg.C)**
- **Temperature compensating operation power supply voltage : 2.0V to 5.5V**
- **Time keeping Voltage : 1.3V to 5.5V**
- **I2C-BUS Serial Interface Voltage : 1.5V to 5.5V**
- **Low consumption current : Typ.0.6μA**
  (VDD=3V、Temperature compensating interval30s, Clock output un-operating)
- **I2C-BUS Serial Interface : 400kHz Fast mode correspondence**
- **Clock function : Hour/ Min / Sec**
- **The leap year automatic distinction calendar function by 2099**
- **Alarm interruption function for day, date, hour and minute settings**
- **A constant cycle timer interruption function : 244.14us to 255 min**
- **Time update interruption function ：Min / Sec**
- **Clock output function ：32.768kHz / 1024Hz / 32Hz / 1Hz**
- **Power supply voltage detection function : 2.0V temperature compensated voltage detection**
  1.5V Low power supply voltage detection

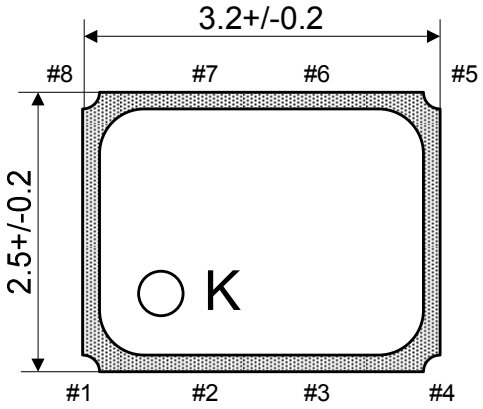
1. Overview

This module is a real time clock module of the I²C-BUS interface system which built in 32.768kHz DTCXO. In addition to the clock and the calendar function, I have an alarm interruption function, the constant cycle timer interruption function, the time update interruption function, the clock output function, and the power supply voltage detection function.

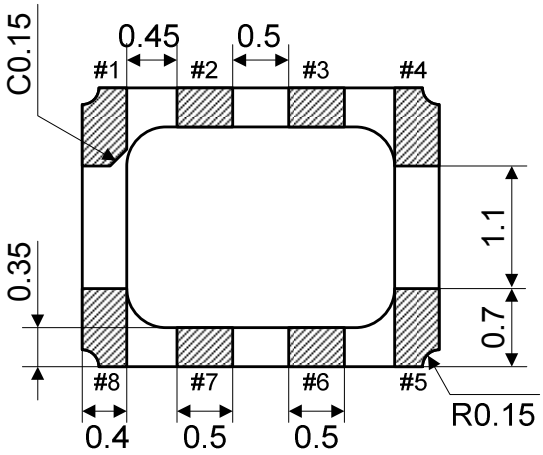
2. Block Diagram



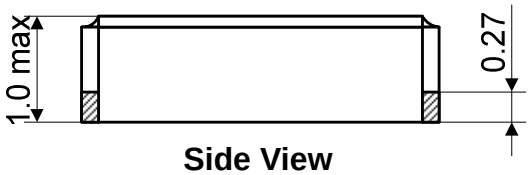
3. Outline Drawing



Top View



Bottom View



Side View

Unit: (mm)

PIN /Function

#1 : CLKOE	#5 : CLKOUT
#2 : /INT	#6 : SCL
#3 : N.C.	#7 : SDA
#4 : V_{SS}	#8 : V_{DD}

***N.C. connected to VSS inside.**

4. Pin Functions

Pin Name	I/O	Function
CLKOE	I	This is an input pin used to control the output mode of the CLKOUT pin. When this pin's level is high, the CLKOUT pin is in output mode. When it is low, the CLKOUT pin is ''Hi-Z" (High Impedance).
/INT	O	This pins is used to output alarm signals, timer signals, timer update signals and other signals. This pin is an open drain pin.
V_{SS}	–	This pin is connected to a ground.
CLKOUT	O	This pin outputs a 32.768kHz signal. This is the C-MOS output pin with output control provided via the CLKOE pin.
SCL	I	This is the serial clock input for I2C BUS communications.
SDA	I/O	This is the serial data input output for I2C BUS communications. This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I2C communication. This pin is an N-ch open drain pin during output.
V_{DD}	–	This pin is connected to a positive power supply.

5. Absolute Maximum Rating

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage(*1)	V_{DD}	---	-0.3 to +6.5	V
Input voltage(*1)	V_{IN}	SCL,SDA,CLKOE	-0.3 to +6.5	V
Output voltage1(*1)(*2)	V_{OUT1}	CLKOUT	-0.3 to V_{DD}+0.3	V
Output voltage2(*1)	V_{OUT2}	SDA,/INT	-0.3 to +6.5	V
Preservation temperature(*3)	T_{STG}	---	-40 to +85	deg.C

*1 : It is a value which must not exceed even a moment.
If it should exceed, there is concern of destruction of IC, characteristic degradation, and a reliability fall.
*2 : It is a value which V_{DD} value is a V_{DD} value of recommendation operation power supply voltage.
*3 : It is a case of N_2 or the simple substance preservation by a vacuum atmosphere.

6. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	Ta=-40 to +85deg.C	1.3	3.0	5.5	V
Time keeping voltage	V_{DDT}	Ta=-40 to +85deg.C	1.3	3.0	5.5	V
Interface operation voltage	V_{INT}	Ta=-40 to +85deg.C	1.5	3.0	5.5	V
Temperature compensated operation voltage	V_{TEM}	Ta=-40 to +85deg.C	2.0	3.0	5.5	V

* Since reliability may be affected if it is used out of the recommendation operation condition range, please use it within the limits of this.

7. Frequency Characteristic

Parameter	Item	Conditions	spec	Unit
Frequency accuracy	df/f	Ta=-40 to 85deg.C,V_{DD}=3.0V	+/-5.0*	ppm
Oscillation time of onset	t_{STA}	Ta=25deg.C,V_{DD}=3.0V	1.0(max.)	sec

* Monthly difference 13 seconds

* About the details of frequency accuracy, I correspond at the time of an individual specification exchange.

8. Electrical Characteristics

8-1. DC Characteristics

V_{SS}=0V, V_{DD}=3.0V, Ta=-40 to 85deg.C

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Current consumption	I_{DD1}	SCL=SDA=/INT=V_{DD}, CLKOE=V_{SS} CLKOUT Non-operating output Compensation interval 30 s	V_{DD}=5 V	---	1.0	4.0	µA
	I_{DD2}		V_{DD}=3 V	---	0.6	2.0	
	I_{DD3}	SCL=SDA=/INT=V_{DD}, CLKOE=V_{DD} CLKOUT output 32.768 kHz C_{LOUT}=0 pF(*1)output at no load Compensation interval 30 s	V_{DD}=5 V	---	2.5	7.0	µA
	I_{DD4}		V_{DD}=3 V	---	1.5	4.0	
	I_{DD5}	SCL=SDA=/INT=V_{DD}, CLKOE=V_{SS} CLKOUT Non-operating output Operating temperature compensation circuit	V_{DD}=5 V	---	350	700	µA
	I_{DD6}		V_{DD}=3 V	---	150	300	
High level input voltage	V_{IH1}	SCL, SDA, CLKOE pins		0.8V_{DD}	---	5.5	V
Low level input voltage	V_{IL1}	SCL, SDA, CLKOE pins		0.0	---	0.2V_{DD}	V
High level Output voltage	V_{OH1}	CLKOUT pins	V_{DD}=5 V, I_{OH1}= -1 mA	4.5	---	5.0	V
	V_{OH2}		V_{DD}=3 V, I_{OH2}= -1 mA	2.2	---	3.0	
Low level Output voltage	V_{OL1}	CLKOUT pins	V_{DD}=5 V, I_{OL1}= 1 mA	0.0	---	0.5	V
	V_{OL2}		V_{DD}=3 V, I_{OL2}= 1 mA	0.0	---	0.8	
	V_{OL3}	/INT pins	V_{DD}=5 V, I_{OL3}= 1 mA	0.0	---	0.25	V
	V_{OL4}		V_{DD}=3 V, I_{OL4}= 1 mA	0.0	---	0.4	
	V_{OL5}	SDA pins	V_{DD} ≥2 V, I_{OL5}= 3 mA	0.0	---	0.4	V
Input leak current	I_{LK}	CLKOE, SCL, SDA pins, V_{IN} = V_{DD} or V_{SS}		-0.5	---	0.5	µA
Output leak current	I_{OZ}	CLKOUT, /INT, SDA pins, V_{OUT} = V_{DD} or V_{SS}		-0.5	---	0.5	µA
Power supply voltage Detection voltage	V_{DET1}	Temperature compensating operation voltage detection (*2)		1.8	1.9	2.0	V
	V_{DET2}	Low power supply voltage detection		1.3	1.4	1.5	V

*1:C_{LOUT} is the external load capacitance connected to CLKOUT.

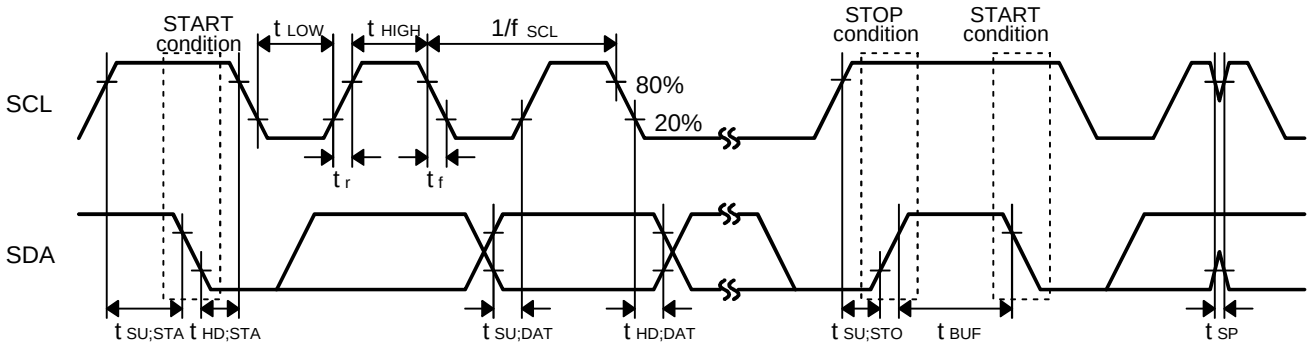
*2:When V_{DD} falls below V_{DET1}, the internal detection circuit operates, and the intermittent temperature sensor output A/D converter stops. At the same time, the current data value in the CL[10-0] oscillator capacitance switching bits is retained. When V_{DD} rises above V_{DET1} again, the intermittent temperature sensor A/D converter is enabled.

8-2. AC Characteristics-1

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SCL clock frequency	f_{SCL}		---	---	400	kHz
Start condition setup time	$t_{SU;STA}$		0.6	---	---	us
Start condition hold time	$t_{HD;STA}$		0.6	---	---	us
Data setup time	$t_{SU;DAT}$		100	---	---	ns
Data hold time	$t_{HD;DAT}$		0	---	900	ns
Stop condition setup time	$t_{SU;STO}$		0.6	---	---	us
Bus free time between start and stop conditions	t_{BUF}		1.3	---	---	us
SCL “L” pulse width	t_{LOW}		1.3	---	---	us
SCL “H” pulse width	t_{HIGH}		0.6	---	---	us
SCL,SDA rise time	t_r	20%→80%	---	---	0.3	us
SCL,SDA fall time	t_f	80%→20%	---	---	0.3	us
Maximum bus spike time	t_{SP}		---	---	50	ns
Bus line load capacitance	C_b	$V_{DD} \geq 1.8V$	---	---	400	pF
		$V_{DD} < 1.8V$	---	---	50	

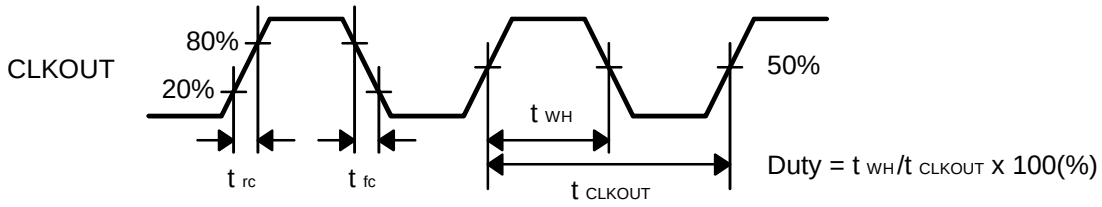
*KR3225Y access from the transfer of the start condition until the stop condition should be completed within 0.5 seconds. If the access exceeds 0.5 seconds, an internal monitor timer forcibly terminates the RTC bus interface access.

8-3. Timing Chart



8-4. AC Characteristics-2

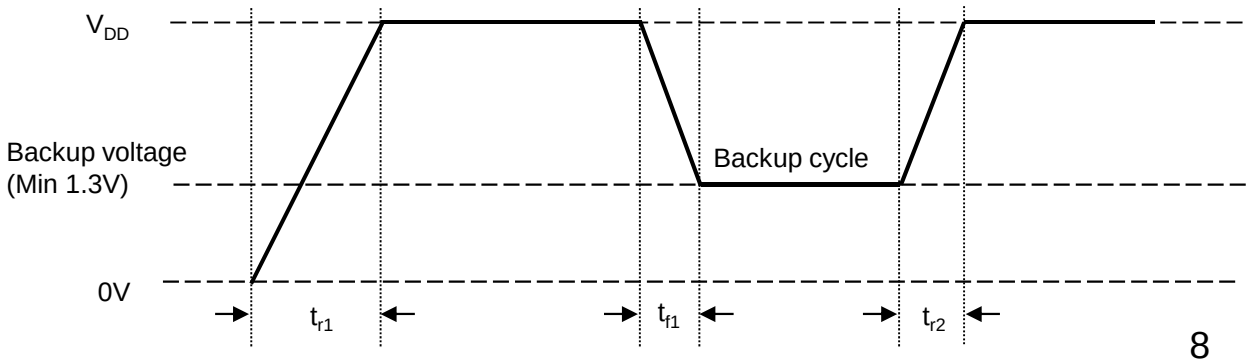
Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
CLKOUT duty	Duty	C_{LOUT}=15pF, 0.5V_{DD} threshold		40	50	60	%
CLKOUT rise time	t_{rC}	C_{LOUT}=15pF 20%→80%	V_{DD}=1.8 to 5.5V	---	---	70	ns
			V_{DD}=1.5 to 5.5V	---	---	180	ns
			V_{DD}=1.5 to 5.5V	---	---	1100	ns
CLKOUT fall time	t_{fC}	C_{LOUT}=15pF 80%→20%	V_{DD}=1.8 to 5.5V	---	---	70	ns
			V_{DD}=1.5 to 5.5V	---	---	180	ns
			V_{DD}=1.3 to 5.5V	---	---	1100	ns



8-5.Power Supply Rise Time and Fall Time

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Startup supply voltage rise time(*1)	t_{r1}		---	---	10	ms/V
Backup transition supply voltage fall time(*1)	t_{f1}		5	---	---	us/V
Backup return supply voltage rise time(*1)	T_{r2}		5	---	---	us/V

*1: This device is equipped with a power-on reset circuit to initialize internal settings when power is first applied. if supply voltage rise time or fall time are outside the specified time, there is a possibility that the power on reset circuit may not be activated when power is first applied or during the backup transition/return cycle. Ensure supply voltage rise times and fall times are within the specified values for stable, correct, power-on reset circuit operation.



9.Method of Application

9-1.Time Control Register Table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	SEC	-	S40	S20	S10	S8	S4	S2	S1
01h	MIN	-	M40	M20	M10	M8	M4	M2	M1
02h	HOUR	-	-	H20	H10	H8	H4	H2	H1
03h	WEEK	-	-	-	-	-	W4	W2	W1
04h	DAY	-	-	D20	D10	D8	D4	D2	D1
05h	MONTH	-	-	-	MO10	MO8	MO4	MO2	MO1
06h	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07h	MIN Alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1
08h	HOUR Alarm	AE	RAM	HA20	HA10	HA8	HA4	HA2	HA1
09h	WEEK Alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0
	DAY Alarm		RAM	DA20	DA10	DA8	DA4	DA2	DA1
0Ah	Timer Counter	T128	T64	T32	T16	T8	T4	T2	T1
0Bh	Select Register	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	UTS
0Ch	Flag Register	-	-	VDHF	VDLF	-	TF	AF	UTF
0Dh	Control Register	RESET	TEST	RAM	FIE	TE	TIE	AIE	UTIE

* The register values are undefined when power is first applied; ensure the device is configured before use. Note that the TCS1, TCS0, CFS1, CFS0, TEST, FIE, TE, TIE, AIE, and UTIE bits are reset to “0”, and the VDLF bit is set to “1” when power is applied.

* Bits indicated by a hyphen ”-” are read-only bits with read output value of “0”.

* Only “0” data values can be written to the VDHF, VDLF, TF, AF, and UTF bits.

* The TEST bit is a reserved bit for manufacturer testing, and should always be set to “0” for normal operation.

* Since the write-in read-out operation to Address 0Eh and 0Fh causes malfunction, it is considered as an access inhibit.

9-2.Register Description

9-2-1.Time and Calendar Register (Address 00h to 06h)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00h	SEC	-	S40	S20	S10	S8	S4	S2	S1
01h	MIN	-	M40	M20	M10	M8	M4	M2	M1
02h	HOUR	-	-	H20	H10	H8	H4	H2	H1
03h	WEEK	-	-	-	-	-	W4	W2	W1
04h	DAY	-	-	D20	D10	D8	D4	D2	D1
05h	MONTH	-	-	-	MO10	MO8	MO4	MO2	MO1
06h	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

•Data format
the time and calendar data is represented in BCD format.

•HOUR register
The HOUR register contains the hour in 24-hour display mode.

•WEEK register
The WEEK register increments using a 7-step up-counter(W4W2W1)=(000)→(001)→…→(110)→(000). The logic table for the (W4W2W1) bits for the day of the week are configurable by the user.

•YEAR register
The YEAR register contains the last 2 digits of the western calendar year.

•Automatic leap year correction function
The automatic leap year correction function corrects for leap years between 2000 and 2099.

•Example time and calendar setting
For a time of 5:43:21 in the morning on Sunday, July6, '98
(assuming the WEEK register setting for Sunday =(W4W2W1)=(000))

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	SEC	–	0	1	0	0	0	0	1
01h	MIN	–	1	0	0	0	0	1	1
02h	HOUR	–	–	0	0	0	1	0	1
03h	WEEK	–	–	–	–	–	0	0	0
04h	DAY	–	–	0	0	0	1	1	0
05h	MONTH	–	–	–	0	0	1	1	1
06h	YEAR	1	0	0	1	1	0	0	0

*Time and calendar setting that are invalid will result in malfunction. Always ensure the data settings are valid.

9-2-2. Alarm Registers (Address 07h to 09h)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07h	MIN Alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1
08h	HOUR Alarm	AE	RAM	HA20	HA10	HA8	HA4	HA2	HA1
09h	WEEK Alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0
	DAY Alarm		RAM	DA20	DA10	DA8	DA4	DA2	DA1

These registers specifies the alarm time using day of the week, day, hour, and minute settings. Address 09h specifies the day of the week or the day setting, selected by the AS (Alarm Select) bit in address 0Bh. The AF (Alarm Flag) bit in address 0Ch is set to “1” when a time is specified in the Alarm Registers.

• Assigning the day of the week using the WEEK Alarm register bits
The WEEK Alarm register WA0 to WA6 bits correspond to the bits in the WEEK register in address 03h: (W4W2W1) = (000) to (110).

Example: When the WEEK register setting for Sunday = (W4W2W1) = (000)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
09h	WEEK Alarm	AE	Sat	Fri	Thu	Wed	Tue	Mon	Sun

The alarm can be set arbitrarily for multiple days of the week.

Example: Monday to Friday alarm, when the WEEK register settingfor Sunday = (W4W2W1) = (000)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
09h	WEEK Alarm	0	0	1	1	1	1	1	0

• Minute alarm, hourly alarm, daily alarm function
When the AE (Alarm Enable) bit 7 in a register is set to “1”, the alarm is set to be triggered after every increment (minute, every hour, or every day) of the corresponding register.

Example: Alarm setting for 15 minutes past the hour for every hour

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07h	MIN Alarm	0	0	0	1	0	1	0	1
08h	HOUR Alarm	1	Don’t care bits when bit 7 = “1”						

• RAM bit
Can be used as a general-purpose RAM bit.

9-2-3. Timer Counter Register (Address 0Ah)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ah	Timer Counter	T128	T64	T32	T16	T8	T4	T2	T1

This register specifies the count value of a down-counter used for fixed-cycle timer interrupts. The fixed-cycle timer source clock is specified using the TSS1 and TSS0 (Timer Source Clock Select) bits in address 0Bh.
When the TE (Timer Enable) bit in address 0Dh is changed from “0” to “1”, the counter starts counting down from the specified count value. When the down-counter reaches zero, the TF (Timer Flag) bit in address 0Ch is set to “1”.
The down-counter continually repeats counting down from the specified count value while the TE bit is set to “1”.

9-2-4. Select Register (Address 0Bh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Bh	Select Register	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	UTS

• TCS (Temperature Compensation Select) bits
The TCS bits select the temperature compensation, operating interval.
Temperature compensation operates in sync with the clock register timing.

TCS1	TCS0	Temperature compensation operating interval
0	0	0.5 sec
0	1	2 sec
1	0	10 sec
1	1	30 sec

* When power is applied, TCS is reset to “00” and 0.5 sec temperature compensation operating interval is selected.

• CFS (CLKOUT Frequency Select) bits
The CFS bits select the CLKOUT output frequency.

CFS1	CFS0	CLKOUT output frequency
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

* When power is applied, CFS is reset to “00” and 32.768 kHz CLKOUT output frequency is selected.

• TSS (Timer Source Clock Select) bits
The TSS bits select the fixed-cycle timer source clock.

TSS1	TSS0	Timer source clock
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

• AS (Alarm Select) bit
The AS bit selects day of week alarm or day alarm.
The alarm data in address 09h is interpreted according to the following alarm setting.

AS	Alarm type
0	Day of week alarm
1	Day alarm

• UTS (Update Time Select) bit
The UTS bit selects the timing for generating time update interrupts.

UTS	Time update interrupt timing
0	Seconds digits update
1	Minutes digits update

9-2-5. Flag Register (Address 0Ch)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ch	Flag Register	-	-	VDHF	VDLF	-	TF	AF	UTF

• VDHF (Voltage Detect High Flag) bit

The VDHF bit is the temperature compensation operating voltage detection flag. Voltage detection is performed intermittently in sync with the temperature compensation operating interval timing.

VDHF	Description
0	Supply voltage is V_{DET1} (2.0 V max.) or higher
1	Supply voltage is V_{DET1} (2.0 V max.) or lower

* After detection, the VDHF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

• VDLF (Voltage Detect Low Flag) bit

The VDLF bit is the supply voltage undervoltage detection and power-ON reset signal detection flag. Voltage detection is performed intermittently in sync with the temperature compensation operating interval timing.

VDLF	Description
0	Supply voltage is V_{DET2} (1.5 V max.) or higher, or power-ON reset signal undetected
1	Supply voltage is V_{DET2} (1.5 V max.) or lower, or power-ON reset signal detected.

* After detection, the VDLF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

• TF (Timer Flag) bit

The TF bit is the fixed-cycle timer interrupt detection flag.

TF	Description
0	Normal operation
1	Fixed-cycle down-counter zero detected

* After detection, the TF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

• AF (Alarm Flag) bit

The AF bit is the alarm interrupt detection flag.

AF	Description
0	Normal operation
1	Alarm time detected

* After detection, the AF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

• UTF (Update Time Flag) bit

The UTF bit is the time update interrupt detection flag.

UTF	Description
0	Normal operation
1	Time update completion detected

* After detection, the UTF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

9-2-6. Control Register (Address 0Dh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Dh	Control Register	RESET	TEST	RAM	FIE	TE	TIE	AIE	UTIE

• RESET bit

RESET	Description
0	Normal operation
1	1 to 64 Hz frequency divider counter reset. Clock function stops.

* After setting the RESET bit to “1”, this bit is reset to “0” after a STOP condition is received, after restart, or after a 0.5 sec I^2C-bus interface reset..

• TEST bit

The TEST bit is for manufacturer testing. Leave set to “0” for normal operation.

TEST	Description
0	Normal operating mode
1	Test mode

• RAM bit

Can be used as a general-purpose RAM bit.

• FIE (Frequency Interrupt Enable) bit

The FIE bit is the enable bit for the 50% duty, 1 Hz signal output on /INT.

FIE	Description
0	/INT 1 Hz output disable
1	/INT 1 Hz output enable

* When power is applied, FIE is reset to “0” and /INT output disable is selected.

• TE (Timer Enable) bit

The TE bit enables the fixed-cycle timer down-counter.

TE	Counter operation
0	Timer count stop
1	Timer count start

* When power is applied, TE is reset to “0” and timer count stop is selected.

• TIE, AIE, UTIE (Timer, Alarm, Update Time Interrupt Enable) bits

The TIE, AIE, and UTIE bits enable the interrupt signal outputs on /INT. TIE controls the fixed-cycle timer interrupt output, AIE controls the alarm interrupt output, and UTIE controls the time update interrupt output.

TIE, AIE, UTIE	Description
0	/INT output disable
1	/INT output enable

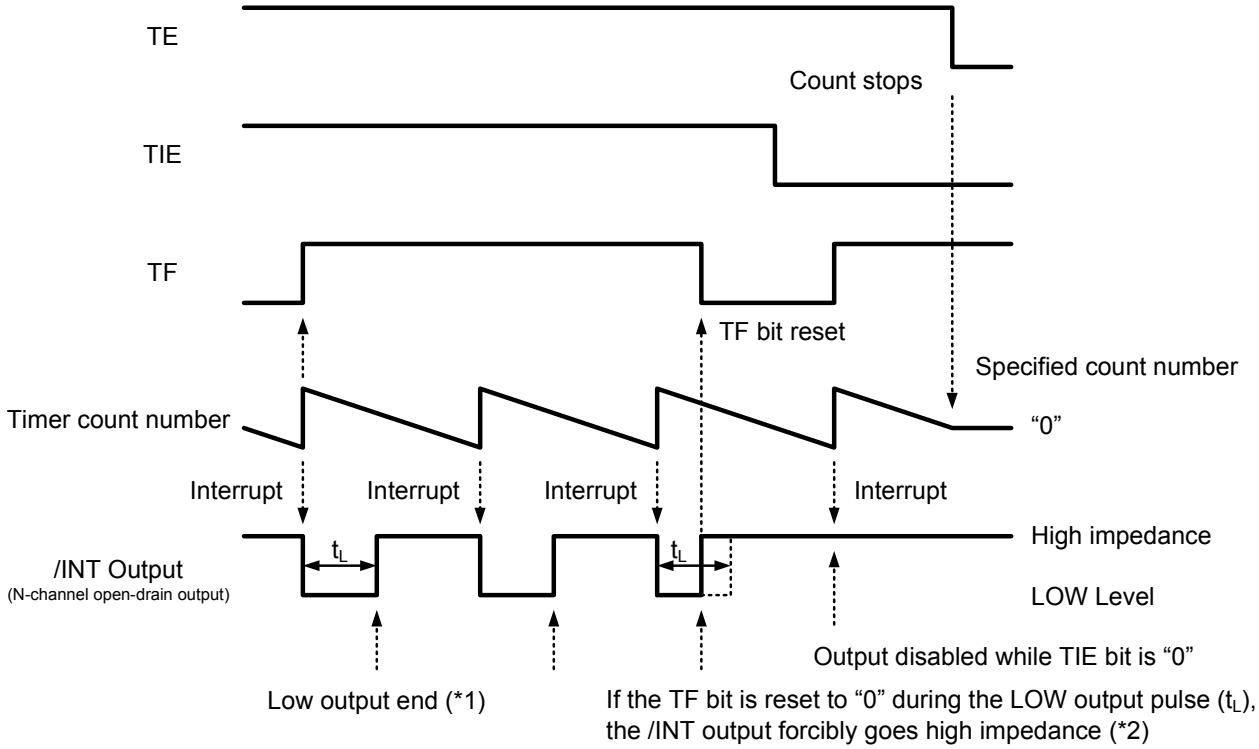
* When power is applied, these bits are reset to “0” and /INT output disable is selected.

The output from /INT is the logical-OR of the fixed-cycle timer interrupt, alarm interrupt, time update interrupt, and FIE-controlled 1 Hz signal outputs.

9-3. Interrupt Function Description

9-3-1. Fixed Cycle Timer Interrupt

The fixed-cycle timer interrupt function generates an interrupt using the cycle count specified by the value in the timer counter register (Address 0Ah) and the frequency specified by the timer source clock bits (TSS1, TSS0, in Address 0Bh). When the interrupt is generated (when the timer count reaches zero), TF is set to “1” and the /INT interrupt signal is output, subject to the state of the TIE timer interrupt enable bit, as shown in the following diagram. The fixed-cycle interrupt operation continues repeatedly while the TE timer enable bit is set to “1”.



*1: When an interrupt is generated and TIE is “1”, a single LOW-level pulse is output on /INT. The pulse width is given below.

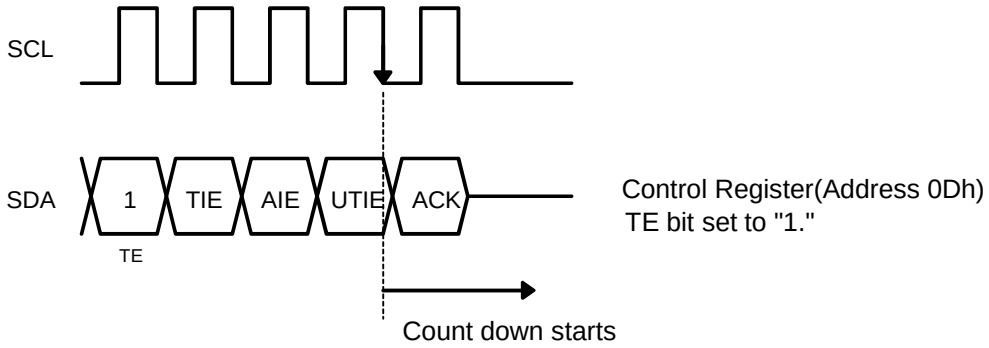
*2: If the TF bit is reset to “0” during the /INT LOW-level pulse output after an interrupt, the /INT output immediately stops

TIE	Description
0	/INT fixed-cycle timer interrupt output disable
1	/INT fixed-cycle timer interrupt output enable

* If not using the fixed-cycle timer interrupt function, the timer counter register (Address 0Ah) can be used as general-purpose RAM by setting the TE and TIE bits to “0”.

TSS1	TSS0	Source clock	Low-level output (t_L)
0	0	4096 Hz	0.122ms
0	1	64 Hz	7.81ms
1	0	1 Hz	7.81ms
1	1	1/60 Hz	7.81ms

• Timer start timing
In write mode, the timer count operation starts from the falling edge of the clock after writing to Address 0Dh, as shown in the following diagram.



• Fixed-cycle timer length
The fixed-cycle timer length is determined by the settings for the timer counter and source clock.

Assignable cycle length : 244.14us to 255min

Fixed-cycle timer length =Timer counter set value x *Source clock period
(* : The source clock period is the inverse of the source clock frequency.)

* : The fixed-cycle timer length has an error of up to 1 source clock period due to the propagation through the internal circuits.

• Example : Register settings for fixed-cycle timer interrupts
For 10-minute fixed-cycle interrupts:

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Ch	---	---	VDHF	VDLF	---	0(TF)	AF	UTF
0Dh	RESET	TEST	RAM	FIE	0(TE)	0(TIE)	AIE	UTIE

-Set TF,TE,TIE to “0” to prevent incorrect operation

↓

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Ah	0	0	0	0	1	0	1	0
0Bh	TCS1	TCS0	CFS1	CFS0	1(TSS1)	1(TSS0)	AS	UTS

-Set fixed-cycle timer length
-Set timer count register to 10(0Ah)
-Set source clock to 1 minute (TSS1,TSS0)=(11)

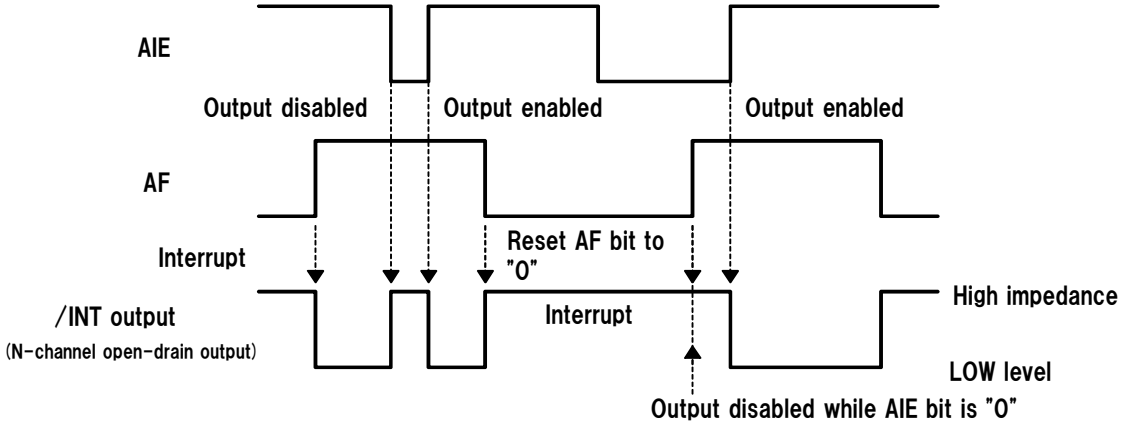
↓

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Dh	RESET	TEST	RAM	FIE	1(TE)	1(TIE)	AIE	UTIE

-Set TE,TIE to “1” to start the timer and enable the /INT output. When the count reaches zero, enters wait state for fixed- cycle timer interrupt

9-3-2. Alarm Interrupt

The alarm interrupt function generates an interrupt when the clock matches the time setting in the alarm register. When the interrupt is generated, AF is set to “1” and the /INT interrupt signal is output, subject to the state of the AIE alarm interrupt enable bit, as shown in the following diagram.
The alarm interrupt timing occurs when the seconds digits change from 59 seconds to 0 seconds and carries over into the minutes digits.



AIE	Description
0	/INT alarm interrupt output disable
1	/INT alarm interrupt output enable

* If not using the alarm interrupt function, the alarm registers (Address 07h to 09h) can be used as general-purpose RAM by setting AIE bit to “0”.

Example: Register setting for alarm interrupts
For 7:00am alarm from Monday to Friday:
(assuming the WEEK register (Address 03h)setting for Sunday=(W4W2W1)=(000))

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Dh	RESET	TEST	RAM	FIE	TE	TIE	0(AIE)	UTIE

-Set AIE to "0“ to prevent incorrect operation

↓

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
07h	0	0	0	0	0	0	0	0
08h	0	0	0	0	0	1	1	1
09h	0	0	1	1	1	1	1	0
0Bh	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	0(AS)	UTS

-Set the alarm time
-Set the minutes alarm register to 0 minutes (00h)
-Set the hour alarm register to 7 o’clock (07h)
-Set the day-of-week alarm register to Monday-Friday (3Eh)
-Set AS to “0” to select day-of-week alarm

↓

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Ch	---	---	VDHF	VDLF	---	TF	0(AF)	UTF

-Reset the AF bit to “0”

↓

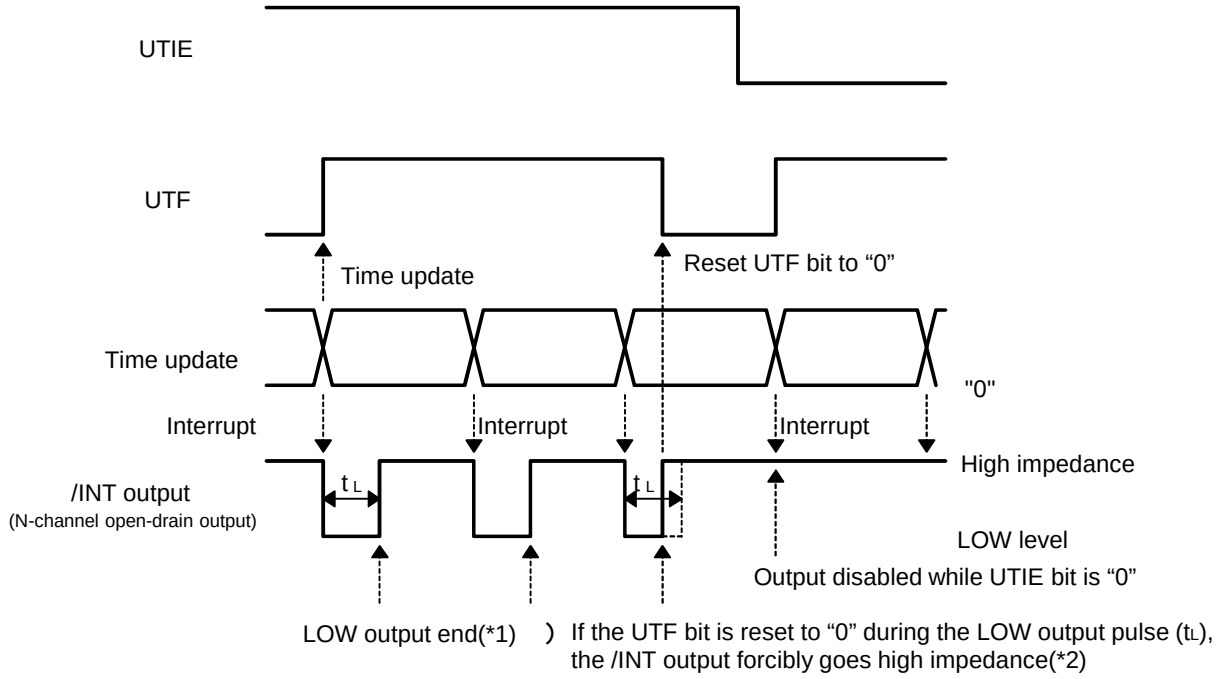
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Dh	RESET	TEST	RAM	FIE	TE	TIE	1(AIE)	UTIE

-Set AIE to “1” to enable the /INT output. Enters wait state for alarm interrupt

9-3-3. Time Update Interrupt

The time update interrupt function generates an interrupt whenever the seconds or minutes digits is updated. When the interrupt is generated, UTF is set to “1” and the /INT interrupt signal is output, subject to the state of the UTIE time update interrupt enable bit, as shown in the following diagram.

The time update interrupt timing occurs when the digits specified by the UTS bit are updated. When the RESET bit in Address 0Dh is set to "1“, time update interrupts are not generated.



*1: When an interrupt is generated and UTIE is “1”, a signal LOW-level pulse is output on /INT. The pulse width is given below.

*2: If the UTF bit is reset to “0” during the /INT LOW-level pulse output after an interrupt, the /INT output immediately stops.

UTS	Time update timing	LOW-level output (t_L)
0	“Second” update	7.81ms
1	“Minute” update	7.81ms

UTIE	Description
0	/INT time update interrupt output disable
1	/INT time update interrupt output enable

• Example: register settings for time update interrupts.
For time update interrupts when minutes digits are updated.

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Ch	---	---	VDHF	VDLF	---	TF	AF	0(UTF)
0Dh	RESET	TEST	RAM	FIE	TE	TIE	AIE	0(UTIE)

-Set UTF, UTIE to “0” to prevent incorrect operation

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Ah	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	1(UTS)

-Set time update interrupt
-Set UTS bit to minutes update(1)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0Dh	RESET	TEST	RAM	FIE	TE	TIE	AIE	1(UTIE)

-Set UTIE to “1” to enable the /INT output. Enters wait state for time update interrupt.

9-3-4. Interrupt Signal Identification

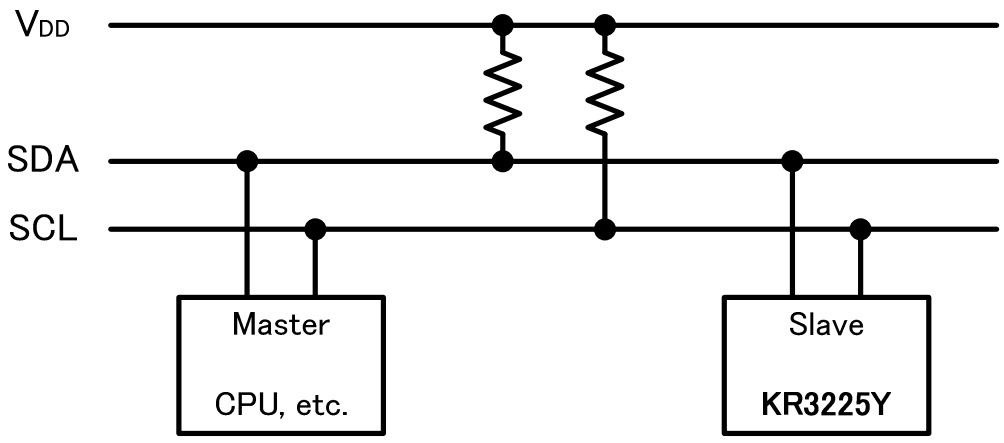
The /INT interrupt output goes LOW when a fixed-cycle timer interrupt, alarm interrupt, or time update interrupt is generated. Whenever an interrupt is generated, the source of the interrupt is indicated by the flags in the flag register (Address 0Ch), so that you can check which interrupt caused the output on /INT.

9-4. I2C-BUS Serial Interface

9-4-1. System Configuration

SCL and SDA are both connected to the V_{DD} line via a pull-up resistance.

All ports connected to the I2C bus must be open drain in order to enable AND connections to multiple devices.



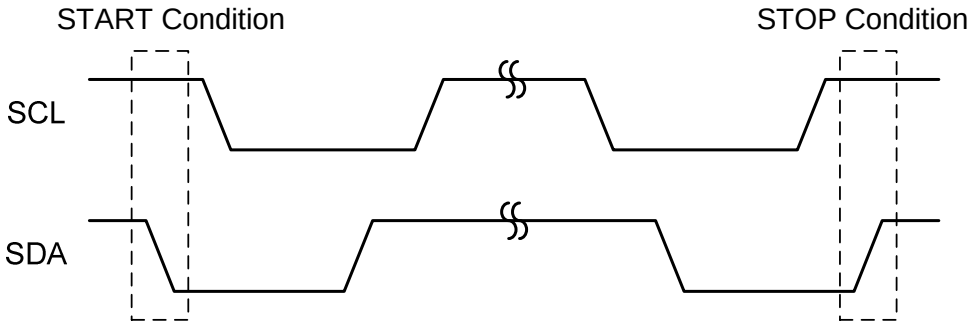
9-4-2. START Condition and STOP Condition

(1) START Condition

The SDA level changes from high to low while SCL is at high level.

(2) STOP Condition

The SDA level changes from low to high while SCL is at high level.

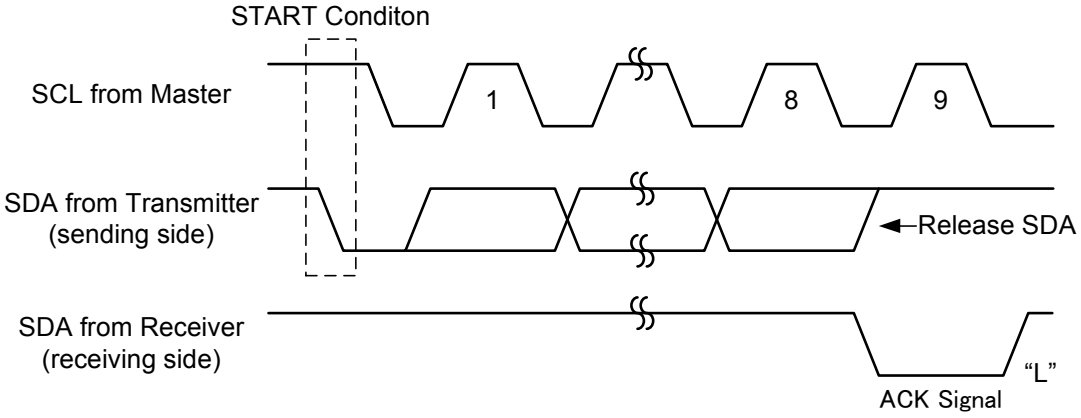


9-4-3. Acknowledge Signal (ACK Signal)

The data transfer is carried out by 8bit START condition after detection.
Data to be transferred does not matter how many times each 8bit.
Every transfer of 8bit, while the sending and the receiving device, it sends a bit of acknowledgment that the data acknowledge signal.

The sending eye on the falling edge of clock pulse and release 8bit (High) the SDA, if the receiver successfully receives the data, and then to Low the SDA.
Make sure that the sender is an acknowledge signal comes back by this.
Or to send a STOP condition, send the following data.

On the other hand, if the receiving side, is recognized as the end of data transfer(KR3225Y) sending, STOP condition is the master side (do not send an acknowledge signal) not to Low SDA after receiving 8bitby side is the master of the CPU or the like willbe transmitted.



9-4-4. Slave Address

The I2C-BUS, 7bit slave address has been set for each device. After detecting a START condition, and react to a subsequent communication from the master to be received by the I2C-BUS slave to this address.

When the actual communication, you will receive a 8bit data added along R / W (read / write) bit with the slave address.

Slave address

	Slave address							R/W bit
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Mode	0	1	1	0	0	1	0	0 (= Write)
Read Mode	0	1	1	0	0	1	0	1 (= Read)

9-5. I2C-BUS Data Transfer Sequence

Since the KR3225Y includes an address auto increment function, once the initial address has been specified, the KR3225Y increments (by one byte) the receive address each time data is transferred.

9-5-1. Data Writing Sequence

(1) CPU transfers START condition [S].

(2) CPU transmits the KR3225Y's slave address with the R/W bit set to write mode.

(3) Check for ACK signal from KR3225Y.

(4) CPU transmits write address to KR3225Y.

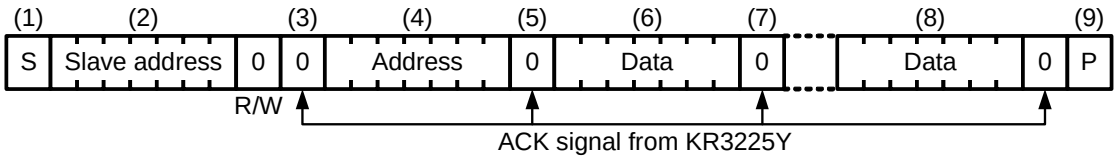
(5) Check for ACK signal from KR3225Y

(6) CPU transfers write data to the address specified at (4) above.

(7) Check for ACK signal from KR3225Y.

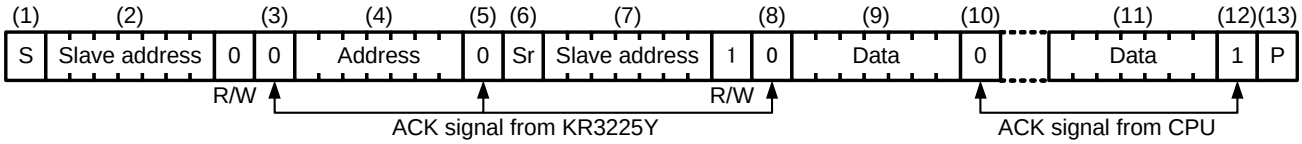
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.

(9) CPU transfers STOP condition [P].



9-5-2. Data Reading Sequence

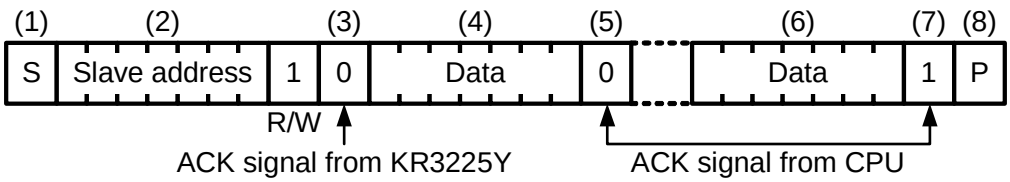
(1) CPU transfers START condition [S].
(2) CPU transmits the KR3225Y's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from KR3225Y.
(4) CPU transfers address for reading from KR3225Y.
(5) Check for ACK signal from KR3225Y.
(6) CPU transfers RESTART condition [Sr].
(7) CPU transfers the KR3225Y's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from KR3225Y.
(9) Data from address specified at (4) above is output by the KR3225Y
(10) CPU transfers ACK signal to KR3225Y.
(11) Repeat (9) and (10) if necessary. Reed addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers STOP condition [P].



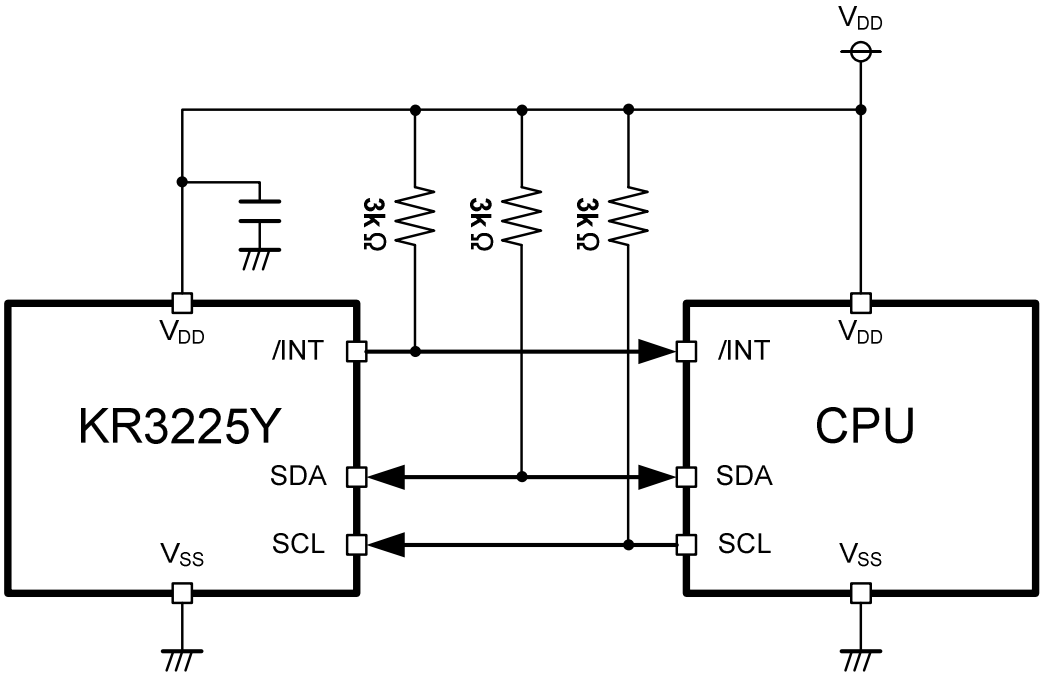
9-5-3. Data Reading Sequence When Address is not Specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address +1.

(1) CPU transfers START condition [S].
(2) CPU transmits the KR3225Y's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from KR3225Y.
(4) Data is output from the KR3225Y to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to KR3225Y.
(6) Repeat (4) and (5) if necessary. Reed addresses are automatically incremented.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers STOP condition [P].



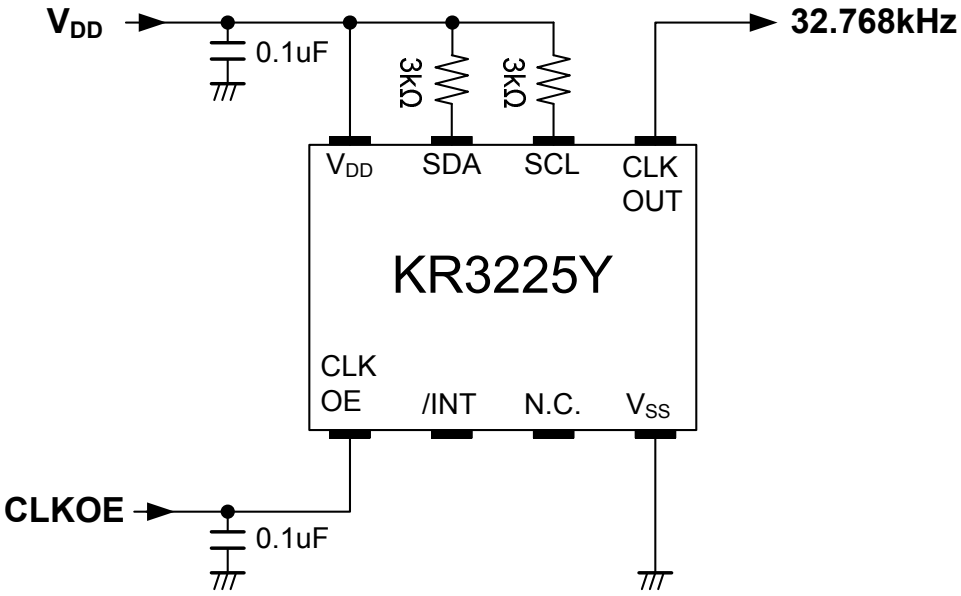
10.Connection with Typical Microcontroller



SCL and SDA are both connected to the V_{DD} line via a pull-up resistance.

All ports connected to the I2C bus must be open drain in order to enable AND connections to multiple devices.

11. 32kHz - TCXO Circuit



12. Notes

1. Specifications described in this manual are for references. Products specifications shall be based on written documents agreed by each party.

2. Contents in this manual are subject to change without notice.
   It is recommended to confirm the latest information at the time of usage.

3. Products in this manual are intended to be used in general electronic equipment such as office equipment, audio and visual equipment, communications equipment, measurement instruments and home appliances. We strongly recommend that the user consult with our sales representatives in advance upon planning to use our products in applications which require extremely high quality and reliability; such as aircraft and aerospace equipment, traffic systems, safety systems, power plant and medical equipment including life maintenance systems.

4. Even though we strive for improvements in the quality and reliability of products, we request that the user provision their design with enough safety margin in the equipment or systems in order not to threaten human lives directly, cause bodily harm or property damage by accidental result of product operation.

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