

1.35V DDR3L SDRAM SODIMM

MT4KTF12864HZ – 1GB

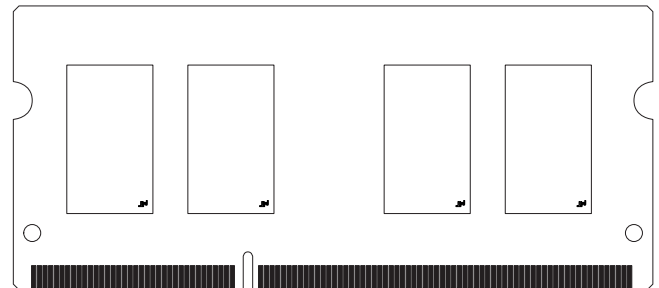
MT4KTF25664HZ – 2GB

Features

- DDR3L functionality and operations supported as defined in the component data sheet
- 204-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-14900, PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 1GB (128 Meg x 64), 2GB (256 Meg x 64)
- $V_{DD} = 1.35V$ (1.283–1.45V)
- $V_{DD} = 1.5V$ (1.425–1.575V)
- Backward-compatible to $V_{DD} = 1.5V \pm 0.075V$
- $V_{DDSPD} = 3.0\text{--}3.6V$
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single-rank
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 204-Pin SODIMM (MO-268 R/C C)

Module height: 30mm (1.18in)



Options

- Operating temperature¹
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
- Package
 - 204-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 1.07ns @ CL = 13 (DDR3-1866)
 - 1.25ns @ CL = 11 (DDR3-1600)
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.87ns @ CL = 7 (DDR3-1066)

Marking

None
Z
-1G9
-1G6
-1G4
-1G1

Note: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 13	CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G9	PC3-14900	1866	1600	1333	1333	1066	1066	800	667	13.125	13.125	47.125
-1G6	PC3-12800	–	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	–	800	667	15	15	52.5



Table 2: Addressing

Parameter	1GB	2GB
Refresh count	8K	8K
Row address	16K A[13:0]	32K A[14:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	2Gb (128 Meg x 16)	4Gb (256 Meg x 16)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	1 S0#	1 S0#

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT41K128M16,¹ 2Gb DDR3L SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT4KTF12864HZ-1G6__	1GB	128 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT4KTF12864HZ-1G4__	1GB	128 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT4KTF12864HZ-1G1__	1GB	128 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41K256M16,¹ 4Gb DDR3L SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT4KTF25664HZ-1G9__	2GB	256 Meg x 64	14.9 GB/s	1.07ns/1866 MT/s	13-13-13
MT4KTF25664HZ-1G6__	2GB	256 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT4KTF25664HZ-1G4__	2GB	256 Meg x 64	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT4KTF25664HZ-1G1__	2GB	256 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

- Notes: 1. The data sheet for the base device can be found on Micron’s Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT4KTF25664HZ-1G6E1.



Pin Assignments

Table 5: Pin Assignments

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{REFDQ}	53	DQ19	105	V _{DD}	157	DQ42	2	V _{SS}	54	V _{SS}	106	V _{DD}	158	DQ46
3	V _{SS}	55	V _{SS}	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V _{SS}	6	DQ5	58	DQ29	110	RAS#	162	V _{SS}
7	DQ1	59	DQ25	111	V _{DD}	163	DQ48	8	V _{SS}	60	V _{SS}	112	V _{DD}	164	DQ52
9	V _{SS}	61	V _{SS}	113	WE#	165	DQ49	10	DQ50#	62	DQ3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	V _{SS}	12	DQ50	64	DQ3	116	ODT0	168	V _{SS}
13	V _{SS}	65	V _{SS}	117	V _{DD}	169	DQS6#	14	V _{SS}	66	V _{SS}	118	V _{DD}	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	NC	172	V _{SS}
17	DQ3	69	DQ27	121	NC	173	V _{SS}	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V _{SS}	71	V _{SS}	123	V _{DD}	175	DQ50	20	V _{SS}	72	V _{SS}	124	V _{DD}	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	NC	126	V _{REFCA}	178	V _{SS}
23	DQ9	75	V _{DD}	127	V _{SS}	179	V _{SS}	24	DQ13	76	V _{DD}	128	V _{SS}	180	DQ60
25	V _{SS}	77	NC	129	DQ32	181	DQ56	26	V _{SS}	78	NC	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	NF/A14 ¹	132	DQ37	184	V _{SS}
29	DQS1	81	V _{DD}	133	V _{SS}	185	V _{SS}	30	RESET#	82	V _{DD}	134	V _{SS}	186	DQS7#
31	V _{SS}	83	A12	135	DQS4#	187	DM7	32	V _{SS}	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V _{SS}	34	DQ14	86	A7	138	V _{SS}	190	V _{SS}
35	DQ11	87	V _{DD}	139	V _{SS}	191	DQ58	36	DQ15	88	V _{DD}	140	DQ38	192	DQ62
37	V _{SS}	89	A8	141	DQ34	193	DQ59	38	V _{SS}	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V _{SS}	40	DQ20	92	A4	144	V _{SS}	196	V _{SS}
41	DQ17	93	V _{DD}	145	V _{SS}	197	SA0	42	DQ21	94	V _{DD}	146	DQ44	198	EVENT#
43	V _{SS}	95	A3	147	DQ40	199	V _{DDSPD}	44	V _{SS}	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V _{SS}	202	SCL
47	DQS2	99	V _{DD}	151	V _{SS}	203	V _{TT}	48	V _{SS}	100	V _{DD}	152	DQS5#	204	V _{TT}
49	V _{SS}	101	CK0	153	DM5	-	-	50	DQ22	102	CK1	154	DQS5	-	-
51	DQ18	103	CK0#	155	V _{SS}	-	-	52	DQ23	104	CK1#	156	V _{SS}	-	-

Note: 1. Pin 80 is NF for 1GB; A14 for 2GB.

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 6: Pin Descriptions

Symbol	Type	Description
Ax	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information.
BAx	Input	Bank address inputs: Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	Clock: Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	Clock enable: Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	Data mask (x8 devices only): DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	On-die termination: Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	Parity input: Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	Reset: RESET# is an active LOW asynchronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	Chip select: Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I ² C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I ² C bus.
CBx	I/O	Check bits: Used for system error detection and correction.
DQx	I/O	Data input/output: Bidirectional data bus.
DQSx, DQSx#	I/O	Data strobe: Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	Serial data: Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I ² C bus.
TDQSx, TDQSx#	Output	Redundant data strobe (x8 devices only): TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	Parity error output: Parity error found on the command and address bus.
EVENT#	Output (open drain)	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V _{DD}	Supply	Power supply: 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component V _{DD} and V _{DDQ} are connected to the module V _{DD} .
V _{DDSPD}	Supply	Temperature sensor/SPD EEPROM power supply: 3.0–3.6V.
V _{REFCA}	Supply	Reference voltage: Control, command, and address V _{DD} /2.
V _{REFDQ}	Supply	Reference voltage: DQ, DM V _{DD} /2.
V _{SS}	Supply	Ground.
V _{TT}	Supply	Termination voltage: Used for control, command, and address V _{DD} /2.
NC	–	No connect: These pins are not connected on the module.
NF	–	No function: These pins are connected within the module, but provide no functionality.



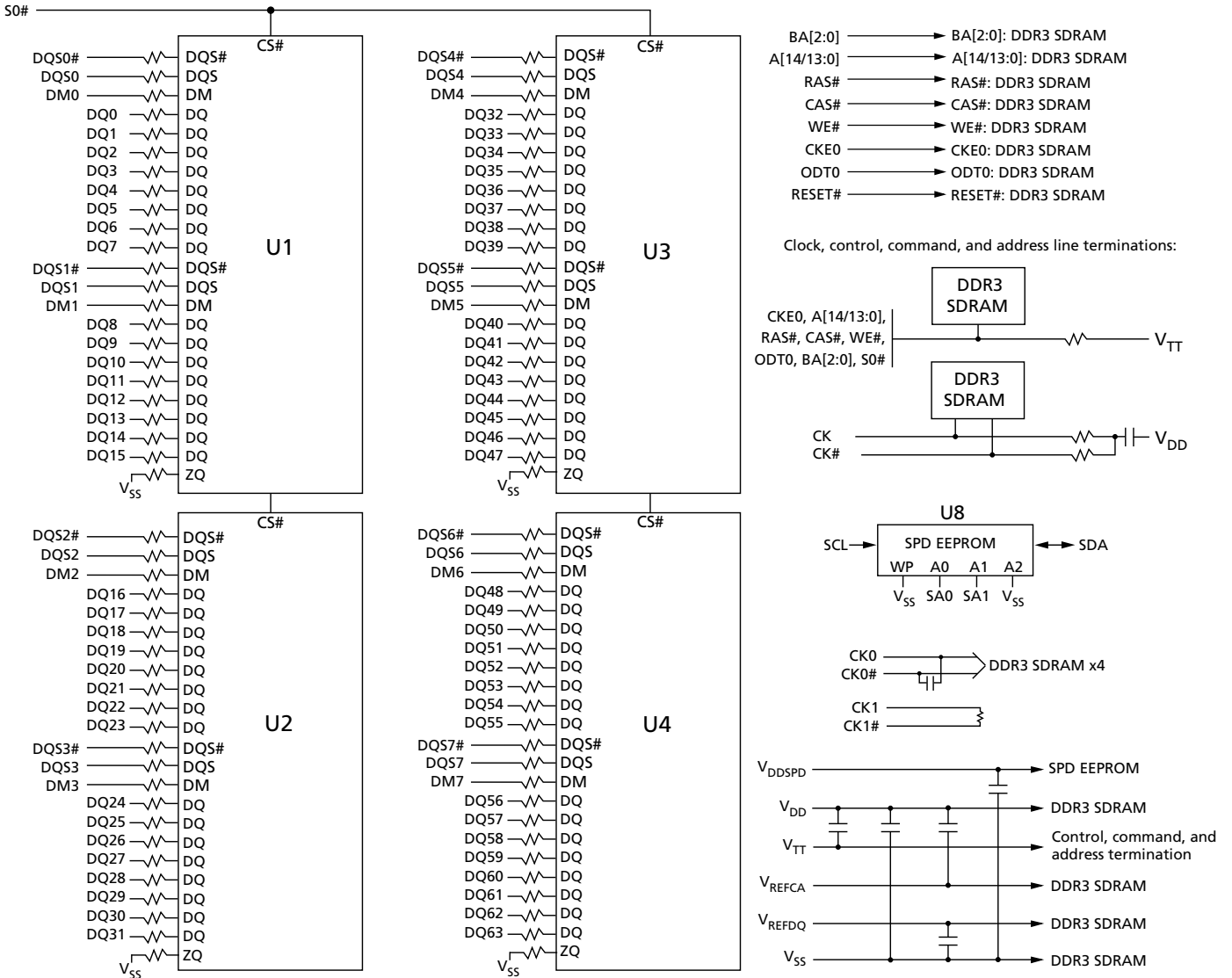
DQ Map

Table 7: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	10	33	U2	0	26	67
	1	13	24		1	29	58
	2	11	35		2	27	69
	3	12	22		3	24	57
	4	14	34		4	30	68
	5	8	21		5	28	56
	6	15	36		6	31	70
	7	9	23		7	25	59
	8	4	4		8	16	39
	9	2	15		9	22	50
	10	0	5		10	20	40
	11	6	16		11	23	52
	12	1	7		12	21	42
	13	3	17		13	18	51
	14	5	6		14	17	41
15	7	18	15	19	53		
U3	0	38	140	U4	0	50	175
	1	37	132		1	53	166
	2	39	142		2	55	176
	3	33	131		3	49	165
	4	34	141		4	54	174
	5	32	129		5	48	163
	6	35	143		6	51	177
	7	36	130		7	52	164
	8	41	149		8	57	183
	9	47	160		9	62	192
	10	44	146		10	56	181
	11	43	159		11	59	193
	12	45	148		12	61	182
	13	42	157		13	58	191
	14	40	147		14	60	180
15	46	158	15	63	194		

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	-0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	1.975	V

Table 9: Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes	
V_{DD}	V_{DD} supply voltage	1.283	1.35	1.45	V		
		1.425	1.5	1.575	V	1	
$V_{REFCA(DC)}$	Input reference voltage command/address bus	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V		
$V_{REFDQ(DC)}$	I/O reference voltage DQ bus	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V		
I_{VTT}	Termination reference current from V_{TT}	-600	-	600	mA		
V_{TT}	Termination reference voltage (DC) – command/address bus	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V	2	
I_I	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; V_{REF} input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	-8	0	8	μA	
		DM	-2	0	2		
I_{OZ}	Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	-5	0	5	μA	
I_{VREF}	V_{REF} supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)		-4	0	4	μA	
T_A	Module ambient operating temperature	Commercial	0	-	70	$^{\circ}\text{C}$	3, 4
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	-	95	$^{\circ}\text{C}$	3, 4, 5

- Notes:
- Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.
 - V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
 - T_A and T_C are simultaneous requirements.
 - For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
 - The refresh rate is required to double when $85^{\circ}\text{C} < T_C \leq 95^{\circ}\text{C}$.



DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's web site. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G1	-093
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.



I_{DD} Specifications

Table 11: DDR3 I_{DD} Specifications and Conditions – 1GB (Die Revision K)

Values are for the MT41K128M16 DDR3L SDRAM only and are computed from values specified in the 2Gb 1.35V (128 Meg x 16) component data sheet

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I _{DD0}	184	180	172	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRE-CHARGE	I _{DD1}	260	252	232	mA
Precharge power-down current: Slow exit	I _{DD2P0}	48	48	48	mA
Precharge power-down current: Fast exit	I _{DD2P1}	56	56	56	mA
Precharge quiet standby current	I _{DD2Q}	80	80	80	mA
Precharge standby current	I _{DD2N}	84	84	84	mA
Precharge standby ODT current	I _{DD2NT}	136	132	120	mA
Active power-down current	I _{DD3P}	84	84	84	mA
Active standby current	I _{DD3N}	136	132	120	mA
Burst read operating current	I _{DD4R}	512	432	352	mA
Burst write operating current	I _{DD4W}	552	476	396	mA
Refresh current	I _{DD5B}	720	716	708	mA
Self refresh temperature current: MAX T _C = 85°C	I _{DD6}	48	48	48	mA
Self refresh temperature current (SRT-enabled): MAX T _C = 95°C	I _{DD6ET}	60	60	60	mA
All banks interleaved read current	I _{DD7}	780	688	608	mA
Reset current	I _{DD8}	56	56	56	mA



Table 12: DDR3 I_{DD} Specifications and Conditions – 2GB (Die Revision E)

Values are for the MT41K256M16 DDR3L SDRAM only and are computed from values specified in the 4Gb 1.35V (256 Meg x 16) component data sheet

Parameter	Symbol	1866	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I _{DD0}	292	264	232	220	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I _{DD1}	364	348	336	320	mA
Precharge power-down current: Slow exit	I _{DD2P0}	64	64	64	64	mA
Precharge power-down current: Fast exit	I _{DD2P1}	148	128	112	104	mA
Precharge quiet standby current	I _{DD2Q}	120	108	100	88	mA
Precharge standby current	I _{DD2N}	124	112	100	96	mA
Precharge standby ODT current	I _{DD2NT}	160	148	136	120	mA
Active power-down current	I _{DD3P}	164	152	140	128	mA
Active standby current	I _{DD3N}	196	188	180	164	mA
Burst read operating current	I _{DD4R}	1008	940	808	740	mA
Burst write operating current	I _{DD4W}	760	684	608	548	mA
Refresh current	I _{DD5B}	968	940	912	896	mA
Self refresh temperature current: MAX T _C = 85°C	I _{DD6}	80	80	80	80	mA
Self refresh temperature current (SRT-enabled): MAX T _C = 95°C	I _{DD6ET}	100	100	100	100	mA
All banks interleaved read current	I _{DD7}	1096	972	868	792	mA
Reset current	I _{DD8}	72	72	72	72	mA



Serial Presence-Detect EEPROM

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 13: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	-0.45	$V_{DDSPD} \times 0.3$	V
Input high voltage: Logic 1; All inputs	V_{IH}	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 1.0$	V
Output low voltage: $I_{OUT} = 3\text{mA}$	V_{OL}	-	0.4	V
Input leakage current: $V_{IN} = \text{GND to } V_{DD}$	I_{LI}	0.1	2.0	μA
Output leakage current: $V_{OUT} = \text{GND to } V_{DD}$	I_{LO}	0.05	2.0	μA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	t_{SCL}	10	400	kHz	
Clock pulse width HIGH time	t_{HIGH}	0.6	-	μs	
Clock pulse width LOW time	t_{LOW}	1.3	-	μs	
SDA rise time	t_R	-	300	μs	1
SDA fall time	t_F	20	300	ns	1
Data-in setup time	$t_{SU:DAT}$	100	-	ns	
Data-in hold time	$t_{HD:DI}$	0	-	μs	
Data-out hold time	$t_{HD:DAT}$	200	900	ns	
Data out access time from SCL LOW	$t_{AA:DAT}$	0.2	0.9	μs	2
Start condition setup time	$t_{SU:STA}$	0.6	-	μs	3
Start condition hold time	$t_{HD:STA}$	0.6	-	μs	
Stop condition setup time	$t_{SU:STO}$	0.6	-	μs	
Time the bus must be free before a new transition can start	t_{BUF}	1.3	-	μs	
WRITE time	t_W	-	10	ms	

- Notes:
1. Guaranteed by design and characterization, not necessarily tested.
 2. To avoid spurious start and stop conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.
 3. For a restart condition, or following a WRITE cycle.

