

500-mA Sub-Miniature Step-Down DC-DC Converter

Check for Samples: [LM2619](#)

FEATURES

- Sub-Miniature 10-Bump Thin DSBGA Package
- Uses Small Ceramic Capacitors
- 5-mV (Typical) PWM Mode Output Voltage Ripple ($C_{OUT} = 22 \mu\text{F}$)
- Internal Soft Start
- Current Overload Protection
- Thermal Shutdown
- External Compensation

KEY SPECIFICATIONS

- Operates from a single Li-ion cell : 2.8V to 5.5V
- Output voltage : 1.5V to 3.6V
- DC feedback voltage precision: $\pm 1\%$
- Maximum Load Capability: 500mA
- PWM Mode Quiescent Current: 600 μA typ
- Shutdown Current: 0.02 μA typ
- PWM switching frequency: 600kHz
- SYNC input for PWM mode frequency synchronization from 0.5MHz to 1MHz
- High efficiency (96% typical at 3.9 V_{IN} , 3.6 V_{OUT} and 200 mA) in PWM mode from internal synchronous rectification
- 100% Maximum Duty Cycle for Lowest Dropout

DESCRIPTION

The LM2619 step down DC-DC converter is optimized for powering circuits from a single lithium-ion cell. It steps down an input voltage of 2.8V to 5.5V to an output of 1.5V to 3.6V at up to 500mA. Output voltage is set using resistor feedback dividers.

The device offers three modes for mobile phones and similar portable applications. Fixed-frequency PWM mode minimizes RF interference. A SYNC input allows synchronizing the switching frequency in a range of 500 kHz to 1 MHz. Low-current hysteretic PFM mode reduces quiescent current to 160 μA (typical). Shutdown mode turns the device off and reduces battery consumption to 0.02 μA (typical).

Current limit and thermal shutdown features protect the device and system during fault conditions.

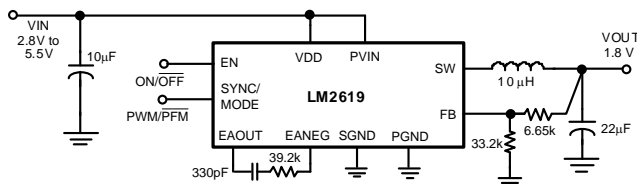
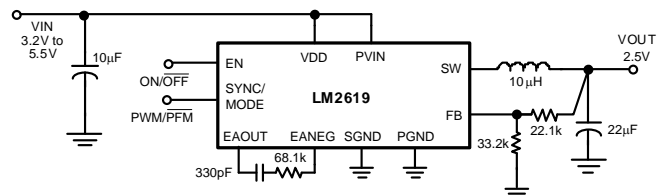
The LM2619 is available in a 10-bump DSBGA package. This packaging uses chip-scale DSBGA technology and offers the smallest possible size. A high switching frequency (600 kHz) allows use of tiny surface-mount components.

The device features external compensation to tailor the response to a wide range of operating conditions.

APPLICATIONS

- Mobile Phones
- Hand-Held Radios
- RF PC Cards
- Wireless LAN Cards

Typical Application Circuits


Figure 1. Typical Circuit for 1.8-V Output Voltage

Figure 2. Typical Circuit for 2.5-V Output Voltage


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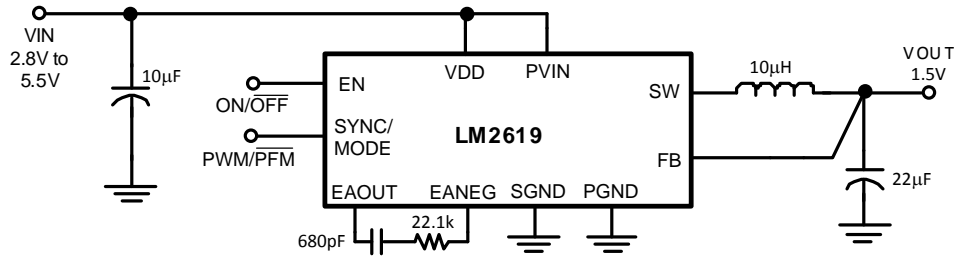


Figure 3. Typical Circuit for 1.5-V Output Voltage

Connection Diagrams

10-Bump DSBGA Package

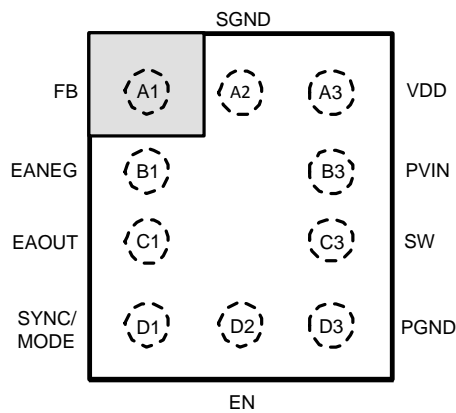


Figure 4. YPA Package Top View

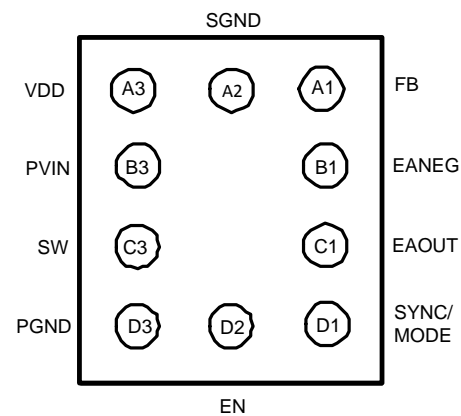


Figure 5. YPA Package Bottom View

Pin Functions

Table 1. Pin Description

Pin No.	Pin Name	Function
A1	FB	Feedback Analog Input.
B1	EANEG	Inverting input of error amplifier.
C1	EAOUT	Output of error amplifier.
D1	SYNC/MODE	Synchronization Input. Use this digital input for frequency selection or modulation control. Set: SYNC/MODE = high for low-noise 600kHz PWM mode SYNC/MODE = low for low-current PFM mode SYNC/MODE = a 500kHz–1MHz external clock for synchronization in PWM mode. (See OPERATING MODE SELECTION and FREQUENCY SYNCHRONIZATION in Device Information.)
D2	EN	Enable Input. Set this Schmitt trigger digital input high for normal operation. For shutdown, set low. Set EN low during system power-up and other low supply voltage conditions. (See SHUTDOWN MODE in Device Information.)
D3	PGND	Power Ground.
C3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the max Switch Peak Current Limit of the LM2619.
B3	PVIN	Power Supply Voltage Input to the internal PFET switch. Connect to the input filter capacitor.
A3	VDD	Analog Supply Input. If board layout is not optimum, an optional 0.1µF ceramic capacitor is suggested.
A2	SGND	Analog and Control Ground.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

PVIN, VDD to SGND	-0.2V to +6V
PGND to SGND, PVIN to VDD	-0.2V to +0.2V
EN, EAOUT, EANEG, SYNC/MODE to SGND	-0.2V to +6V
FB, SW	(GND -0.2V) to (VDD +0.2V)
Storage temperature range	-45°C to +150°C
Lead temperature (soldering, 10 sec.)	260°C
Junction temperature ⁽²⁾	-25°C to +125°C
Minimum ESD rating (Human Body Model, C = 100 pF, R = 1.5 kΩ)	±2 kV
Thermal resistance (θ_{JA}) ⁽³⁾	140°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. For specifications and associated test conditions, see the Min and Max limits and Conditions in the Electrical Characteristics table. Typical (typ) specifications are mean or average values at 25°C.
- (2) Thermal shutdown will occur if the junction temperature exceeds 150°C.
- (3) Thermal resistance specified with 2 layer PCB (0.5/0.5 oz. cu).

Electrical Characteristics

Specifications with standard typeface are for $T_A = T_J = 25^\circ\text{C}$, and those in **boldface type** apply over the full **Operating Temperature Range** of $T_A = T_J = -25^\circ\text{C}$ to $+85^\circ\text{C}$. Unless otherwise specified, $PVIN = VDD = EN = SYNC/MODE = 3.6\text{V}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	$PVIN = VDD = V_{IN}^{(1)}$	2.8	3.6	5.5	V
V_{FB}	Feedback voltage		1.485	1.50	1.515	V
V_{HYST}	PFM comparator hysteresis voltage	PFM Mode (SYNC/MODE = 0V) ⁽²⁾		24		mV
I_{SHDN}	Shutdown supply current	$VIN = 3.6\text{V}$, EN = 0V		0.02	3	μA
I_{Q1_PWM}	DC bias current into VDD	SYNC/MODE = VIN, FB = 2V		600	725	μA
I_{Q2_PFM}		SYNC/MODE = 0V, FB = 2V		160	195	μA
$R_{DSON (P)}$	Pin-pin resistance for PFET			395	550	mΩ
$R_{DSON (N)}$	Pin-pin resistance for NFET			330	500	mΩ
$R_{DSON (TC)}$	FET resistance temperature coefficient			0.5		%/C
I_{LIM}	Switch peak current limit ⁽³⁾		620	810	1100	mA
V_{IH}	Logic high input, EN, SYNC/MODE			0.95	1.3	V
V_{IL}	Logic low input, EN, SYNC/MODE		0.4	0.80		V
F_{SYNC}	SYNC/MODE clock frequency range	⁽⁴⁾	500		1000	kHz
F_{OSC}	Internal oscillator frequency	PWM Mode	468	600	732	kHz
T_{min}	Minimum on-time of PFET switch in PWM mode			200		ns

- (1) The LM2619 is designed for mobile phone applications where turn-on after system power-up is controlled by the system controller. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.8V.
- (2) The hysteresis voltage is the minimum voltage swing on the FB pin that causes the internal feedback and control circuitry to turn the internal PFET switch on and then off during PFM mode. When resistor dividers are used like in the operating circuit of [Figure 20](#), the hysteresis at the output will be the value of the hysteresis at the feedback pin times the resistor divider ratio. In this case, 24mV (typ) x ((46.4k + 33.2k)/33.2k).
- (3) Current limit is built-in, fixed, and not adjustable. If the current limit is reached while the voltage at the FB pin is pulled below 0.7V, the internal PFET switch turns off for 2.5μs to allow the inductor current to diminish.
- (4) SYNC driven with an external clock switching between V_{IN} and GND. When an external clock is present at SYNC; the IC is forced to be in PWM mode at the external clock frequency. The LM2619 synchronizes to the rising edge of the external clock.

Typical Performance Characteristics

LM2619ATL, Circuit of Figure 3, $V_{IN} = 3.6V$, $T_A = 25^\circ C$, unless otherwise noted.

Quiescent Supply Current vs Supply Voltage

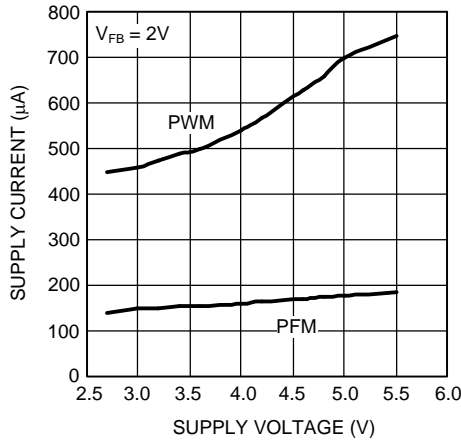


Figure 6.

Shutdown Quiescent Current vs Temperature (Circuit in Figure 3)

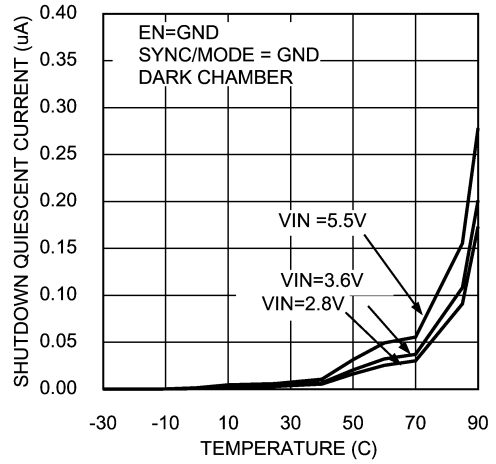


Figure 7.

Output Voltage vs Supply Voltage ($V_{OUT} = 1.5V$, PWM MODE)

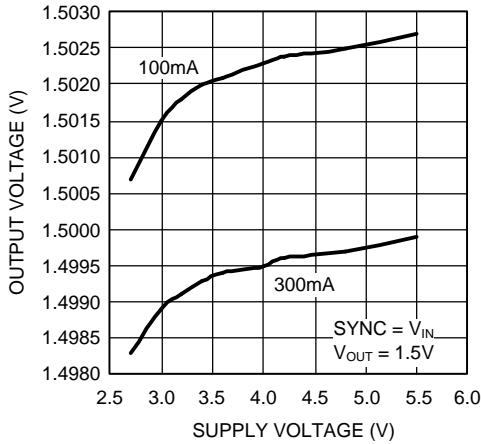


Figure 8.

Output Voltage vs Supply Voltage ($V_{OUT} = 1.5V$, PFM MODE)

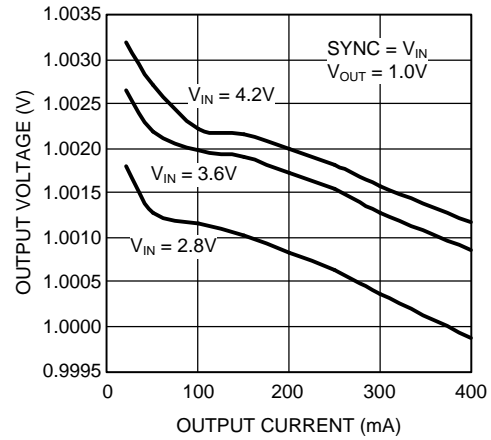


Figure 9.

Output Voltage vs Output Current ($V_{OUT} = 1.5V$, PWM MODE)

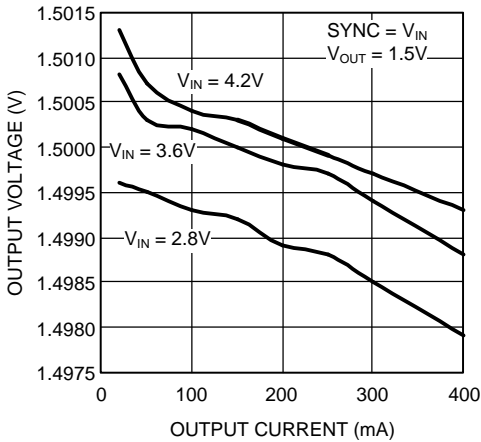


Figure 10.

Output Voltage vs Output Current ($V_{OUT} = 1.5V$, PFM MODE)

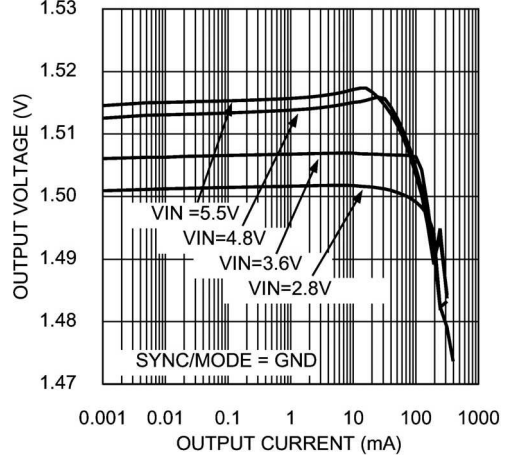


Figure 11.

Typical Performance Characteristics (continued)

LM2619ATL, Circuit of Figure 3, $V_{IN} = 3.6V$, $T_A = 25^\circ C$, unless otherwise noted.

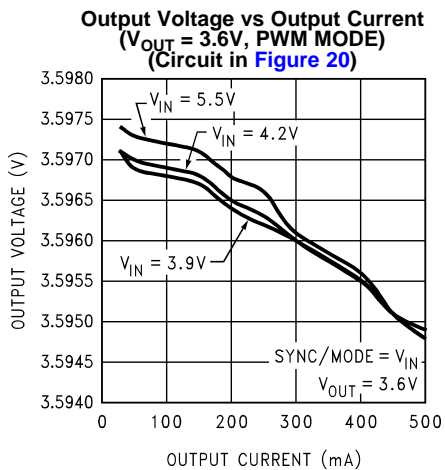


Figure 12.

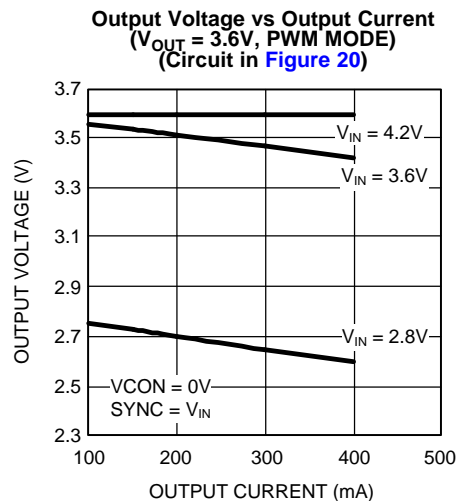


Figure 13.

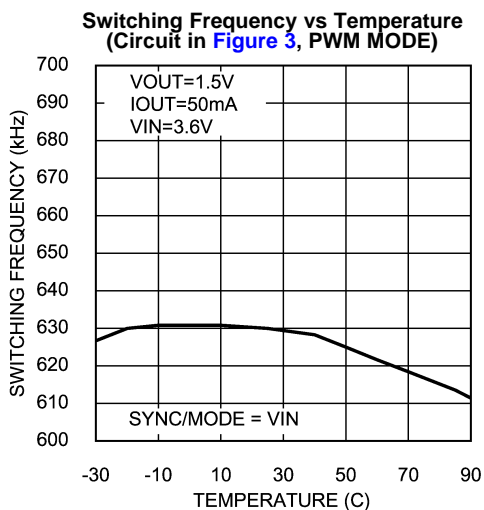


Figure 14.

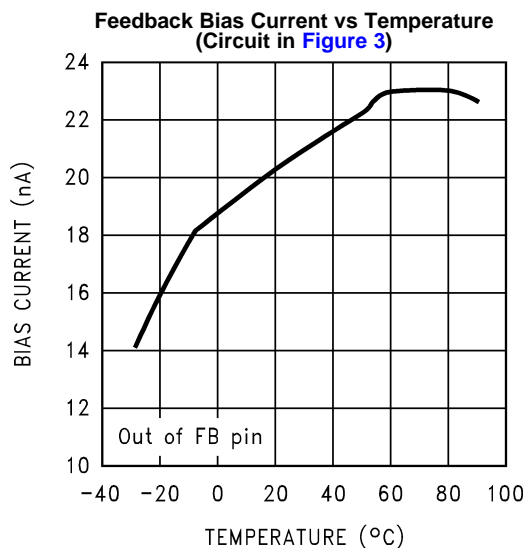


Figure 15.

Typical Performance Characteristics (continued)

LM2619ATL, Circuit of Figure 3, $V_{IN} = 3.6V$, $T_A = 25^\circ C$, unless otherwise noted.

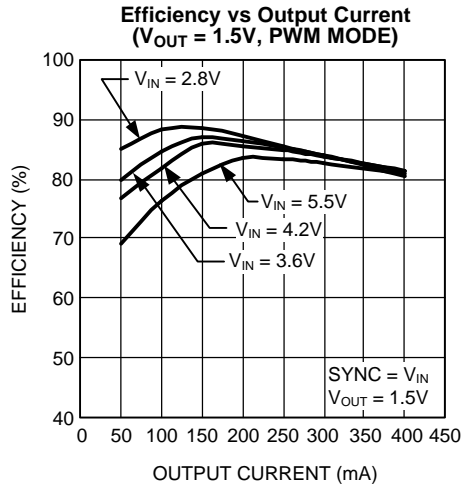


Figure 16.

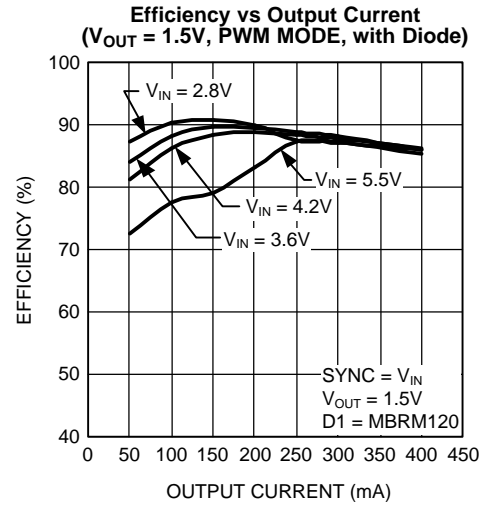


Figure 17.

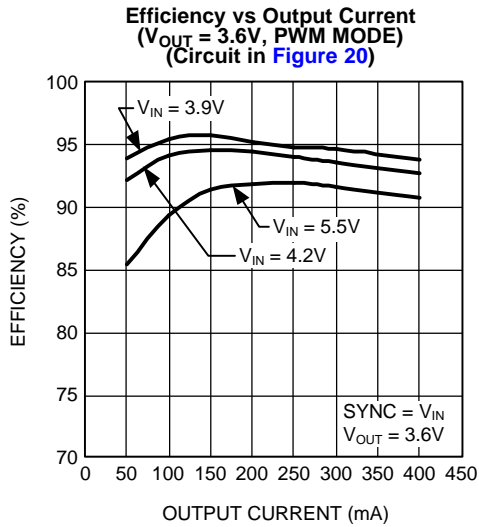


Figure 18.

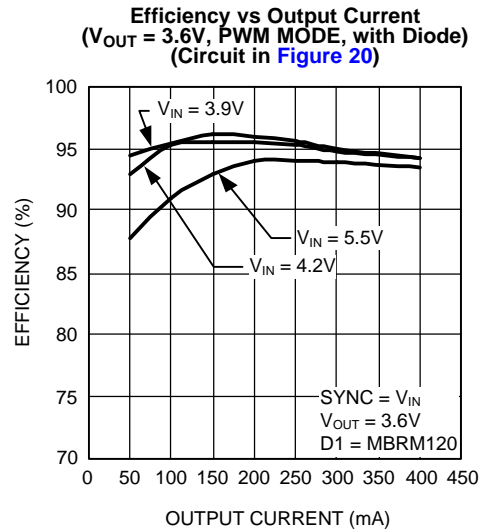


Figure 19.

DEVICE INFORMATION

The LM2619 is a simple, step-down DC-DC converter optimized for powering circuits in mobile phones, portable communicators, and similar battery powered RF devices. It is based on a current-mode buck architecture, with synchronous rectification in PWM mode for high efficiency. It is designed for a maximum load capability of 500mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

The device has all three of the pin-selectable operating modes required for powering circuits in mobile phones and other sophisticated portable devices with complex power management needs. Fixed-frequency PWM operation offers full output current capability at high efficiency while minimizing interference with sensitive IF and data acquisition circuits. During standby operation, hysteretic PFM mode reduces quiescent current to 160µA typ. to maximize battery life. Shutdown mode turns the device off and reduces battery consumption to 0.02µA (typ).

DC PWM mode feedback voltage precision is ±1%. Efficiency is typically 96% for a 200mA load with 3.6V output, 3.9V input. The efficiency can be further increased by using a schottky diode like MBRM120L as shown in [Figure 20](#). PWM mode quiescent current is 600µA typ. The output voltage can be set from 1.5V to 3.6V by using external feedback resistors.

Additional features include soft-start, current overload protection, over voltage protection and thermal shutdown protection.

The LM2619 is constructed using a chip-scale 10-pin thin DSBGA package. This package offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (600kHz) reduces the size of external components. Board area required for implementation is only 0.58in²(375mm²).

Use of a DSBGA package requires special design considerations for implementation. (See [DSBGA PACKAGE ASSEMBLY AND USE](#) in [Application Information](#).) Its fine bump-pitch requires careful board design and precision assembly equipment.

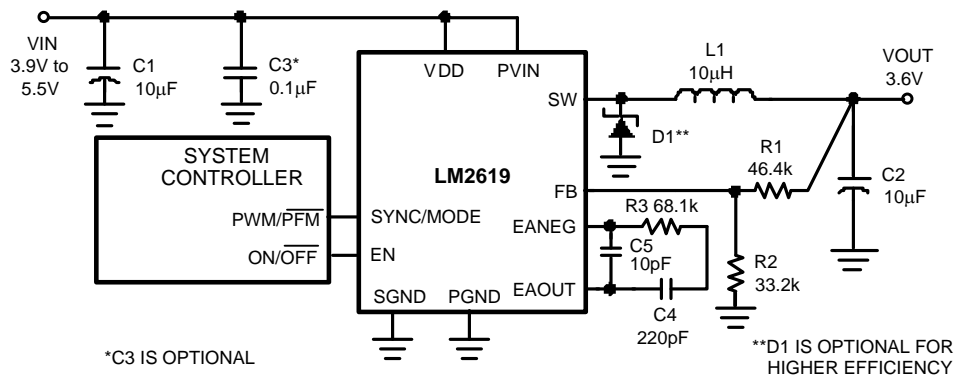


Figure 20. Typical Operating Circuit for 3.6V Output Voltage

CIRCUIT OPERATION

Referring to [Figure 20](#), [Figure 21](#), [Figure 22](#), and [Figure 23](#), the LM2619 operates as follows. During the first part of each switching cycle, the control block in the LM2619 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN}-V_{OUT})/L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope of V_{OUT}/L . If the inductor current reaches zero before the next cycle, the synchronous rectifier is turned off to prevent current reversal. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

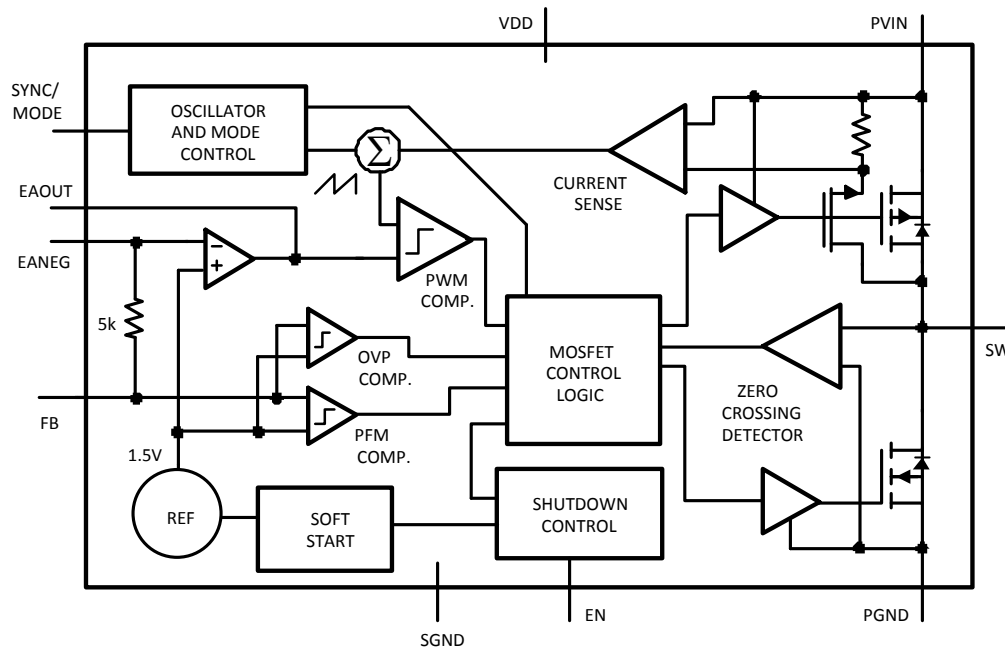
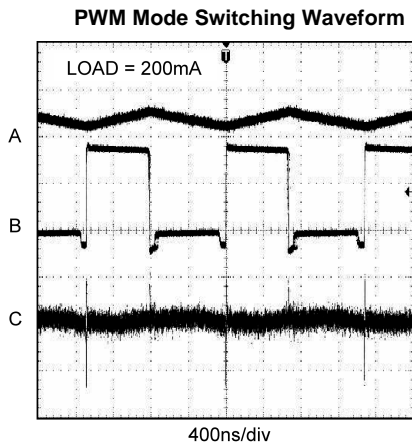


Figure 21. Simplified Functional Diagram

PWM OPERATION

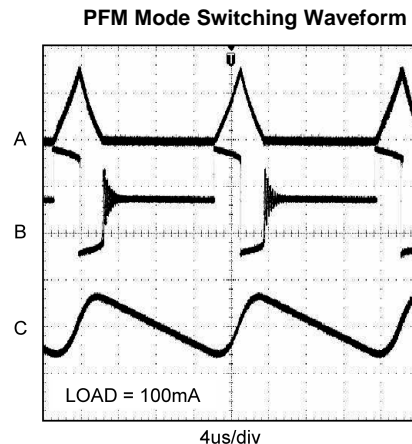
While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse-width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output voltage down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load.

Before going to the PWM comparator, the error signal is summed with a slope compensation ramp from the oscillator for stability of the current feedback loop. During the second part of the cycle, a zero crossing detector turns off the NFET synchronous rectifier if the inductor current ramps to zero. The minimum on time of the PFET in PWM mode is about 200ns.



A: Inductor Current, 500mA/div
B: SW Pin, 2V/div
C: V_{OUT} , 10mV/div, AC Coupled

Figure 22.



A: Inductor Current, 500mA/div
B: SW Pin, 2V/div
C: V_{OUT} , 50mV/div, AC Coupled

Figure 23.

PFM OPERATION

Connecting the SYNC/MODE to SGND sets the LM2619 to hysteretic PFM operation. While in PFM (Pulse Frequency Modulation) mode, the output voltage is regulated by switching with a discrete energy per cycle and then modulating the cycle rate, or frequency, to control power to the load. This is done by using an error comparator to sense the output voltage. The device waits as the load discharges the output filter capacitor, until the output voltage drops below the lower threshold of the PFM error-comparator. Then the device initiates a cycle by turning on the PFET switch. This allows current to flow from the input, through the inductor to the output, charging the output filter capacitor. The PFET is turned off when the output voltage rises above the regulation threshold of the PFM error comparator. Thus, the output voltage ripple in PFM mode is proportional to the hysteresis of the error comparator.

In PFM mode, the device only switches as needed to service the load. This lowers current consumption by reducing power consumed during the switching action in the circuit, due to transition losses in the internal MOSFETs, gate drive currents, eddy current losses in the inductor, etc. It also improves light-load voltage regulation. During the second half of the cycle, the intrinsic body diode of the NFET synchronous rectifier conducts until the inductor current ramps to zero.

OPERATING MODE SELECTION

The LM2619 is designed for digital control of the operating modes by the system controller. This prevents the spurious switch over from low-noise PWM mode between transmission intervals in mobile phone applications that can occur in other products.

The SYNC/MODE digital input pin is used to select the operating mode. Setting SYNC/MODE high (above 1.3V) selects 600kHz current-mode PWM operation. PWM mode is optimized for low-noise, high-power operation for use when the load is active. Setting SYNC/MODE low (below 0.4V) selects hysteretic voltage-mode PFM operation. PFM mode is optimized for reducing power consumption and extending battery life when the load is in a low-power standby mode. In PFM mode, quiescent current into the V_{DD} pin is 160 μ A typ. In contrast, PWM mode V_{DD} -pin quiescent current is 600 μ A typ.

PWM operation is intended for use with loads of 50mA or more, when low noise operation is desired. Below 100mA, PFM operation can be used to allow precise regulation, and reduced current consumption. The LM2619 has an over-voltage feature that prevents the output voltage from rising too high, when the device is left in PWM mode under low-load conditions. See *Overvoltage Protection*, for more information.

Switch modes with the SYNC/MODE pin, using a signal with a slew rate faster than 5V/100 μ s. Use a comparator, Schmitt trigger or logic gate to drive the SYNC/MODE pin. Do not leave the pin floating or allow it to linger between thresholds. These measures will prevent output voltage errors in response to an indeterminate logic state. The LM2619 switches on each rising edge of SYNC. Ensure a minimum load to keep the output voltage in regulation when switching modes frequently.

FREQUENCY SYNCHRONIZATION

The SYNC/MODE input can also be used for frequency synchronization. During synchronization, the LM2619 initiates cycles on the rising edge of the clock. When synchronized to an external clock, it operates in PWM mode. The device can synchronize to a 50% duty-cycle clock over frequencies from 500kHz to 1MHz. If a different duty cycle is used other than 50% the range for acceptable duty cycles is 30% to 70%.

Use the following waveform and duty cycle guidelines when applying an external clock to the SYNC/MODE pin. Clock under/overshoot should be less than 100mV below GND or above V_{DD} . When applying noisy clock signals, especially sharp edged signals from a long cable during evaluation, terminate the cable at its characteristic impedance and add an RC filter to the SYNC pin, if necessary, to soften the slew rate and over/undershoot. Note that sharp edged signals from a pulse or function generator can develop under/overshoot as high as 10V at the end of an improperly terminated cable.

OVERVOLTAGE PROTECTION

The LM2619 has an over-voltage comparator that prevents the output voltage from rising too high when the device is left in PWM mode under low-load conditions. When the output voltage rises by about 100mV (Figure 3) over its regulation threshold, the OVP comparator inhibits PWM operation to skip pulses until the output voltage returns to the regulation threshold. When resistor dividers are used the OVP threshold at the output will be the value of the threshold at the feedback pin times the resistor divider ratio. In over voltage protection, output voltage and ripple will increase.

SHUTDOWN MODE

Setting the EN digital input pin low (<0.4V) places the LM2619 in a 0.02 μ A (typ) shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference, control and bias circuitry of the LM2619 are turned off. Setting EN high enables normal operation. While turning on, soft start is activated.

EN should be set low to turn off the LM2619 during system power-up and undervoltage conditions when the supply is less than the 2.8V minimum operating voltage. The LM2619 is designed for compact portable applications, such as mobile phones. In such applications, the system controller determines power supply sequencing. Although the LM2619 is typically well behaved at low input voltages, this is not specified.

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the LM2619 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

The internal NFET synchronous rectifier is turned on during the inductor current down slope during the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle, or when the inductor current ramps to zero at light loads. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

CURRENT LIMITING

A current limit feature allows the LM2619 to protect itself and external components during overload conditions. In PWM mode cycle-by-cycle current limit is normally used. If an excessive load pulls the voltage at the feedback pin down to approximately 0.7V, then the device switches to a timed current limit mode. In timed current limit mode the internal P-FET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 2.5 μ s to force the instantaneous inductor current to ramp down to a safe value. Timed current limit mode prevents the loss of current control seen in some products when the voltage at the feedback pin is pulled low in serious overload conditions.

DROPOUT CONSIDERATIONS

The LM2619 can be used to provide fixed output voltages by using external feedback resistors. The output voltage can be set from 1.5V to 3.6V. The internal reference voltage for the error amplifier is 1.5V. In cases where the output voltage is set higher than 2.5V, the part will go into dropout or 100% duty cycle when the input voltage gets close to the set output voltage. Near dropout the on time of the P-FET may exceed one PWM clock cycle and cause higher ripple on the output for load currents greater than 450mA. This increased ripple will exist for a narrow range of input voltages close to the 100% duty cycle and once the input voltage goes down further the P-FET will be fully on. See [SETTING THE OUTPUT VOLTAGE](#) in [Application Information](#) for further details.

In dropout conditions the output voltage is $V_{IN} - I_{OUT} (R_{dc} + R_{DS(on) (P)})$ where R_{dc} is the series resistance of the inductor and $R_{DS(on) (P)}$ is the on resistance of the PFET.

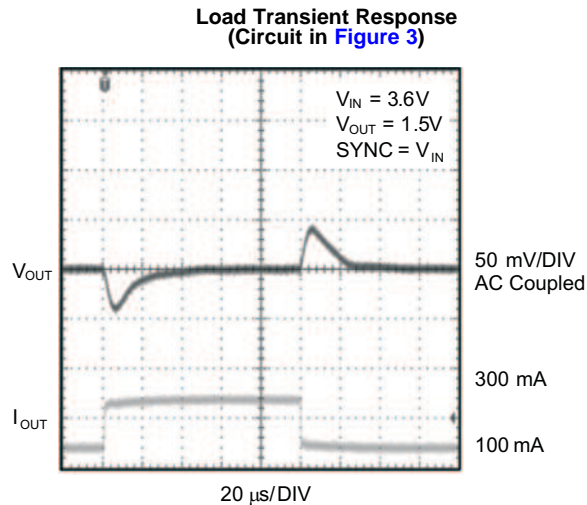


Figure 24.

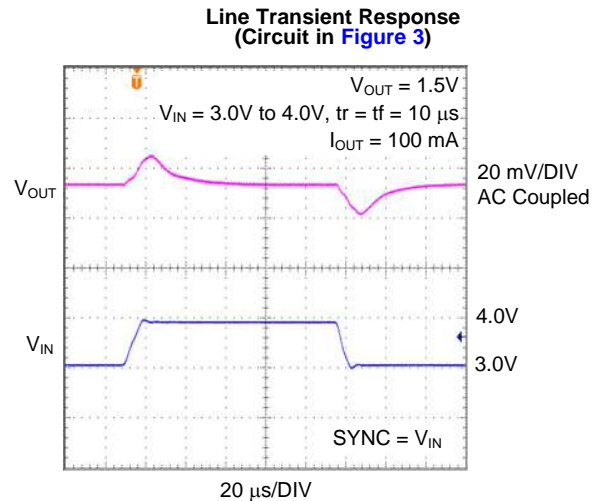


Figure 25.

SOFT-START

The LM2619 has soft start to reduce current inrush during power-up and startup. This reduces stress on the LM2619 and external components. It also reduces startup transients on the power source. Soft start is implemented by ramping up the reference input to the error amplifier of the LM2619 to gradually increase the output voltage.

THERMAL SHUTDOWN PROTECTION

The LM2619 has a thermal shutdown protection function to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds 150°C the device turns off the output stage and when the temperature drops below 130°C it initiates a soft start cycle. Prolonged operation in thermal shutdown conditions may damage the device and is considered bad practice.

APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

The LM2619 can be used with external feedback resistors to set the output voltage. Select the value of R2 to allow at least 100 times the feedback pin bias current to flow through it.

$$V_{OUT} = V_{FB} (1 + R1/R2)$$

EXTERNAL COMPENSATION

The LM2619 uses external components connected to the EANEG and EAOUT pins to compensate the regulator (Figure 20). Typically, all that is required is a series connection of one capacitor (C4) and one resistor (R3). A capacitor (C5) can be connected across the EANEG and EAOUT pins to improve the noise immunity of the loop. C5 reacts with R3 to give a high frequency pole. C4 reacts with the high open loop gain of the error amplifier and the resistance at the EANEG pin to create the dominant pole for the system, while R3 and C4 react to create a zero in the frequency response. The pole rolls off the loop gain, to give a bandwidth somewhere between 10kHz and 50kHz, this avoids a 100kHz parasitic pole contributed by the current mode controller. Typical values in the 220pF to 1nF (C4) range are recommended to create a pole on the order of 10Hz or less.

The next dominant pole in the system is formed by the output capacitance (C2) and the parallel combination of the load resistance and the effective output resistance of the regulator. This combined resistance (Ro) is dominated by the small signal output resistance, which is typically in the range of 3Ω to 15Ω. The exact value of this resistance, and therefore this load pole depends on the steady state duty cycle and the internal ramp value. Ideally we want the zero formed by R3 and C4 to cancel this load pole, such that $R3 = RoC2/C4$. Due to the large variation in Ro, this ideal case can only be achieved at one operating condition. Therefore a compromise of about 5Ω for Ro should be used to determine a starting value for R3. This value can then be optimized on the bench to give the best transient response to load changes, under all conditions. Typical values are 10pF for C5, 220pF to 1nF for C4 and 22K to 100K for R3.

$A_O = 20000$, Open loop gain of error amplifier

$R_f = 1$, Transresistance of output stage

$M_c = 362000$ A/s , Corrective ramp slope

$D = V_{OUT}/V_{IN}$, $D' = 1-D$, duty cycle

$M_1 = (V_{IN} - V_{OUT})/L1$, slope of current through inductor during PFET on time

$R_p = (R1 \parallel R2) + 5k\Omega$, effective resistance at inverting input of error amp

$R_o = (F \cdot L1) / (D' \cdot (M_c/M_1) + \frac{1}{2} - D)$

where R_o is the effective small signal output resistance of power stage

$f_{P1} = 1/(2 \cdot \pi \cdot A_O \cdot R_p \cdot C4)$, low frequency pole

$f_{P2} = 1/(2 \cdot \pi \cdot (R_{load} \parallel R_o) \cdot C2)$, pole due to Rload, Ro and C2

$f_{P3} = R_o / (2 \cdot \pi \cdot L1)$, high frequency pole from current mode control

$f_{P4} = 1/(2 \cdot \pi \cdot R3 \cdot C5)$, high frequency pole due to R3 and C5

$f_{Z1} = 1/(2 \cdot \pi \cdot R3 \cdot C4)$, zero due to R3 and C4

$\alpha = R2/(R1 + R2)$

$f_x = (\alpha \cdot (R_o \parallel R_{load})/R_f)/(2 \cdot \pi \cdot R_p \cdot C4)$

where f_x gives the approximate crossover frequency. This equation for crossover frequency assumes that $f_{P2} = f_{Z1}$.

INDUCTOR SELECTION

Use a 10μH inductor with saturation current rating higher than the peak current rating of the device. The inductor's resistance should be less than 0.3Ω for good efficiency. Table 2 lists suggested inductors and suppliers.

Table 2. Suggested Inductors and Their Suppliers

Part Number	Vendor	Phone	FAX
DO1608C-103	Coilcraft	847-639-6400	847-639-1469
ELL6SH100M	Panasonic	714-373-7366	714-373-7323
ELL6RH100M	Panasonic	714-373-7366	714-373-7323
CDRH5D18-100	Sumida	847-956-0666	847-956-0702
P0770.103T	Pulse	858-674-8100	858-674-8262

For low-cost applications, an unshielded inductor is suggested. For noise critical applications, a toroidal or shielded inductor should be used. A good practice is to lay out the board with footprints accommodating both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost unshielded models is unacceptable.

The saturation current rating is the current level beyond which an inductor loses its inductance. Different manufacturers specify the saturation current rating differently. Some specify saturation current point to be when inductor value falls 30% from its original value, others specify 10%. It is always better to look at the inductance versus current curve and make sure the inductor value doesn't fall below 30% at the peak current rating of the LM2619. Beyond this rating, the inductor loses its ability to limit current through the PWM switch to a ramp. This can cause poor efficiency, regulation errors or stress to DC-DC converters like the LM2619. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field.

CAPACITOR SELECTION

Use a 10 μ F ceramic input capacitor. Use X7R or X5R types, do not use Y5V.

Use of tantalum capacitors is not recommended.

Ceramic capacitors provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. A 22 μ F ceramic output capacitor is recommended for applications that require increased tolerance to heavy load transients. A 10 μ F ceramic output capacitor can be used in applications where the worst case load transient step is less than 200mA. Use of a 10 μ F output capacitor trades off smaller size for an increase in output voltage ripple, and undershoot during load transients. [Table 3](#) lists suggested capacitors and suppliers.

The input filter capacitor supplies current to the PFET switch of the LM2619 in the first part of each cycle and reduces voltage ripple imposed on the input power source. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The ESR, or equivalent series resistance, of the filter capacitors is a major factor in voltage ripple.

Table 3. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Phone	FAX
C1, C2 (Input or Output Filter Capacitor)				
C2012X5ROJ106M	Ceramic	TDK	847-803-6100	847-803-6296
JMK212BJ106MG	Ceramic	Taiyo-Yuden	847-925-0888	847-925-0899
ECJ3YB0J106K	Ceramic	Panasonic	714-373-7366	714-373-7323
JMK325BJ226MM	Ceramic	Taiyo-Yuden	847-925-0888	847-925-0899
C3225X5RIA226M	Ceramic	TDK	847-803-6100	847-803-6296

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful reflow techniques, as detailed in application note AN-1112. Refer to the section *Surface Mount Technology (SMT) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device.

The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See application note AN-1112 for specific instructions how to do this.

The 10-Bump package used for the LM2619 has 300 micron solder balls and requires 10.82mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 6–7mil wide, for a section approximately 6mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM2619 reflow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps D3–B3. Because PGND and PVIN are typically connected to large copper planes, inadequate thermal reliefs can result in late or inadequate reflow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metalization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in reflow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance.

Good layout for the LM2619 can be implemented by following a few simple design rules.

1. Place the LM2619 on 10.82 mil (10.82/1000 in.) pads. As a thermal relief, connect to each pad with a 7 mil wide, approximately 7 mil long traces, and then incrementally increase each trace to its optimal width. The important criterion is symmetry to ensure the solder bumps on the LM2619 reflow evenly (see *DSBGA Package Assembly and Use*).
2. *Place the LM2619, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2 in. (5 mm) of the LM2619.
3. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor, through the LM2619 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM2619 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. *Connect the ground pins of the LM2619, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM2619 by giving it a low-impedance ground connection.
5. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
6. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM2619 circuit and should be routed directly from V_{OUT} at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
7. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2619ATL/NOPB	ACTIVE	DSBGA	YPA	10	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-25 to 85	S76A	Samples
LM2619ATLX/NOPB	ACTIVE	DSBGA	YPA	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-25 to 85	S76A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

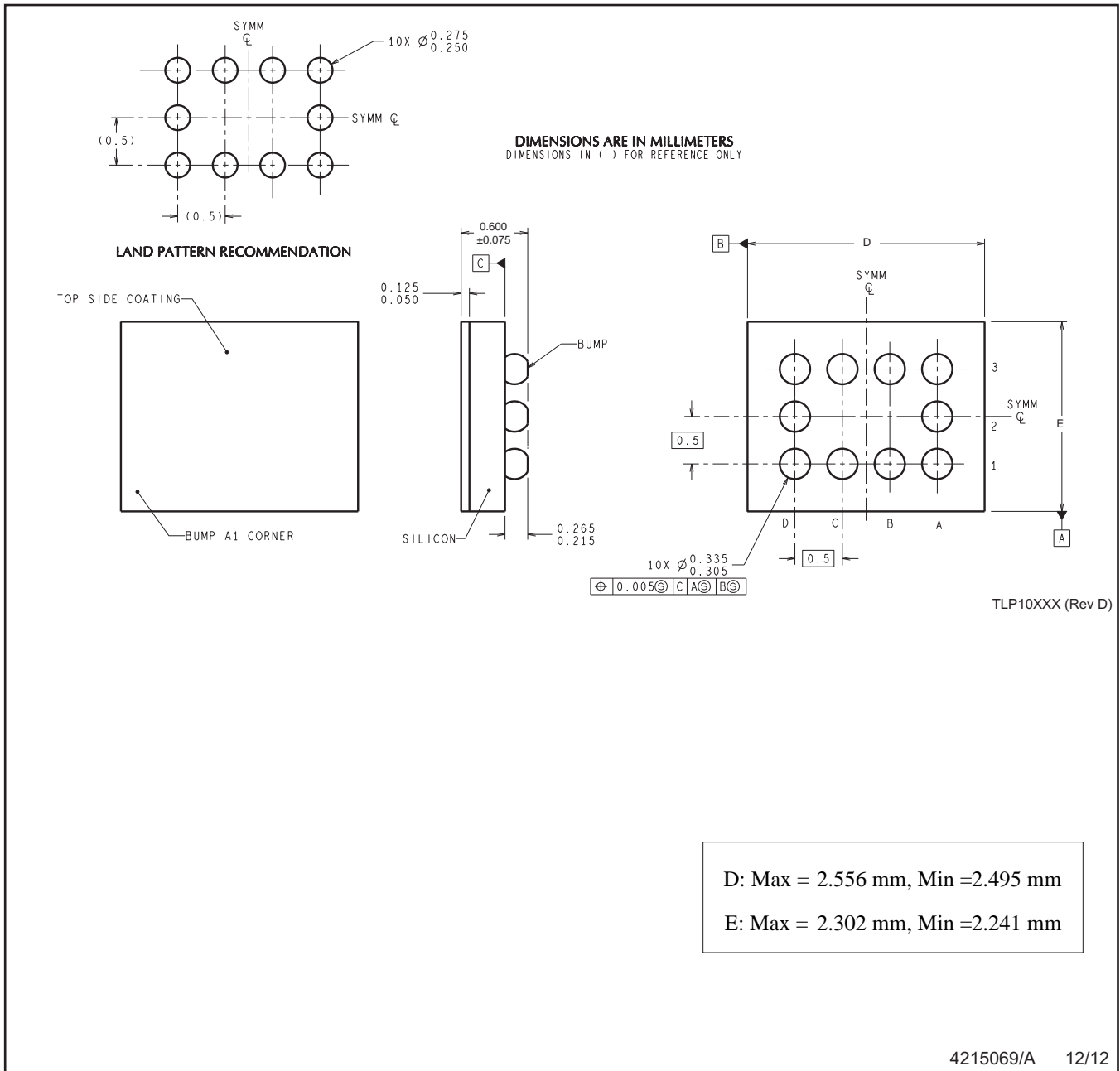
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2619ATL/NOPB	DSBGA	YPA	10	250	178.0	8.4	2.39	2.64	0.76	4.0	8.0	Q1
LM2619ATLX/NOPB	DSBGA	YPA	10	3000	178.0	8.4	2.39	2.64	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2619ATL/NOPB	DSBGA	YPA	10	250	210.0	185.0	35.0
LM2619ATLX/NOPB	DSBGA	YPA	10	3000	210.0	185.0	35.0

YPA0010



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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