LM2722 High Speed Synchronous/Asynchronous MOSFET Driver

Check for Samples: LM2722

FEATURES

- **Synchronous or Asynchronous Operation**
- **Adaptive Shoot-Through Protection**
- **Input Under-Voltage-Lock-Out**
- **Typical 20ns Internal Delay**
- **Plastic 8-pin SOIC package**

APPLICATIONS

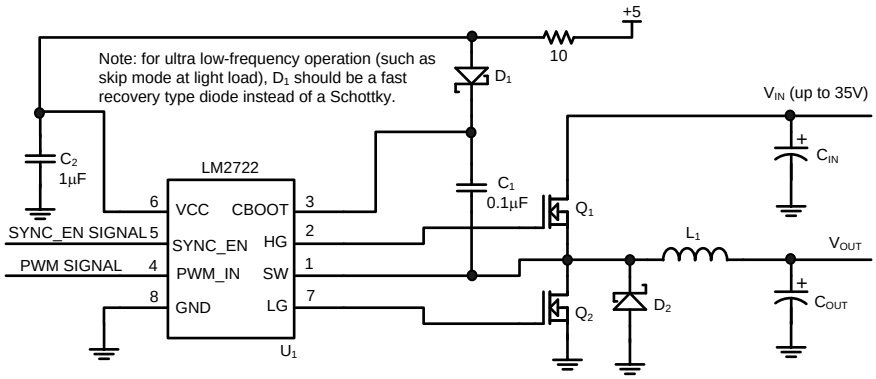
- **Driver for LM2723 Intel Mobile Northwood CPU Core Power Supply.**
- **High Current DC/DC Power Supplies**
- **High Input Voltage Switching Regulators**
- **Fast Transient Microprocessors**

DESCRIPTION

The LM2722, part of the LM2726 family, is designed to be used with multi-phase controllers. This part differs from the LM2726 by changing the functionality of the SYNC_EN pin from a whole chip enable to a low side MOSFET enable. As a result, the SYNC_EN pin now provides control between Synchronous and Asynchronous operations. Having this control can be advantageous in portable systems since Asynchronous operations can be more efficient at very light loads.

The LM2722 drives both top and bottom MOSFETs in a push-pull structure simultaneously. It takes a logic level PWM input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom FETs from turning on simultaneously. The cross-conduction protection circuitry detects both the driver outputs and will not turn on a driver until the other driver output is low. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2722 is typically 3A. In an SOIC-8 package, each driver is able to handle 50mA average current. Input UVLO (Under-Voltage-Lock-Out) forces both driver outputs low to ensure proper power-up and power-down operation. The gate drive bias voltage needed by the high side MOSFET is obtained through an external bootstrap. Minimum pulse width is as low as 55ns.

Typical Application



NOTE

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Connection Diagram

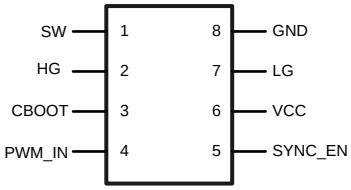


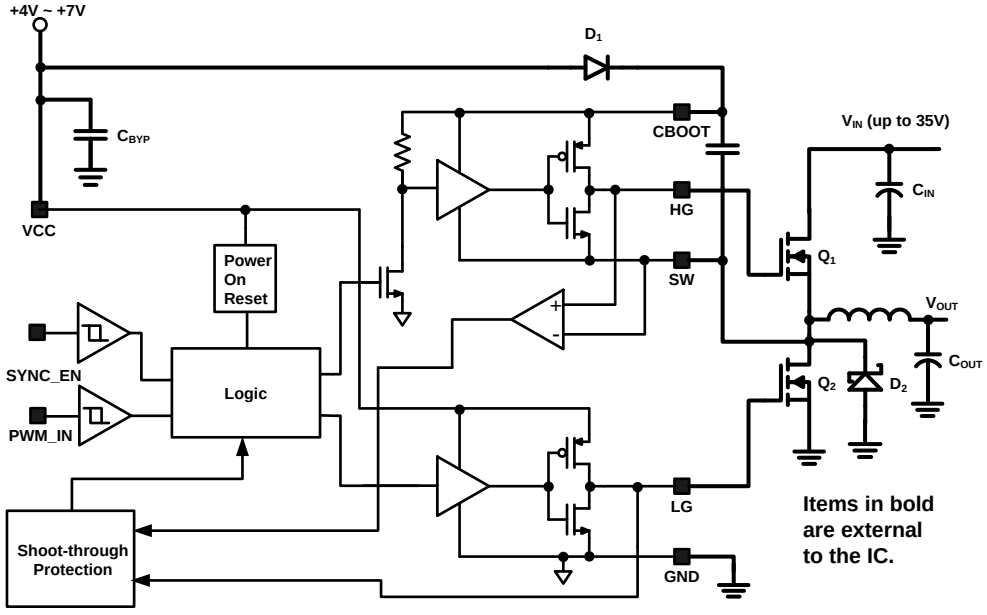
Figure 1. SOIC (D)
(Top View)

Pin Functions

Pin Descriptions

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output
3	CBOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	PWM_IN	Accepts a 5V-logic control signal
5	SYNC_EN	Low gate Enable
6	VCC	Connect to +5V supply
7	LG	Bottom gate drive output
8	GND	Ground

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)

VCC	7.5V
CBOOT	42V
CBOOT to SW	8V
SW to PGND	36V
Junction Temperature	+150°C
Power Dissipation (2)	720mW
Storage Temperature	−65° to 150°C
ESD Susceptibility Human Body Model (3)	1kV
Soldering Time, Temperature	10sec., 300°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply ensured performance limits.
(2) Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX}-T_A) / \theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for the LM2722, it is 172°C/W. For a T_{JMAX} of 150°C and T_A of 25°C, the maximum allowable power dissipation is 0.7W.
(3) ESD machine model susceptibility is 100V.

Operating Ratings (1)

VCC	4V to 7V
Junction Temperature Range	−40° to 125°C

(1) **Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply ensured performance limits.

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Electrical Characteristics

VCC = CBOOT = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	PWM_IN = 0V		190	**300**	µA
TOP DRIVER						
	Peak Pull-Up Current	Test Circuit 1, V_{bias} = 5V, R = 0.1Ω		3.0		A
	Pull-Up Rds_on	I_{CBOOT} = I_{HG} = 0.7A		1.0		Ω
	Peak Pull-down Current	Test Circuit 2, V_{bias} = 5V, R = 0.1Ω		−3.2		A
	Pull-down Rds_on	I_{SW} = I_{HG} = 0.7A		0.5		Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time			12		ns
t_3	Pull-Up Dead Time	Timing Diagram		23		ns
t_5	Pull-Down Delay	Timing Diagram, from PWM_IN Falling Edge		27		ns
BOTTOM DRIVER						
	Peak Pull-Up Current	Test Circuit 3, V_{bias} = 5V, R = 0.1Ω		3.2		A
	Pull-up Rds_on	I_{VCC} = I_{LG} = 0.7A		1.0		Ω
	Peak Pull-down Current	Test Circuit 4, V_{bias} = 5V, R = 0.1Ω		3.2		A
	Pull-down Rds_on	I_{GND} = I_{LG} = 0.7A		0.5		Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_2	Fall Time			14		ns
t_7	Pull-up Dead Time	Timing Diagram		28		ns
t_1	Pull-down Delay	Timing Diagram, from PWM_IN Rising Edge		13		ns
LOGIC						
V_{uvlo_up}	Power On Threshold	VCC rises from 0V toward 5V	**4**	3.7		V
V_{uvlo_dn}	Under-Voltage-Lock-Out Threshold			3.0	**2.5**	V
V_{uvlo_hys}	Under-Voltage-Lock-Out Hysteresis			0.7		V
V_{IH_EN}	SYNC_EN Pin High Input		**2.4**			V
V_{IL_EN}	SYNC_EN Pin Low Input				**0.8**	V
I_{leak_EN}	SYNC_EN Pin Leakage Current	EN = 5V	**−2**		**2**	µA
		EN = 0V	**−2**		**2**	
t_{on_min}	Minimum Positive Input Pulse Width (1)			55		ns
t_{off_min}	Minimum Negative Input Pulse Width (2)			55		
V_{IH_PWM}	PWM_IN High Level Input Voltage	When PWM_IN pin goes high from 0V	**2.4**			V
V_{IL_PWM}	PWM_IN Low Level Input Voltage	When PWM_IN pin goes low from 5V			**0.8**	

(1) If after a rising edge, a falling edge occurs sooner than the specified value, the IC may intermittently fail to turn on the bottom gate when the top gate is off. As the falling edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

(2) If after a falling edge, a rising edge occurs sooner than the specified value, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

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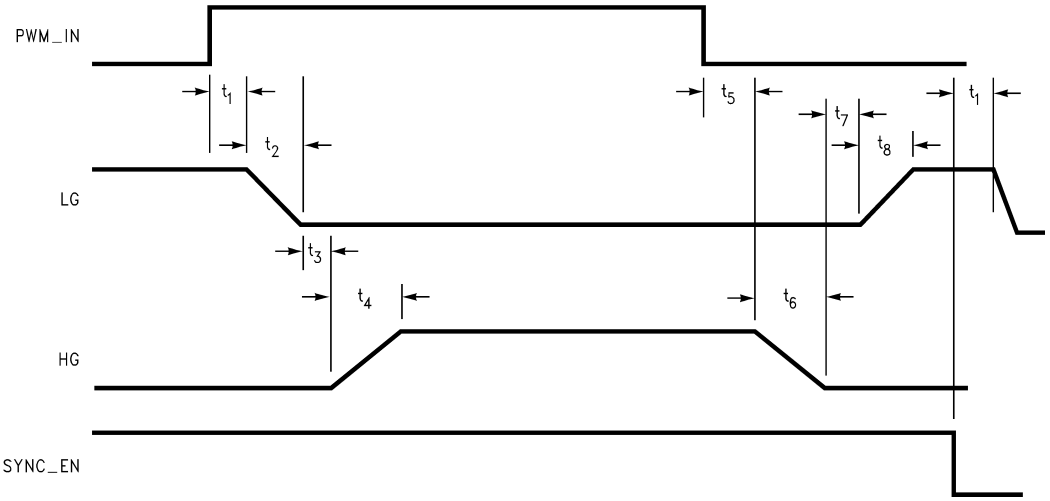
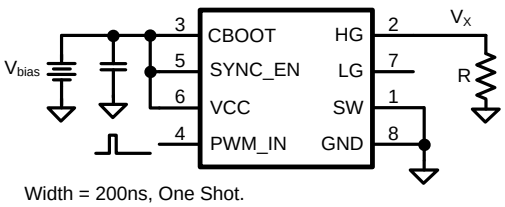
TEST CIRCUIT DIAGRAMS

Timing Diagram

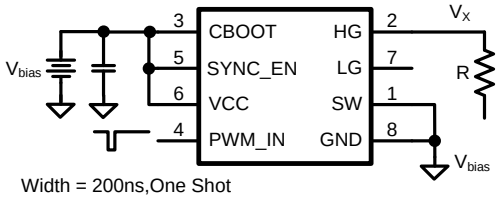


Test Circuits



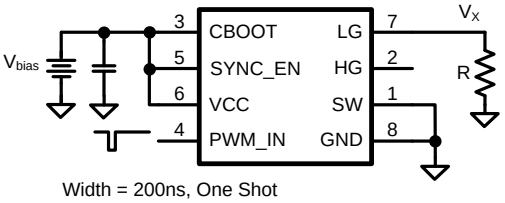
Width = 200ns, One Shot.

Figure 2. Test Circuit 1



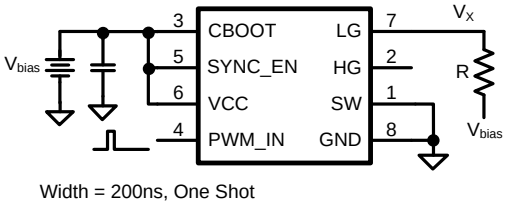
Width = 200ns,One Shot

Figure 3. Test Circuit 2



Width = 200ns, One Shot

Figure 4. Test Circuit 3



Width = 200ns, One Shot

Figure 5. Test Circuit 4

$$I_{pull\_up} = \frac{V_x}{R} \quad (1)$$

$$I_{pull\_down} = \frac{V_{bias} - V_x}{R} \quad (2)$$

$$R_{ds\_pull\_up} = \frac{V_{bias} - V_x}{V_x} . R \quad (3)$$

$$R_{ds\_pull\_down} = \frac{V_x}{V_{bias} - V_x} . R \quad (4)$$

Typical Waveforms

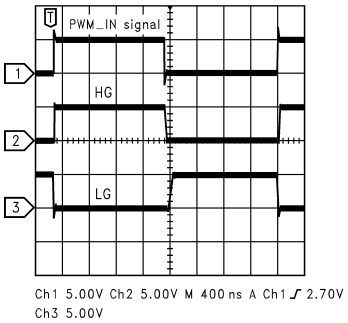


Figure 6. Switching Waveforms of Test Circuit

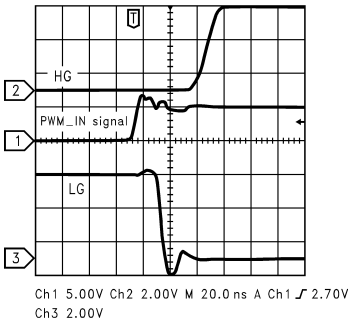


Figure 7. When Input Goes High

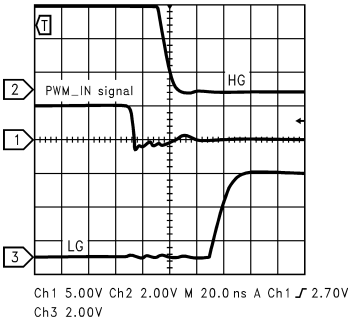


Figure 8. When Input Goes Low

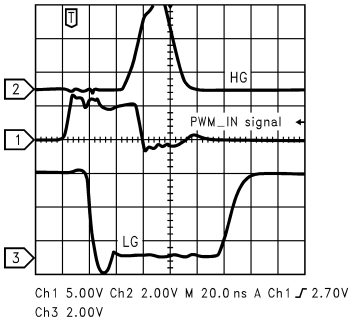


Figure 9. Minimum Positive Pulse

Application Information

MINIMUM PULSE WIDTH

In order for the shoot-through prevention circuitry in the LM2722 to work properly, the pulses into the PWM_IN pin must be longer than 55ns. The internal logic waits until the first FET is off plus 20ns before turning on the opposite FET. If, after a falling edge, a rising edge occurs sooner than the specified time, t_{off_min}, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output. This condition results in the PWM_IN pin in a high state and neither FET turned on. To get out of this state, the PWM_IN pin must see a low signal for greater than 55ns, before the rising edge.

This will also assure that the gate drive bias voltage has been restored by forcing the top FET source and C_{boot} to ground first. Then the internal circuitry is reset and normal operation will resume.

Conversely, if, after a rising edge, a falling edge occurs sooner than the specified miniumum pulse width, t_{on_min}, the IC may intermittently fail to turn on the bottom FET. As the falling edge occurs sooner and sooner, the driver will start to ignore the pulse and produce no output. This will result in the t_{off} inductor current taking a path through a diode provided for non-synchronous operation. The circuit will resume synchronous operation when the rising PWM pulses exceed 55ns in duration.

HIGH INPUT VOLTAGES OR HIGH OUTPUT CURRENTS

At input voltages above twice the output voltage and at higher power levels, the designer may find snubber networks and gate drive limiting useful in reducing EMI and preventing injurious transients. A small resistor, 1Ω to 5Ω, between the driver outputs and the MOSFET gates will slightly increase the rise time and fall time of the output stage and reduce switching noise. The trade-off is 1% to 2% in efficiency.

A series R-C snubber across in parallel with the bottom FET can also be used to reduce ringing. Values of 10nF and 10Ω to 100Ω are a good starting point.

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REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	6

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2722MX/NOPB	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		2722 M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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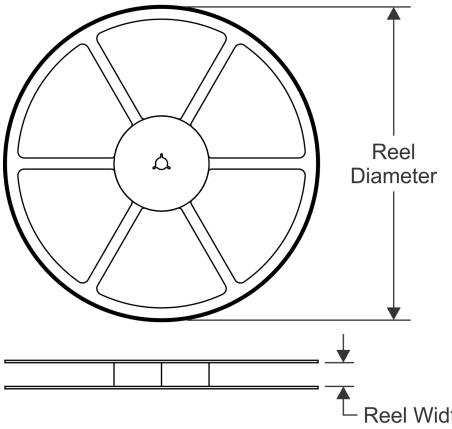
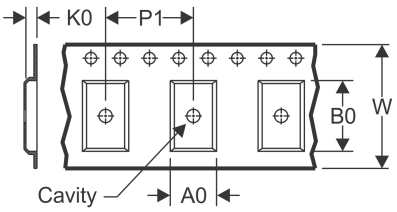
TAPE AND REEL INFORMATION

REEL DIMENSIONS

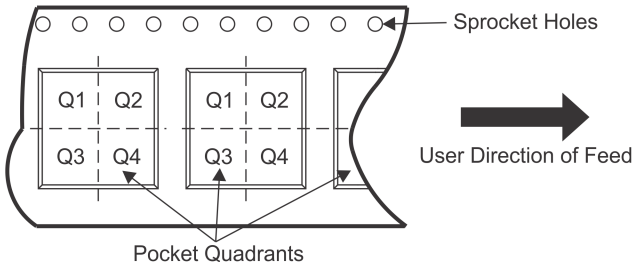


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

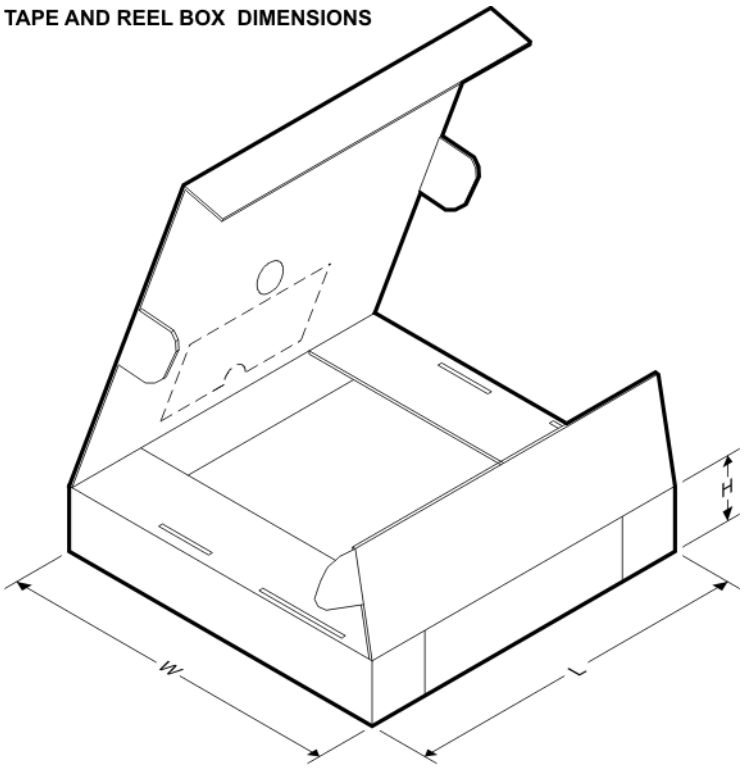
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2722MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

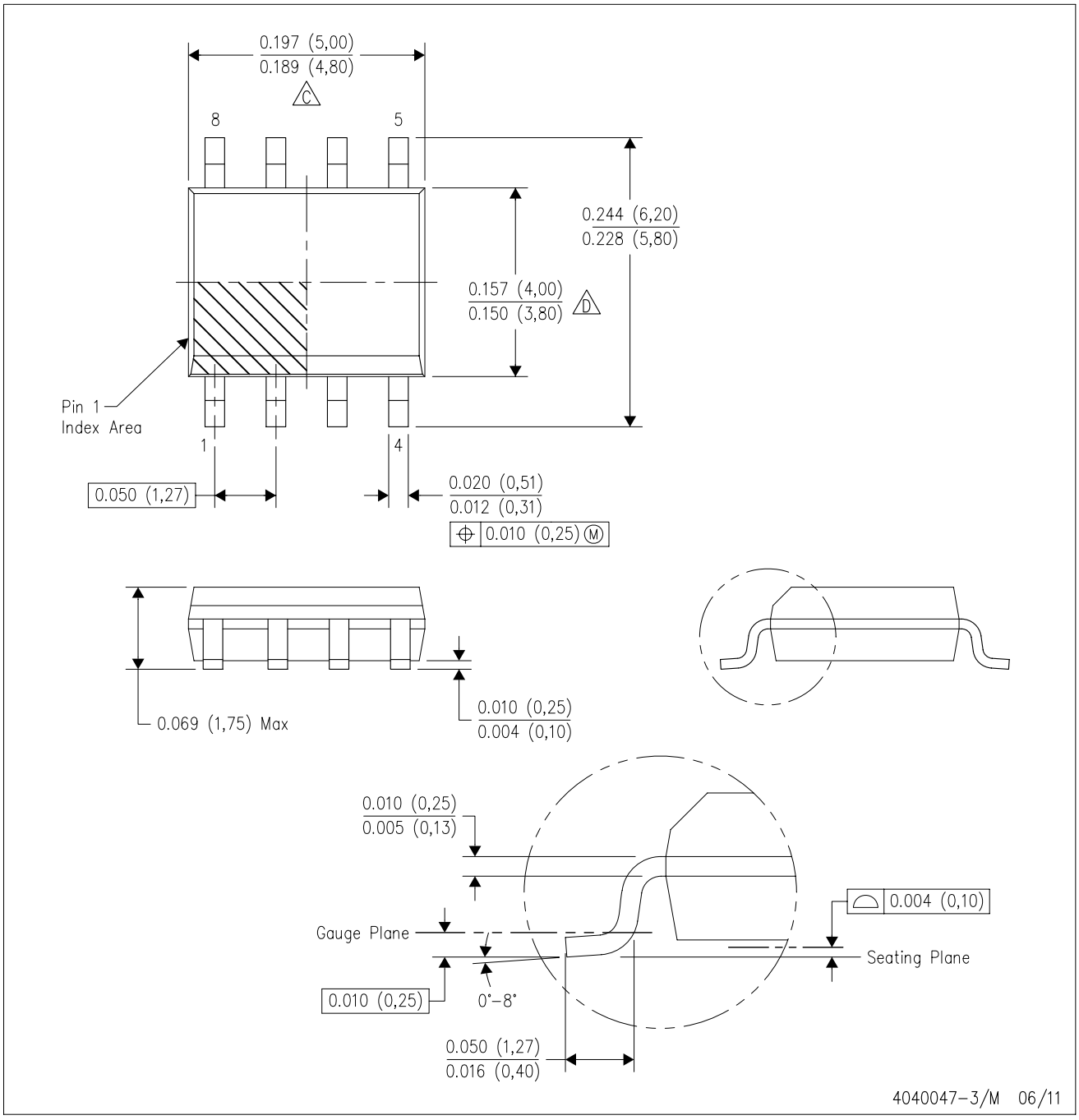
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2722MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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