LM3530 High Efficiency White LED Driver with Programmable Ambient Light Sensing Capability and I^{2}C-Compatible Interface

Check for Samples: LM3530

FEATURES

- **Drives up to 11 LED's in series**
- **1000:1 Dimming Ratio**
- **90% Efficient**
- **Programmable Dual Ambient Light Sensor Inputs with internal ALS Voltage Setting Resistors**
- **I^{2}C Programmable Logarithmic or Linear Brightness Control**
- **External PWM Input for Simple Brightness Adjustment**
- **True Shutdown Isolation for LED's and Ambient Light Sensors**
- **Internal Soft-Start Limits Inrush Current**
- **Wide 2.7V to 5.5V Input Voltage Range**
- **40V and 25V Over-Voltage Protection Options**
- **500kHz Fixed Frequency Operation**
- **839mA Peak Current Limit**
- **Low-Profile 12-Bump DSBGA Package**

APPLICATIONS

- **Smartphone LCD Backlighting**
- **Personal Navigation LCD Backlighting**
- **2 to 11 Series White LED Backlit Display Power Source**

DESCRIPTION

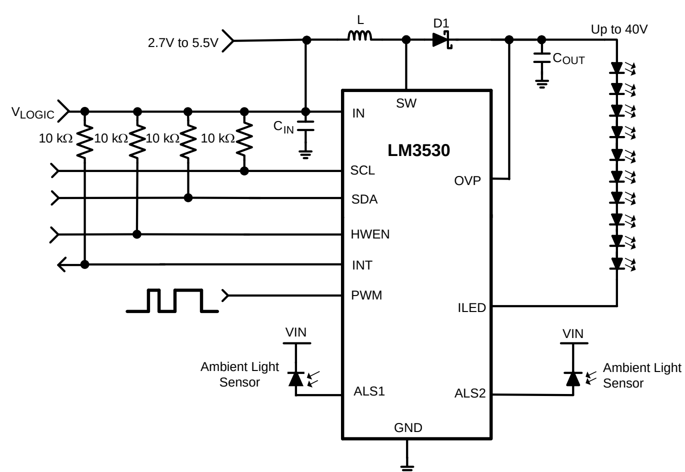
The LM3530 current mode boost converter supplies the power and controls the current in up to 11 series white LED's. The 839mA current limit and 2.7V to 5.5V input voltage range make the device a versatile backlight power source ideal for operation in portable applications.

The LED current is adjustable from 0 to 29.5mA via an I^{2}C-compatible interface. The 127 different current steps and 8 different maximum LED current levels give over 1000 programmable LED current levels. Additionally, PWM brightness control is possible through an external logic level input.

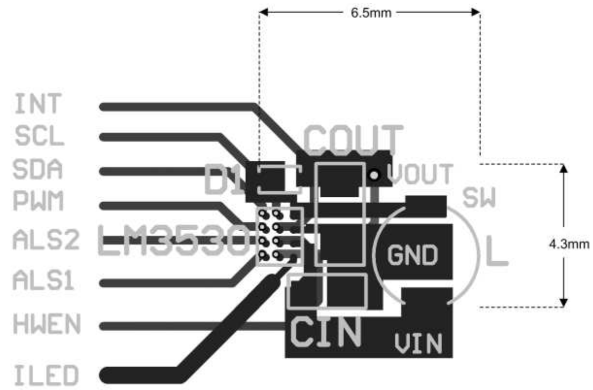
The device also features two Ambient Light Sensor inputs. These are designed to monitor analog output ambient light sensors and provide programmable adjustment of the LED current with changes in ambient light. Each ambient light sensor input has independently programmable internal voltage setting resistors which can be made high impedance to reduce power during shutdown. The LM3530's 500kHz switching frequency allows for high converter efficiency over a wide output voltage range accommodating from 2 to 11 series LEDs. Finally, the support of Content Adjusted Backlighting maximizes battery life while maintaining display image quality.

The LM3530 is available in a tiny 12-bump (1.6mm × 1.2mm × 0.425mm) DSBGA package and operates over the −40°C to +85°C temperature range.

Typical Application Circuit



LM3530 Layout Example



Connection Diagram

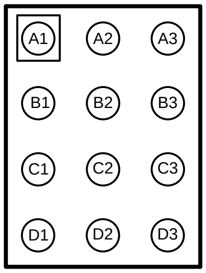


Figure 1. 12-Bump (1.215mm × 1.615mm x XXXmm)
YFZ0012 (XXX = 0.425mm)
YFQ0012 (XXX = 0.625mm)

PIN DESCRIPTIONS

Pin	Name	Description
C3	IN	Input Voltage Connection. Connect a 2.7V to 5.5V supply to IN and bypass to GND with a 2.2µF or greater ceramic capacitor.
D2	OVP	Output Voltage Sense Connection for Over-Voltage Sensing. Connect OVP to the positive terminal of the output capacitor.
A3	SW	Inductor Connection, Diode Anode Connection, and Drain Connection for Internal NFET. Connect the inductor and diode as close as possible to SW to reduce parasitic inductance and capacitive coupling to nearby traces.
D3	ILED	Input Terminal to Internal Current Sink. The boost converter regulates ILED to 0.4V.
D1	ALS1	Ambient Light Sensor Input #1 with Programmable Internal Pull-down Resistor.
A1	SDA	Serial Data Connection for I^2C-Compatible Interface.
A2	SCL	Serial Clock Connection for I^2C-Compatible Interface.
B3	GND	Ground
C1	ALS2	Ambient Light Sensor Input #2 with Programmable Internal Pull-down Resistor.
B1	PWM	External PWM Brightness Control Input and Simple Enable Input.
B2	INT	Logic Interrupt Output Signaling the ALS Zone Has Changed.
C2	HWEN	Active High Hardware Enable (Active Low Reset). Pull this pin high to enable the LM3530.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2][3]

V_{IN} to GND	−0.3V to +6V
V_{SW}, V_{OVP}, V_{ILED} to GND	−0.3V to 45V
V_{SCL}, V_{SDA}, V_{ALS1}, V_{PWM}, V_{INT}, V_{HWEN} to GND	−0.3V to +6V
$V_{ALS2}$to GND	-0.3V to V_{IN} + 0.3V
Continuous Power Dissipation	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10s)	[4]
ESD Rating [5] Human Body Model	2.0kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics table.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pin.
(4) For detailed soldering specifications and information, please refer to Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112).
(5) The human body model is a 100pF capacitor discharged through 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7).

Operating Ratings [1][2]

V_{IN} to GND	2.7V to 5.5V
V_{SW}, V_{OVP}, V_{ILED}, to GND	0 to +40V
Junction Temperature Range (T_J) [3]	−40°C to +125°C
Ambient Temperature Range (T_A) [4]	−40°C to +85°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics table.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=+140°C (typ.) and disengages at T_J=+125°C (typ.).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction to Ambient Thermal Resistance (T_{JA})[1]	61.7°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102mm x 76mm x 1.6mm with a 2 x 1 array of thermal vias. The ground plane on the board is 50mm x 50mm. Thickness of copper layers are 36µm/18µm/18µm/36µm (1.5oz/1oz/1oz/1.5oz). Ambient temperature in simulation is 22°C in still air. Power dissipation is 1W. The value of θ_{JA} of this product in the DSBGA package could fall in a range as wide as 60ºC/W to 110ºC/W (if not wider), depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists special care must be paid to thermal dissipation issues.

Electrical Characteristics [1][2]

Limits in standard type face are for T_A = +25°C and those in **boldface type** apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified V_{IN} = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LED}	Output Current Regulation	2.7V ≥ V_{IN} ≥ 5.5V, Full-Scale Current = 19mA, BRT Code = 0x7F, ALS Select Bit = 0, I2C Enable = 1	**17.11**	18.6	**20.08**	mA
V_{REG_CS}	Regulated Current Sink Headroom Voltage			400		mV

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical (typ.) numbers are not guaranteed, but represent the most likely norm.

Electrical Characteristics (1)(2) (continued)

Limits in standard type face are for T_A = +25°C and those in **boldface type** apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified V_{IN} = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{HR}	Current Sink Minimum Headroom Voltage	I_{LED} = 95% of nominal		200		mV
R_{DSON}	NMOS Switch On Resistance	I_{SW} = 100 mA		0.25		Ω
I_{CL}	NMOS Switch Current Limit	2.7V ≤ V_{IN} ≤ 5.5V	**739**	839	**936**	mA
V_{OVP}	Output Over-Voltage Protection	ON Threshold, 2.7V ≤ V_{IN} ≤ 5.5V: 40V version	**40**	41	**42**	V
		ON Threshold, 2.7V ≤ V_{IN} ≤ 5.5V: 25V version	**23.6**	24	**24.6**	V
		Hysteresis		1		V
f_{SW}	Switching Frequency	2.7V ≤ V_{IN} ≤ 5.5V	**450**	500	**550**	kHz
D_{MAX}	Maximum Duty Cycle			94		%
D_{MIN}	Minimum Duty Cycle			10		%
I_Q	Quiescent Current, Device Not Switching	V_{HWEN} = V_{IN}		490	**600**	µA
I_{Q_SW}	Switching Supply Current	I_{LED} = 19mA, V_{OUT} = 36V		1.35		mA
I_{SHDN}	Shutdown Current	V_{HWEN} = GND, 2.7V ≥ V_{IN} ≥ 5.5V		1	**2**	µA
I_{LED_MIN}	Minimum LED Current	Full-Scale Current = 19mA setting BRT = 0x01		9.5		µA
V_{ALS}	Ambient Light Sensor Reference Voltage	2.7V ≥ V_{IN} ≥ 5.5V (3)	**0.97**	1	**1.03**	V
V_{HWEN}	Logic Thresholds - Logic Low		**0**		**0.4**	V
	Logic Thresholds - Logic High		**1.2**		**V_{IN}**	V
T_{SD}	Thermal Shutdown			+140		°C
	Hysteresis			15		°C
RALS1, RALS2	ALS Input Internal Pull-down Resistors	2.7V ≥ V_{IN} ≥ 5.5V	**12.77**	13.531	**14.29**	kΩ
			8.504	9.011	**9.518**	
			5.107	5.411	**5.715**	
			2.143	2.271	**2.399**	
			1.836	1.946	**2.055**	
			1.713	1.815	**1.917**	
			1.510	1.6	**1.69**	
			1.074	1.138	**1.202**	
			0.991	1.050	**1.109**	
			0.954	1.011	**1.068**	
			0.888	0.941	**0.994**	
			0.717	0.759	**0.802**	
			0.679	0.719	**0.760**	
			0.661	0.700	**0.740**	
			0.629	0.666	**0.704**	
Logic Voltage Specifications (SCL, SDA, PWM, INT)						
V_{IL}	Input Logic Low	2.7V ≤ V_{IN} ≤ 5.5V	**0**		**0.54**	V
V_{IH}	Input Logic High	2.7V ≤ V_{IN} ≤ 5.5V	**1.26**		**V_{IN}**	V

(3) The ALS voltage specification is the maximum trip threshold for the ALS zone boundary (Code 0xFF). Due to random offsets and the mechanism for which the hysteresis voltage varies, it is recommended that only Codes 0x04 and above be used for Zone Boundary Thresholds. See **Zone Boundary Trip Points and Hysteresis** and **Minimum Zone Boundary Settings** sections.

Electrical Characteristics (1)(2) (continued)

Limits in standard type face are for T_A = +25°C and those in **boldface type** apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified V_{IN} = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Logic Low (SDA, INT)	I_{LOAD} = 3 mA			**400**	mV
I²C-Compatible Timing Specifications (SCL, SDA) (4)						
t_1	SCL (Clock Period)		**2.5**			µs
t_2	Data In Setup Time to SCL High		**100**			ns
t_3	Data Out Stable After SCL Low		**0**			ns
t_4	SDA Low Setup Time to SCL Low (Start)		**100**			ns
t_5	SDA High Hold Time After SCL High (Stop)		**100**			ns
Simple Interface (PWM pin)						
t_{PWM_HIGH}	Enable time, PWM pin must be held high		**1.5**	2	**2.6**	ms
t_{PWM_LOW}	Disable time, PWM pin must be held low		**1.48**	2	**2.69**	

(4) SCL and SDA must be glitch-free in order for proper brightness control to be realized.

Timing Diagrams

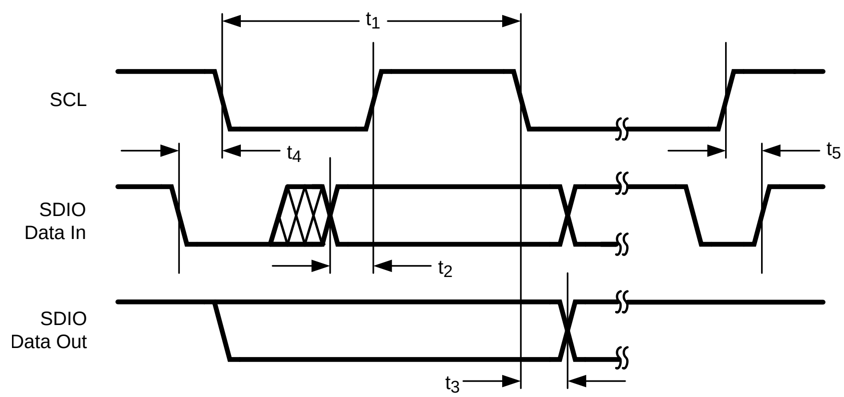


Figure 2. I²C-Compatible Timing

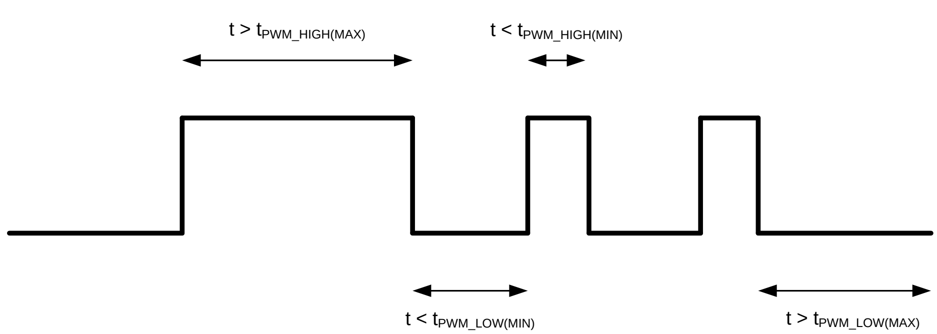


Figure 3. Simple Enable/Disable Timing

Typical Performance Characteristics

V_{IN} = 3.6V, LEDs are OVSRWAC1R6 from OPTEK Technology, C_{OUT} = 1µF, C_{IN} = 1µF, L = TDK VLF5012ST-100M1R0, (R_L = 0.24Ω), I_{LED} = 19mA, T_A = +25°C unless otherwise specified.

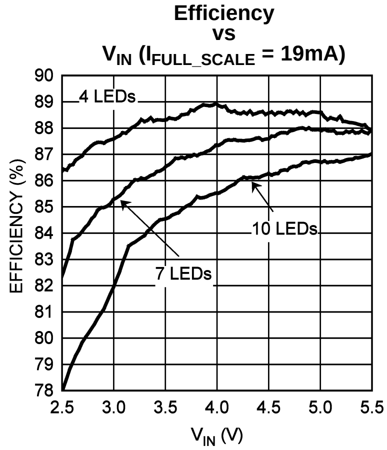


Figure 4.

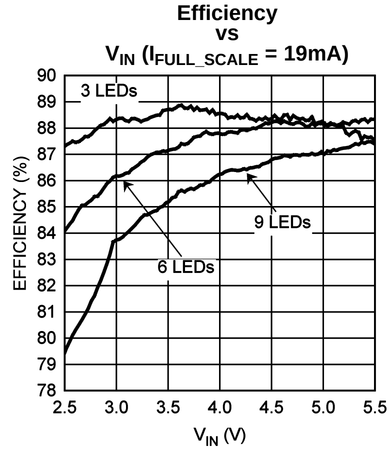


Figure 5.

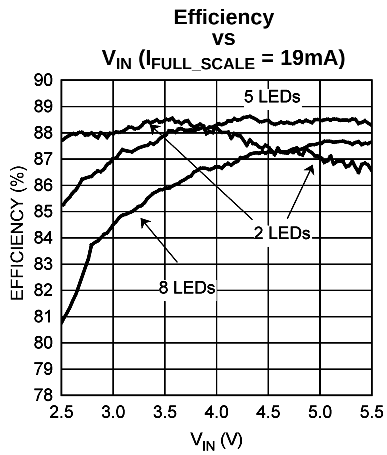


Figure 6.

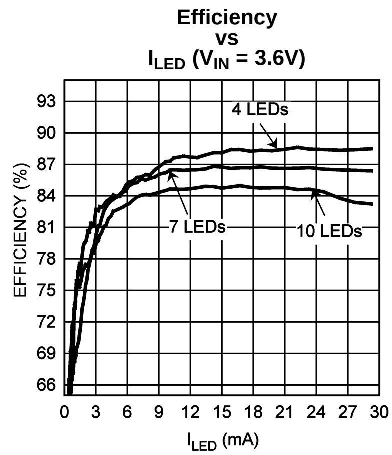


Figure 7.

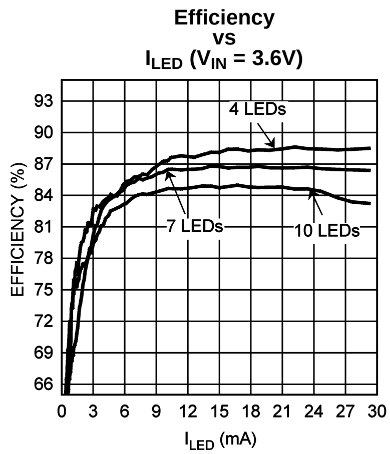


Figure 8.

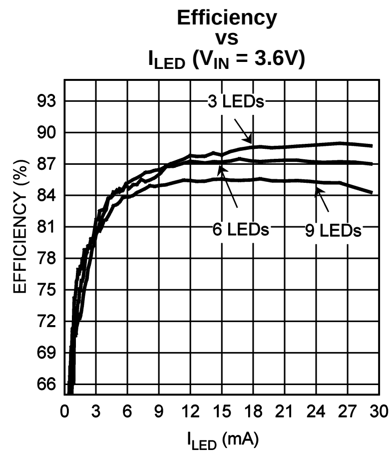


Figure 9.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are OVSRWAC1R6 from OPTEK Technology, C_{OUT} = 1µF, C_{IN} = 1µF, L = TDK VLF5012ST-100M1R0, (R_L = 0.24Ω), I_{LED} = 19mA, T_A = +25°C unless otherwise specified.

LED Current vs V_{IN} (19mA Full-Scale Setting)

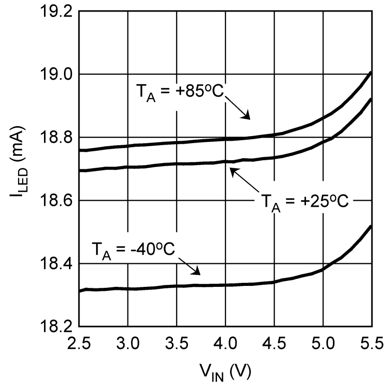


Figure 10.

Shutdown Current vs V_{IN}

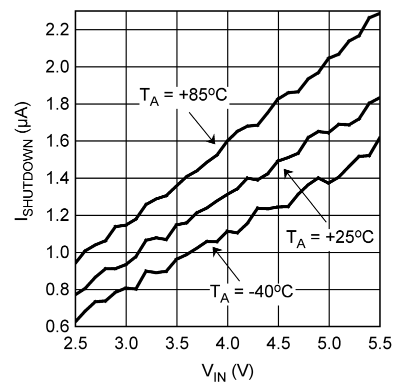


Figure 11.

Internal ALS Resistor vs V_{IN} (T_A = +25°C) ALS Resistor Select Register = 0x44

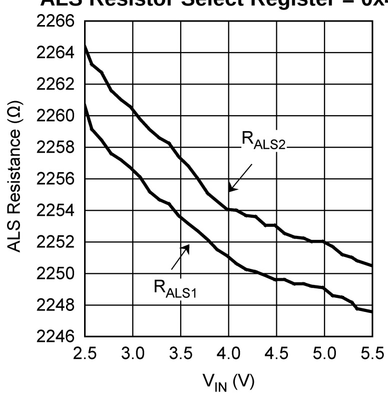


Figure 12.

Internal ALS Resistor vs V_{IN} (T_A = +85°C) ALS Resistor Select Register = 0x44

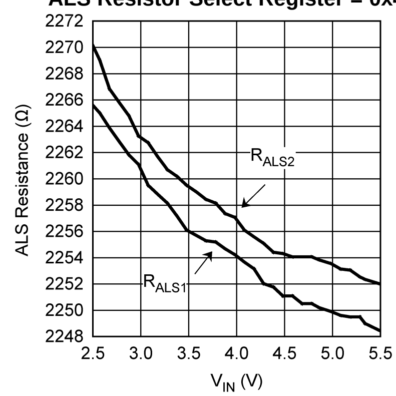


Figure 13.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are OVSRWAC1R6 from OPTEK Technology, C_{OUT} = 1µF, C_{IN} = 1µF, L = TDK VLF5012ST-100M1R0, (R_L = 0.24Ω), I_{LED} = 19mA, T_A = +25°C unless otherwise specified.

Internal ALS Resistor vs V_{IN} (T_A = −40°C) ALS Resistor Select Register = 0x44

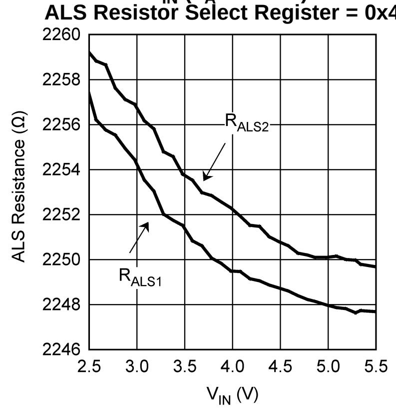


Figure 14.

Current Limit vs V_{IN}(Closed Loop, L = 22µH (1))

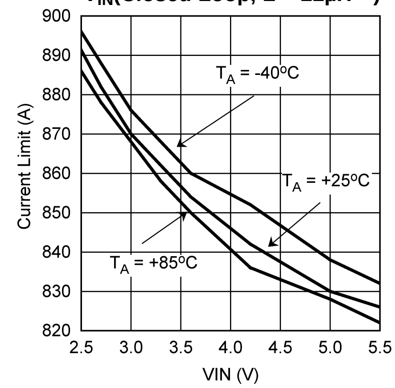


Figure 15.

Over Voltage Protection vs V_{IN} (V_{OUT} Rising)

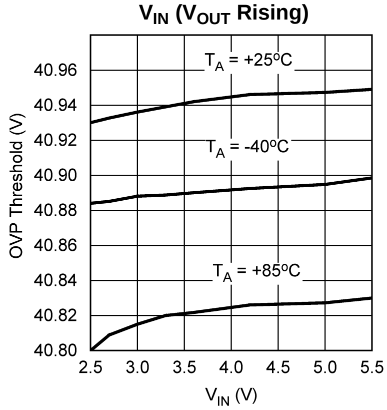


Figure 16.

Max Duty Cycle vs V_{IN}

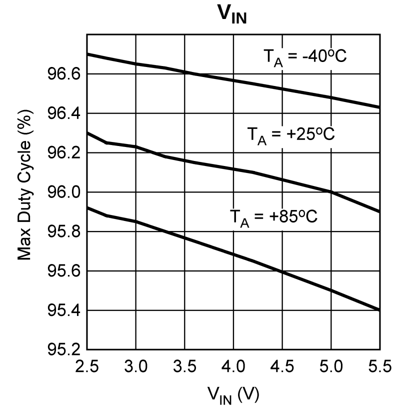


Figure 17.

NFET Switch On-Resistance vs V_{IN}

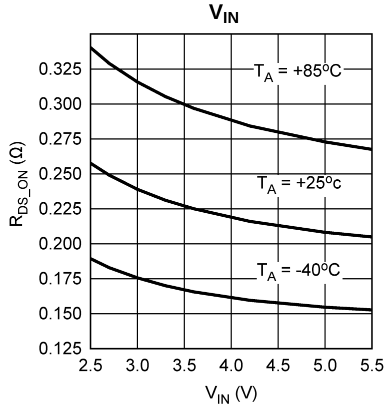


Figure 18.

Switching Frequency vs V_{IN}

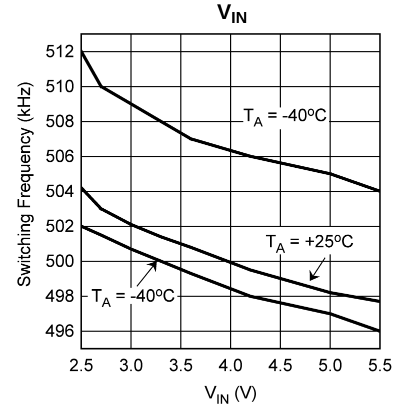


Figure 19.

(1) The value for current limit given in the Electrical Table is measured in an open loop test by forcing current into SW until the current limit comparator threshold is reached. The typical curve for current limit is measured in closed loop using the typical application circuit by increasing IOUT until the peak inductor current stops increasing. Closed loop data appears higher due to the delay between the comparator trip point and the NFET turning off. This delay allows the closed loop inductor current to ramp higher after the trip point by approximately 100ns × VIN/L

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are OVSRWAC1R6 from OPTEK Technology, C_{OUT} = 1µF, C_{IN} = 1µF, L = TDK VLF5012ST-100M1R0, (R_L = 0.24Ω), I_{LED} = 19mA, T_A = +25°C unless otherwise specified.

Simple Enable Time vs V_{IN}

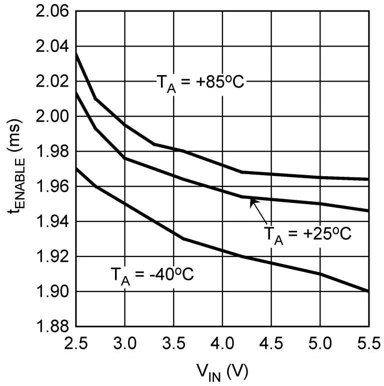


Figure 20.

Simple Disable Time vs V_{IN}

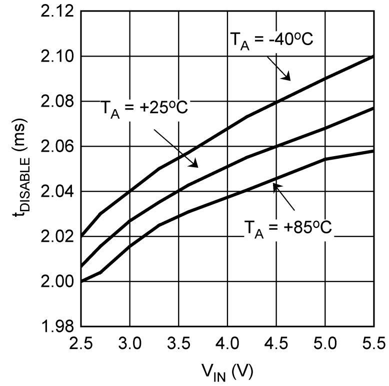


Figure 21.

I_{LED} vs f_{PWM} (50% duty cycle, I_{LED} Full Scale = 19mA)

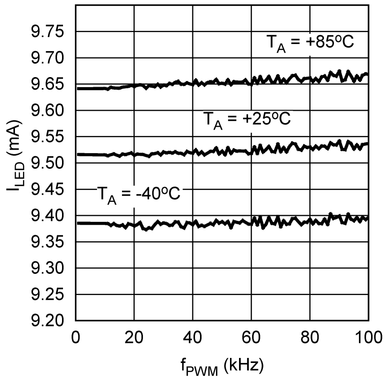
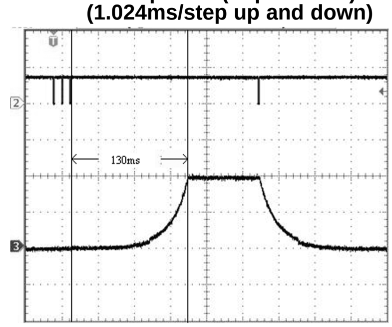


Figure 22.

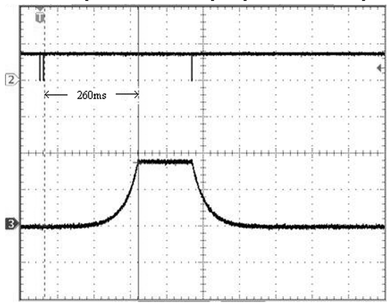
Ramp Rate (Exponential) (1.024ms/step up and down)



Channel 2: SDA (5V/div)
Channel 3: ILED (10mA/div)
Time Base (40ms/div)

Figure 23.

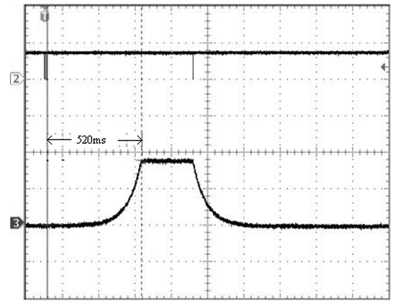
Ramp Rate (Exponential) (2.048ms/step up and down)



Channel 2: SDA (5V/div)
Channel 3: ILED (10mA/div)
Time Base (100ms/div)

Figure 24.

Ramp Rate (Exponential) (4.096ms/step up and down)



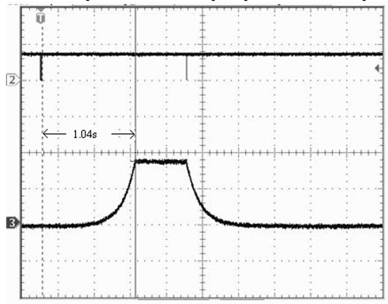
Channel 2: SDA (5V/div)
Channel 3: ILED (10mA/div)
Time Base (200ms/div)

Figure 25.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are OVSRWAC1R6 from OPTEK Technology, C_{OUT} = 1µF, C_{IN} = 1µF, L = TDK VLF5012ST-100M1R0, (R_L = 0.24Ω), I_{LED} = 19mA, T_A = +25°C unless otherwise specified.

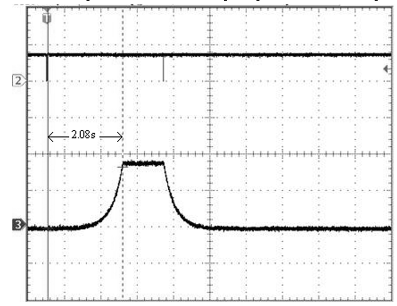
Ramp Rate (Exponential)
(8.192ms/step up and down)



Channel 2: SDA (5V/div)
Channel 3: ILED (10mA/div)
Time Base (400ms/div)

Figure 26.

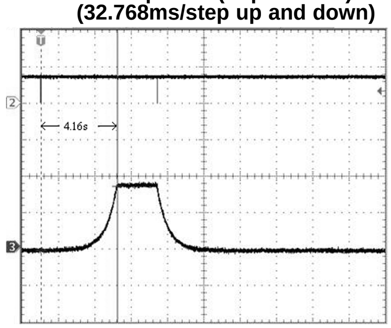
Ramp Rate (Exponential)
(16.384ms/step up and down)



Channel 2: SDA (5V/div)
Channel 3: ILED (10mA/div)
Time Base (1s/div)

Figure 27.

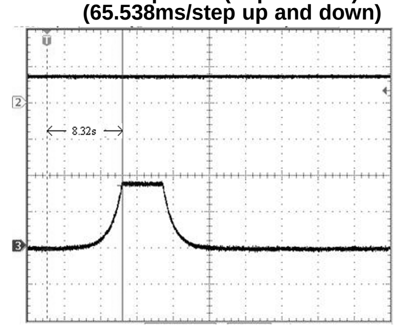
Ramp Rate (Exponential)
(32.768ms/step up and down)



Channel 2: SDA (5V/div)
Channel 3: ILED (10mA/div)
Time Base (2s/div)

Figure 28.

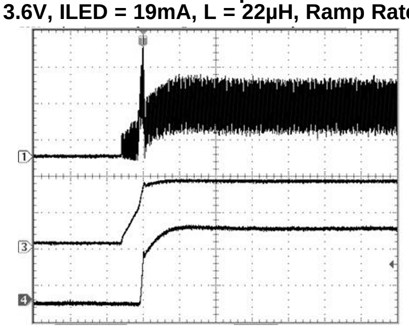
Ramp Rate (Exponential)
(65.538ms/step up and down)



Channel 2: SDA (5V/div)
Channel 3: ILED (10mA/div)
Time Base (4s/div)

Figure 29.

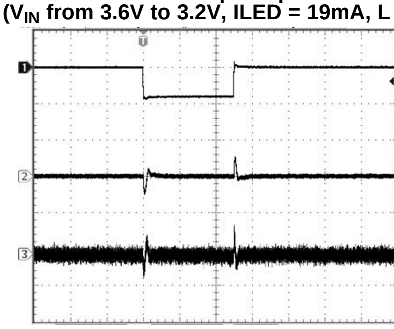
Startup Plot
(V_{IN} = 3.6V, ILED = 19mA, L = 22µH, Ramp Rate = 8µs/step)



Channel 1: IIN (200mA/div)
Channel 3: VOUT (20V/div)
Channel 4 (10mA/div)
Time Base (2ms/div)

Figure 30.

Line Step Response
(V_{IN} from 3.6V to 3.2V, ILED = 19mA, L = 22µH)



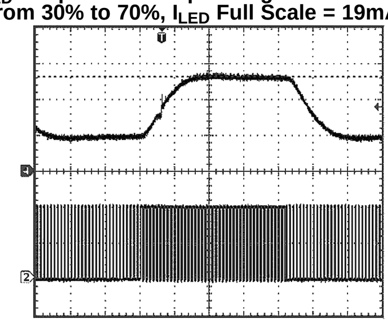
Channel 1: VIN (500mV/div)
Channel 2: VOUT (500mV/div)
Channel 3: ILED (500µA/div)
Time Base (400µs/div)

Figure 31.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are OVSRWAC1R6 from OPTEK Technology, C_{OUT} = 1µF, C_{IN} = 1µF, L = TDK VLF5012ST-100M1R0, (R_L = 0.24Ω), I_{LED} = 19mA, T_A = +25°C unless otherwise specified.

I_{LED} Response to Step Change in PWM Duty Cycle (D_{PWM} from 30% to 70%, I_{LED} Full Scale = 19mA, f_{PWM} = 5kHz)



Channel 4: ILED (5mA/div)
Channel 2: PWM (5V/div)
Time Base (2ms/div)

Figure 32.

OPERATIONAL DESCRIPTION

The LM3530 utilizes an asynchronous step-up, current mode, PWM controller and regulated current sink to provide an efficient and accurate LED current for white LED bias. The device powers a single series string of LEDs with output voltages of up to 40V and a peak inductor current of typically 839mA. The input active voltage range is from 2.7V to 5.5V.

Startup

An internal soft-start prevents large inrush currents during startup that can cause excessive current spikes at the input. For the typical application circuit (using a 10µH inductor, a 2.2µF input capacitor, and a 1µF output capacitor) the average input current during startup ramps from 0 to 300mA in 3ms. See Start Up Plots in the Typical Performance Characteristics.

Light Load Operation

The LM3530's boost converter operates in three modes: continuous conduction, discontinuous conduction, and skip mode. Under heavy loads when the inductor current does not reach zero before the end of the switching period, the device switches at a constant frequency (500kHz typical). As the output current decreases and the inductor current reaches zero before the end of the switching period, the device operates in discontinuous conduction. At very light loads the LM3530 will enter skip mode operation causing the switching period to lengthen and the device to only switch as required to maintain regulation at the output. Light load operation provides for improved efficiency at lighter LED currents compared to continuous and discontinuous conduction. This is due to the pulsed frequency operation resulting in decreased switching losses in the boost converter.

Ambient Light Sensor

The LM3530 incorporates a dual input Ambient Light Sensing interface (ALS1 and ALS2) which translates an analog output ambient light sensor to a user-specified brightness level. The ambient light sensing circuit has 4 programmable boundaries (ZB0 – ZB3) which define 5 ambient brightness zones. Each ambient brightness zone corresponds to a programmable brightness threshold (Z0T – Z4T). The ALS interface is programmable to accept the ambient light information from either the highest voltage of ALS1 or ALS2, the average voltage of ALS1 or ALS2, or selectable from either ALS1 or ALS2.

Furthermore, each ambient light sensing input (ALS1 or ALS2) features 15 internal software selectable voltage setting resistors. This allows the LM3530 the capability of interfacing with a wide selection of ambient light sensors. Additionally, the ALS inputs can be configured as high impedance, thus providing for a true shutdown during low power modes. The ALS resistors are selectable through the ALS Resistor Select Register (see Table 10). Figure 33 shows a functional block diagram of the ambient light sensor input. VSNS represents the active input as described in Table 7 bits [6:5].

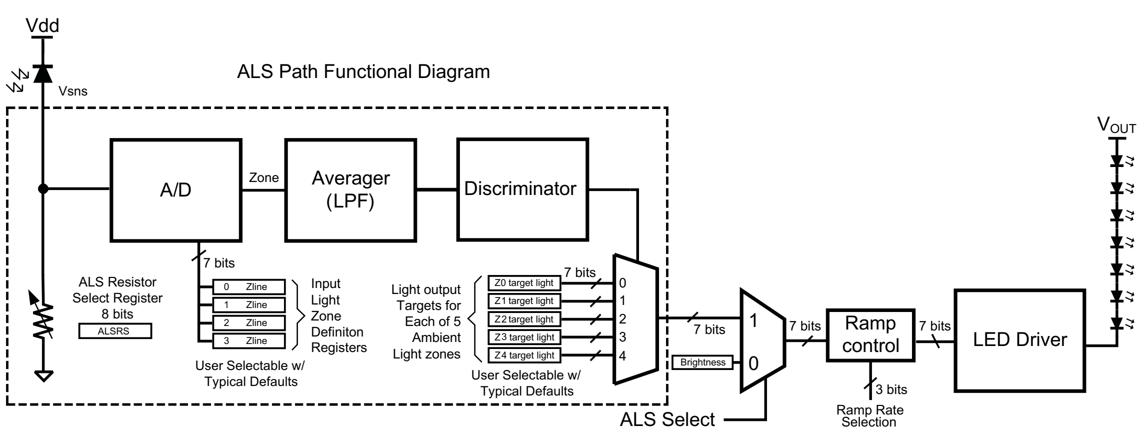


Figure 33. Ambient Light Sensor Functional Block Diagram

ALS Operation

The ambient light sensor input has a 0 to 1V operational input voltage range. The Typical Application Circuit shows the LM3530 with dual ambient light sensors (AVAGO, APDS-9005) and the internal ALS Resistor Select Register set to 0x44 (2.27kΩ). This circuit converts 0 to 1000 LUX light into approximately a 0 to 850mV linear output voltage. The voltage at the active ambient light sensor input (ALS1 or ALS2) is compared against the 8 bit values programmed into the Zone Boundary Registers (ZB0-ZB3). When the ambient light sensor output crosses one of the ZB0 – ZB3 programmed thresholds the internal ALS circuitry will smoothly transition the LED current to the new 7 bit brightness level as programmed into the appropriate Zone Target Register (Z0T – Z4T) (see Figure 34).

The ALS Configuration Register bits [6:5] programs which input is the active input, bits [4:3] control the on/off state of the ALS circuitry, and bits [2:0] control the ALS input averaging time. Additionally, the ALS Information Register is a read-only register which contains a flag (bit 3) which is set each time the active ALS input changes to a new zone. This flag is reset when the register is read back. Bits [2:0] of this register contain the current active zone information.

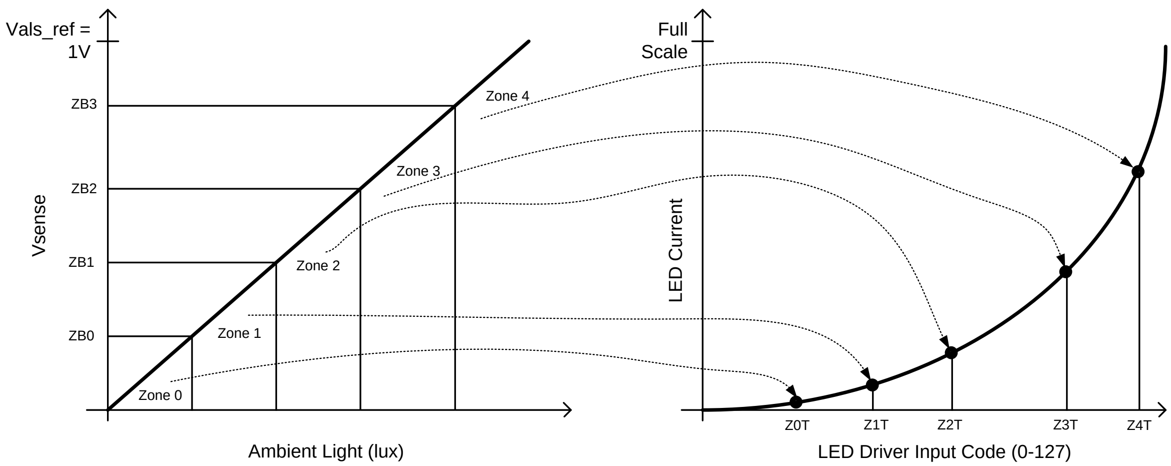


Figure 34. Ambient Light Input to Backlight Mapping

ALS Averaging Time

The ALS Averaging Time is the time over which the Averager block collects samples from the A/D converter and then averages them to pass to the discriminator block (see Figure 33). Ambient light sensor samples are averaged and then further processed by the discriminator block to provide rejection of noise and transient signals. The averager is configurable with 8 different averaging times to provide varying amounts of noise and transient rejection (see Table 6). The discriminator block algorithm has a maximum latency of two averaging cycles; therefore, the averaging time selection determines the amount of delay that will exist between a steady-state change in the ambient light conditions and the associated change of the backlight illumination. For example, the A/D converter samples the ALS inputs at 16kHz. If the averaging time is set to 1024ms then the Averager will send the updated zone information to the discriminator every 1024ms. This zone information contains the average of 16384 samples (1024ms × 16kHz). Due to the latency of 2 averaging cycles, the LED current will not change until there has been a steady-state change in the ambient light for at least 2 averaging periods.

Averager Operation

The magnitude and direction (either increasing or decreasing) of the Averager output is used to determine whether the LM3530 should change brightness zones. The Averager block functions as follows:

1. First, the Averager always begins with a Zone 0 reading stored at startup. If the main display LEDs are active before the ALS block is enabled, it is recommended that the ALS Enable 1 bit is set to '1' at least 3 averaging periods before the ALS Enable 2 bit is set.
2. The Averager will always round down to the lower zone in the event of a non-integer zone average. For

example, if during an averaging period the ALS input transitions between zone's 1 and 2 resulting in an averager output of 1.75, then the averager output will round down to 1 (see Figure 35).

3. The two most current averaging samples are used to make zone change decisions.
4. To make a zone change, data from three averaging cycles are needed. (Starting Value, First Transition, Second Transition or Rest).
5. To Increase the brightness zone, the Averager output must have increased for at least 2 averaging periods or increased and remained at the new level for at least two averaging periods ('+' to '+' or '+' to 'Rest' in Figure 36).
6. To decrease the brightness zone, the Averager output must have decreased for at least 2 averaging periods or decreased and remained at the new level for at least two averaging periods ('-' to '-' or '-' to 'Rest' in Figure 36).

In the case of two consecutive increases or decreases in the Averager output, the LM3530 will transition to zone equal to the last averager output (Figure 36).

Using the diagram for the ALS block (Figure 33), the flow of information is shown in (Figure 37). This starts with the ALS input into the A/D, into the Averager, and then into the Discriminator. Each state filters the previous output to help prevent unwanted zone to zone transitions.

When using the ALS averaging function, it is important to remember that the averaging cycle is free running and is not synchronized with changing ambient lighting conditions. Due to the nature of the averager round down, an increase in brightness can take between 2 and 3 averaging cycles to change zones, while a decrease in brightness can take between 1 and 2 averaging cycles. See Table 7 for a list of possible Averager periods. Figure 38 shows an example of how the perceived brightness change time can vary.

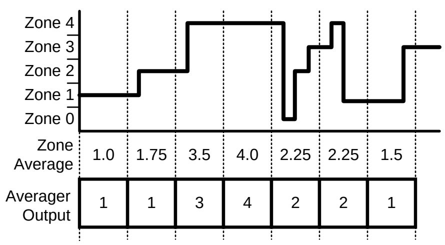


Figure 35. Averager Calculation

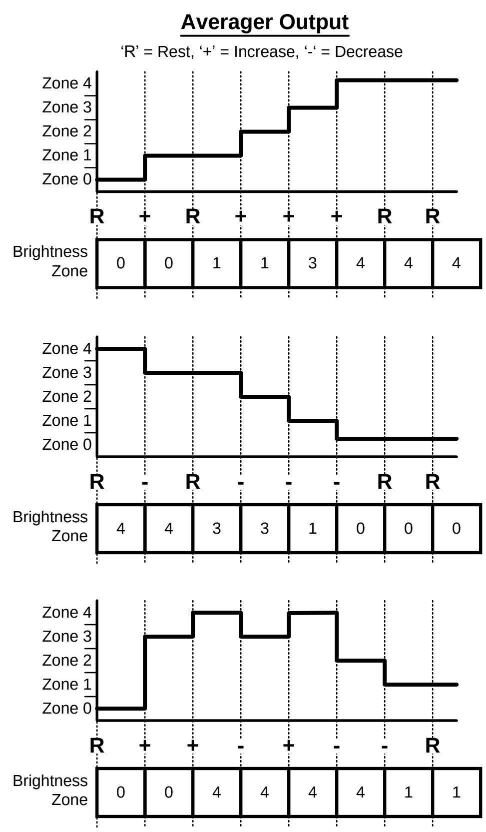


Figure 36. Brightness Zone Change Examples

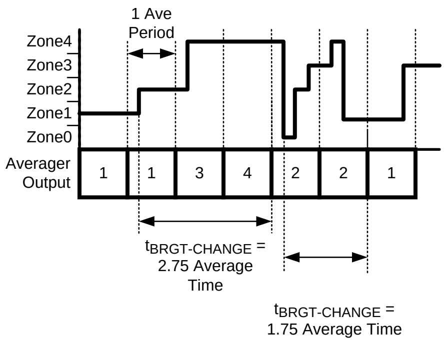


Figure 37. Ambient Light Input to Backlight Transition

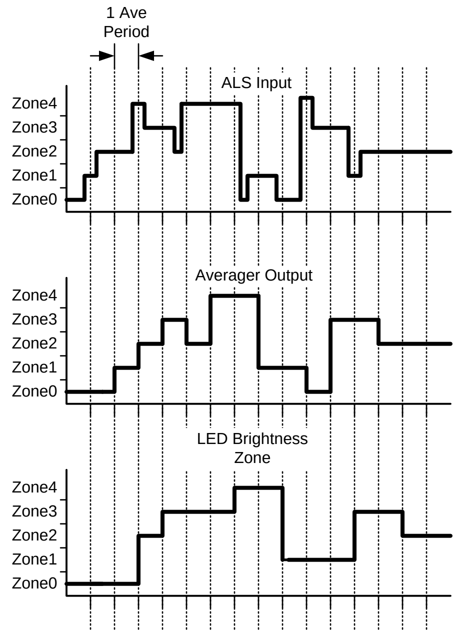


Figure 38. Perceived Brightness Change Time

Zone Boundary Settings

Registers 0x60, 0x61, 0x62, and 0x63 set the 4 zone boundaries (thresholds) for the ALS inputs. These 4 zone boundaries create 5 brightness zones which map over to 5 separate brightness zone targets (see Figure 34). Each 8–bit zone boundary register can set a threshold from typically 0 to 1V with linear step sizes of approximately 1/255 = 3.92mV. Additionally, each zone boundary has built in hysteresis which can be either lower or higher then the programmed Zone Boundary depending on the last direction (either up or down) of the ALS input voltage.

Zone Boundary Trip Points and Hysteresis

For each zone boundary setting, the trip point will vary above or below the nominal set point depending on the direction (either up or down) of the ALS input voltage. This is designed to keep the ALS input from oscillating back and forth between zones in the event that the ALS voltage is residing near to the programmed zone boundary threshold. The Zone Boundary Hysteresis will follow these 2 rules:

1. If the last zone transition was from low to high, then the trip point (V_{TRIP}) will be $V_{ZONE\_BOUNDARY}$ - $V_{HYST}/2$, where $V_{ZONE\_BOUNDARY}$ is the zone boundary set point as programmed into the Zone Boundary registers, and V_{HYST} is typically 7mV.
2. If the last zone transition was from high to low then the trip point (V_{TRIP}) will be $V_{ZONE\_BOUNDARY}$ + $V_{HYST}/2$.

Figure 39 details how the LM3530's ALS Input Zone Boundary Thresholds vary depending on the direction of the ALS input voltage.

Referring to Figure 39, each numbered trip point shown is determined from the direction of the previous ALS zone transition.

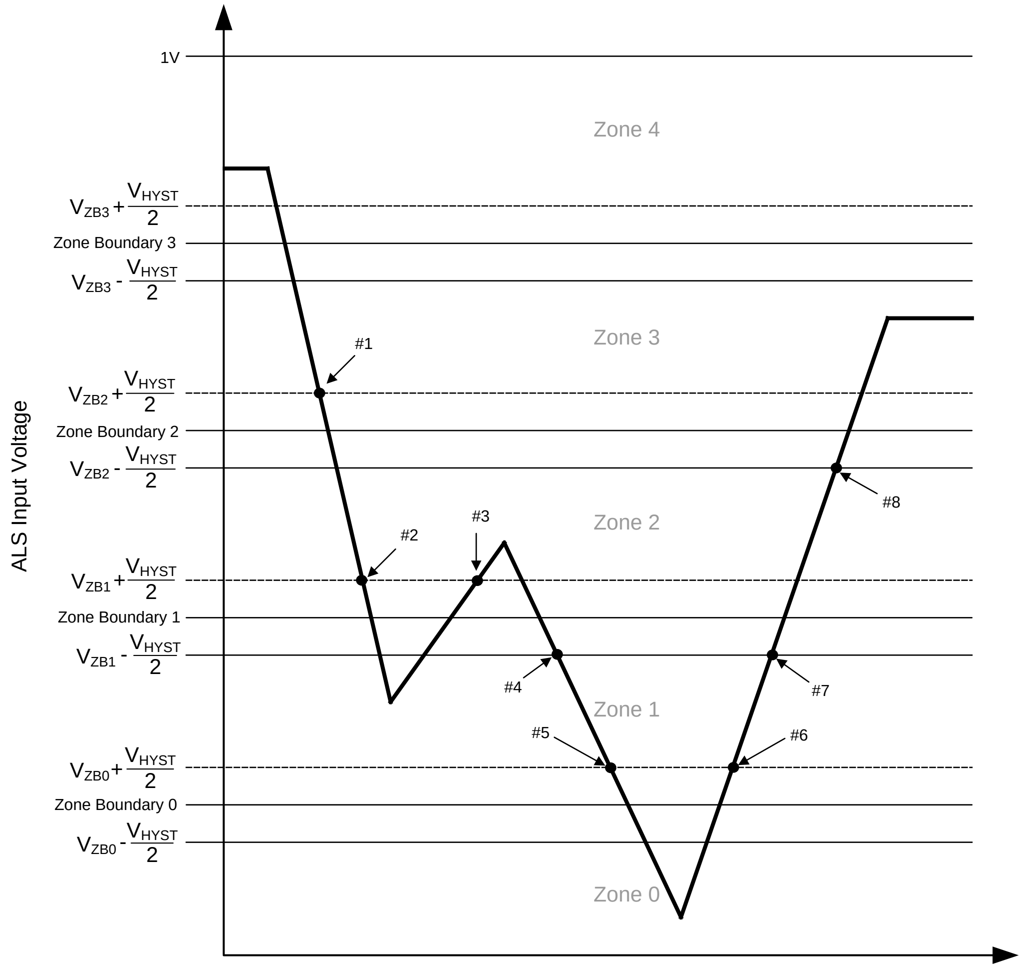


Figure 39. Zone Boundaries With Hysteresis

Minimum Zone Boundary Settings

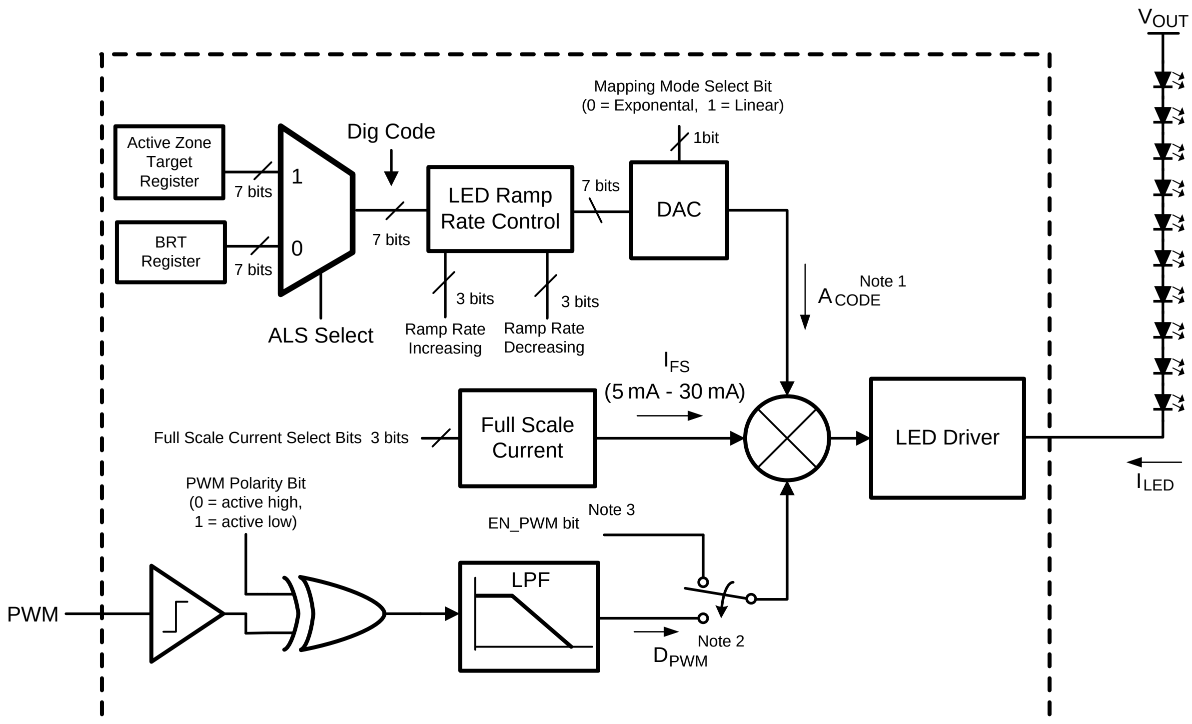
The actual minimum zone boundary setting is code 0x03. Codes of 0x00, 0x01, and 0x02 are all mapped to code 0x03. Table 1 shows the: Zone Boundary codes 0x00 through 0x04, the typical thresholds, and the high and low hysteresis values. The remapping of codes 0x00 - 0x02 plus the additional 4mV of offset voltage is necessary to prevent random offsets and noise on the ALS inputs from creating threshold levels that are below GND. This essentially guarantees that any Zone Boundary threshold selected is achievable with positive ALS voltages.

Table 1. Ideal Zone Boundary Settings with Hysteresis (Lower 5 Codes)

Zone Boundary Code	Typical Zone Boundary Threshold	Typical Threshold + Hysteresis	Typical Threshold - Hysteresis
0x00	15.8mV	19.3mV	12.3mV
0x01	15.8mV	19.3mV	12.3mV
0x02	15.8mV	19.3mV	12.3mV
0x03	15.8mV	19.3mV	12.3mV
0x04	19.7mV	23.2mV	16.2mV

LED Current Control

The LED current is is a function of the Full Scale Current, the Brightness Code, and the PWM input duty cycle. The Brightness Code can either come from the BRT Register (0xA0) in I2C Compatible Current Control, or from the ALS Zone Target Registers (Address 0x70-0x74) in Ambient Light Current Control. Figure 40 shows the current control block diagram.



Note 1: A_{CODE} Is a Scaler between 0 and 1 based on the Brightness Data or Zone Target Data Depending on the ALS Select Bit

Note 2: D_{PWM} Is a Scaler between 0 and 1 and corresponds to the duty cycle of the PWM input signal

Note 3: For EN_PWM bit = 1

$I_{LED} = I_{FS} \times A_{CODE} \times D_{PWM}$

For EN_PWM bit = 0

$I_{LED} = I_{FS} \times A_{CODE}$

Figure 40. Current Control Block Diagram

The following sections describe each of these LED current control methods.

PWM + I^2C-Compatible Current Control

PWM + I^2C-compatible current control is enabled by writing a '1' to the Enable PWM bit (General Configuration Register bit [5]) and writing a '1' to the I^2C Device Enable bit (General Configuration Register bit 0). This makes the LED current a function of the PWM input duty cycle (D), the Full-Scale LED current (I_{LED_FS}), and the % of full-scale LED current . The % of Full-Scale LED current is set by the code in the Brightness Control Register. The LED current using PWM + I^2C-Compatible Control is given by the following equation:

$$I_{LED} = I_{LED\_FS} \times BRT \times D \quad (1)$$

BRT is the percentage of Full Scale Current as set in the Brightness Control Register. The Brightness Control Register can have either exponential or linear brightness mapping depending on the setting of the BMM bit (bit [1] in General Configuration Register).

Exponential or Linear Brightness Mapping Modes

With bit [1] of the General Configuration Register set to 0 (default) exponential mapping is selected and the code in the Brightness Control Register corresponds to the Full-Scale LED current percentages in Table 2 and Figure 41. With bit [1] set to 1 linear mapping is selected and the code in the Brightness Control Register corresponds to the Full-Scale LED current percentages in Table 3 and Figure 42.

PWM Input Polarity

Bit [6] of the General Configuration Register controls the PWM input polarity. Setting this bit to 0 (default) selects positive polarity and makes the LED current (with PWM mode enabled) a function of the positive duty cycle at PWM. With this bit set to '0' the LED current (with PWM mode enabled) becomes a function of the negative duty cycle at PWM.

The PWM input is a logic level input with a frequency range of 400Hz to 50kHz. Internal filtering of the PWM input signal converts the duty cycle information to an average (analog) control signal which directly controls the LED current.

Example: PWM + I^2C-Compatible Current Control

As an example, assume the the General Configuration Register is loaded with (0x2D). From Table 6, this sets up the LM3530 with:

Simple Enable OFF (bit 7 = 0)

Positive PWM Polarity (bit 6 = 0)

PWM Enabled (bit 5 = 1)

Full-Scale Current set at 15.5mA (bits [4:2] = 100)

Brightness Mapping set for Exponential (bit 1 = 0)

Device Enabled via I^2C (bit 0 = 1)

Next, the Brightness Control Register is loaded with 0x73. This sets the LED current to 51.406% of full scale (see Equation 2). Finally, the PWM input is driven with a 0 to 2V pulse waveform at 70% duty cycle. The LED current under these conditions will be:

Where BRT is the percentage of I_{LED_FS} as set in the Brightness Control Register,

$$I_{LED} = I_{LED\_FS} \times BRT \times D = 15.5\text{ mA} \times 51.4\% \times 70\% \approx 5.58\text{ mA}. \quad (2)$$

I^2C-Compatible Current Control Only

I^2C-Compatible Control is enabled by writing a '1' to the I^2C Device Enable bit (bit [0] of the General Configuration Register), a '0' to the Simple Enable bit (bit 7), and a '0' to the PWM Enable bit (bit 5). With bit 5 = 0, the duty cycle information at the PWM input is not used in setting the LED current.

In this mode the LED current is a function of the Full-Scale LED current bits (bits [4:2] of the General Configuration Register) and the code in the Brightness Control Register. The LED current mapping for the Brightness Control Register can be linear or exponential depending on bit [1] in the General Configuration Register (see Exponential or Linear Brightness Mapping Modes section). Using I^2C-Compatible Control Only, the Full-Scale LED Current bits and the Brightness Control Register code provides nearly 1016 possible current levels selectable over the I^2C-compatible interface.

Example: I^2C-Compatible Current Control Only

As an example, assume the General Configuration Register is loaded with 0x15. From Table 6 this sets up the LM3530 with:

Simple Enable OFF (bit 7 = 0)

Positive PWM Polarity (bit 6 = 0)

PWM Disabled (bit 5 = 0)

Full-Scale Current set at 22.5mA (bits [4:2] = 101)

Brightness Mapping set for Exponential (bit 1 = 0)

Device Enabled via I2C (bit 0 = 1)

The Brightness Control Register is then loaded with 0x72 (48.438% of full-scale current from Equation 3). The LED current with this configuration becomes:

$$I_{LED} = I_{LED\_FS} \times BRT = 22.5\ mA \times 0.48438 \approx 10.9\ mA. \quad (3)$$

Where BRT is the % of I_{LED_FS} as set in the Brightness Control Register.

Next, the brightness mapping is set to linear mapping mode (bit [1] in General Configuration Register set to 1). Using the same Full-Scale current settings and Brightness Control Register settings as before, the LED current becomes:

$$I_{LED} = I_{LED\_FS} \times BRT = 22.5\ mA \times 0.8976 \approx 20.2\ mA. \quad (4)$$

Which is higher now since the code in the Brightness Control Register (0x72) corresponds to 89.76% of Full-Scale LED Current due to the different mapping mode given in Figure 41.

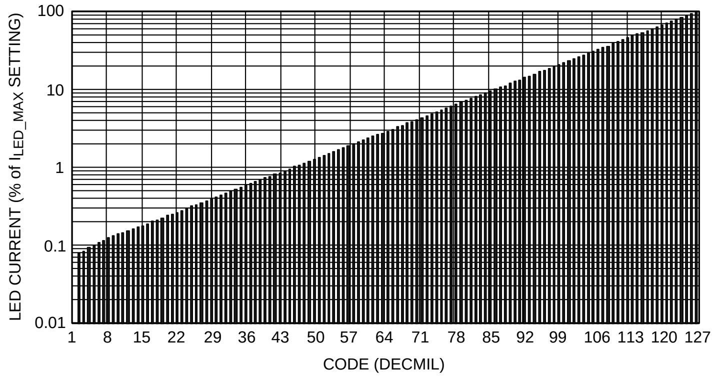


Figure 41. Exponential Brightness Mapping

Table 2. I_{LED} vs. Brightness Register Data (Exponential Mapping)

BRT Data (Hex)	% Full-Scale Current	BRT Data (Hex)	% of Full-Scale Current	BRT Data (Hex)	% of Full-Scale Current	BRT Data (Hex)	% of Full-Scale Current
0x00	0.00%	0x20	0.500%	0x40	2.953%	0x60	17.813%
0x01	0.080%	0x21	0.523%	0x41	3.125%	0x61	18.750%
0x02	0.086%	0x22	0.555%	0x42	3.336%	0x62	19.922%
0x03	0.094%	0x23	0.586%	0x43	3.500%	0x63	20.859%
0x04	0.102%	0x24	0.617%	0x44	3.719%	0x64	22.266%
0x05	0.109%	0x25	0.656%	0x45	3.906%	0x65	23.438%
0x06	0.117%	0x26	0.695%	0x46	4.141%	0x66	24.844%
0x07	0.125%	0x27	0.734%	0x47	4.375%	0x67	26.250%
0x08	0.133%	0x28	0.773%	0x48	4.648%	0x68	27.656%
0x09	0.141%	0x29	0.820%	0x49	4.922%	0x69	29.297%
0x0A	0.148%	0x2A	0.867%	0x4A	5.195%	0x6A	31.172%
0x0B	0.156%	0x2B	0.914%	0x4B	5.469%	0x6B	32.813%
0x0C	0.164%	0x2C	0.969%	0x4C	5.781%	0x6C	34.453%
0x0D	0.172%	0x2D	1.031%	0x4D	6.125%	0x6D	35.547%
0x0E	0.180%	0x2E	1.078%	0x4E	6.484%	0x6E	38.828%
0x0F	0.188%	0x2F	1.148%	0x4F	6.875%	0x6F	41.016%
0x10	0.203%	0x30	1.219%	0x50	7.266%	0x70	43.203%

Table 2. I_{LED} vs. Brightness Register Data (Exponential Mapping) (continued)

BRT Data (Hex)	% Full-Scale Current	BRT Data (Hex)	% of Full-Scale Current	BRT Data (Hex)	% of Full-Scale Current	BRT Data (Hex)	% of Full-Scale Current
0x11	0.211%	0x31	1.281%	0x51	7.656%	0x71	45.938%
0x12	0.227%	0x32	1.359%	0x52	8.047%	0x72	48.438%
0x13	0.242%	0x33	1.430%	0x53	8.594%	0x73	51.406%
0x14	0.250%	0x34	1.523%	0x54	9.063%	0x74	54.141%
0x15	0.266%	0x35	1.594%	0x55	9.609%	0x75	57.031%
0x16	0.281%	0x36	1.688%	0x56	10.078%	0x76	60.703%
0x17	0.297%	0x37	1.781%	0x57	10.781%	0x77	63.984%
0x18	0.320%	0x38	1.898%	0x58	11.250%	0x78	67.813%
0x19	0.336%	0x39	2.016%	0x59	11.953%	0x79	71.875%
0x1A	0.352%	0x3A	2.109%	0x5A	12.656%	0x7A	75.781%
0x1B	0.375%	0x3B	2.250%	0x5B	13.359%	0x7B	79.688%
0x1C	0.398%	0x3C	2.367%	0x5C	14.219%	0x7C	84.375%
0x1D	0.422%	0x3D	2.508%	0x5D	15.000%	0x7D	89.844%
0x1E	0.445%	0x3E	2.648%	0x5E	15.859%	0x7E	94.531%
0x1F	0.469%	0x3F	2.789%	0x5F	16.875%	0x7F	100.00%

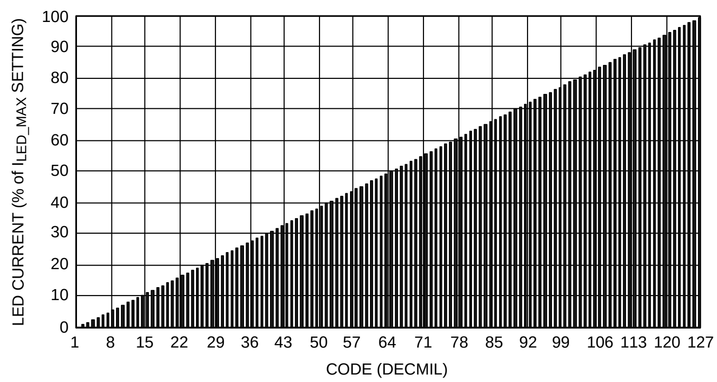


Figure 42. Linear Brightness Mapping

Table 3. I_{LED} vs. Brightness Register Data (Linear Mapping)

BRT Data (Hex)	% Full-Scale Current (Linear)	BRT Data (Hex)	% of Full-Scale Current (Linear)	BRT Data (Hex)	% of Full-Scale Current (Linear)	BRT Data (Hex)	% of Full-Scale Current (Linear)
0x00	0.00%	0x20	25.79%	0x40	50.78%	0x60	75.78%
0x01	1.57%	0x21	26.57%	0x41	51.57%	0x61	76.56%
0x02	2.35%	0x22	27.35%	0x42	52.35%	0x62	77.35%
0x03	3.13%	0x23	28.13%	0x43	53.13%	0x63	78.13%
0x04	3.91%	0x24	28.91%	0x44	53.91%	0x64	78.91%
0x05	4.69%	0x25	29.69%	0x45	54.69%	0x65	79.69%
0x06	5.48%	0x26	30.47%	0x46	55.47%	0x66	80.47%
0x07	6.26%	0x27	31.25%	0x47	56.25%	0x67	81.25%

Table 3. I_{LED} vs. Brightness Register Data (Linear Mapping) (continued)

BRT Data (Hex)	% Full-Scale Current (Linear)	BRT Data (Hex)	% of Full-Scale Current (Linear)	BRT Data (Hex)	% of Full-Scale Current (Linear)	BRT Data (Hex)	% of Full-Scale Current (Linear)
0x08	7.04%	0x28	32.04%	0x48	57.03%	0x68	82.03%
0x09	7.82%	0x29	32.82%	0x49	57.82%	0x69	82.81%
0x0A	8.60%	0x2A	33.60%	0x4A	58.60%	0x6A	83.59%
0x0B	9.38%	0x2B	34.38%	0x4B	59.38%	0x6B	84.38%
0x0C	10.16%	0x2C	35.16%	0x4C	60.16%	0x6C	85.16%
0x0D	10.94%	0x2D	35.94%	0x4D	60.94%	0x6D	85.94%
0x0E	11.72%	0x2E	36.72%	0x4E	61.72%	0x6E	86.72%
0x0F	12.51%	0x2F	37.50%	0x4F	62.50%	0x6F	87.50%
0x10	13.29%	0x30	38.29%	0x50	63.28%	0x70	88.28%
0x11	14.07%	0x31	39.07%	0x51	64.06%	0x71	89.06%
0x12	14.85%	0x32	39.85%	0x52	64.85%	0x72	89.84%
0x13	15.63%	0x33	40.63%	0x53	65.63%	0x73	90.63%
0x14	16.41%	0x34	41.41%	0x54	66.41%	0x74	91.41%
0x15	17.19%	0x35	42.19%	0x55	67.19%	0x75	92.19%
0x16	17.97%	0x36	42.97%	0x56	67.97%	0x76	92.97%
0x17	18.76%	0x37	43.75%	0x57	68.75%	0x77	93.75%
0x18	19.54%	0x38	44.53%	0x58	69.53%	0x78	94.53%
0x19	20.32%	0x39	45.32%	0x59	70.39%	0x79	95.31%
0x1A	21.10%	0x3A	46.10%	0x5A	71.10%	0x7A	96.09%
0x1B	21.88%	0x3B	46.88%	0x5B	71.88%	0x7B	96.88%
0x1C	22.66%	0x3C	47.66%	0x5C	72.66%	0x7C	97.66%
0x1D	23.44%	0x3D	48.44%	0x5D	73.44%	0x7D	98.44%
0x1E	24.22%	0x3E	49.22%	0x5E	74.22%	0x7E	99.22%
0x1F	25.00%	0x3F	50.00%	0x5F	75.00%	0x7F	100.00%

Note: When determining the LED current from (Table 2 and Table 3) there is a typical offset of 113µA with a +/-300µA variation that must be added to the calculated value for codes 0x0A and below. For example, in linear mode with I_{FULL_SCALE} = 19mA and brightness code 0x09 chosen, the nominal current setting is 0.0782 x 19mA = 1.4858mA. Adding in the 113µA typical offset gives 1.4858mA + 0.113mA = 1.5988mA. With the typical +/-300µA range, the high and low currents can be I_{LOW} = 1.2988mA, I_{HIGH} = 1.8988mA. For exponential mode with codes 0x0A and below, this offset and variation error gets divided down by 10 (11.3µA offset with +/-30µA typical range).

Simple Enable Disable With Pwm Current Control

With bits [7 and 5] of the General Configuration Register set to '1' the PWM input is enabled as a simple enable/disable. The simple enable/disable feature operates as described in Figure 43. In this mode, when the PWM input is held high (PWM Polarity bit = 0) for > 2ms the LM3530 will turn on the LED current at the programmed Full-Scale Current × % of Full-Scale Current as set by the code in the Brightness Control Register. When the PWM input is held low for > 2ms the device will shut down. With the PWM Polarity bit = 1 the PWM input is configured for active low operation. In this configuration holding PWM low for > 2ms will turn on the device at the programmed Full-Scale Current × % of Full-Scale Current as set by the code in the Brightness Control Register. Likewise, holding PWM high for > 2ms will put the device in shutdown.

Driving the PWM input with a pulsed waveform at a variable duty cycle is also possible in simple enable/Disable mode, so long as the low pulse width is < 2ms. When a PWM signal is used in this mode the input duty cycle information is internally filtered, and an analog voltage is used to control the LED current. This type of PWM control (PWM to Analog current control) prevents large voltage excursions across the output capacitor that can result in audible noise. Simple Enable/Disable mode can be useful since the default bit setting for the General Configuration Register is 0xCC (Simple Enable bit = 1, PWM Enable = 1, and Full-Scale Current = 19mA). Additionally, the default Brightness Register setting is 0x7F (100% of Full-Scale current). This gives the LM3530 the ability to turn on after power up (or after reset) without having to do any writes to the I^2C-compatible bus.

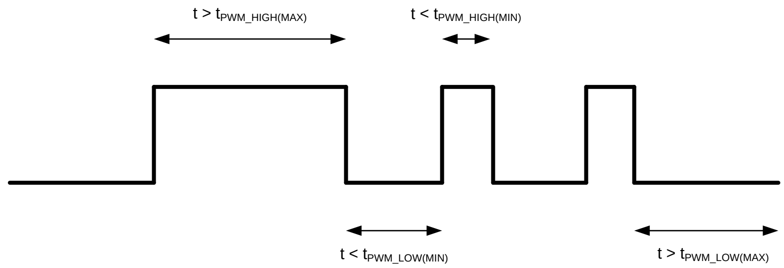


Figure 43. Simple Enable/Disable Timing

Example: Simple Enable Disable with PWM Current Control)

As an example, assume that the HWEN input is toggled low then high. This resets the LM3530 and sets all the registers to their default value. When the PWM input is then pulled high for > 2ms the LED current becomes:

$$I_{LED} = I_{LED\_FS} \times BRT \times D = 19\ mA \times 1.00 \times 100\% \approx 19\ mA. \quad (5)$$

where BRT is the % of I_{LED_FS} as set in the Brightness Control Register.

If then the PWM input is fed with a 5kHz pulsed waveform at 40% duty cycle the LED current becomes:

$$I_{LED} = I_{LED\_FS} \times BRT \times D = 19\ mA \times 1.00 \times 0.4 \approx 7.6\ mA. \quad (6)$$

Then, if the Brightness Control Register is loaded with 0x55 (9.6% of Full-Scale Current) the LED current becomes:

$$I_{LED} = I_{LED\_FS} \times BRT \times D = 19\ mA \times 9.65 \times 0.4 \approx 0.73\ mA. \quad (7)$$

Ambient Light Current Control

With bits [4:3] of the ALS Configuration Register both set to 1, the LM3530 is configured for Ambient Light Current Control. In this mode the ambient light sensing inputs (ALS1, and/or ALS2) monitor the outputs of analog output ambient light sensing photo diodes and adjust the LED current depending on the ambient light. The ambient light sensing circuit has 4 configurable Ambient Light Boundaries (ZB0 – ZB3) programmed through the four (8-bit) Zone Boundary Registers. These zone boundaries define 5 ambient brightness zones (Figure 34). Each zone corresponds to a programmable brightness setting which is programmable through the 5 Zone Target Registers (Z0T – Z4T). When the ALS1, and/or ALS2 input (depending on the bit settings of the ALS Input Select bits) detects that the ambient light has crossed to a new zone (as defined by one of the Zone Boundary Registers) the LED current becomes a function of the Brightness Code loaded in the Zone Target Register which corresponds to the new ambient light brightness zone.

On startup the 4 Zone Boundary Registers are pre-loaded with 0x33 (51d), 0x66 (102d), 0x99 (153d), and 0xCC (204d). Each ALS input has a 1V active input voltage range with a 4mV offset voltage which makes the default Zone Boundaries set at:

Zone Boundary 0 = 1V × 51/255 + 4mV = 204mV

Zone Boundary 1 = 1V × 102/255 + 4mV = 404mV

Zone Boundary 2 = 1V × 153/255 + 4mV = 604mV

Zone Boundary 3 = 1V × 204/255 + 4mV = 804mV

These Zone Boundary Registers are all 8-bit (readable and writable) registers. The first zone (Z0) is defined between 0 and 204mV, Z1's default is defined between 204mV and 404mV, Z2's default is defined between 404mV and 604mV, Z3's default is defined between 604mV and 804mV, and Z4's default is defined between 804mV and 1.004V. The default settings for the 5 Zone Target Registers are 0x19, 0x33, 0x4C, 0x66, and 0x7F. This corresponds to LED brightness settings of 0.336%, 1.43%, 5.781%, 24.844%, and 100% of full-scale current respectively (assuming exponential backlight mapping).

Example: Ambient Light Control Current

As an example, assume that the APDS-9005 is used as the ambient light sensing photo diode with its output connected to the ALS1 input. The ALS Resistor Select Register is loaded with 0x04 which configures the ALS1 input for a 2.27kΩ internal pull-down resistor (see Table 10). The APDS-9005 has a typical 400nA/LUX response. With a 2.27kΩ resistor the sensor output would see a 0 to 908mV swing with a 0 to 1000 LUX change in ambient light. Next, the ALS Configuration Register is programmed with 0x3C. From Table 7, this configures the LM3530's ambient light sensing interface for:

ALS1 as the active ALS input (bits [6:5] = 01)

Ambient Light Current Control Enabled (bit 4 = 1)

ALS circuitry Enabled (bit 3 = 1)

Sets the ALS Averaging Time to 512ms (bits [2:0] = 100)

Next, the General Configuration Register is programmed with 0x19 which sets the Full-Scale Current to 26mA, selects Exponential Brightness Mapping, and enables the device via the I^2C-compatible interface.

Now assume that the APDS-9005 ambient light sensor detects a 100 LUX ambient light at its input. This forces the ambient light sensors output (and the ALS1 input) to 87.5mV corresponding to Zone 0. Since Zone 0 points to the brightness code programmed in Zone Target Register 0 (loaded with code 0x19), the LED current becomes:

$$I_{LED} = I_{LED\_FS} \times \text{ZoneTarget0} = 26\text{ mA} \times 0.336\% \approx 87\ \mu\text{A}. \quad (8)$$

Where the code in Zone Target Register 0 points to the % of ILED_FS as given by Table 2 or Table 3, depending on whether Exponential or Linear Mapping are selected.

Next, assume that the ambient light changes to 500 LUX (corresponding to an ALS1 voltage of 454mV). This moves the ambient light into Zone 2 which corresponds to Zone Target Register 2 (loaded with code 0x4C) the LED current then becomes:

$$I_{LED} = I_{LED\_FS} \text{ x ZoneTarget2} = 26\text{ mA x } 5.781\% \approx 1.5\text{ mA}. \quad (9)$$

Ambient Light Current Control + PWM

The Ambient Light Current Control can also be a function of the PWM input duty cycle. Assume the LM3530 is configured as described in the above Ambient Light Current Control example, but this time the Enable PWM bit set to '1' (General Configuration Register bit [5]).

Example: Ambient Light Current Control + PWM

In this example, the APDS-9005 detects that the ambient light has changed to 1 kLUX. The voltage at ALS1 is now around 908mV and the ambient light falls within Zone 5. This causes the LED brightness to be a function of Zone Target Register 5 (loaded with 0x7F). Now assume the PWM input is also driven with a 50% duty cycle pulsed waveform. The LED current now becomes:

$$I_{LED} = I_{LED\_FS} \text{ x ZoneTarget5 x D} = 26\text{ mA x }100\%\text{ x }50\% \approx 13\text{ mA}.$$

Example: ALS Averaging

As an example, suppose the LM3530's ALS Configuration Register is loaded with 0x3B. This configures the device for:

ALS1 as the active ALS input (bits [6:5] = 01)

Enables Ambient Light Current Control (bit 4 = 1)

Enables the ALS circuitry (bit 3 = 1)

Sets the ALS Averaging Time to 256ms (bits [2:0] = 011)

Next, the ALS Resistor Select Register is loaded with 0x04. This configures the ALS2 input as high impedance and configures the ALS1 input with a 2.27kΩ internal pull-down resistor. The Zone Boundary Registers and Zone Target Registers are left with their default values. The Brightness Ramp Rate Register is loaded with 0x2D. This sets up the LED current ramp rate at 16.384ms/step. Finally, the General Configuration Register is loaded with 0x15. This sets up the device with:

Simple Enable OFF (bit 7 = 0)

PWM Polarity High (bit 6 = 0)

PWM Input Disabled (bit 5 = 0)

Full-Scale Current = 22.5mA (bits [4:2] = 101)

Brightness Mapping Mode as Exponential (bit 1 = 0)

Device Enabled via I^2C (bit 0 = 1)

As the device starts up the APDS-9005 ambient light sensor (connected to the ALS1 input) detects 500 LUX. This puts approximately 437.5mV at ALS1 (see Figure 44). This places the measured ambient light between Zone Boundary Registers 1 and 2, thus corresponding to Zone Target Register 2. The default value for this register is 0x4C. The LED current is programmed to:

$$I_{LED} = I_{LED\_FS} \text{ x ZoneTarget2} = 22.5 \text{ mA x } 5.781\% \approx 1.3 \text{ mA.} \quad (10)$$

Referring to Figure 44, initially the Averager is loaded with Zone 0 so it takes 2 averaging periods for the LM3530 to change to the new zone. After the ALS1 voltage remains at 437.5mV for two averaging periods (end of period #2) the LM3530 sees a repeat of Zone 2 and signals the LED current to begin ramping to Zone 2's target beginning at average period #3. Since the ramp rate is set at 16.384ms/step the LED current goes from 0 to 1.3mA in 76 × 16.384ms = 1.245s (approximately 5 average periods).

After the LED current has been at its steady state of 1.3mA for a while, the ambient light suddenly steps to 900 LUX for 500ms and then steps back to 500 LUX. In this case the 900 LUX will place the ALS1 voltage at approximately 979mV corresponding to Zone 4 somewhere during average period #10 and fall back to 437.5mV somewhere during average period #12. The averager output during period #10 goes to 3, and then during period #11, goes to 4. Since there have been 2 increases in the average during #10 and #11, the beginning of average period #12 shows a change in the brightness zone to Zone 4. This results in the LED current ramping to the new value of 22.5mA (Zone 4's target). During period #12 the ambient light steps back to 500 LUX and forces ALS1 to 437.5mV (corresponding to Zone 2). After average periods #12 and #13 have shown that the averager transitioned lower two times, the brightness zone changes to the new target at the beginning of period #14. This signals the LED current to ramp down to the zone 2 target of 1.3mA. Looking back at average periods #12 and #13, the LED current was only able to ramp up to 7.38mA due to the ramp rate of 16.384ms/step (2 average periods of 256ms each) before it was instructed to ramp back to Zone 2's target at the start of period #14. This example demonstrates not only the averaging feature, but how additional filtering of transient events on the ALS inputs can be accomplished by using the LED current ramp rates.

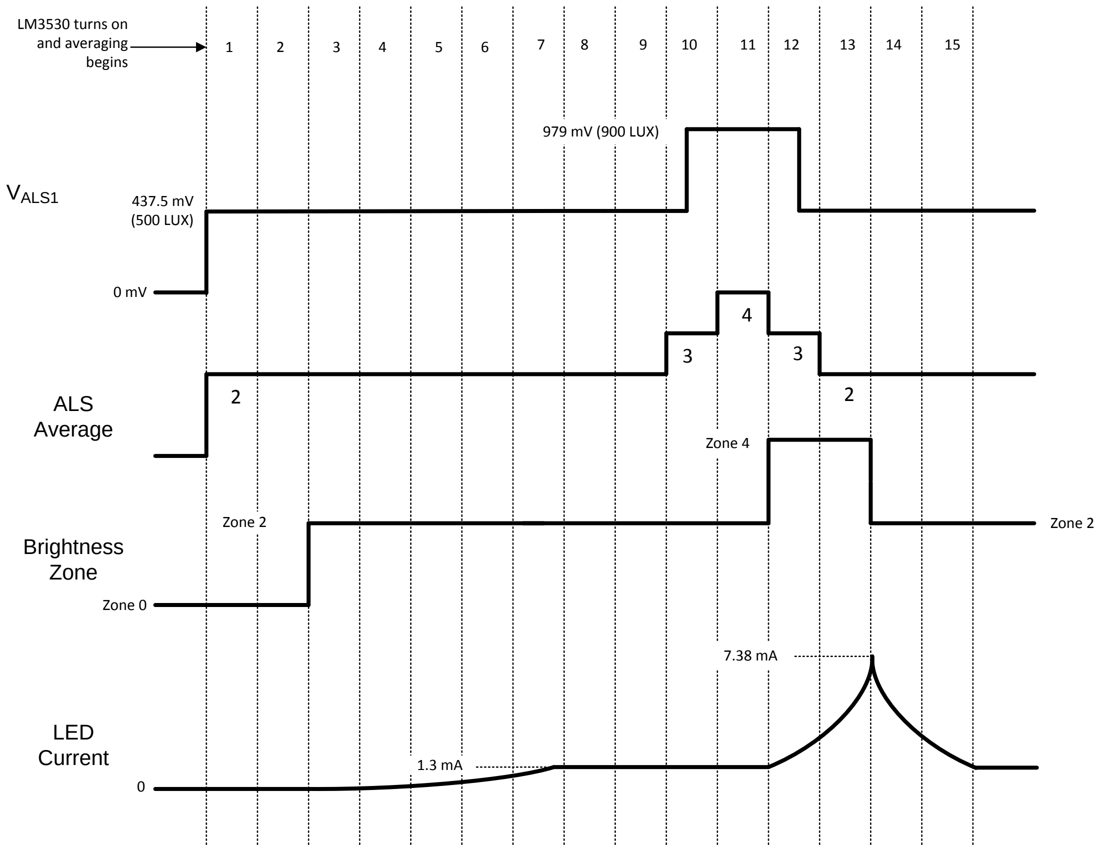


Figure 44. ALS Averaging Example

Interrupt Output

INT is an open-drain output which pulls low when the Ambient Light Sensing circuit has transitioned to a new ambient brightness zone. When a read-back of the ALS Information Register is done INT is reset to the open drain state.

Over-Voltage Protection

Over-voltage protection is set at 40V (minimum) for the LM3530-40 and 23.6V minimum for the LM3530-25. The 40V version allows typically up to 11 series white LEDs (assuming 3.5V per LED + 400mV headroom voltage for the current sink = 38.9V). When the OVP threshold is reached the LM3530's switching converter stops switching, allowing the output voltage to discharge. Switching will resume when the output voltage falls to typically 1V below the OVP threshold. In the event of an LED open circuit the output will be limited to around 40V with a small amount of voltage ripple. The 25V version allows up to 6 series white LEDs (assuming 3.5V per LED + 400mV headroom voltage for the current sink = 21.4V). The 25V OVP option allows for the use of lower voltage and smaller sized (25V) output capacitors. The 40V device would typically require a 50V output capacitor.

Hardware Enable

The HWEN input is an active high hardware enable which must be pulled high to enable the device. Pulling this pin low disables the I^2C-compatible interface, the simple enable/disable input, the PWM input, and resets all registers to their default state (see Table 5).

Thermal Shutdown

In the event the die temperature reaches +140°C, the LM3530 will stop switching until the die temperature cools by 15°C. In a thermal shutdown event the device is not placed in reset; therefore, the contents of the registers are left in their current state.

I^2C-Compatible Interface

Start and Stop Condition

The LM3530 is controlled via an I^2C-compatible interface. START and STOP conditions classify the beginning and the end of the I^2C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I^2C master always generates the START and STOP conditions. The I^2C bus is considered busy after a START condition and free after a STOP condition. During data transmission, the I^2C master can generate repeated START conditions. A START and a repeated START conditions are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

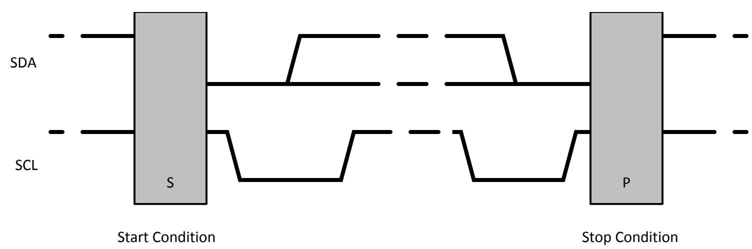


Figure 45. Start and Stop Sequences

I^2C-Compatible Address

The 7bit chip address for the LM3530 is (0x38, or 0x39) for the 40V version and (0x36) for the 25V version. After the START condition, the I^2C master sends the 7-bit chip address followed by an eighth bit (LSB) read or write (R/W). R/W= 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data will be written. The third byte contains the data for the selected register.

MSB			I2C Compatible Address				LSB
0 Bit 7	1 Bit 6	1 Bit 5	1 Bit 4	0 Bit 3	0 Bit 2	0 Bit 1	R/W Bit 0

Figure 46. I^2C-Compatible Chip Address (0x38)

MSB			I2C Compatible Address				LSB
0 Bit 7	1 Bit 6	1 Bit 5	0 Bit 4	1 Bit 3	1 Bit 2	0 Bit 1	R/W Bit 0

Figure 47. I^2C-Compatible Chip Address (0x36)

Table 4. I²C Orderable Device Options

ORDERABLE NUMBER	I2C DEVICE OPTION
LM3530TME-40	0x38
LM3530TMX-40	0x38
LM3530UME-25A	0x36
LM3530UME-40	0x38
LM3530UME-40B	0x39
LM3530UMX-25A	0x36
LM3530UMX-40	0x38
LM3530UMX-40B	0x39

Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master then releases SDA (HIGH) during the 9th clock pulse. The LM3530 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

There are fourteen 8-bit registers within the LM3530 as detailed in Table 5.

Register Descriptions

Table 5. LM3530 Register Definition

Register Name	Function	Address	POR Value
General Configuration	1. Simple Interface Enable 2. PWM Polarity 3. PWM enable 4. Full-Scale Current Selection 5. Brightness Mapping Mode Select 6. I²C Device Enable	0x10	0xB0
ALS Configuration	1. ALS Current Control Enable 2. ALS Input Enable 3. ALS Input Select 4. ALS Averaging Times	0x20	0x2C
Brightness Ramp Rate	Programs the rate of rise and fall of the LED current	0x30	0x00
ALS Zone Information	1. Zone Boundary Change Flag 2. Zone Brightness Information	0x40	0x00
ALS Resistor Select	Internal ALS1 and ALS2 Resistances	0x41	0x00
Brightness Control (BRT)	Holds the 7 bit Brightness Data	0xA0	0x7F
Zone Boundary 0 (ZB0)	ALS Zone Boundary #0	0x60	0x33
Zone Boundary 1 (ZB1)	ALS Zone Boundary #1	0x61	0x66
Zone Boundary 2 (ZB2)	ALS Zone Boundary #2	0x62	0x99
Zone Boundary 3 (ZB3)	ALS Zone Boundary #3	0x63	0xCC
Zone Target 0 (Z0T)	Zone 0 LED Current Data. The LED Current Source transitions to the brightness code in Z0T when the ALS_ input is less than the zone boundary programmed in ZB0.	0x70	0x19
Zone Target 1 (Z1T)	Zone 1 LED Current Data. The LED Current Source transitions to the brightness code in Z1T when the ALS_ input is between the zone boundaries programmed in ZB1 and ZB0.	0x71	0x33

Table 5. LM3530 Register Definition (continued)

Register Name	Function	Address	POR Value
Zone Target 2 (Z2T)	Zone 2 LED Current Data. The LED Current Source transitions to the brightness code in Z2T when the ALS_ input is between the zone boundaries programmed in ZB2 and ZB1.	0x72	0x4C
Zone Target 3 (Z3T)	Zone 3 LED Current Data. The LED Current Source transitions to the brightness code in Z3T when the ALS_ input is between the zone boundaries programmed in ZB3 and ZB2.	0x73	0x66
Zone Target 4 (Z4T)	Zone 4 LED Current Data. The LED Current Source transitions to the brightness code in Z4T when the ALS_ input is between the zone boundaries programmed in ZB4 and ZB3.	0x74	0x7F

*Note: Unused bits in the LM3530's Registers default to a logic '1'.

General Configuration Register (GP)

The General Configuration Register (address 0x10) is described in Figure 48 and Table 6.

General Configuration Register
Address 0x10, Default Value 0xB0

MSB							LSB
Bit 7 Simple Interface Enable	Bit 6 PWM Polarity	Bit 5 PWM Enable	Bit 4 Full Scale Current Select	Bit 3 Full Scale Current Select	Bit 2 Full Scale Current Select	Bit 1 Brightness Mapping Mode Select	Bit 0 I2C Interface Enable

Figure 48. General Configuration Register

Table 6. General Configuration Register Description (0x10)

Bit 7 (PWM Simple Enable	Bit 6 (PWM Polarity)	Bit 5 (EN_PWM) see Figure 38	Bit 4 (Full-Scale Current Select)	Bit 3 (Full-Scale Current Select)	Bit 2 (Full-Scale Current Select)	Bit 1 (Mapping Mode Select)	Bit 0 (I^2C Device Enable)
0 = Simple Interface at PWM Input is Disabled 1 = Simple Interface at PWM Input is Enabled	0 = PWM active high 1 = PWM active low	0 = LED current is not a function of PWM duty cycle 1 = LED current is a function of duty cycle	000 = 5 mA full-scale current 001 = 8.5 mA full-scale current 010 = 12 mA full-scale current 011 = 15.5 mA full-scale current 100 = 19 mA full-scale current 101 = 22.5 mA full-scale current 110 = 26 mA full-scale current 111 = 29.5 mA full-scale current			0 = exponential mapping 1 = linear mapping	0 = Device Disabled 1 = Device Enabled

ALS Configuration Register

The ALS Configuration Register controls the Ambient Light Sensing input functions and is described in Figure 49 and Table 7.

ALS Configuration Register
Address 0x20, Default Value 0x2C

MSB							LSB
Bit 7 (Not Used)	Bit 6 ALS Input Select 2	Bit 5 ALS Input Select 1	Bit 4 ALS Mode	Bit 3 ALS Enable	Bit 2 ALS Averaging Time	Bit 1 ALS Averaging Time	Bit 0 ALS Averaging Time

Figure 49. ALS Configuration Register

Table 7. ALS Configuration Register Description (0x20)

Bit 7	Bit 6 ALS Input Select	Bit 5 ALS Input Select	Bit 4 ALS Enable	Bit 3 ALS Enable	Bit 2 ALS Averaging Time	Bit 1 ALS Averaging Time	Bit 0 ALS Averaging Time
N/A	00 = The Average of ALS1 and ALS2 is used to control the LED brightness 01 = ALS1 is used to control the LED brightness 10 = ALS2 is used to control the LED brightness 11 = The ALS input with the highest voltage is used to control the LED brightness		00 or 10 = ALS is **disabled.** The Brightness Register is used to determine the LED current. 01 = ALS is **enabled.** The Brightness Register is used to determine the LED Current. 11 = ALS inputs are **enabled.** Ambient light determines the LED current.		000 = 32 ms 001 = 64 ms 010 = 128 ms 011 = 256 ms 100 = 512 ms 101 = 1024 ms 110 = 2048 ms 111 = 4096 ms		

Brightness Ramp Rate Register

The Brightness Ramp Rate Register controls the rate of rise or fall of the LED current. Both the rising rate and falling rate are independently adjustable Figure 50 and Table 8 describe the bit settings.

Brightness Ramp Rate Register
Address 0x30, Default Value 0x00

MSB							LSB
Bit 7 Not Used	Bit 6 Not Used	Bit 5 BRRI2	Bit 4 BRRI1	Bit 3 BRRI0	Bit 2 BRRD2	Bit 1 BRRD1	Bit 0 BRRD0

Figure 50. Brightness Ramp Rate Register

Table 8. Brightness Ramp Rate Register Description (0x30)

Bit 7	Bit 6	Bit 5 (BRRI2)	Bit 4 (BRRI1)	Bit 3 (BRRI0)	Bit 2 (BRRD2)	Bit 1 (BRRD1)	Bit 0 (BRRD0)
N/A	N/A	000 = 8 µs/step (1.106ms from 0 to Full Scale) 001 = 1.024 ms/step (130ms from 0 to Full Scale) 010 = 2.048 ms/step (260ms from 0 to Full Scale) 011 = 4.096 ms/step (520ms from 0 to Full Scale) 100 = 8.192 ms/step (1.04s from 0 to Full Scale) 101 = 16.384 ms/step (2.08s from 0 to Full Scale) 110 = 32.768 ms/step (4.16s from 0 to Full Scale) 111 = 65.538 ms/step (8.32s from 0 to Full Scale)			000 = 8 µs/step (1.106ms from Full Scale to 0) 001 = 1.024 ms/step (130ms from Full Scale to 0) 010 = 2.048 ms/step (260ms from Full Scale to 0) 011 = 4.096 ms/step (520ms from Full Scale to 0) 100 = 8.192 ms/step (1.04s from Full Scale to 0) 101 = 16.384 ms/step (2.08s from Full Scale to 0) 110 = 32.768 ms/step (4.16s from Full Scale to 0) 111 = 65.538 ms/step (8.32s from Full Scale to 0)		

ALS Zone Information Register

The ALS Zone Information Register is a read-only register that is updated every time the active ALS input(s) detect that the ambient light has changed to a new zone as programmed in the Zone Boundary Registers. See Zone Boundary Register description. A new update to the ALS Zone Information Register is signaled by the INT output going from high to low. A read-back of the ALS Zone Information Register will cause the INT output to go open-drain again. The Zone Change Flag (bit 3) is also updated on a Zone change and cleared on a read back of the ALS Zone Information Register. Figure 51 and Table 9 detail the ALS Zone Information Register.

ALS Zone Information Register
Address 0x40, Default Value 0x00

MSB							LSB
Bit 7 (Not Used)	Bit 6 (Not Used)	Bit 5 (Not Used)	Bit 4 (Not Used)	Bit 3 Zone Boundry Change Flag	Bit 2 Z2 Zone Data	Bit 1 Z1 Zone Data	Bit 0 Z0 Zone Data

Figure 51. ALS Zone Information Register

Table 9. ALS Zone Information Register Description (0x40)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3 (Zone Boundary Change Flag)	Bit 2 (Z2)	Bit 1 (Z1)	Bit 0 (Z0)
N/A	N/A	N/A	N/A	1 = the active ALS input has changed to a new ambient light zone as programmed in the Zone Boundary Registers (ZB0 -ZB3) 0 = no zone change	000 = Zone 0 001 = Zone 1 010 = Zone 2 011 = Zone 3 100 = Zone 4		

ALS Resistor Select Register

The ALS Resistor Select Register configures the internal resistance from either the ALS1 or ALS2 input to GND. Bits [3:0] program the input resistance at the ALS1 input and bits [7:4] program the input resistance at the ALS2 input. With bits [3:0] set to all zeroes the ALS1 input is high impedance. With bits [7:4] set to all zeroes the ALS2 input is high impedance.

ALS Resistor Select Register
Address 0x41, Default Value 0x00

MSB							LSB
Bit 7 ALSR2A	Bit 6 ALSR2B	Bit 5 ALSR2C	Bit 4 ALSR2D	Bit 3 ALSR1A	Bit 2 ALSR1B	Bit 1 ALSR1C	Bit 0 ALSR1D

Figure 52. ALS Resistor Select Register

Table 10. ALS Resistor Select Register Description (0x41)

Bit 7 (ALSR2A)	Bit 6 (ALSR2B)	Bit 5 (ALSR2C)	Bit 4 (ALSR2D)	Bit 3 (ALSR1A)	Bit 2 (ALSR1B)	Bit 1 (ALSR1C)	Bit 0 (ALSR1D)
0000 = ALS2 is high impedance 0001 = 13.531kΩ (73.9µA at 1V) 0010 =9.011kΩ (111µA at 1V) 0011 = 5.4116kΩ (185µA at 1V) 0100 = 2.271kΩ (440µA at 1V) 0101 = 1.946kΩ (514µA at 1V) 0110 = 1.815kΩ (551µA at 1V) 0111 = 1.6kΩ (625µA at 1V) 1000 = 1.138kΩ (879µA at 1V) 1001 = 1.05kΩ (952µA at 1V) 1010 = 1.011kΩ (989µA at 1V) 1011 = 941Ω (1.063mA at 1V) 1100 = 759Ω (1.318mA at 1V) 1101 = 719Ω (1.391mA at 1V) 1110 =700Ω (1.429mA at 1V) 1111 = 667Ω (1.499mA at 1V)				0000 = ALS2 is high impedance 0001 = 13.531kΩ (73.9µA at 1V) 0010 =9.011kΩ (111µA at 1V) 0011 = 5.4116kΩ (185µA at 1V) 0100 = 2.271kΩ (440µA at 1V) 0101 = 1.946kΩ (514µA at 1V) 0110 = 1.815kΩ (551µA at 1V) 0111 = 1.6kΩ (625µA at 1V) 1000 = 1.138kΩ (879µA at 1V) 1001 = 1.05kΩ (952µA at 1V) 1010 = 1.011kΩ (989µA at 1V) 1011 = 941Ω (1.063mA at 1V) 1100 = 759Ω (1.318mA at 1V) 1101 = 719Ω (1.391mA at 1V) 1110 =700Ω (1.429mA at 1V) 1111 = 667Ω (1.499mA at 1V)			

Brightness Control Register

The Brightness Register (BRT) is an 8-bit register that programs the 127 different LED current levels (Bits [6:0]). The code written to BRT is translated into an LED current as a percentage of $I_{LED\_FULLSCALE}$ as set via the Full-Scale Current Select bits (General Configuration Register bits [4:2]). The LED current response has a typical 1000:1 dimming ratio at the maximum full-scale current (General Configuration Register bits [4:2] = (111) and using the exponential weighted dimming curve.

There are two selectable LED current profiles. Setting the General Configuration Register bit 1 to 0 selects the exponentially weighted LED current response (see Figure 41). Setting this bit to '1' selects the linear weighted curve (see Figure 42). Table 2 and Table 3 show the percentage Full-Scale LED Current at a given Brightness Register Code for both the Exponential and Linear current response.

Brightness Control Register
Address 0xA0, Default Value 0x7F

MSB							LSB
Bit 7 (Not Used)	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Figure 53. Brightness Control Register

Table 11. Brightness Control Register Description (0xA0)

Bit 7 N/A	Bit 6 Data (MSB)	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data
	LED Brightness Data (Bits [6:0])						
	Exponential Mapping (see Table 2) 0000000 = LEDs Off 0000001 = 0.08% of Full Scale : : : 1111111 = 100% of Full Scale			**Linear Mapping** (see Table 3) 0000000 = LEDs Off 0000001 = 0.79% of Full Scale : : : 1111111 = 100% of Full Scale			

Zone Boundary Register

The Zone Boundary Registers are programmed with the ambient light sensing zone boundaries. The default values are set at 20% (200mV), 40% (400mV), 60% (600mV), and 80% (800mV) of the full-scale ALS input voltage range (1V). The necessary conditions for proper ALS operation are that the data in ZB0 < data in ZB1 < data in ZB2 < data in ZB3.

Zone Boundary Register 0 (ZB0)
Address 0x60, Default Value 0x33

MSB							LSB
Bit 7 Data	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Zone Boundary Register 1 (ZB1)
Address 0x61, Default Value 0x66

MSB							LSB
Bit 7 Data	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Zone Boundary Register 2 (ZB2)
Address 0x62, Default Value 0x99

MSB							LSB
Bit 7 Data	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Zone Boundary Register 3 (ZB3)
Address 0x63, Default Value 0xCC

MSB							LSB
Bit 7 Data	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Figure 54. Zone Boundary Registers

Zone Target Registers

The Zone Target Registers contain the LED brightness data that corresponds to the current active ALS zone. The default values for these registers and their corresponding percentage of full-scale current for both linear and exponential brightness is shown in Figure 55 and Table 12.

Zone Target Register 0 (ZT0)
Address 0x70, Default Value 0x19

MSB							LSB
N/A	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Zone Target Register 1 (ZT1)
Address 0x71, Default Value 0x33

MSB							LSB
N/A	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Zone Target Register 2 (ZT2)
Address 0x72, Default Value 0x4C

MSB							LSB
N/A	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Zone Target Register 3 (ZT3)
Address 0x73, Default Value 0x66

MSB							LSB
N/A	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Zone Target Register 4 (ZT4)
Address 0x74, Default Value 0x7F

MSB							LSB
N/A	Bit 6 Data	Bit 5 Data	Bit 4 Data	Bit 3 Data	Bit 2 Data	Bit 1 Data	Bit 0 Data

Figure 55. Zone Target Registers

Table 12. Zone Boundary and Zone Target Default Mapping

Zone Boundary (Default)	Zone Target Register (Default)	Full-Scale Current (Default)	Linear Mapping (Default)	Exponential Mapping (Default)
Boundary 0, Active ALS input is less than 200 mV	0x19	19 mA	19.69% (3.74 µA)	0.336% (68.4 µA)
Boundary 1, Active ALS input is between 200 mV and 400 mV	0x33	19 mA	40.16% (7.63 µA)	1.43% (272 µA)
Boundary 2, Active ALS input is between 400 mV and 600 mV	0x4C	19 mA	59.84% (11.37 mA)	5.78% (1.098 mA)
Boundary 3, Active ALS input is between 600 mV and 800 mV	0x66	19 mA	80.31% (15.26 mA)	24.84% (4.72 mA)
Boundary 4, Active ALS input is greater than 800mV	0x7F	19 mA	100% (19 mA)	100% (19 mA)

Applications Information

Led Current Setting/Maximum LED Current

The maximum LED current is restricted by the following factors: the maximum duty cycle that the boost converter can achieve, the peak current limitations, and the maximum output voltage.

Maximum Duty Cycle

The LM3530 can achieve up to typically 94% maximum duty cycle. Two factors can cause the duty cycle to increase: an increase in the difference between V_{OUT} and V_{IN} and a decrease in efficiency. This is shown by the following equation:

$$D = 1 - \frac{VIN \times \eta}{VOUT} \quad (11)$$

For a 9-LED configuration V_{OUT} = (3.6V x 9LED + VHR) = 33V operating with η = 70% from a 3V battery, the duty cycle requirement would be around 93.6%. Lower efficiency or larger V_{OUT} to V_{IN} differentials can push the duty cycle requirement beyond 94%.

Peak Current Limit

The LM3530's boost converter has a peak current limit for the internal power switch of 839mA typical (739mA minimum). When the peak switch current reaches the current limit, the duty cycle is terminated resulting in a limit on the maximum output current and thus the maximum output power the LM3530 can deliver. Calculate the maximum LED current as a function of V_{IN}, V_{OUT}, L, efficiency (η) and I_{PEAK} as:

$$I_{OUT\_MAX} = \frac{(I_{PEAK} - \Delta I_L) \times \eta \times V_{IN}}{V_{OUT}}$$

$$\text{where } \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (12)$$

where f_{SW} = 500 kHz,and η and I_{PEAK} can be found in the efficiency and I_{PEAK} curves in the *Typical Performance Characteristics*.

Output Voltage Limitations

The LM3530 has a maximum output voltage of 41V typical (40V minimum) for the LM3530-40 version and 24V typical (23.6V minimum) for the 25V version. When the output voltage rises above this threshold (V_{OVP}) the over-voltage protection feature is activated and the duty cycle is terminated. Switching will cease until V_{OUT} drops below the hysteresis level (typically 1V below V_{OVP}). For larger numbers of series connected LEDs the output voltage can reach the OVP threshold at larger LED currents and colder ambient temperatures. Typically white LEDs have a -3mV/°C temperature coefficient.

Output Capacitor Selection

The LM3530's output capacitor has two functions: filtering of the boost converters switching ripple, and to ensure feedback loop stability. As a filter, the output capacitor supplies the LED current during the boost converters on time and absorbs the inductor's energy during the switch off time. This causes a sag in the output voltage during the on time and a rise in the output voltage during the off time. Because of this, the output capacitor must be sized large enough to filter the inductor current ripple that could cause the output voltage ripple to become excessive. As a feedback loop component, the output capacitor must be at least 1µF and have low ESR otherwise the LM3530's boost converter can become unstable. This requires the use of ceramic output capacitors. Table 13 lists part numbers and voltage ratings for different output capacitors that can be used with the LM3530.

Table 13. Recommended Input/Output Capacitors

Manufacturer	Part Number	Value	Size	Rating	Description
Murata	GRM21BR71H105KA12	1µF	0805	50V	COUT
Murata	GRM188B31A225KE33	2.2µF	0805	10V	CIN
TDK	C1608X5R0J225	2.2µF	0603	6.3V	CIN

Inductor Selection

The LM3530 is designed to work with a 10µH to 22µH inductor. When selecting the inductor, ensure that the saturation rating for the inductor is high enough to accommodate the peak inductor current . The following equation calculates the peak inductor current based upon LED current, V_{IN}, V_{OUT}, and Efficiency.

$$I_{PEAK} = \frac{I_{LED}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad (13)$$

where:

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (14)$$

When choosing L, the inductance value must also be large enough so that the peak inductor current is kept below the LM3530's switch current limit. This forces a lower limit on L given by the following equation.

$$L > \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times V_{OUT} \times \left(I_{SW\_MAX} - \frac{I_{LED\_MAX} \times V_{OUT}}{\eta \times V_{IN}} \right)} \quad (15)$$

I_{SW_MAX} is given in the Electrical Table, efficiency (η) is shown in the Typical Performance Characteristics, and f_{SW} is typically 500kHz.

Table 14. Suggested Inductors

Manufacturer	Part Number	Value	Size	Rating	DC Resistance
TDK	VLF3014ST-100MR82	10µH	2.8mm × 3mm × 1.4mm	820mA	0.25Ω
TDK	VLF3010ST-220MR34	22µH	2.8mm × 3mm × 1mm	340mA	0.81Ω
TDK	VLF3010ST-100MR53	10µH	2.8mm × 3mm × 1mm	530mA	0.41Ω
TDK	VLF4010ST-100MR80	10µH	2.8mm × 3mm × 1mm	800mA	0.25Ω
TDK	VLS252010T-100M	10µH	2.5mm × 2mm × 1mm	650mA	0.71Ω
Coilcraft	LPS3008-103ML	10µH	2.95mm × 2.95mm × 0.8mm	520mA	0.65Ω
Coilcraft	LPS3008-223ML	22µH	2.95mm × 2.95mm × 0.8mm	340mA	1.5Ω
Coilcraft	LPS3010-103ML	10µH	2.95mm × 2.95mm × 0.9mm	550mA	0.54Ω
Coilcraft	LPS3010-223ML	22µH	2.95mm × 2.95mm × 0.9mm	360mA	1.2Ω
Coilcraft	XPL2010-103ML	10µH	1.9mm × 2mm × 1mm	610mA	0.56Ω
Coilcraft	EPL2010-103ML	10µH	2mm × 2mm × 1mm	470mA	0.91Ω
TOKO	DE2810C-1117AS-100M	10µH	3mm × 3.2mm × 1mm	600mA	0.46Ω

Diode Selection

The diode connected between SW and OUT must be a Schottky diode and have a reverse breakdown voltage high enough to handle the maximum output voltage in the application. Table 15 lists various diodes that can be used with the LM3530. For 25V OVP devices a 30V Schottky is adequate. For 40V OVP devices, a 40V Schottky diode should be used.

Table 15. Suggested Diodes

Manufacturer	Part Number	Value	Size	Rating
Diodes Inc	B0540WS	Schottky	SOD-323 ()	40V/500mA
Diodes Inc	SDM20U40	Schottky	SOD-523 (1.2mm × 0.8mm × 0.6mm)	40V/200mA
On Semiconductor	NSR0340V2T1G	Schottky	SOD-523 (1.2mm × 0.8mm × 0.6mm)	40V/250mA
On Semiconductor	NSR0240V2T1G	Schottky	SOD-523 (1.2mm × 0.8mm × 0.6mm)	40V/250mA

Board Layout Guidelines

The LM3530 contains an inductive boost converter which sees a high switched voltage (up to 40V) at the SW pin, and a step current (up to 900mA) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OVP pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 56 highlights these two noise generating components.

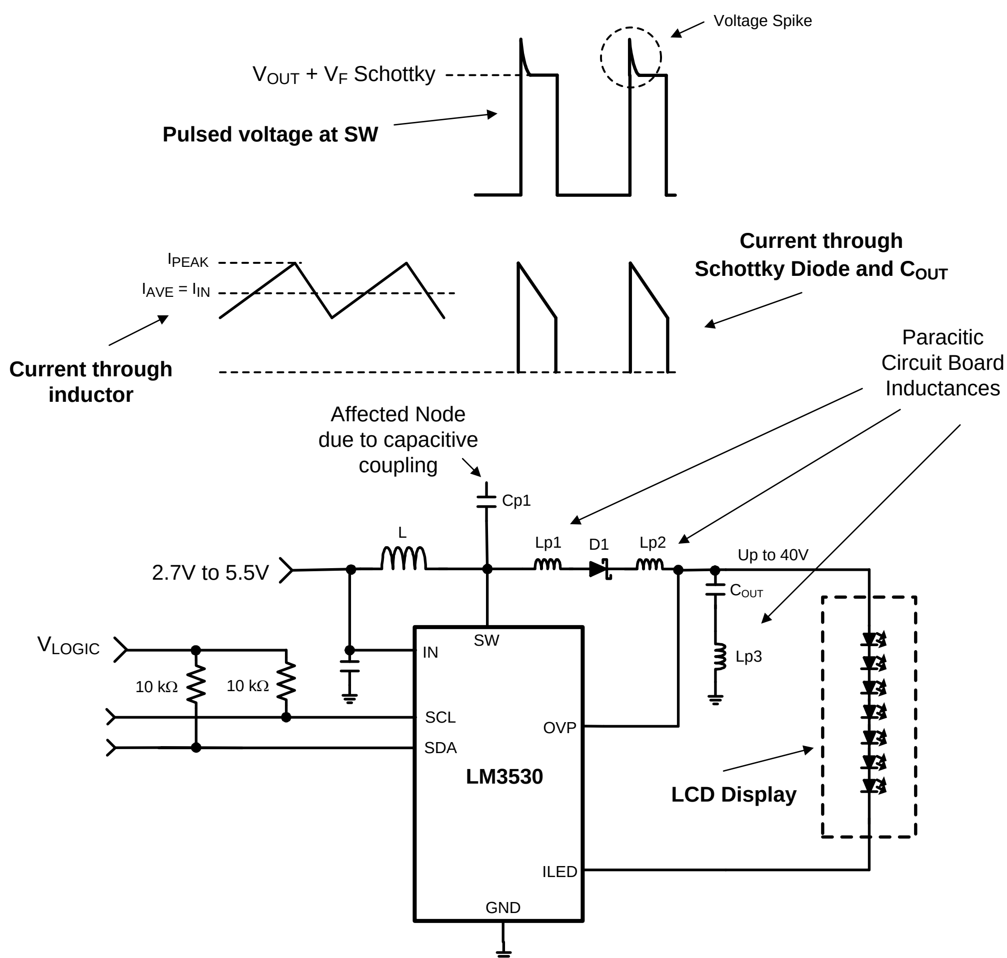


Figure 56. LM3530's Boost Converter Showing Pulsed Voltage at SW (High dV/dt) and Current Through Schottky and C_{OUT} (High dI/dt)

The following lists the main (layout sensitive) areas of the LM3530 in order of decreasing importance:

Output Capacitor

- Schottky Cathode to C_{OUT}+
- C_{OUT}- to GND

Schottky Diode

- SW Pin to Schottky Anode
- Schottky Cathode to $_{COUT}$+

Inductor

- SW Node PCB capacitance to other traces

Input Capacitor

- CIN+ to IN pin
- CIN- to GND

Output Capacitor Placement

The output capacitor is in the path of the inductor current discharge path. As a result C_{OUT} sees a high current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through C_{OUT} and back into the LM3530's GND pin will contribute to voltage spikes ($V_{SPIKE} = L_{P\_} \times dI/dt$) at SW and OUT which can potentially over-voltage the SW pin, or feed through to GND. To avoid this, C_{OUT}+ must be connected as close as possible to the Cathode of the Schottky diode and C_{OUT}- must be connected as close as possible to the LM3530's GND bump. The best placement for C_{OUT} is on the same layer as the LM3530 so as to avoid any vias that can add excessive series inductance (see Figure 58, Figure 59, and Figure 60).

Schottky Diode Placement

The Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode will cause a voltage spike ($V_{SPIKE} = L_{P\_} \times dI/dt$) at SW and OUT which can potentially over-voltage the SW pin, or feed through to V_{OUT} and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to C_{OUT}+ will reduce the inductance ($L_{P\_}$) and minimize these voltage spikes (see Figure 58, Figure 59 , and Figure 60).

Inductor Placement

The node where the inductor connects to the LM3530’s SW bump has 2 issues. First, a large switched voltage (0 to $V_{OUT} + V_{F\_SCHOTTKY}$) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause large voltage drops that will negatively affect efficiency.

To reduce the capacitively coupled signal from SW into nearby traces, the SW bump to inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, the other traces need to be routed away from SW and not directly beneath. This is especially true for high impedance nodes that are more susceptible to capacitive coupling such as (SCL, SDA, HWEN, PWM, and possibly ASL1 and ALS2). A GND plane placed directly below SW will dramatically reduce the capacitive coupling from SW into nearby traces

To limit the trace resistance of the VBATT to inductor connection and from the inductor to SW connection, use short, wide traces (see Figure 58, Figure 59 , and Figure 60).

Input Capacitor Selection and Placement

The input bypass capacitor filters the inductor current ripple, and the internal MOSFET driver currents during turn on of the power switch.

The driver current requirement can range from 50mA at 2.7V to over 200mA at 5.5V with fast durations of approximately 10ns to 20ns. This will appear as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical since any series inductance between IN and C_{IN}+ or C_{IN}- and GND can create voltage spikes that could appear on the V_{IN} supply line and in the GND plane.

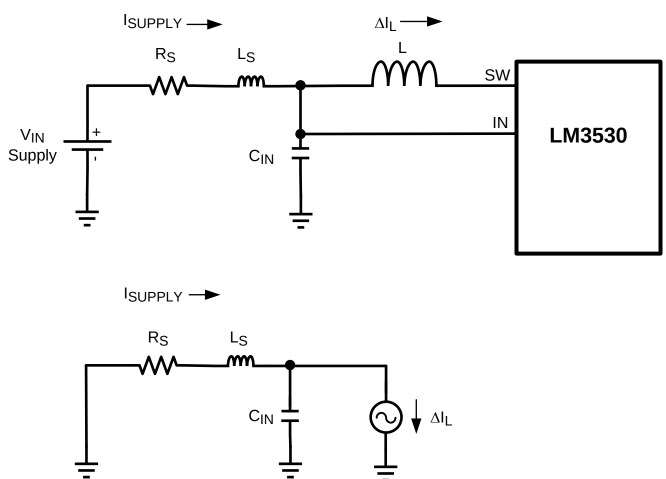
Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM3530, form a series RLC circuit. If the output resistance from the source (R_S) is low enough the circuit will be underdamped and will have a resonant frequency (typically the case). Depending on the size of L_S the resonant frequency could occur below, close to, or above the LM3530's switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM3530's switching frequency;
2. Greater then the inductor current ripple when the resonant frequency occurs near the switching frequency; and
3. Less then the inductor current ripple when the resonant frequency occurs well below the switching frequency.

Figure 57 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor. The circuit is re-drawn for the AC case where the V_{IN} supply is replaced with a short to GND and the LM3530 + Inductor is replaced with a current source (ΔI_L).

Equation 1 is the criteria for an underdamped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of L_S, R_S, and C_{IN}.

As an example, consider a 3.6V supply with 0.1Ω of series resistance connected to C_{IN} through 50nH of connecting traces. This results in an underdamped input filter circuit with a resonant frequency of 712kHz. Since the switching frequency lies near to the resonant frequency of the input RLC network, the supply current is probably larger then the inductor current ripple. In this case usingEquation 3 from Figure 57 the supply current ripple can be approximated as 1.68×'s the inductor current ripple. Increasing the series inductance (L_S) to 500nH causes the resonant frequency to move to around 225kHz and the supple current ripple to be approximately 0.25×'s the inductor current ripple.



1. $$\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$$

2. $$f_{RESONANT} = \frac{1}{2\pi\sqrt{L_S \times C_{IN}}}$$

3. $$I_{SUPPLYRIPPLE} \approx \Delta I_L \times \frac{\frac{1}{2\pi \times 500\,\text{kHz} \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times 500\,\text{kHz} \times L_S - \frac{1}{2\pi \times 500\,\text{kHz} \times C_{IN}}\right)^2}}$$

Figure 57. Input RLC Network

Example Layouts

The following three figures show example layouts which apply the required proper layout guidelines. These figures should be used as guides for laying out the LM3530's circuit.

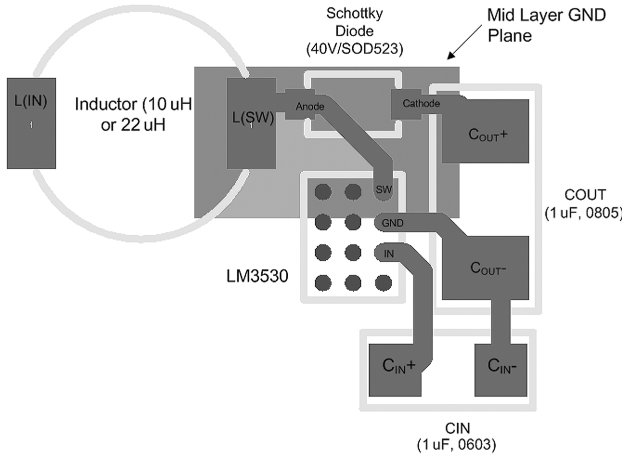


Figure 58. Layout Example #1

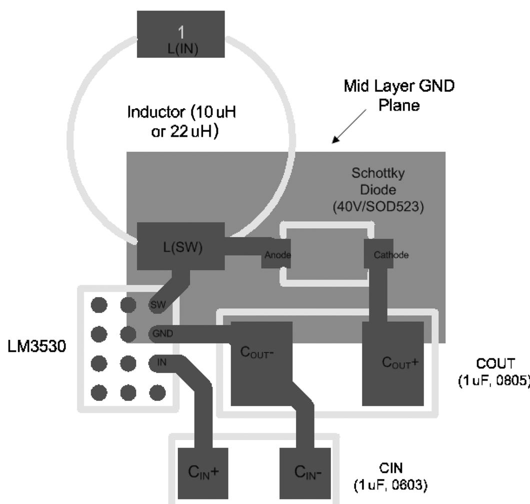


Figure 59. Layout Example #2

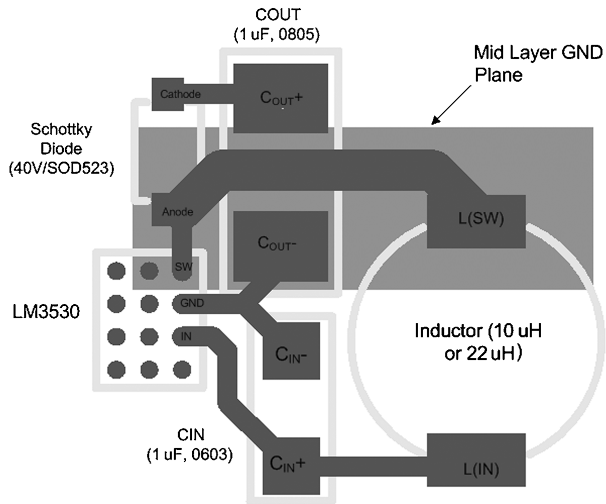


Figure 60. Layout Example #3

Table 16. Application Circuit Component List

Compon-ent	Manufact-urer	Part Number	Value	Size	Current/Voltage Rating
L	TDK	VLF3014ST-100MR82	10 µH	3mm × 3mm × 1.4mm	I_{SAT} = 820mA
COUT	Murata	GRM21BR71H105KA12	1 µF	0805	50V
CIN	Murata	GRM188B31A225KE33	2.2 µF	0603	10V
D1	Diodes Inc.	B0540WS	Schottky	SOD-323	40V/500mA
ALS1	Avago	APDS-9005	Ambient Light Sensor	1.6mm x 1.5mm × 0.6mm	0 to 1100 Lux
ALS2	Avago	APDS-9005	Ambient Light Sensor	1.6mm x 1.5mm × 0.6mm	0 to 1100 Lux

REVISION HISTORY

Changes from Revision J (March 2013) to Revision K	Page
• Changed layout of National Data Sheet to TI format	39

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3530TME-40/NOPB	ACTIVE	DSBGA	YFQ	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		DX	Samples
LM3530TMX-40/NOPB	ACTIVE	DSBGA	YFQ	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		DX	Samples
LM3530UME-25A/NOPB	ACTIVE	DSBGA	YFZ	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	DS	Samples
LM3530UME-40/NOPB	ACTIVE	DSBGA	YFZ	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	40	Samples
LM3530UME-40B/NOPB	ACTIVE	DSBGA	YFZ	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		DT	Samples
LM3530UMX-25A/NOPB	ACTIVE	DSBGA	YFZ	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	DS	Samples
LM3530UMX-40/NOPB	ACTIVE	DSBGA	YFZ	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	40	Samples
LM3530UMX-40B/NOPB	ACTIVE	DSBGA	YFZ	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		DT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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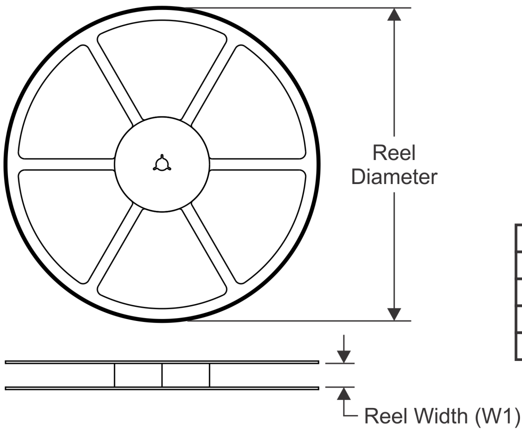
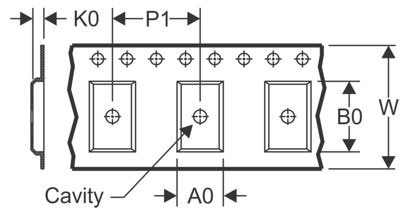
TAPE AND REEL INFORMATION

REEL DIMENSIONS

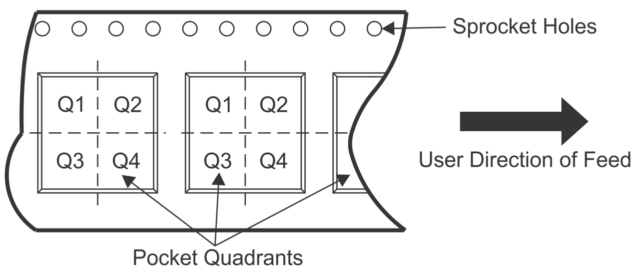


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

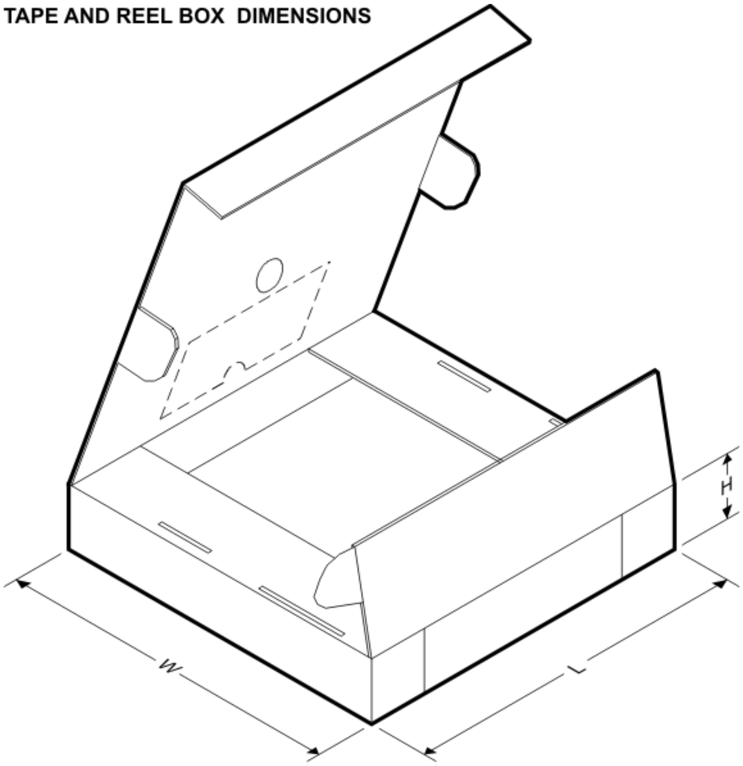
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3530TME-40/NOPB	DSBGA	YFQ	12	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3530TMX-40/NOPB	DSBGA	YFQ	12	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3530UME-25A/NOPB	DSBGA	YFZ	12	250	178.0	8.4	1.37	1.77	0.56	4.0	8.0	Q1
LM3530UME-40/NOPB	DSBGA	YFZ	12	250	178.0	8.4	1.37	1.77	0.56	4.0	8.0	Q1
LM3530UME-40B/NOPB	DSBGA	YFZ	12	250	178.0	8.4	1.37	1.77	0.56	4.0	8.0	Q1
LM3530UMX-25A/NOPB	DSBGA	YFZ	12	3000	178.0	8.4	1.37	1.77	0.56	4.0	8.0	Q1
LM3530UMX-40/NOPB	DSBGA	YFZ	12	3000	178.0	8.4	1.37	1.77	0.56	4.0	8.0	Q1
LM3530UMX-40B/NOPB	DSBGA	YFZ	12	3000	178.0	8.4	1.37	1.77	0.56	4.0	8.0	Q1

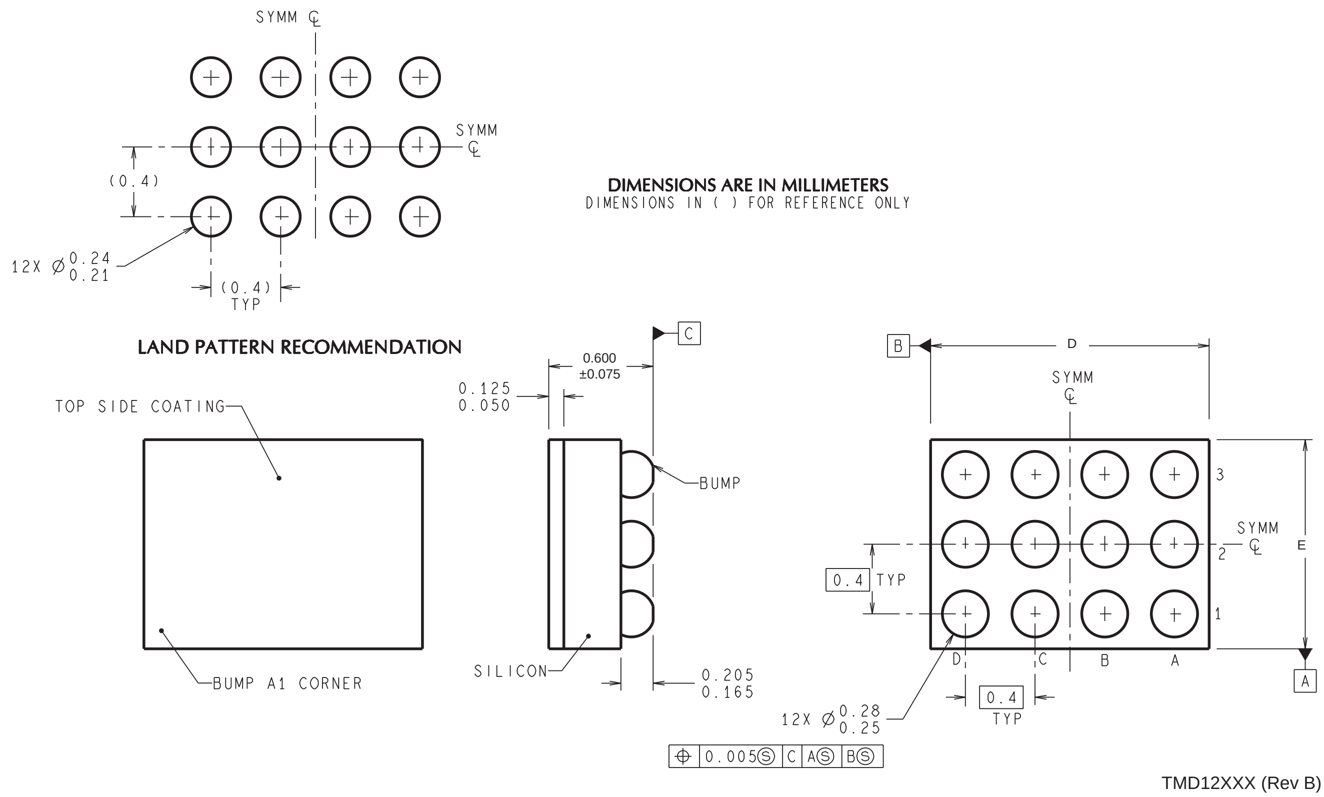
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3530TME-40/NOPB	DSBGA	YFQ	12	250	210.0	185.0	35.0
LM3530TMX-40/NOPB	DSBGA	YFQ	12	3000	210.0	185.0	35.0
LM3530UME-25A/NOPB	DSBGA	YFZ	12	250	210.0	185.0	35.0
LM3530UME-40/NOPB	DSBGA	YFZ	12	250	210.0	185.0	35.0
LM3530UME-40B/NOPB	DSBGA	YFZ	12	250	210.0	185.0	35.0
LM3530UMX-25A/NOPB	DSBGA	YFZ	12	3000	210.0	185.0	35.0
LM3530UMX-40/NOPB	DSBGA	YFZ	12	3000	210.0	185.0	35.0
LM3530UMX-40B/NOPB	DSBGA	YFZ	12	3000	210.0	185.0	35.0

YFQ0012



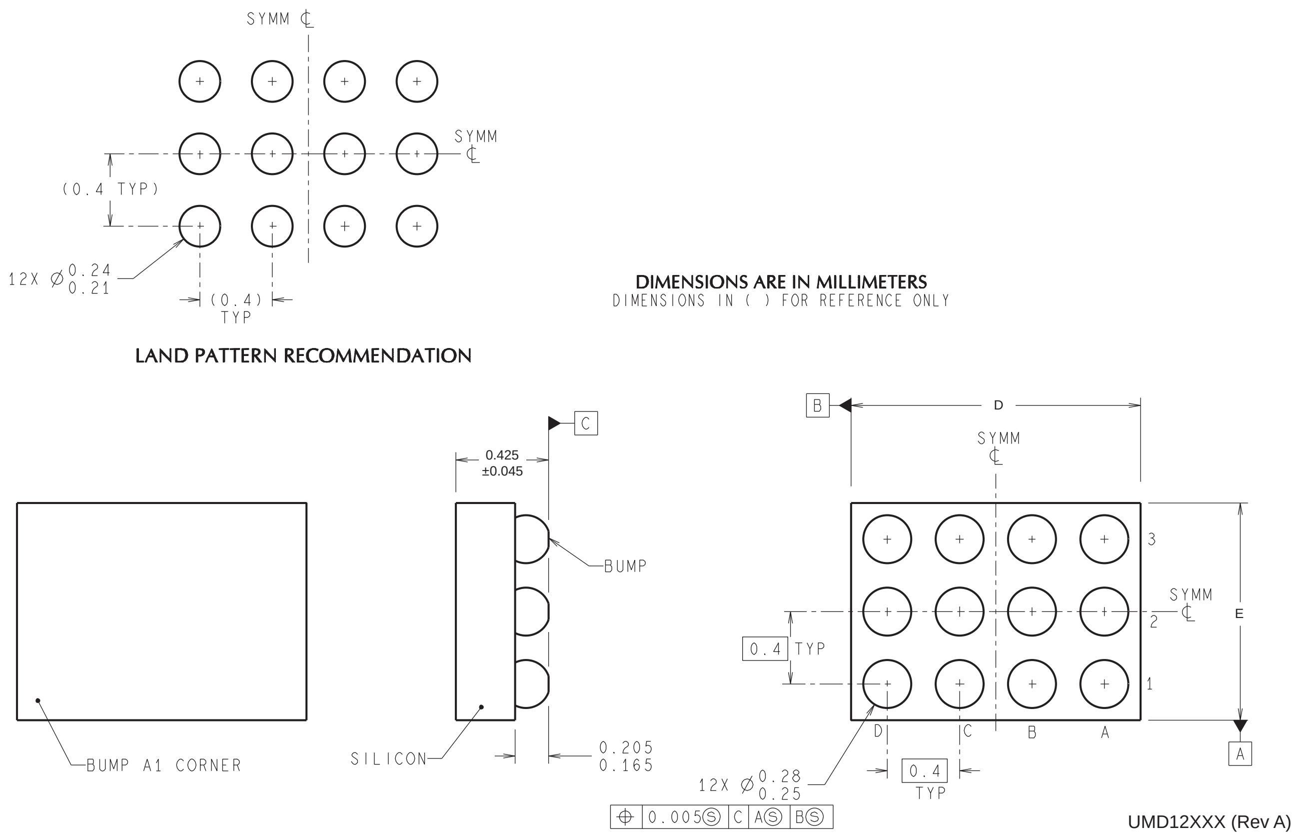
D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.24 mm, Min = 1.18 mm

4215079/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

YFZ0012



D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.24 mm, Min = 1.18 mm

4215133/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.