LM3533 Complete Lighting Power Solution for Smartphone Handsets

Check for Samples: LM3533

FEATURES

- **Drives Two Parallel High-Voltage LED Strings for Display and Keypad Lighting**
- **High-Voltage Strings Capable of up to 40V Output Voltage and up to 90% Efficiency**
- **Up to 30mA per Current Sink (Both Backlight and Indicator)**
- **14-Bit Equivalent Exponential Dimming with 8-Bit Programmable Backlight Code**
- **Selectable Analog ALS Input with 128 Programmable Gain Setting Resistors or PWM ALS Input with Internal Low Pass Filter**
- **PWM Input for Content Adjustable Brightness Control (CABC)**
- **Five Low-Voltage Current Sinks for Indicator LEDs**
- **Integrated Charge Pump for Improved Efficiency and VIN Operating Range**
- **Internal Pattern Generation Engine**
- **Fully Configurable LED Grouping and Control**
- **Four Programmable Over-voltage Protection Thresholds (16V, 24V, 32V, and 40V)**
- **Programmable 500kHz and 1MHz Switching Frequency**
- **27mm^2 Total Solution Size**

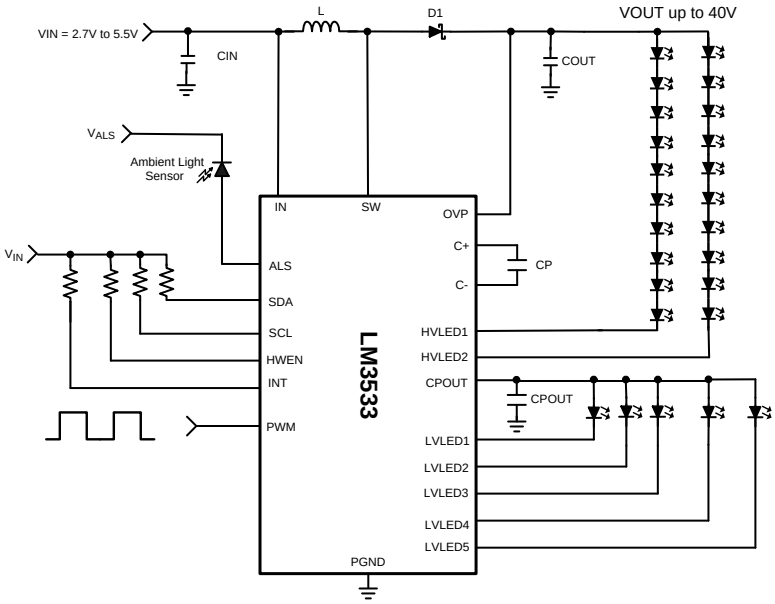
APPLICATIONS

- **Power Source for Smart Phone Illumination**
- **Display, Keypad and Indicator Illumination**
- **RGB Indicator Driver**

DESCRIPTION

The LM3533 is a complete power source for backlight, keypad, and indicator LEDs in smartphone handsets. The high-voltage inductive boost converter provides the power for two series LED strings for display backlight and keypad functions (HVLED1 and HVLED2). The integrated charge pump provides the bias for the five low-voltage indicator LED current sinks (LVLED1-LVLED5). All low-voltage current sinks can have a programmable pattern modulated onto their output current for a wide variety of blinking patterns.

Typical Application Circuit



DESCRIPTION (CONTINUED)

Additional features include a Pulse Width Modulation (PWM) control input for content adjustable backlight control, and an Ambient Light Sensor interface (ALS) with an internal 8-bit ADC to provide automatic current adjustment based upon ambient light conditions. Both the PWM and ALS inputs can be used to control any high- or low-voltage current sink.

The LM3533 is fully programmable via an I^2C-compatible interface. The device is available in a 20-bump (1.755mm x 2.015mm x 0.6mm) DSBGA and operates over a 2.7V to 5.5V input voltage range and a −40°C to +85°C temperature range.

Table 1. Application Circuit Component List

Component	Manufacturer	Value	Part Number	Size (mm)	Current/Voltage Rating (Resistance)
L	TDK	10µH	VLF302512MT-100M	2.5mm x 3.0mm x 1.2mm	620mA/0.25Ω
COUT	TDK	1µF	C2012X5R1H105	0805	50V
CIN	TDK	2.2µF	C1005X5R1A225	0402	10V
CPOUT/CP	TDK	1µF	C1005X5R1A105	0402	10V
Diode	On-Semi	Schottky	NSR0240V2T1G	SOD-523	40V, 250mA

Connection Diagram

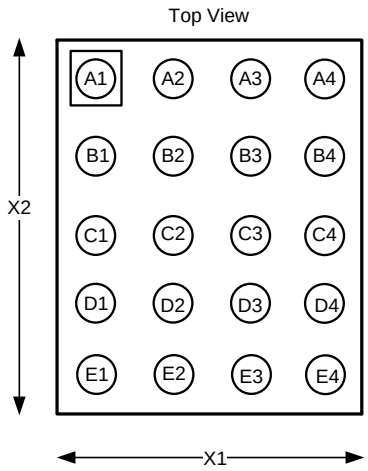


Figure 1. 20-Bump DSBGA Package (Top View)
Package YFQ0020

PIN DESCRIPTIONS

Pin	Name	Description
A1	C−	Integrated Charge Pump Flying Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C+ and C−.
A2	C+	Integrated Charge Pump Flying Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C+ and C−.
A3	CPOUT	Integrated Charge Pump Output Terminal. Bypass CPOUT to GND with a 1µF ceramic capacitor.
A4	IN	Input Voltage Connection. Bypass IN to GND with a minimum 2.2µF ceramic capacitor.
B1	SCL	Serial Clock Connection for I^2C-Compatible Interface.
B2	SDA	Serial Data Connection for I^2C-Compatible Interface.
B3	OVP	Over Voltage Sense Input. Connect OVP to the positive terminal of the inductive boost's output capacitor (COUT).
B4	GND	Ground

PIN DESCRIPTIONS (continued)

Pin	Name	Description
C1	HVLED1	Input Terminal to high-voltage Current Sink #1 (40V max). The boost converter regulates the minimum of HVLED1 and HVLED2 to 0.4V.
C2	INT	ALS Interrupt Output (INT). When INT Mode is enabled this pin becomes an open-drain output that pulls low when the ALS changes zones. On power-up, INT Mode is disabled and is high impedance and must be tied high or low.
C3	PWM	PWM Brightness Control Input for CABC operation. PWM is a high-impedance input and cannot be left floating.
C4	SW	Drain Connection for the internal NFET. Connect SW to the junction of the inductor and the Schottky diode anode.
D1	HVLED2	Input Terminal to high-voltage Current Sink #2 (40V max). The boost converter regulates the minimum of HVLED1 and HVLED2 to 0.4V.
D2	ALS	Ambient Light Sensor Input.
D3	HWEN	Hardware enable input. Drive this pin high to enable the device. Drive this pin low to force the device into a low power shutdown. HWEN is a high-impedance input and cannot be left floating.
D4	LVLED5	Low-Voltage Current Sink #5
E1	LVLED1	Low-Voltage Current Sink #1
E2	LVLED2	Low-Voltage Current Sink #2
E3	LVLED3	Low-Voltage Current Sink #3
E4	LVLED4	Low-Voltage Current Sink #4

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

V_{IN} to GND	−0.3V to +6V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{HVLED2} to GND	−0.3V to +45V
V_{SCL}, V_{SDA}, V_{ALS}, V_{PWM} to GND	−0.3V to +6V
V_{INT}, V_{HWEN}, V_{CPOUT} to GND	−0.3V to +6V
V_{LVLED1}- V_{LVLED5}, to GND	−0.3V to +6V
Continuous Power Dissipation	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering)	(4)
ESD Rating Human Body Model (5)	2.0kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications. For specified specifications and test conditions, see Electrical Characteristics.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112) available at www.ti.com.
(5) The human body model is a 100pF capacitor discharged through 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7).

Operating Ratings(1)

V_{IN} to GND	2.7V to 5.5V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{VHLED2} to GND	0V to +40V
V_{LVLED1}- V_{LVLED5} to GND	0V to 6V
Junction Temperature Range (T_J) (2) (3)	−40°C to +125°C

(1) All voltages are with respect to the potential at the GND pin.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=+140°C (typ.) and disengages at T_J=+125°C (typ.).
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Thermal Resistance Junction to Ambient (T_{JA})(1)	55.3°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102mm x 76mm x 1.6mm with a 2 x 1 array of thermal vias. The ground plane on the board is 50mm x 50mm. Thickness of copper layers are 36µm/18µm/18µm/36µm (1.5oz/1oz/1oz/1.5oz). Ambient temperature in simulation is 22°C in still air. Power dissipation is 1W. The value of θ_{JA} of this product in the DSBGA package could fall in a range as wide as 60ºC/W to 110ºC/W (if not wider), depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists special care must be paid to thermal dissipation issues.

Electrical Characteristics (1)(2)

Limits in standard type face are for T_A = +25°C and those in **boldface type** apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified V_{IN} = 3.6V.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{SHDN}	Shutdown Current	2.7V ≤ V_{IN} ≤ 5.5V, HWEN = GND			1	**5**	µA
I_{LED_MIN}	Minimum LED Current	Full-Scale Current = 20.2mA Exponential Mapping			9.5		µA
T_{SD}	Thermal Shutdown				+140		°C
	Hysteresis				15		
Boost Converter							
$I_{HVLED(1/2)}$	Output Current Regulation (HVLED1 or HVLED2)	2.7V ≤ V_{IN} ≤ 5.5V, Full-Scale Current = 20.2mA, Brightness Code = 0xFF		**17**	20.2	**23**	mA
I_{MATCH_HV}	HVLED1 to HVLED2 Matching (3)	2.7V ≤ V_{IN} ≤ 5.5V	Both current sinks are assigned to Control Bank A	**−2**	1	**2**	%
V_{REG_CS}	Regulated Current Sink Headroom Voltage				400		mV
V_{HR_HV}	Minimum Current Sink Headroom Voltage for HVLED Current Sinks	I_{LED} = 95% of nominal, Full-Scale Current = 20.2mA			190	**250**	mV
R_{DSON}	NMOS Switch On Resistance	I_{SW} = 500 mA			0.3		Ω
I_{CL_BOOST}	NMOS Switch Current Limit	V_{IN} = 3.6V		**880**	1000	**1120**	mA
V_{OVP}	Output Over-Voltage Protection	ON Threshold, 2.7V ≤ V_{IN} ≤ 5.5V OVP select bits = 11		**39**	40	**41**	V
		Hysteresis			1		
f_{SW}	Switching Frequency	2.7V ≤ V_{IN} ≤ 5.5V	Boost Frequency Select Bit = 0	**450**	500	**550**	kHz
			Boost Frequency Select Bit = 1	**900**	1000	**1100**	
D_{MAX}	Maximum Duty Cycle				94		%
Charge Pump							
$I_{LVLED(1/2/3/4/5)}$	Output Current Regulation (Low-Voltage Current sinks)	2.7V ≤ V_{IN} ≤ 5.5V, Full-Scale Current = 20.2mA, Brightness Code = 0xFF		**17**	20.2	**23**	mA
I_{MATCH_LV}	LVLED Current Sink Matching (4)	2.7V ≤ V_{IN} ≤ 5.5V		**−2**	1	**2**	%
V_{HR_LV}	Minimum Current Sink Headroom Voltage for LVLED Current Sinks	I_{LED} = 95% of nominal, Full-Scale Current = 20.2mA			80	**110**	mV
V_{GTH}	Threshold for gain transition	V_{LVLED} falling			110		mV
I_{CL_PUMP}	Charge Pump Current Limit	3V ≤ V_{IN} ≤ 5.5V, Output Referred	1X Gain	**180**	350		mA
			2X Gain		240		
R_{OUT}	Charge Pump Output Resistance	1X Gain			1.1		Ω
HWEN Input							
V_{HWEN}	Logic Thresholds	Logic Low		**0**		**0.4**	V
		Logic High		**1.2**		**V_{IN}**	

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ) numbers represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6V and T_A = +25ºC.
(3) LED current sink matching between HVLED1 and HVLED2 is given by taking the difference between either (IHVLED1 or IHVLED2) and the average current between the two, and dividing by the average current between the two. This simplifies to (I_{HVLED1} (or IHVLED2) – $I_{HVLED(AVE)}$)/($I_{HVLED(AVE)}$) x 100. In this test, both HVLED1 and HVLED2 are assigned to Bank A.
(4) LED current sink matching in the low-voltage current sinks (LVLED1 through LVLED5) is given as the maximum matching value between any two current sinks, where the matching between any two low voltage current sinks (X and Y) is given as (I_{LVLEDX} (or I_{LVLEDY}) - $I_{AVE(X-Y)}$)/($I_{AVE(X-Y)}$) x 100. In this test all LVLED current sinks are assigned to Bank C.

Electrical Characteristics[1][2] (continued)

Limits in standard type face are for T_A = +25°C and those in **boldface type** apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified V_{IN} = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PWM Input						
V_{PWM_L}	Input Logic Low	2.7V ≤ V_{IN} ≤ 5.5V	**0**		**400**	mV
V_{PWM_H}	Input Logic High	2.7V ≤ V_{IN} ≤ 5.5V	**1.25**		**V_{IN}**	
INT Output						
V_{LOW}	Output Logic Low (INT Mode)	2.7V ≤ V_{IN} ≤ 5.5V			**400**	mV
I^2C-Compatible Voltage Specifications (SCL, SDA)						
V_{IL}	Input Logic Low	2.7V ≤ V_{IN} ≤ 5.5V	**0**		**400**	mV
V_{IH}	Input Logic High	2.7V ≤ V_{IN} ≤ 5.5V	**1.25**		**V_{IN}**	V
V_{OL}	Output Logic Low (SDA)	I_{LOAD} = 3mA			**400**	mV
I^2C-Compatible Timing Specifications (SCL, SDA) [5], see Figure 2						
t_1	SCL (Clock Period)		**2.5**			µs
t_2	Data In Setup Time to SCL High		**100**			ns
t_3	Data Out Stable After SCL Low		**0**			ns
t_4	SDA Low Setup Time to SCL Low (Start)		**100**			ns
t_5	SDA High Hold Time After SCL High (Stop)		**100**			ns
Ambient Light Sensor (ALS)						
R_{ALS}	ALS Internal Pulldown Resistor in Analog Sensor Input Mode	R_ALS Select Register = 0x0F, 2.7V ≤ V_{IN} ≤ 5.5V	**12.36**	13.33	**13.94**	kΩ
V_{ALS_REF}	Ambient Light Sensor Reference Voltage	2.7V ≤ V_{IN} ≤ 5.5V	**1.9**	2	**2.1**	V
V_{ALS_MIN}	Minimum Threshold for ALS Input Voltage Sensing	Analog Sensor Mode, 2.7V ≤ V_{IN} ≤ 5.5V, Code 0 to 1 transition point	**3**	10	**15**	mV
t_{CONV}	Conversion Time			140		µs
LSB	ADC Resolution	2.7V ≤ V_{IN} ≤ 5.5V		7.8		mV

(5) SCL and SDA must be glitch-free in order for proper brightness control to be realized.

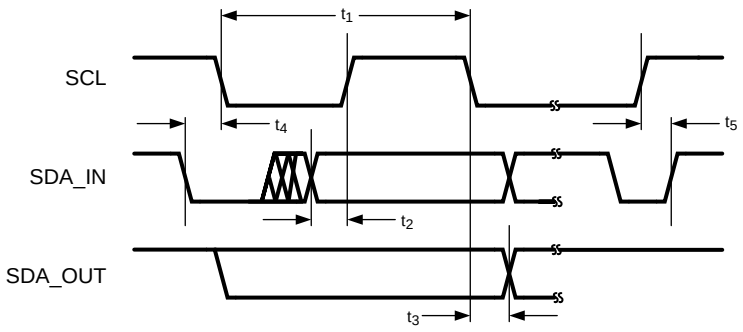


Figure 2. I^2C-Compatible Interface Timing

Typical Performance Characteristics

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Efficiency vs VIN, Dual String,
L = 22µH, 20mA/string, f_{SW} = 500kHz
Top to Bottom: 2x4, 2x5, 2x6, 2x7, 2x8, 2x9 (LEDs)

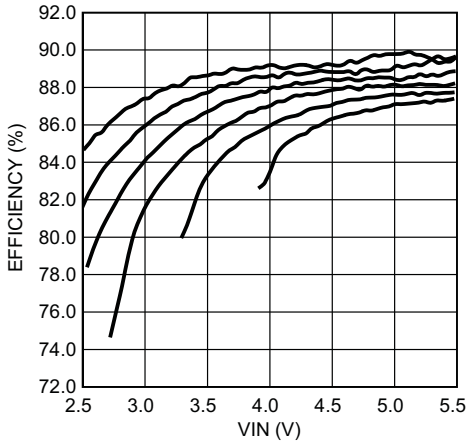


Figure 3.

Efficiency vs VIN, Dual String
L = 22µH, 20mA/string, f_{SW} = 1MHz
Top to Bottom: 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

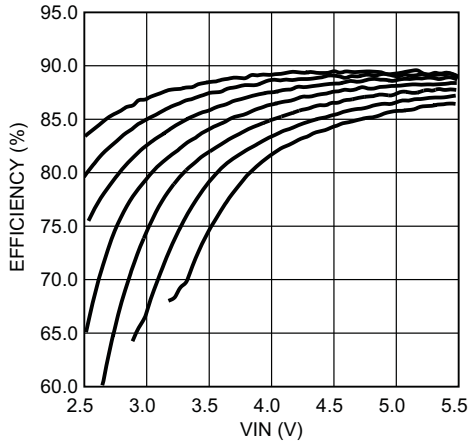


Figure 4.

Efficiency vs VIN, Single String,
L = 22µH, 20mA/string, f_{SW} = 500kHz
Top to Bottom:1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

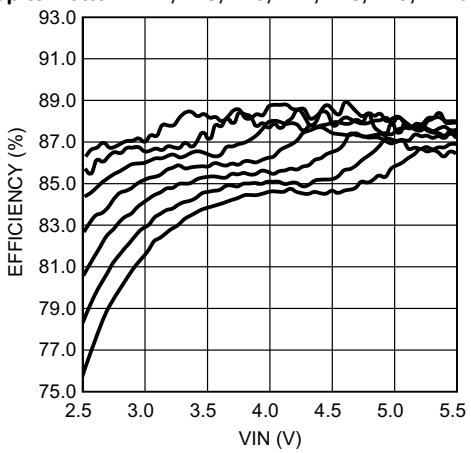


Figure 5.

Efficiency vs VIN, Single String
L = 22µH, 20mA/string, f_{SW} = 1MHz
Top to Bottom:1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

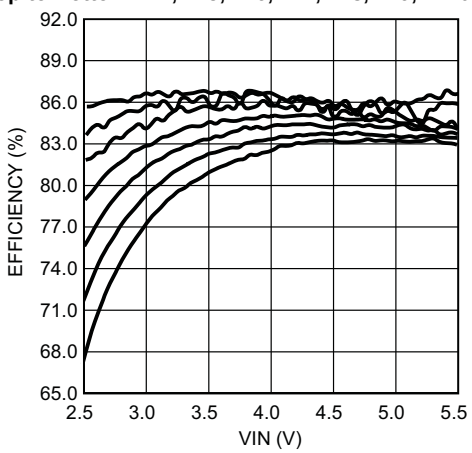


Figure 6.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Efficiency vs VIN, Dual String
L = 10µH, 20mA/string, f_{SW} = 500kHz
Top to Bottom: 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

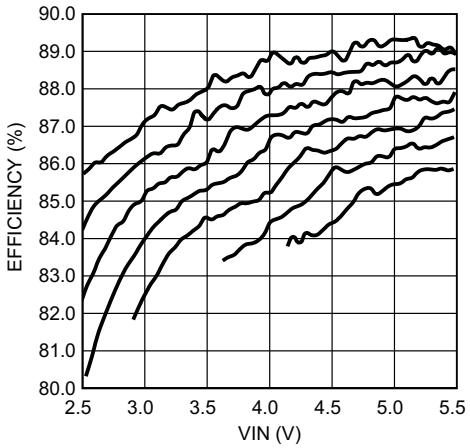


Figure 7.

Efficiency vs VIN, Dual String,
L = 10µH, 20mA/string, f_{SW} = 1MHz
Top to Bottom: 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

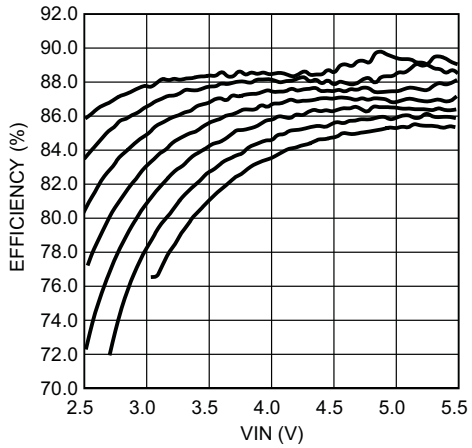


Figure 8.

Efficiency vs VIN, Single String,
L = 10µH, 20mA/string, f_{SW} = 500kHz
Top to Bottom:1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

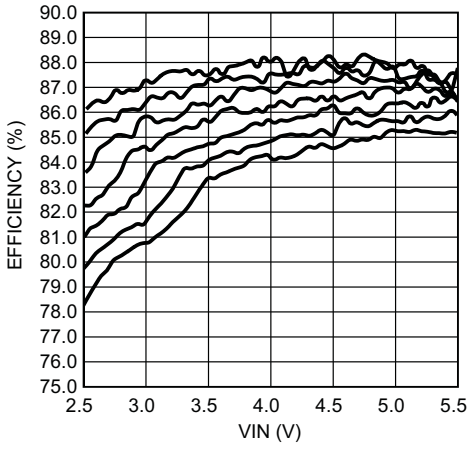


Figure 9.

Efficiency vs VIN, Single String,
L = 10µH, 20mA/string, f_{SW} = 1MHz
Top to Bottom:1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

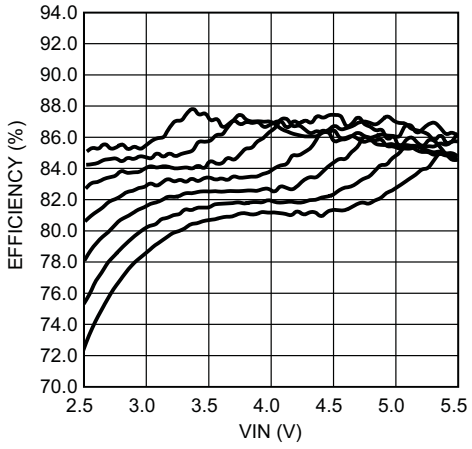


Figure 10.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Efficiency vs VIN, Dual String,
L = 4.7µH, 20mA/string, f_{SW} = 1MHz
Top to Bottom: 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

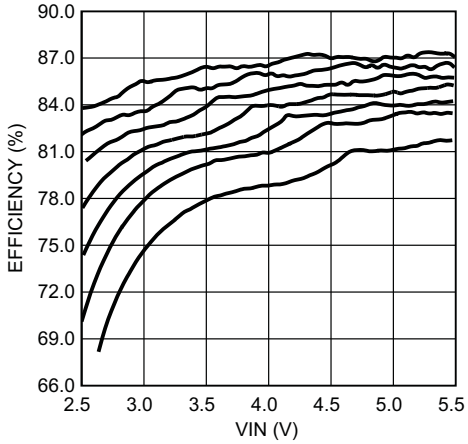


Figure 11.

Efficiency vs VIN, Single String,
L = 4.7µH, 20mA/string
Top to Bottom:1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

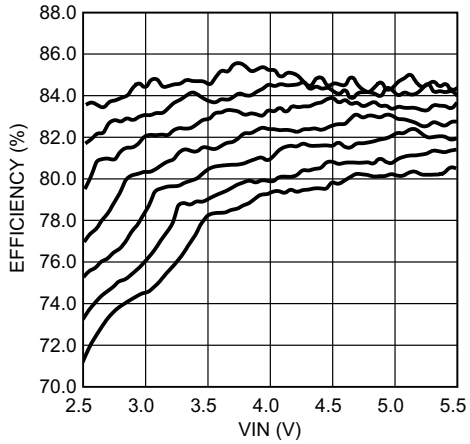


Figure 12.

Efficiency vs ILED
L = 22µH, V_{IN} = 3.6V, f_{SW} = 500kHz
Top to Bottom:2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

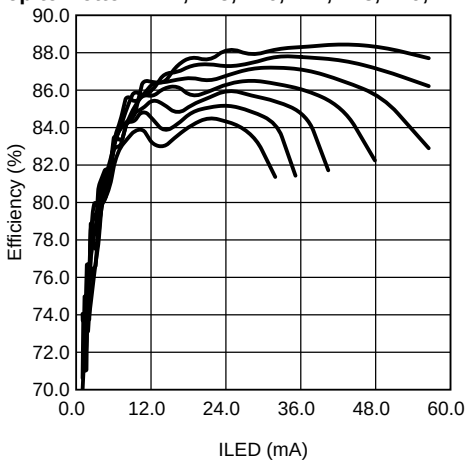


Figure 13.

Efficiency vs ILED
L = 22µH, V_{IN} = 3.6V, f_{SW} = 1MHz
Top to Bottom:2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

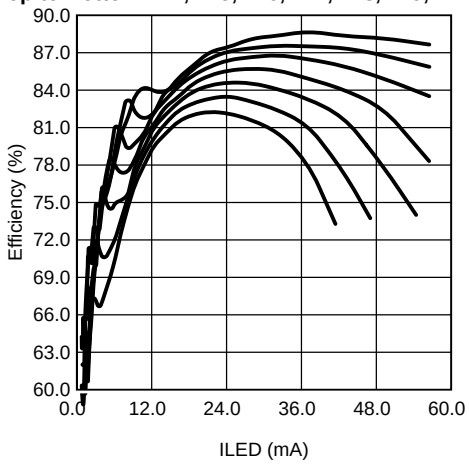


Figure 14.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Efficiency vs ILED
L = 10µH, V_{IN} = 3.6V, f_{SW} = 500kHz
Top to Bottom:2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

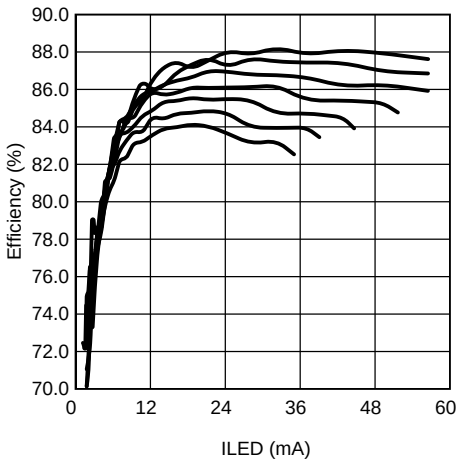


Figure 15.

Efficiency vs ILED
L = 10µH, V_{IN} = 3.6V, f_{SW} = 1MHz
Top to Bottom:2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

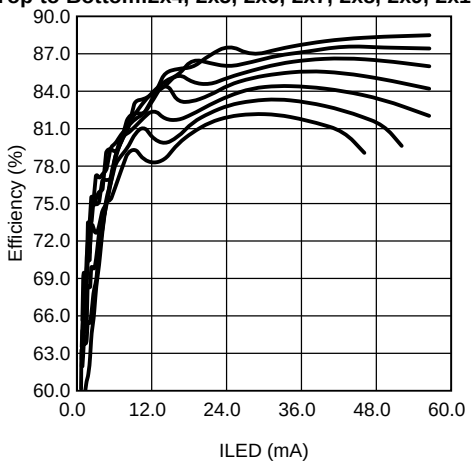


Figure 16.

Efficiency vs ILED
L = 4.7µH, VIN = 3.6V, f_{SW} = 1MHz
Top to Bottom:2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

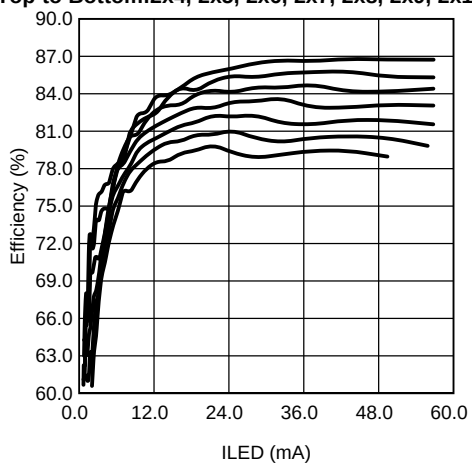


Figure 17.

HVLED Matching vs VIN, Temp (ILED = 20mA)

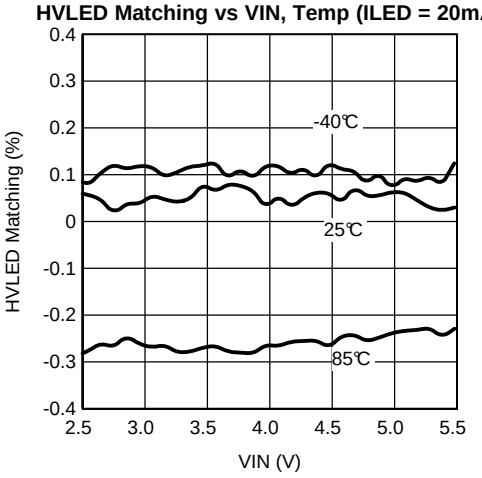


Figure 18.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

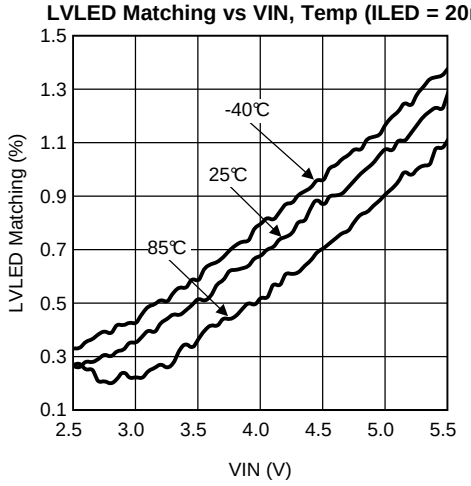


Figure 19.

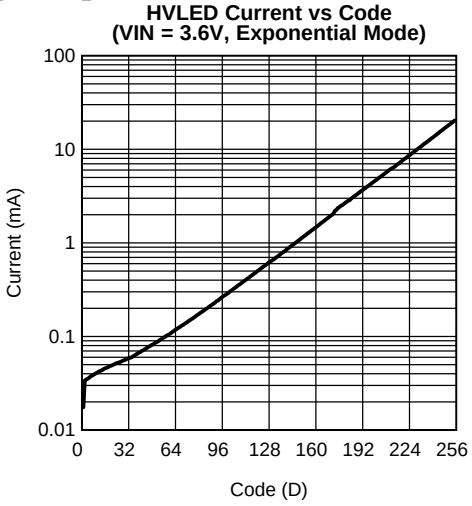


Figure 20.

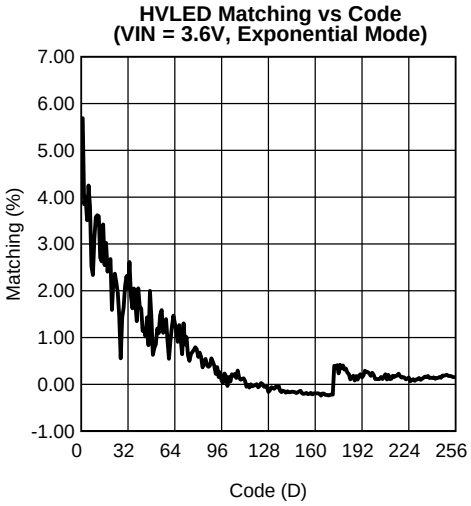


Figure 21.

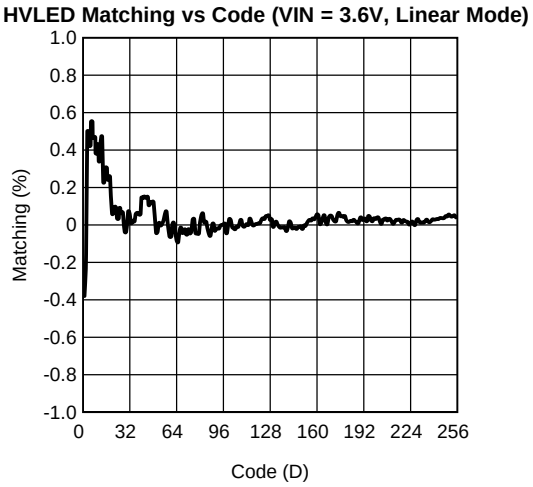


Figure 22.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

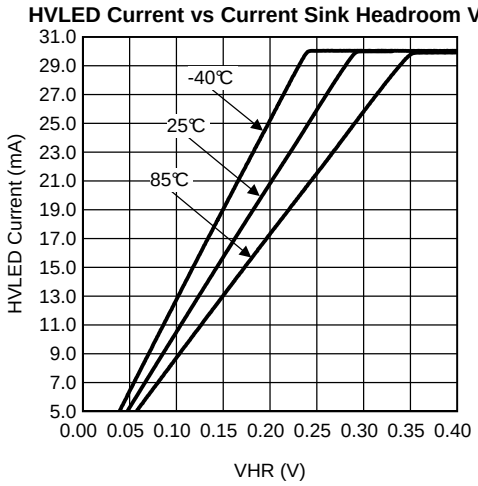


Figure 23.

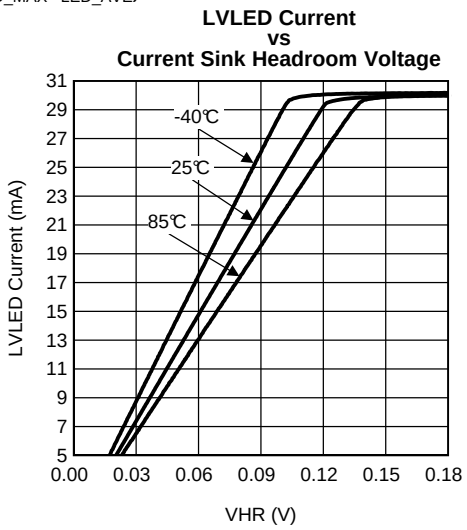


Figure 24.

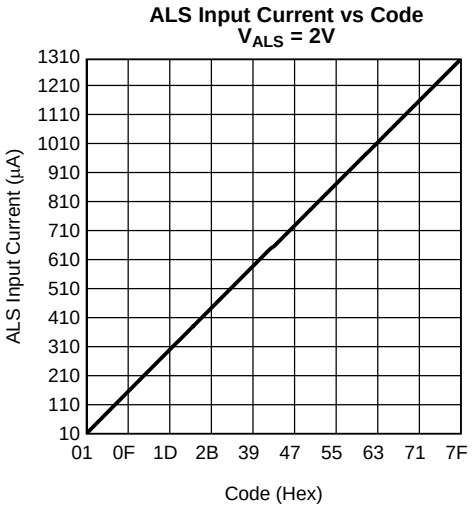


Figure 25.

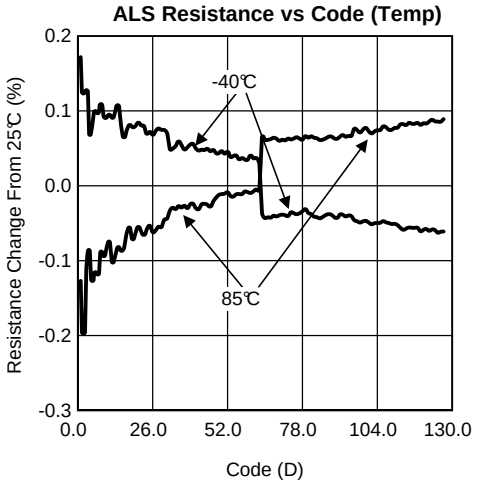


Figure 26.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

ALS Resistance vs VIN (Code 0x50)

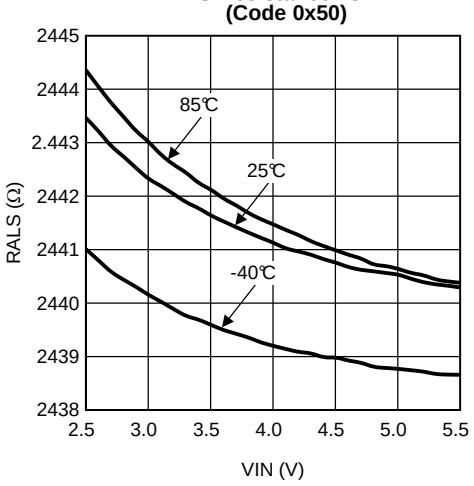


Figure 27.

Shutdown Current vs VIN

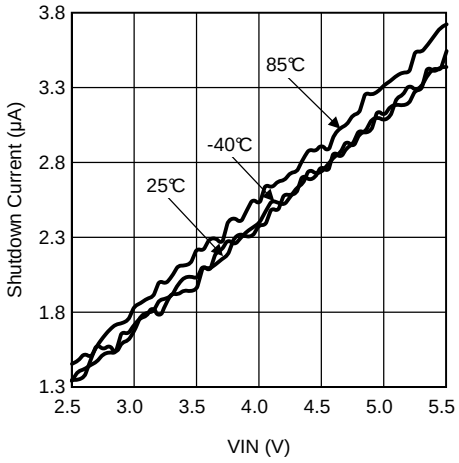


Figure 28.

Closed Loop Current Limit vs VIN

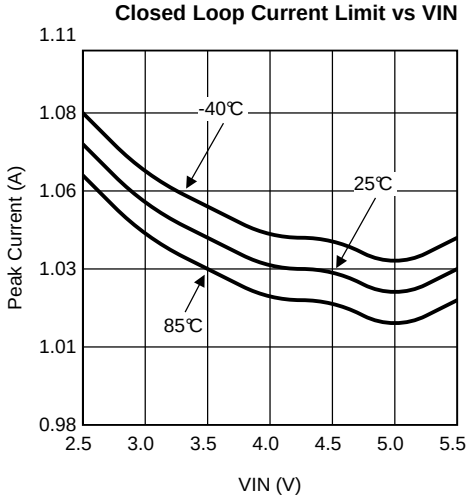


Figure 29.

LED Current Ripple vs f_{PWM} (50% Duty Cycle, ILED FULL_SCALE = 20.2mA)

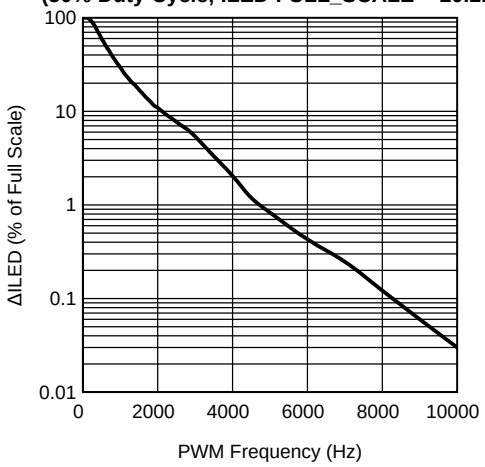


Figure 30.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

NMOS On Resistance vs VIN

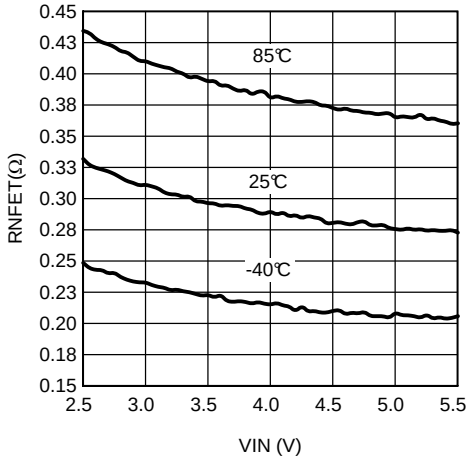


Figure 31.

IN to CPOUT Resistance vs VIN (1X Gain)

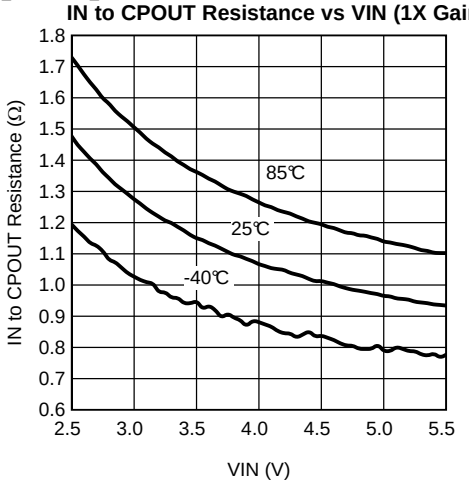


Figure 32.

Charge Pump Short Circuit Current Limit vs VIN (2X Gain)

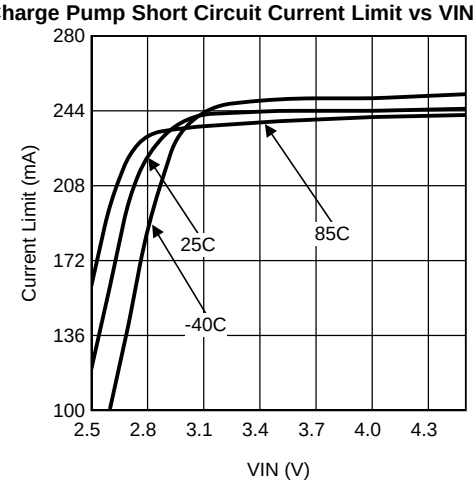


Figure 33.

Charge Pump Short Circuit Current Limit vs VIN (1X Gain)

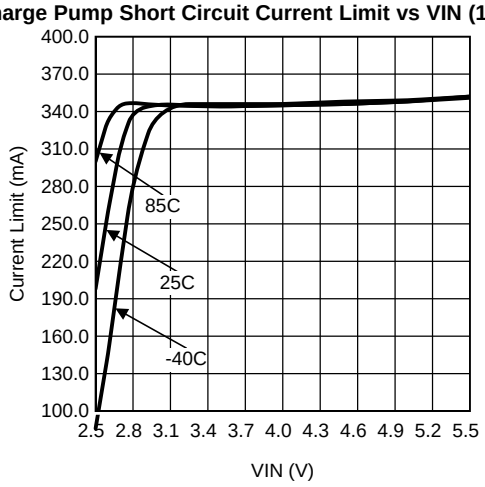


Figure 34.

Typical Performance Characteristics (continued)

V_{IN} = 3.6V, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit with L = TDK (VLF302512, 4.7µH, 10µH, 22µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = +25°C unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$, matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

Idle State Supply Current (Pattern Generator Enabled on LVLED1, LVLED2, LVLED3)

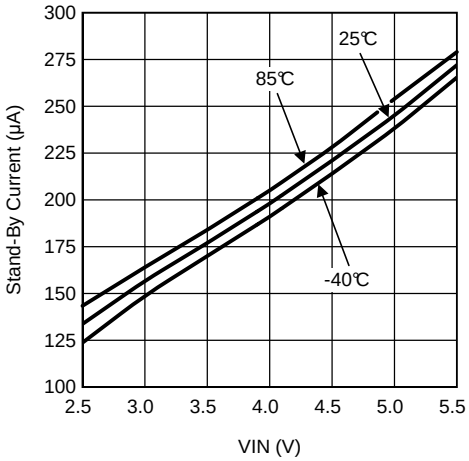


Figure 35.

Startup Response (VIN = 3.6V,2x8 LEDs,20mA/string)

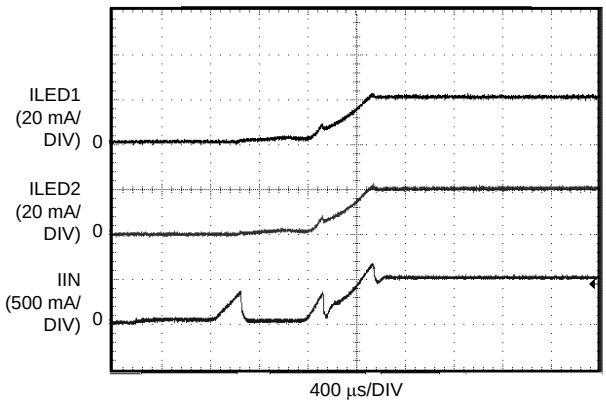


Figure 36.

Response to Step Change in PWM Input Duty Cycle (D = 30% to 90%,f_{PWM} = 10kHz, $I_{LED\_FULL\ SCALE}$ = 20.2mA)

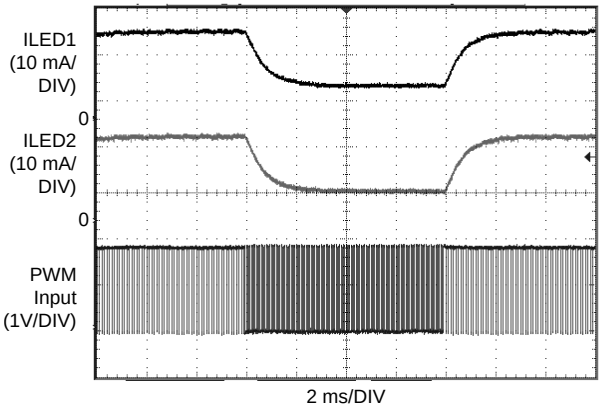


Figure 37.

Line Step Response (Typical Application Circuit, 2x8 LEDs, 20.2mA/string)

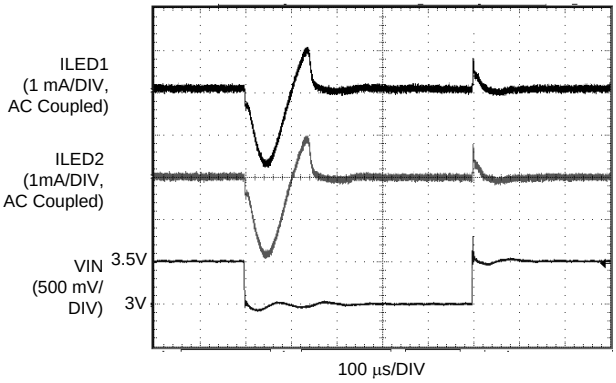


Figure 38.

OPERATIONAL DESCRIPTION

The LM3533 provides the power for two high-voltage LED strings (up to 40V at 30mA each) and 5 low-voltage LEDs (up to 6V at 30mA each). The two high-voltage LED strings are powered from an integrated boost converter. The five low-voltage LEDs are powered from an integrated 2X charge pump.

The device is programmable over an I^2C-compatible interface. Additional features include a Pulse Width Modulation (PWM) input for content adjustable brightness control, an ambient light sensor input (ALS) for ambient light current control, and 4 programmable pattern generators for RGB and indicator blinking functions on the low-voltage LEDs.

CONTROL BANK MAPPING

Control of the LM3533's current sinks is not done directly, but through the programming of Control Banks. The current sinks are then assigned to the programmed Control Bank. This allows for a wide variety of current control possibilities where LEDs can be grouped and controlled via specific Control Banks (see Figure 40).

High-Voltage Control Banks (A/B)

There are 2 high-voltage control banks (A and B). Both high-voltage current sinks can be assigned to either Control Bank A or Control Bank B. Assigning both current sinks to the same control bank allows for better LED current matching. Assigning each current sink to different control banks allows for each current sink to be programmed with a different current. The high-voltage control bank mapping is done via bits [1:0] of the Current Sink Output Configuration Register #1 (address 0x10).

Low-Voltage Control Banks (C, D, E, and F)

There are 4 low-voltage control banks (C, D, E, and F). Any low-voltage current sink (LVLED1-LVLED5) can be assigned to any of the low-voltage control banks. Assigning every low-voltage current sink to the same control bank allows for the best matching between LEDs. Assigning each low-voltage current sink to different control banks allows for each current sink to be programmed with different current levels.

PATTERN GENERATOR

The LM3533 contains 4 independently programmable pattern generators for each Control Bank. Each pattern generator can have its own separate pattern: different rise and fall times, delays from turn-on, high and low-current settings, and pattern high and low times.

AMBIENT LIGHT SENSOR INTERFACE

The LM3533 contains an ambient light sensor interface (ALS). The ALS input is designed to connect to the output of either an analog output or PWM output ambient light sensor. The sensor output (or ambient light information) is digitized and processed by the LM3533. The light information is then compared against the LM3533's five user-configurable brightness zones. Each brightness zone points to a brightness zone target current. Each group of target currents forms an ALS mapper. The LM3533 has three groups of ALS Mappers where each mapper can be assigned to any of the high or low-voltage control banks (see Figure 44).

PWM INPUT

The PWM input which can be assigned to any of the high- or low-voltage control banks. When assigned to a control bank, the programmed current in the control bank also becomes a function of the duty cycle at the PWM input.

HWEN INPUT

HWEN is the global hardware enable to the LM3533. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the LM3533 is placed in shutdown, and all the registers are reset to their default state.

THERMAL SHUTDOWN

The LM3533 contains a thermal shutdown protection. In the event the die temperature reaches +140°C, the boost, charge pump and current sinks will shutdown until the die temperature drops to typically +125°C.

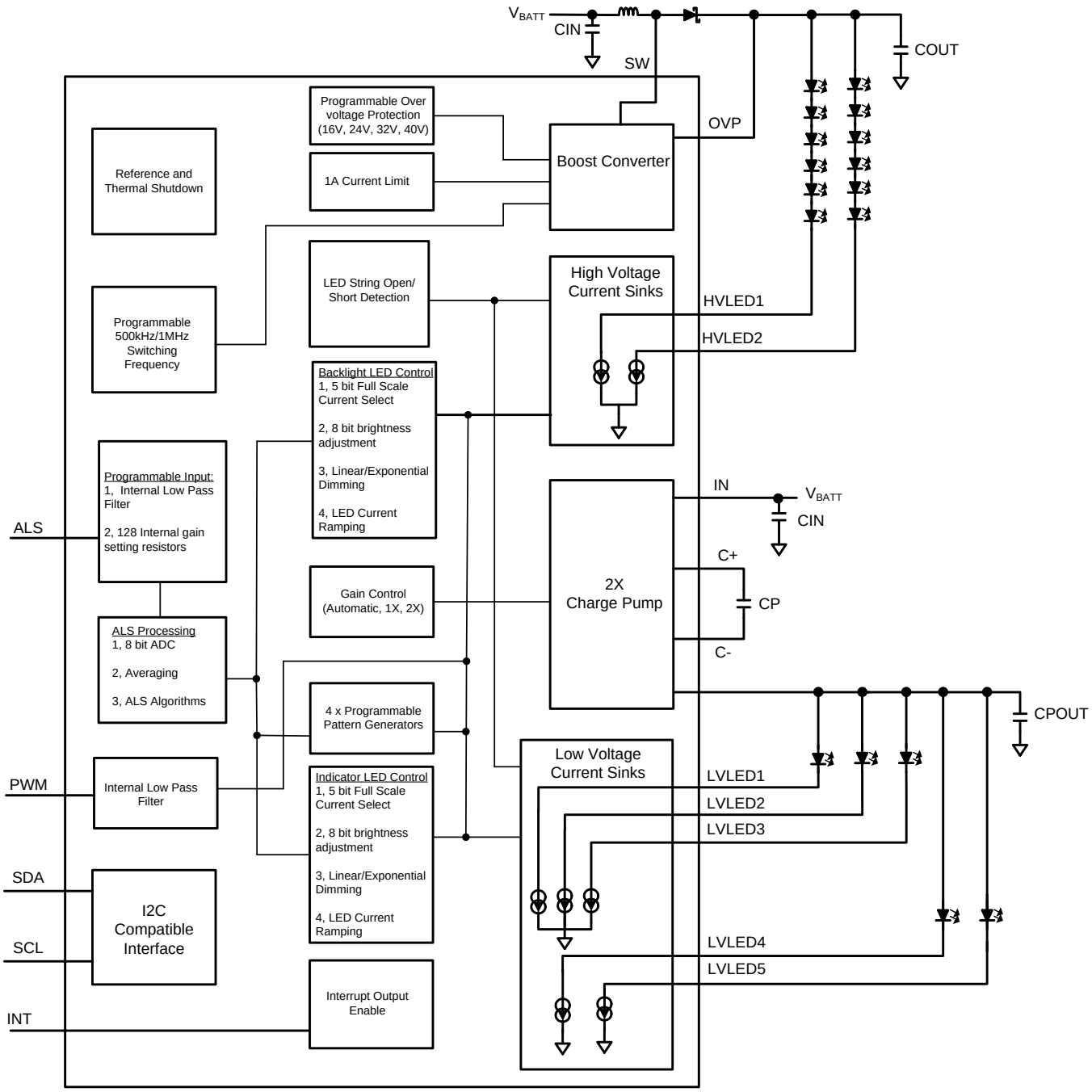


Figure 39. Functional Block Diagram

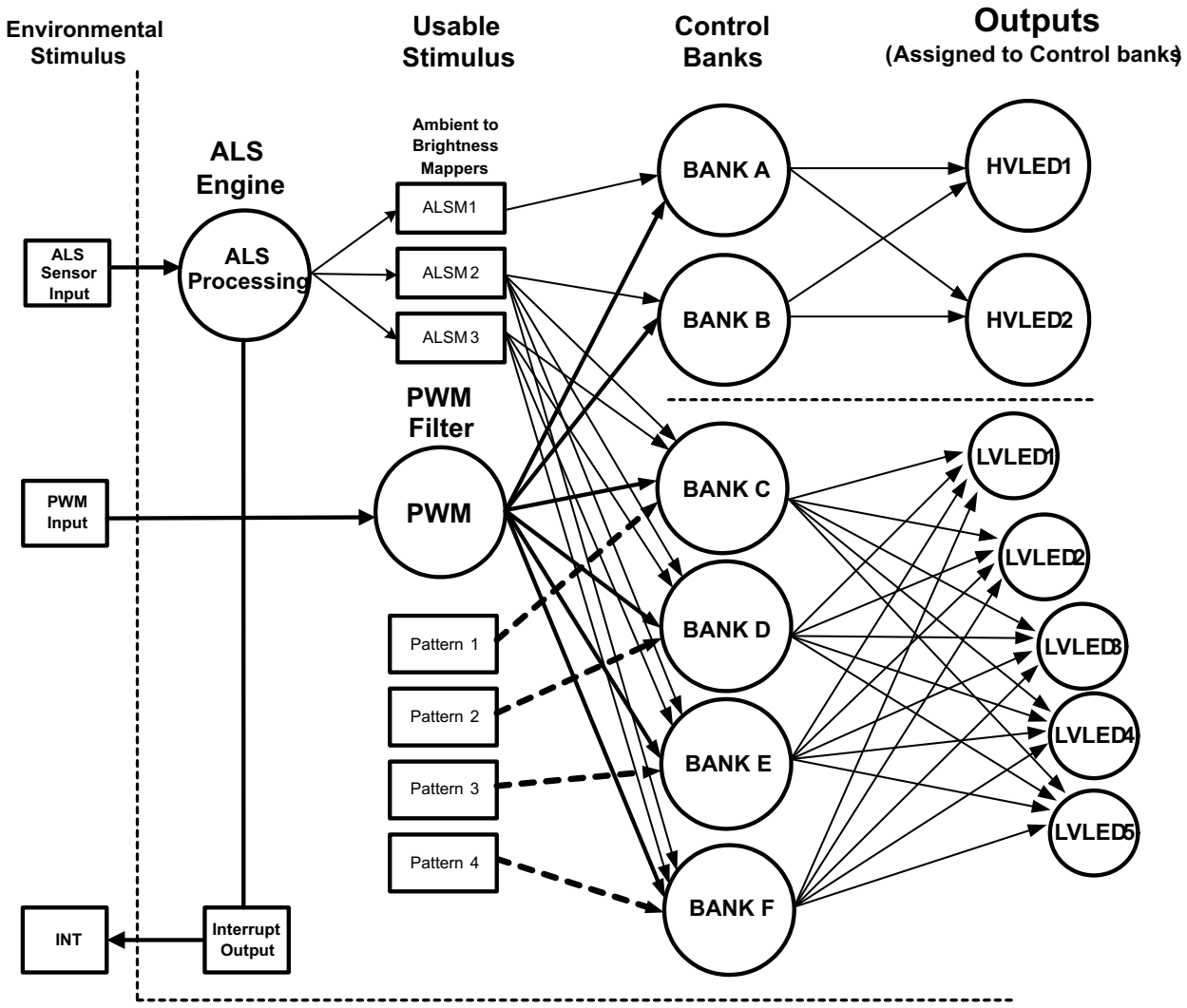


Figure 40. Functional Control Diagram

High-Voltage Boost Converter

The high-voltage boost converter provides power for the two high-voltage current sinks (HVLED1 and HVLED2). The boost circuit operates using a 4.7µH to 22µH inductor and a 1µF output capacitor. The selectable 500kHz or 1MHz switching frequency allows for the use of small external components and provides for high boost-converter efficiency. Both HVLED1 and HVLED2 feature an adaptive current regulation scheme where the feedback point (HVLED1 or HVLED2) is regulated to a minimum of 400mV. When there are different voltage requirements in both high-voltage LED strings (string mismatch), the LM3533 will regulate the feedback point of the highest voltage string to 400mV and drop the excess voltage of the lower voltage string across the lower strings current sink.

HIGH-VOLTAGE CURRENT SINKS (HVLED1 and HVLED2)

HVLED1 and HVLED2 control the current in the high-voltage LED strings. Each current sink has 5-bit full-scale current programmability and 8-bit brightness control. Either current sink can have its current set through a dedicated brightness register or be controlled via the ambient light sensor interface. Configuration of the high-voltage current sinks is done through the Control A/B Brightness Configuration Register (see Table 9).

HIGH-VOLTAGE CURRENT STRING BIASING

Each high-voltage current string can be powered from the LM3533's boost output (COUT) or from an external source. The Anode Connect Register bits [1:0] determine where the high-voltage current string anodes will be connected. When set to '1' (default) the high-voltage current sink inputs are included in the boost feedback loop. This allows the boost converter to adjust its output voltage in order to maintain at least 400mV at the current sink input.

When powered from alternate sources, bits [1:0] should be set to '0'. This removes the particular current sink from the boost feedback loop. In these configurations the application must ensure that the headroom voltage across the high-voltage current sink is high enough to prevent the current sink from going into dropout (see the Typical Performance Characteristics for data on the high-voltage LED current vs headroom voltage).

Setting the Anode Connect Register bits also determines how the shorted high-voltage LED String Fault flag is triggered (see Fault Flags/Protection Features section).

BOOST SWITCHING-FREQUENCY SELECT

The LM3533's boost converter can have a 1MHz or 500kHz switching frequency. For a 500kHz switching frequency the inductor must be between 10µH and 22µH. For the 1MHz switching frequency the inductor can be between 4.7µH and 22µH. The boost frequency is programmed through bit [1] of the OVP/Boost Frequency/PWM Polarity Select register.

Integrated Charge Pump

The LM3533 features an integrated (2x/1x) charge pump capable of supplying up to 150mA. The fixed 1MHz switching frequency allows for use of tiny 1µF ceramic flying capacitors (CP) and output capacitor (CPOUT). The charge pump can supply the power for the low-voltage LEDs connected to LVLED1-LVLED5 and can operate in 4 different modes: disabled, automatic gain, 1X gain, or 2X gain (see Figure 41).

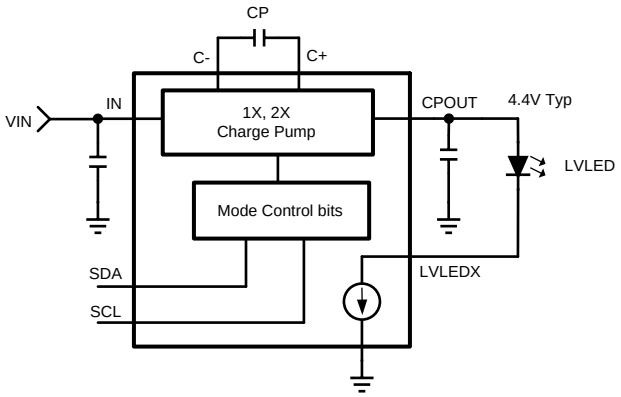


Figure 41. Integrated Charge Pump

CHARGE PUMP DISABLED

With the charge pump disabled, the path from IN to CPOUT is high impedance. Additionally, with the charge pump disabled, the low-voltage current sinks can still be active, thus allowing the low-voltage LEDs to be biased from external sources (see LOW-VOLTAGE LED BIASING section). Disabling the charge pump also has no influence on the state of the low-voltage current sinks. For instance, if a low-voltage current string is set to have its anode connected to CPOUT, and the charge pump is disabled, the current sink will continue to try to sink current.

AUTOMATIC GAIN

In Automatic Gain Mode the charge pump gain transition is actively selected to maintain LED current regulation in the CPOUT-connected, low-voltage current sinks. At higher input voltages the charge pump will operate in Pass Mode (1x gain) allowing the voltage at CPOUT to track the input voltage. As VIN drops, the voltage on the low-voltage current sink(s) will drop also. Once any of the active, CPOUT-connected, low-voltage current sink input voltages reach typically 100mV, the charge pump will automatically switch to a gain of 2x thus preventing dropout (see 2X GAIN). Once the charge pump switches over to 2X gain it will remain in 2X gain, even if the current sink input voltage goes above the switch over threshold.

AUTOMATIC GAIN (FLYING CAPACITOR DETECTION)

In Automatic Gain Mode the LM3533 will start up and automatically detect if there is a flying capacitor (CP) connected between C+ and C−. If there is, Automatic Gain Mode will operate normally. If the detection circuitry detects that there is no flying capacitor connected, the LM3533 will automatically switch to 1X Gain mode.

1X GAIN

In 1X Gain Mode the charge pump will pass VIN directly through to CPOUT. There is a resistive drop between IN and CPOUT in this mode (1.1Ω) which should be accounted for when determining the headroom requirement for the low-voltage current sinks. In forced 1X Gain Mode the charge pump will not switch; thus, the flying capacitor (CP) and output capacitor (CPOUT) can be omitted from the circuit.

2X GAIN

In 2X Gain Mode the internal charge pump will double VIN and post-regulate CPOUT to typically 4.4V. This allows for biasing LEDs whose forward voltages are greater than the input supply (VIN).

LOW-VOLTAGE CURRENT SINKS (LVLED1–LVLED5)

Current sinks LVLED1 to LVLED5 each provide the current for a single LED. These low-voltage sinks are configurable with different blinking patterns via the 4 internal pattern generators. Each low-voltage current sink has 8-bit brightness control and 5-bit full-scale current programmability. Additionally, each low-voltage current sink can have its current set through a dedicated brightness register, the PWM input, the ambient light sensor interface, or a combination of these. Configuration of the low-voltage current sinks is done through the low-voltage Control Banks (C, D, E, or F). Any low-voltage current sink can be mapped to any of the low-voltage control banks.

LOW-VOLTAGE LED BIASING

Each low-voltage LED can be powered from the LM3533's charge pump output (CPOUT) or from an external source. When powered from CPOUT the anode connect bit (Anode Connect Register bits [6:2]) for that particular low-voltage current sink must be set to '1' (default). This allows for the specific low-voltage current sink to have control over the charge pumps gain control (see AUTOMATIC GAIN section).

When powered from alternate sources (such as VIN) the anode connect bit for the particular low-voltage current sink must be set to '0'. This removes the particular current sink from the charge pump feedback loop. In these configurations the application must ensure that the headroom voltage across the low-voltage current sink is high enough to prevent the low-voltage current sinks from going into dropout (see Typical Performance Characteristics for data on the low-voltage LED current vs headroom voltage).

The LVLEDX Anode Connect bits also determine how the Shorted low-voltage LED String fault flag is triggered (see Fault Flags/Protection Features).

LED Current Mapping Modes

All control banks can be programmed for either exponential or linear mapping modes (see Figure 42). These modes determine the transfer characteristic of backlight code to LED current.

EXPONENTIAL MAPPING

In Exponential Mapping Mode the brightness code to backlight current transfer function is given by the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.862^{\left[46.6 - \left(\frac{Code+1}{5.5}\right)\right]} \times D_{PWM} \quad (1)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting (see Table 12), Code is the backlight code in the brightness register, and D_{PWM} is the PWM input duty cycle. In Exponential Mapping Mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

LINEAR MAPPING

In Linear Mapping Mode the brightness code to backlight current has a linear relationship and follows the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \times D_{PWM} \quad (2)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting, Code is the backlight code in the brightness register, and D_{PWM} is the PWM input duty cycle.

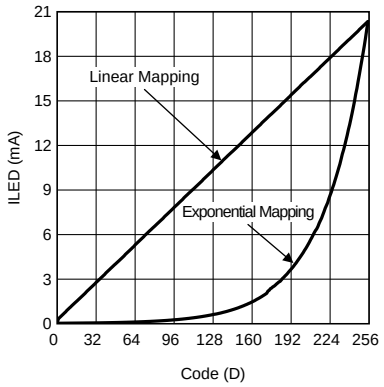


Figure 42. LED Current Mapping Modes

LED Current Ramping

STARTUP/SHUTDOWN RAMP

The startup and shutdown ramp times are independently programmable in the Startup/Shutdown Transition Time Register (see Table 5). There are 8 different Startup and 8 different Shutdown times. The startup times can be programmed independently from the shutdown times, but teach Control bank is not independently programmable. For example, programming a startup or shutdown time will not affect the already pre-programmed ramp time for each Control Bank.

The startup ramp time is from when the Control Bank is enabled to when the LED current reaches its initial set point. The shutdown ramp time is from when the Control Bank is disabled to when the LED current reaches 0.

RUN-TIME RAMP

Current ramping from one brightness level to the next is programmed via the Run-Time Transition Time Register (see Table 6**).** There are 8 different ramp-up times and 8 different ramp-down times. The ramp-up time can be programmed independently from the ramp-down time, but each Control Bank cannot be independently programmed. For example, programming a ramp-up or ramp-down time is a global setting for all Control Banks.

Brightness Register Current Control

For simple user-adjustable current control, the LM3533 features Brightness Register Current Control. This mode is selected via the Control Bank Brightness Configuration Registers (see Table 9 and Table 11). Once set for Brightness Register Current Control, the LED current is set by writing directly to the appropriate Control Bank Brightness Registers (see Table 29). In this mode the current for a particular Control Bank becomes a function of the full-scale LED current, the 8-bit code in the respective brightness register, and the PWM input duty cycle (if PWM is enabled). The Control Bank Brightness Register contains an 8-bit code which represents the percentage of the full-scale LED current. This percentage of full-scale current is different depending on the selected mapping mode (see LED Current Mapping Modes).

PWM Control

The LM3533's PWM input can be enabled for any of the Control Banks (see Table 8). Once enabled, the LED current becomes a function of the code in the Control Bank Brightness Configuration Register and the PWM input-duty cycle.

The PWM input accepts a logic level voltage and internally filters it to an analog control voltage. This results in a linear response of duty cycle to current, where 100% duty cycle corresponds to the programmed brightness code multiplied by the Full-Scale Current setting.

PWM INPUT FREQUENCY RANGE

The usable input frequency range for the PWM input is governed on the low end by the cutoff frequency of the internal low-pass filter (540Hz, Q = 0.33) and on the high end by the propagation delays through the internal logic. For frequencies below 2kHz the current ripple begins to become a larger portion of the DC LED current. Additionally, at lower PWM frequencies the boost output voltage ripple increases, causing a non-linear response from the PWM duty cycle to the average LED current due to the response time of the boost. For the best response of current vs. duty cycle, the PWM input frequency should be kept between 2kHz and 100kHz.

PWM INPUT POLARITY

The PWM Input can be set for active low polarity, where the LED current is a function of the negative duty cycle. This is set via the OVP/Boost Frequency/PWM Polarity Register (see Table 21).

ALS Current Control

The LM3533 features Ambient Light Sensor (ALS) current control which allows the LED current to be automatically set based upon the received ambient light. To implement ambient light current control the LM3533 uses a 5 brightness zone implementation with 3 sets of Zone Targets.

ALS BRIGHTNESS ZONES (ZONE BOUNDARIES)

The LM3533 provides for a 5 brightness zone ambient light sensor interface. This allows for the LED current in any current sink to change based upon which zone the received ambient light falls into. The brightness zones are configured via 4 ALS Zone Boundary High and 4 ALS Zone Boundary Low Registers. Each Zone Boundary register is 8 bits with a full-scale voltage of 2V. This gives a 2V/255 = 7.843mV per bit. Figure 44 shows the mapping from the ALS Brightness Zone to the target backlight current.

ZONE BOUNDARY HYSTERESIS

For each Zone Boundary there are two Zone Boundary Registers: a Zone Boundary High Register and a Zone Boundary Low Register (see Table 31). The difference between the Zone Boundary High and Zone Boundary Low Registers (for a specific zone) creates the hysteresis that is required to transition between zones. This hysteresis prevents the backlight current from oscillating between zones when the ALS voltage is close to a Zone Boundary Threshold. For Zone-to-Zone transitions the increasing ALS voltage must cross the Zone Boundary High Threshold in order to get into the next higher zone. Conversely, the ALS decreasing voltage must cross below the Zone Boundary Low Threshold in order to get into the next lower zone. Figure 43 describes this Zone Boundary Hysteresis.

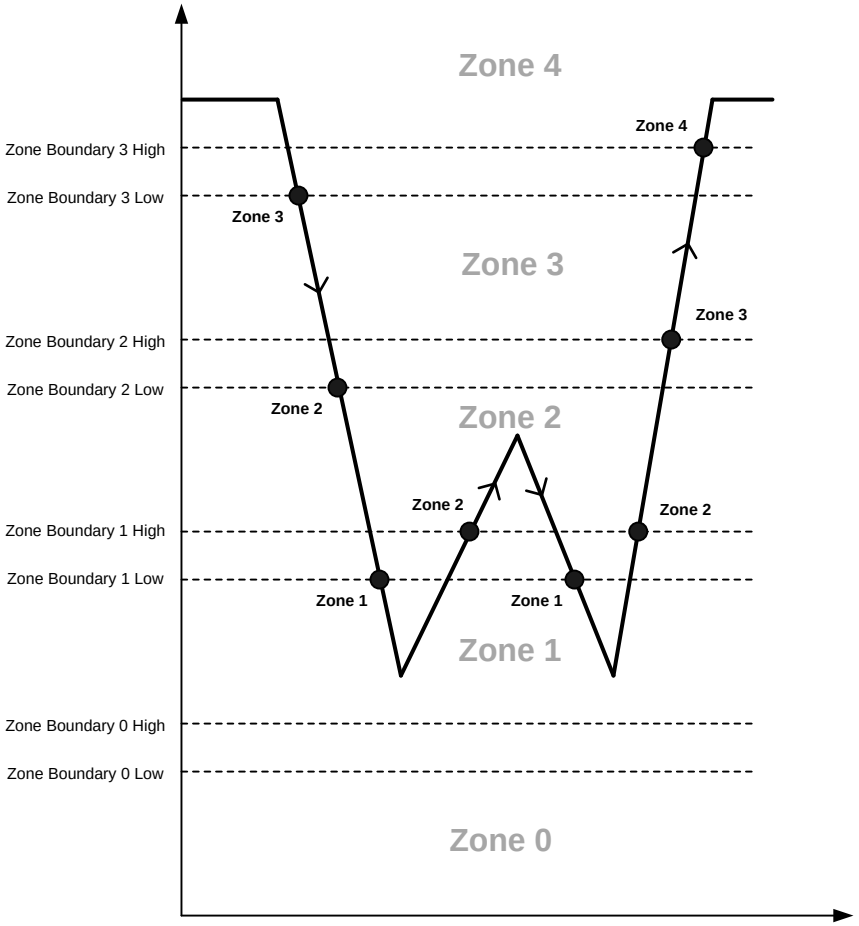


Figure 43. ALS Zone Boundary + Hysteresis

Note: The arrows indicate the direction of the ALS voltage.

ZONE TARGET REGISTERS (ALSM1, ALSM2, ALSM3)

For each brightness zone there is a programmable brightness target which is set via the ALS Zone Target Registers (see Table 32, Table 33, and Table 34). There are 3 sets of ALS Zone Target Registers (ALSM1, ALSM2, and ALSM3). The ALSM1 Zone Target Registers are dedicated to only Control Bank 1. ALSM2 and ALSM3 registers can be assigned to any of the Control Banks (B – F) (see Table 9 and Table 11). Each of the Zone Target Registers consists of an 8-bit code which is a percentage of the programmed full-scale current. This percentage of full-scale current is dependent on the selected mapping mode. Figure 44 details the mapping of the ALS Brightness Zone to the ALSM_ Zone Target Registers.

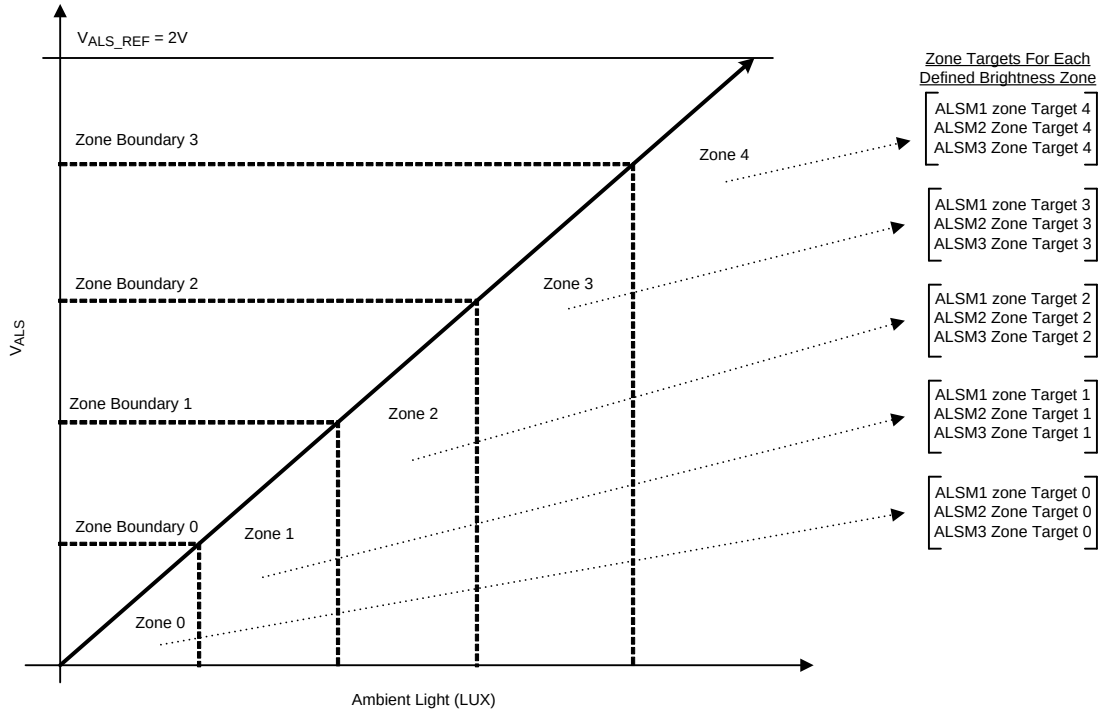


Figure 44. ALS Brightness Zone to Backlight Current Mapping

PWM INPUT IN ALS MODE

The PWM input can be enabled for any of the 5 Brightness Zones (see Table 8). This makes the brightness target for the PWM enabled zone have its current a function of the PWM input duty cycle, the full-scale current setting for that particular bank, and the brightness target for that particular zone.

ALS Functional Blocks

Figure 45 shows the functional block diagram of the LM3533's ambient light sensor (ALS) interface.

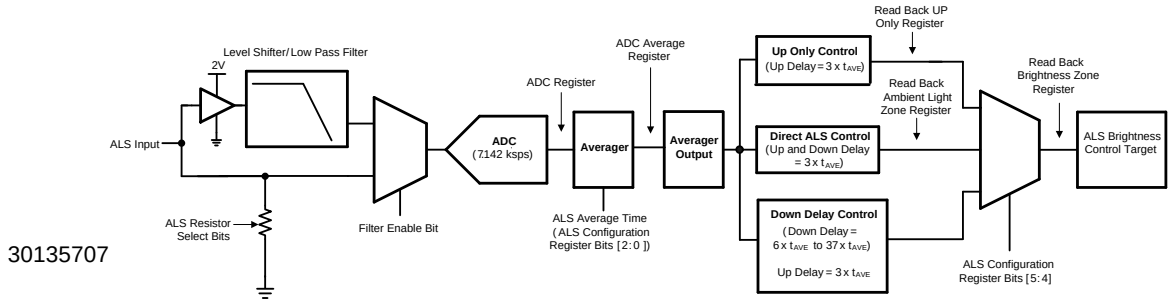


Figure 45. Ambient Light Sensing Block Diagram

AMBIENT LIGHT SENSOR INPUT

The ALS input is designed to connect to an analog or PWM output ambient light sensor. The ALS Configuration Register Bit [1] selects which type of sensor interface will be used at the ALS input (see Table 23).

ANALOG OUTPUT AMBIENT LIGHT SENSORS (ALS GAIN SETTING RESISTORS)

With ALS Cnfiguration Register bit [1] = 0, the ALS input is set for Analog Sensor mode. In this mode the LM3533 offers 128 programmable internal resistors at the ALS input (including a high-impedance option); see Table 22. These resistors are designed to take the output of an analog ambient light sensor and convert it into a voltage. The value of the resistor selected is typically chosen such that the ALS input voltage is 2V at the maximum ambient light (LUX) value. The sensed voltage at the ALS input is digitized by the LM3533's internal 8-bit ADC with a full-scale value (0xFF) corresponding to 2V.

PWM OUTPUT AMBIENT LIGHT SENSORS (INTERNAL FILTERING)

With the ALS Configuration Register bit [1] = 1, the ALS input is set for PWM-Sensor mode. In this mode the LM3533 offers an internal level shifter and low-pass filter (ALS PWM Input mode). With this mode enabled the ALS input accepts logic level PWM signals and converts them into a 0-to-2V analog voltage which is then filtered. This 0-to-2V analog representation of the PWM signal is then applied to the internal 8-bit ADC, where 2V is the full scale (code 0xFF). The internal filter has a corner frequency of 540Hz and provides 51dB of attenuation (355x) at a 10kHz input frequency.

Since the internal ADC for the ambient light sensor utilizes an 8-bit ADC, the attenuation of the ALS input signal needs to be greater than 1/255 (1 LSB = 7.843mV) in order to realize the full 8-bit range. This forces the frequency for the PWM signal at the ALS input to be around 6kHz or greater. For slower moving signals an external RC filter may need to be combined with the Analog Sensor Mode (see Applications Information section).

When the ALS input is set for ALS PWM Input Mode the internal ALS resistor setting is automatically set for high impedance, no matter what the setting in the ALS Select Register.

INTERNAL 8-BIT ADC

The LM3533 digitizes the ALS voltage using an internal 8-bit ADC. The ADC is active as long as the ALS enable bit is set. Once set, the ADC begins sampling and converting the voltage at the ALS input at 7.142ksps. The ADC output can be read back via the ADC register (address 0x37). With the ALS enable bit set, the ADC register is updated every 140µs. Figure 46 details the timing of the ADC.

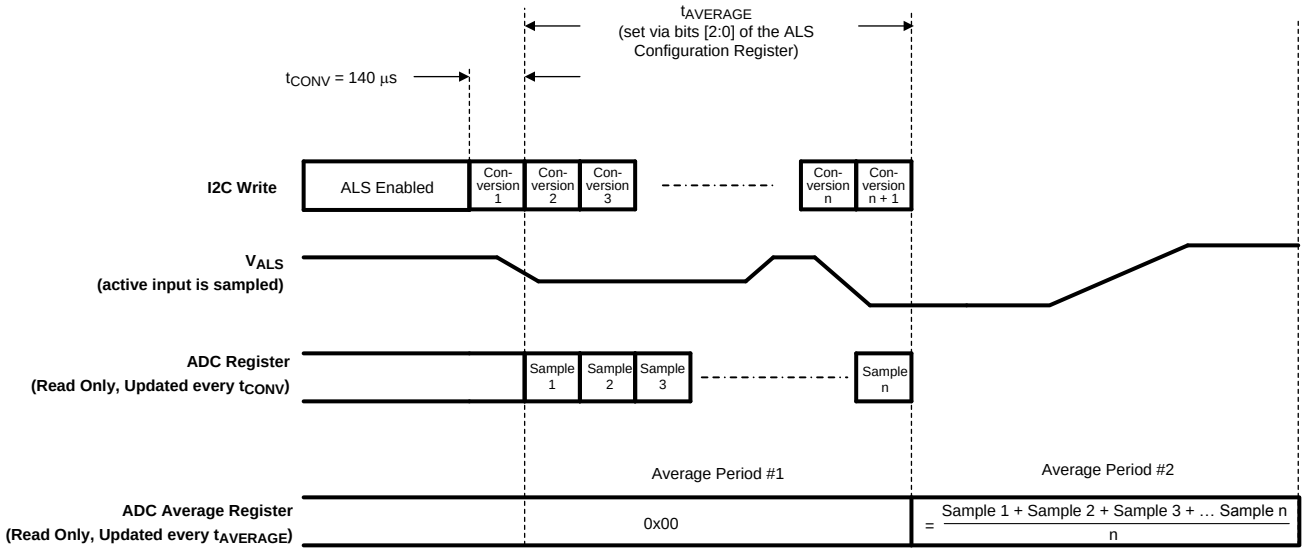


Figure 46. ADC Timing

ALS AVERAGER

Once digitized the output of the ADC is sent into the ALS averager. The averager will compute the average of the number of samples taken over the programmed average period. The ALS average times are set via bits [5:3] in the ALS Configuration Register. The output of the ALS average can be read back via the ADC Average register (address 0x38). With the ALS Enable bit set, the ADC Average register is updated after each average period (see Figure 46). After every average period the Averager Output stores the information for which brightness zone the ALS input voltage resides in (see Figure 45).

INITIALIZING THE ALS

On initial startup of the ALS Interface, the Ambient Light Zone will default to Zone 0. This allows the ALS to start off in a predictable state. The drawback is that Zone 0 is often not representative of the true ALS Brightness Zone, since the ALS input can get to its ambient light representative voltage much faster than the LED current is allowed to change. In order to avoid a multiple average time wait for the backlight current to get to its correct state, the LM3533 switches over to a fast average period (1.1 ms) during the ALS startup. This will quickly bring the ALS Brightness Zone (and the backlight current) to its correct setting (see Figure 47).

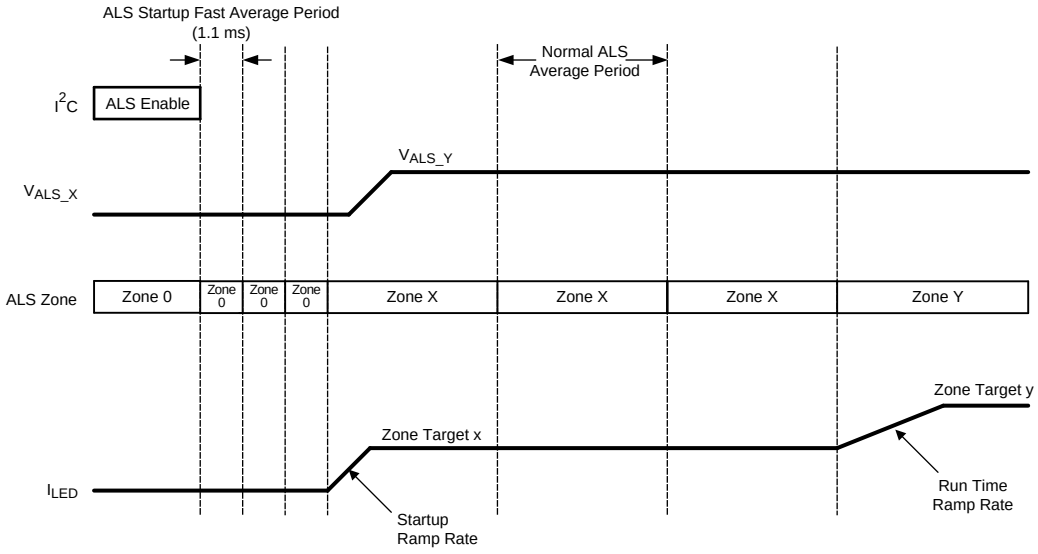


Figure 47. ALS Startup Sequence

ALS ALGORITHMS

There are three ALS algorithms that can be selected independently by each ALS Mapper (ALSM1, ALSM2, and ALSM3) (see Table 24). The ALS algorithms are: direct, up only, and down delay.

ALS RULES

For each algorithm, the ALS follows these basic rules:

1. For the ALS Interface to force a change in the backlight current (to a higher zone target), the averager output must have shown an increase for 3 consecutive average periods, or an increase and a remain at the new zone for 3 consecutive average periods.
2. For the ALS Interface to force a change in the backlight current (to a lower zone target), the averager output must have shown a decrease for 3 consecutive average periods, or a decrease and remain at the new zone for 3 consecutive average periods.
3. If condition #1 or #2 is satisfied and during the next average period the averager output changes again in the same direction as the last change, the LED current will immediately change at the beginning of the next average period.
4. If condition #1 or #2 is satisfied, and the next average period shows no change in the average zone, or

shows a change in the opposite direction, then the criteria in step #1 or #2 must be satisfied again before the ALS interface can force a change in the backlight current.

5. The Averager Output (see Figure 45) contains the zone that is determined from the most recent full average period.
6. The ALS Interface only forces a change in the backlight current at the beginning of an average period.
7. When the ALS forces a change in the backlight current the change will be to the brightness target pointed to by the zone in the Averager Output.

DIRECT ALS CONTROL

In direct ALS control the LM3533's ALS Interface can force the backlight current to either a higher zone target or a lower zone target using the rules described in the ALS RULES section. In the example of Figure 48, the plot shows the ALS voltage, the current average zone which is the zone determined by averaging the ALS voltage in the current average period, the Averager Output which is the zone determined from the previous full average period, and the target backlight current that is controlled by the ALS Interface. The following steps detail the Direct ALS algorithm:

1. When the ALS is enabled the ALS fast startup (1.1ms average period) quickly brings the Averager Output to the correct zone. This takes 3 fast average periods or approximately 3.3ms.
2. The 1st average period the ALS voltage averages to Zone 4.
3. The 2nd average period the ALS voltage averages to Zone 3.
4. The 3rd average period the ALS voltage averages to Zone 0 and the Averager Output shows a change from Zone 4 to Zone 3.
5. The 4th average period the ALS voltage averages to Zone 2 and the Averager Output remains at its changed state of Zone 3.
6. The 5th average period the ALS voltage averages to Zone 1. The Averager Output shows a change from Zone 3 to Zone 2. Since this is the 3rd average period that the Averager Output has shown a change in the decreasing direction from the initial Zone 4, the backlight current is forced to change to the current Averager Output (Zone 2's) target current.
7. The 6th average period the ALS voltage averages to Zone 2. The Averager Output changes from Zone 2 to Zone 1. Since this is in the same direction as the previous change, the backlight current is forced to change to the current Averager Output (Zone 1's) target current.
8. The 7th average period the ALS voltage averages to Zone 3. The Averager Output changes from Zone 1 to Zone 2. Since this change is in the opposite direction from the previous change, the backlight current remains at Zone 1's target.
9. The 8th average period the ALS voltage averages to Zone 3. The Averager Output changes from Zone 2 to Zone 3.
10. The 9th average period the ALS voltage averages to Zone 3. The Averager Output remains at Zone 3. Since this is the 3rd average period that the Averager Output has shown a change in the increasing direction from the initial Zone 1, the backlight current is forced to change to the current Averager Output (Zone 3's) target current.
11. The 10th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 3.
12. The 11th average period the ALS voltage averages to Zone 4. The Averager Output changes to Zone 4.
13. The 12th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4.
14. The 13th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4. Since this is the 3rd average period that the Averager Output has shown a change in the increasing direction from the initial Zone 3, the backlight current is forced to change to the current Averager Output (Zone 4's) target current.

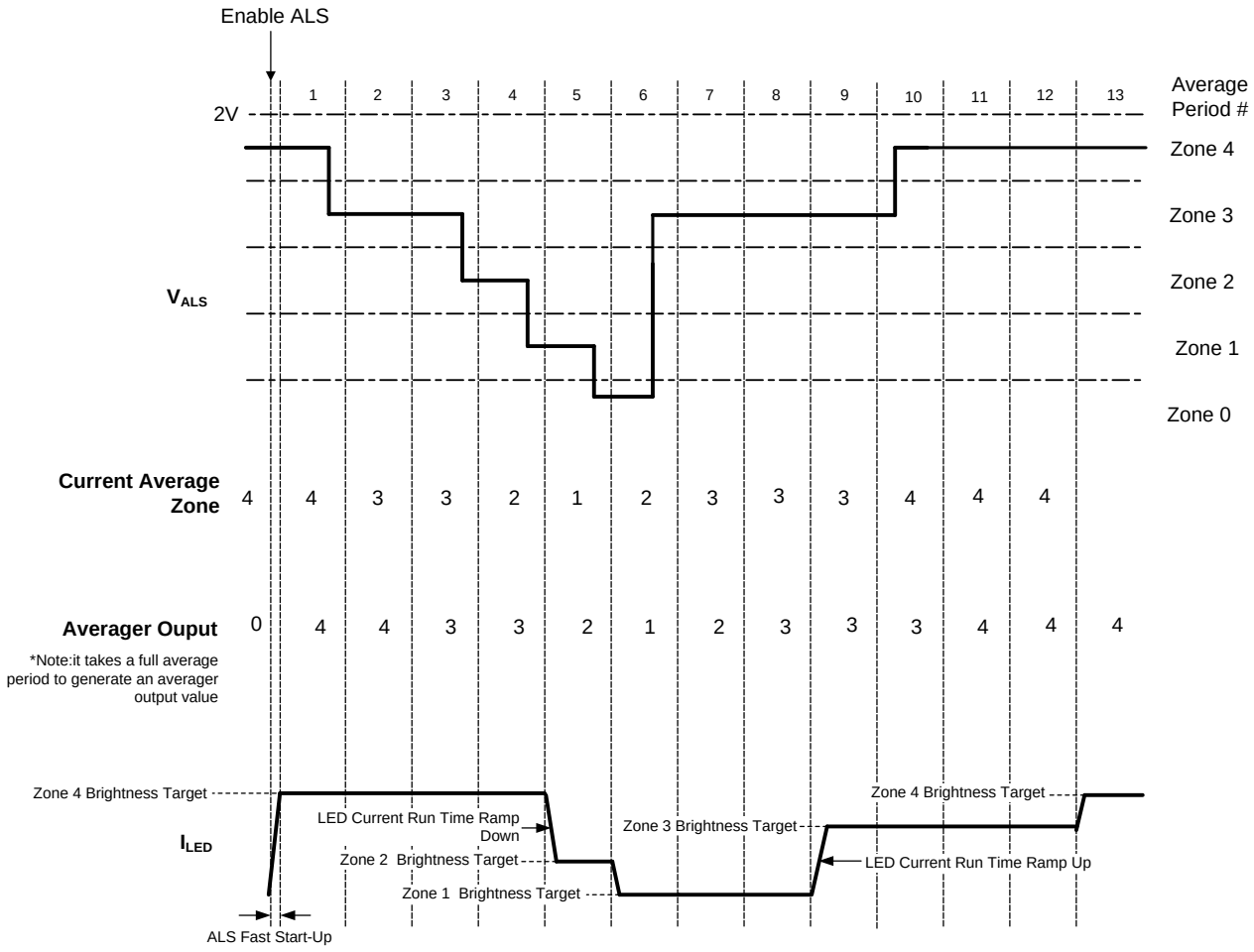


Figure 48. Direct ALS Control

UP-ONLY CONTROL

The ALS Up-Only Control algorithm is similar to Direct ALS Control except the ALS Interface can only program the backlight current to a higher zone target. Referring to Figure 49:

1. When the ALS is enabled the ALS fast startup (1.1ms average period) quickly brings the Averager Output to the correct zone. This takes 3 fast average periods or approximately 3.3ms.
2. The 1st average period the ALS voltage averages to Zone 1.
3. The 2nd average period the ALS voltage averages to Zone 0.
4. The 3rd average period the ALS voltage averages to Zone 0, and the Averager Output shows a change from Zone 1 to Zone 0.
5. The 4th average period the ALS voltage averages to Zone 2, and the Averager Output remains at its changed state of Zone 0.
6. The 5th average period the ALS voltage averages to Zone 2. The Averager Output remains at Zone 0. Since the Up Only algorithm is chosen the backlight current remains at the Zone 1 target even though this is the 3rd consecutive average period that the Averager Output has shown a change since the initial Zone 1.
7. The 6th average period the ALS voltage averages to Zone 2. The Averager Output changes from Zone 0 to Zone 2.
8. The 7th average period the ALS voltage averages to Zone 3. The Averager Output remains at Zone 2.
9. The 8th average period the ALS voltage averages to Zone 3. The Averager Output remains at Zone 2. Since this is the 3rd average period that the Averager Output has shown a change in the up direction, the backlight

current is forced to change to the current Averager Output (Zone 2's) target current.

10. The 9th average period the ALS voltage averages to Zone 3. The Averager Output changes from Zone 2 to Zone 3. Since this is a change in the increasing Zone direction, and is a consecutive change following a new backlight target current transition, the backlight current is again forced to change to the current Averager Output (Zone 3's) target current.
11. The 10th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 3.
12. The 11th average period the ALS voltage averages to Zone 4. The Averager Output changes to Zone 4.
13. The 12th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4.
14. The 13th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4. Since this is the 3rd average period that the Averager Output has shown a change in the increasing direction from the initial Zone 3, the backlight current is forced to change to the current Averager Output (Zone 4's) target current.

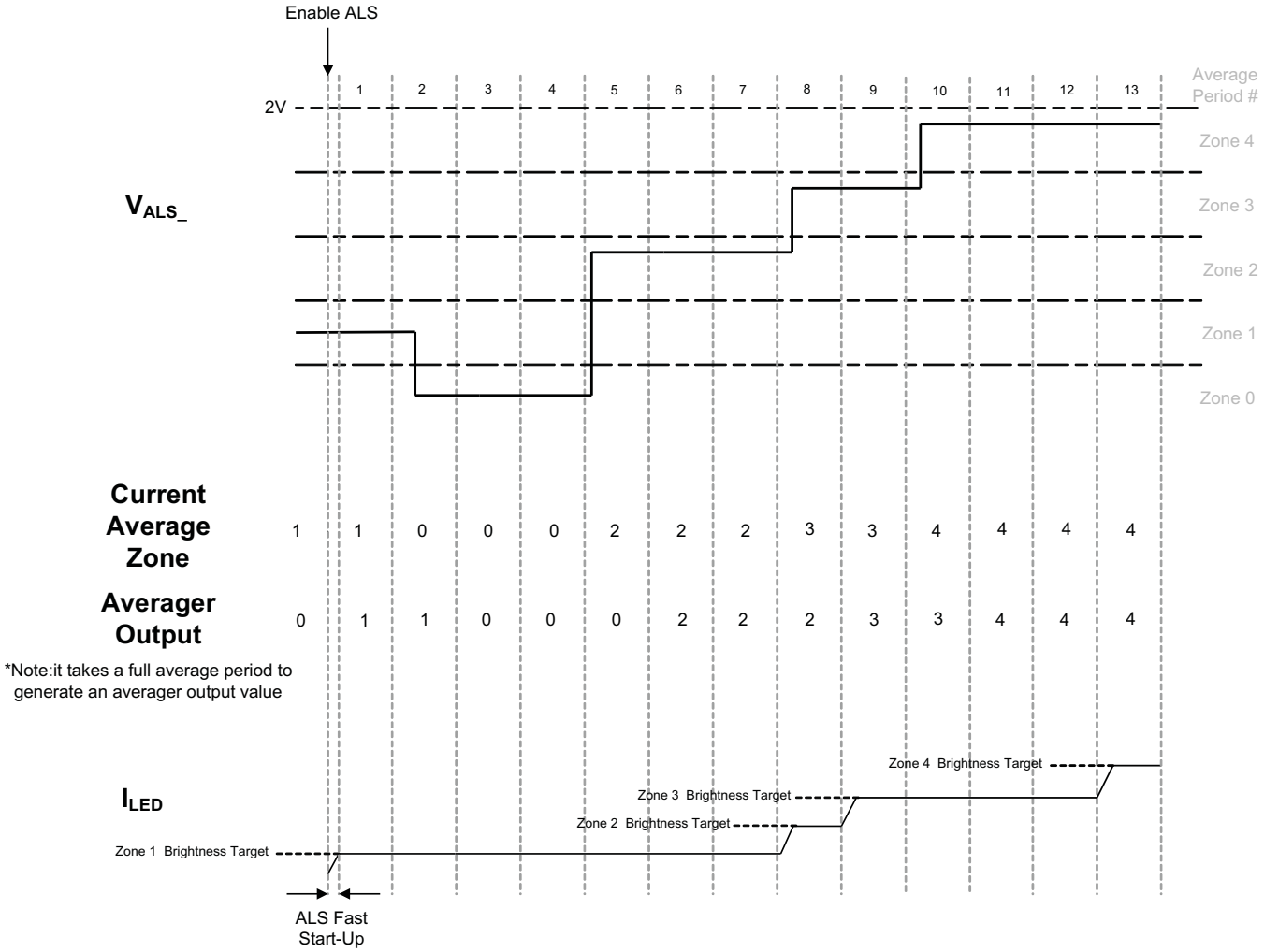


Figure 49. ALS Up-Only Control

DOWN-DELAY CONTROL

The Down-Delay algorithm uses all the same rules from the ALS RULES section, except it provides for adding additional average period delays required for decreasing transitions of the Averager Output, before the LED current is programmed to a lower zone target current. The additional average period delays are programmed via the ALS Down Delay register. The register provides 32 settings for increasing the down delay from 3 extra (code 00000) up to 34 extra (code 11111). For example, if the down delay algorithm is enabled, and the ALS Down

Delay register was programmed with 0x00 (3 extra delays), then the Averager Output would need to see 6 consecutive changes in decreasing Zones (or 6 consecutive average periods that changed and remained lower), before the backlight current was programmed to the lower zones target current. Referring to Figure 50, assume that Down Delay is enabled, and the ALS Down Delay register is programmed with 0x02 (5 extra delays, or 8 average period total delays for downward changes in the backlight target current):

1. When the ALS is enabled the ALS fast startup (1.1ms average period) quickly brings the Averager Output to the correct zone. This takes 3 fast average periods or approximately 3.3ms.
2. The first average period the ALS voltage averages to Zone 3.
3. The second average period the ALS voltage averages to Zone 2. The Averager Output remains at Zone 3.
4. The 3rd through 7th average period the ALS voltage averages to Zone 2, and the Averager Output stays at Zone 2.
5. The 8th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 2.
6. The 9th and 10th average periods the ALS voltage averages to Zone 4. The Averager Output is at Zone 4. Since the Averager Output increased from Zone 2 to Zone 4 and the required Down Delay time was not met (8 average periods), the backlight current was never changed to the Zone 2's target current.
7. The 11th average period the ALS voltage averages to Zone 2. The Averager Output remains at Zone 4. Since this is the 3rd consecutive average period where the Averager Output has shown a change (increasing direction) since the change from Zone 2, the backlight current transitions to Zone 4's target current.
8. The 12th through 26th average periods the ALS voltage averages to Zone 2. The Averager Output remains at Zone 2. At the start of average period #19 the Averager Output has shown the required 8 average period delay from the initial change from Zone 4 to Zone 2. As a result the backlight current is programmed to Zone 2's target current.

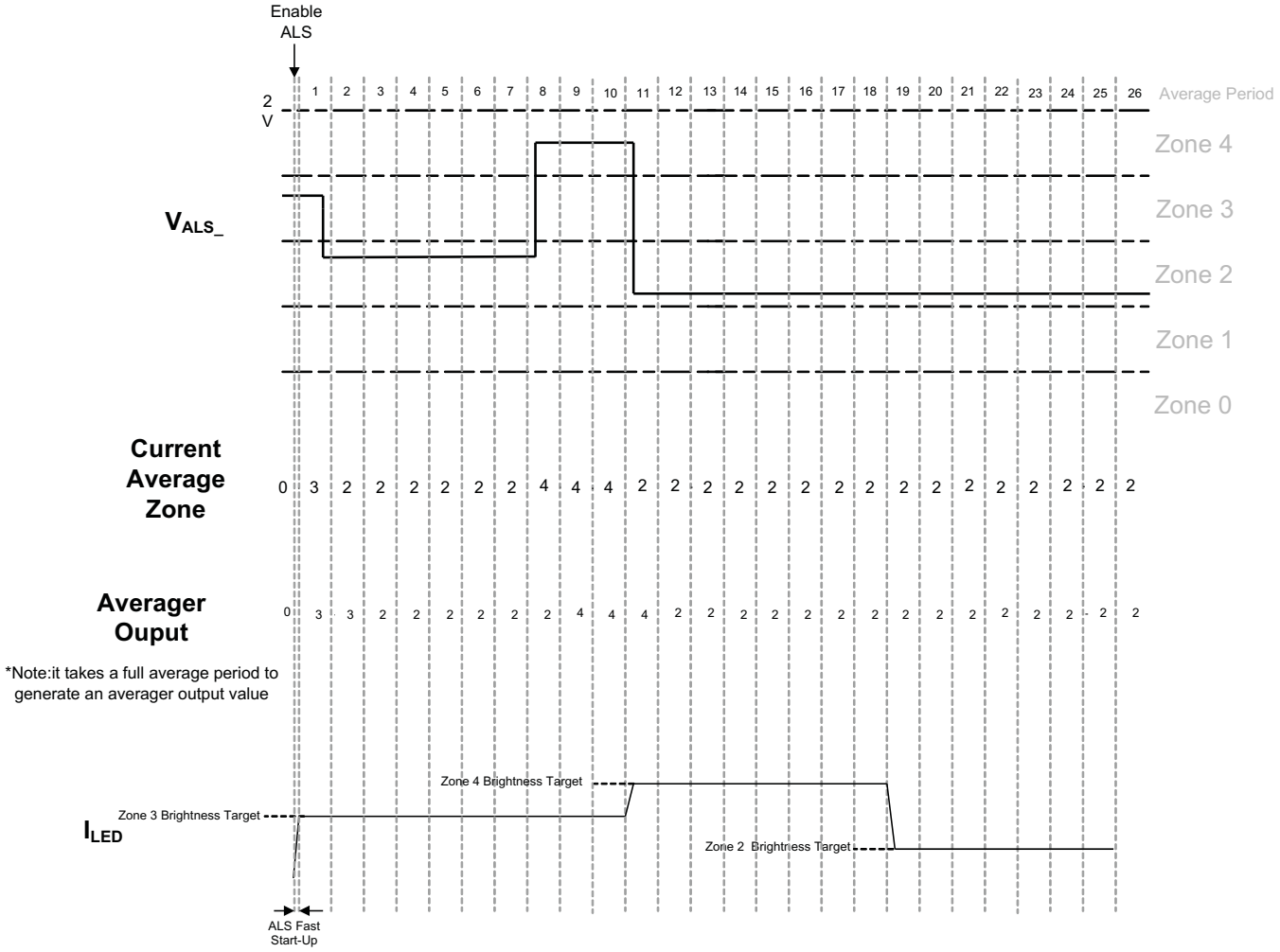


Figure 50. ALS Down-Delay Control

Pattern Generator

The LM3533 contains 4 programmable pattern generators (one for each low-voltage control bank). Each pattern generator has the ability to drive a unique programmable pattern. Each pattern generator has its own set of registers available for pattern programming. The programmable patterns are : delay time, rise time, fall time, high period, low period, high current and low current (see Figure 51).

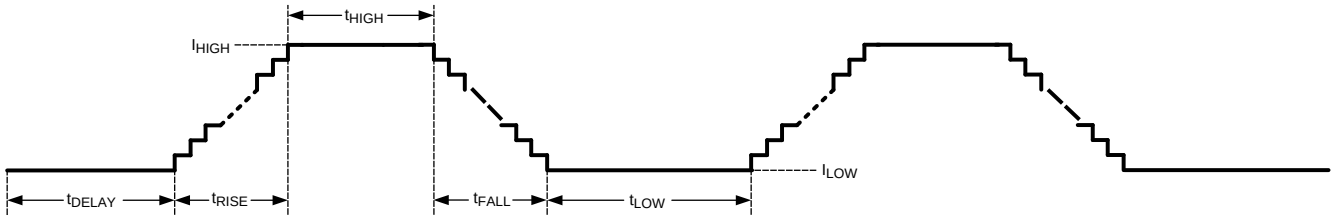


Figure 51. Pattern Generator Timing

DELAY TIME

The Delay time (t_{DELAY}) is the delay from when the pattern is enabled to when the LED current begins ramping up in the control bank's assigned current source(s). The pattern starts when bit [3] of the respective Control Bank Brightness Configuration Register is written high. There is one t_{DELAY} register for each pattern generator (4 total). The selectable times are programmed with the lower 6 bits of the t_{DELAY} registers. The times are split into 2 groups where codes 0x00 to 0x3C are short durations from 16.384ms (code 0x00) up to 999.424ms (code 0x3C) or 16.384ms/bit. The higher codes (0x3D to 0x7F) select t_{DELAY} from 1130.496ms up to 9781.248ms, or 131.072ms/bit (see Table 36).

RISE TIME

The LED current rise time (t_{RISE}) is the time the LED current takes to move from the low-current brightness level (I_{LOW}) to the high-current brightness level (I_{HIGH}). The rise time of the LED current (t_{RISE}) is set via the Pattern Generator Rise Time Registers. Each Pattern Generator has its own rise-time register. There are 8 available rise-time settings (see Table 43).

FALL TIME

The LED current fall time (t_{FALL}) is the time the LED current takes to move from the high-current brightness level (I_{HIGH}) to the low-current brightness level (I_{LOW}). The fall time of the LED current (t_{FALL}) is set via the Pattern Generator Fall Time Registers. Each Pattern Generator has its own fall-time register. There are 8 available fall-time settings (see Table 44).

HIGH PERIOD

The LED current high period (t_{HIGH}) is the duration that the LED pattern spends at the high LED current set point (t_{HIGH}). The t_{HIGH} times are programmed via the Pattern Generator t_{HIGH} Registers. The programmable times are broken into 2 groups. The first set (from code 0x00 to 0x3C) increases the t_{HIGH} time in steps of 16.384ms. The second set (from code 0x3D to 0x7F) increases the t_{HIGH} time in steps of 131.072ms (see Table 40).

LOW PERIOD

The LED current low period (t_{LOW}) is the duration that the LED current spends at the low LED current set point (I_{LOW}). The t_{LOW} times are programmed via one of the Pattern Generator t_{LOW} Registers. There are 256 t_{LOW} settings and are broken into 3 groups of linearly increasing times. The first set (from code 0x00 to 0x3C) increases the t_{LOW} time in steps of 16.384ms. The second set (from code 0x3D to 0x7F) increases the t_{LOW} time in steps of 131.072ms. The third set (from code 0x80 to 0xFF) increases the t_{LOW} time in steps of 524.288ms (see Table 38).

LOW-LEVEL BRIGHTNESS

The LED current low brightness level (I_{LOW}) is the LED current set point that the pattern rests at during the t_{LOW} period. This level is set via the Pattern Generator Low Level Brightness Register(s). The brightness level has 8 bits of programmability. I_{LOW} is a function of the Control Banks full-scale Current setting, the code in the Pattern Generator Low-Level Brightness Register, the Mapping Mode selected, and the PWM input duty cycle (if PWM is enabled).

For exponential mapping I_{LOW} is:

$$I_{LOW} = I_{LED\_FULLSCALE} \times 0.85^{\left[40 - \left(\frac{BREGL\_X + 1}{6.4}\right)\right]} \times D_{PWM} \quad (3)$$

For linear mapping I_{LOW} is:

$$I_{LOW} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times BREGL\_X \times D_{PWM} \quad (4)$$

BREGL_X is the Pattern Generator Low-Level Brightness Register setting for the specific Control Bank (see Table 41).

HIGH-LEVEL BRIGHTNESS

The LED current high brightness level (I_{HIGH}) is the LED current set point that the pattern rests at during the t_{HIGH} period. This high-current level is set via the Control Banks Brightness Register (BREGCH-BREGFH). The brightness level has 8 bits of programmability. I_{HIGH} is a function of the Control Banks Full-Scale Current setting, the code in the Control Banks Brightness Register, the Mapping Mode selected, and the PWM input duty cycle (if PWM is enabled).

For exponential mapping I_{HIGH} is:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.862^{\left[46.6 - \left(\frac{Code+1}{5.5}\right)\right]} \times D_{PWM} \quad (5)$$

For linear mapping I_{HIGH} is:

$$I_{HIGH} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times BREGH\_X \times D_{PWM} \quad (6)$$

BREGH_X is the Control Banks Brightness Register setting for the specific Control Bank (see Table 29).

ALS CONTROLLED PATTERN CURRENT

The current levels (I_{HIGH} and I_{LOW}) of the programmable pattern can also be influenced by the ALS input. All the same ALS algorithms apply to the pattern generator current levels (Direct, Up Only, and Down Delay). The difference, however, for the ALS Controlled Pattern Current is that the pattern current is not changed to zone-defined brightness targets, but is changed by a scaled factor of the existing I_{HIGH} and I_{LOW} levels. These scaled factors are programmable in the ALS Pattern Scaler Registers (see Table 18, Table 19 , and Table 20). Each defined brightness zone has a 4-bit (16-level) scale factor, which takes the programmed pattern current code and multiplies it by the programmed scale factor. This produce a new I_{HIGH} and I_{LOW} current level ranging from 1/16 × BREGH and 1/16 × BREGL up to 16/16 × BREGH and 16/16 × BREGL for each ALS zone (see Figure 52). There is only one set of scale factors for all the pattern generators.

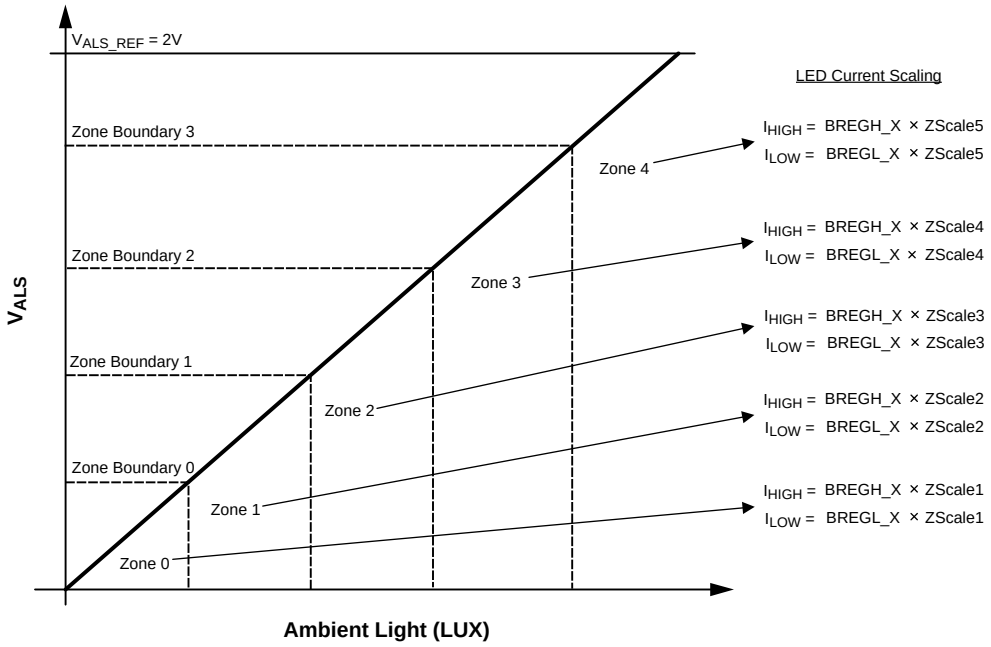


Figure 52. ALS Controlled Pattern Current Scaling

For low-voltage control banks that do not have their pattern generator enabled, ALS current control is done via the ALS Mappers. Once a pattern generator is enabled, that particular Control Bank will then use the pattern scalers for ALS Current Control.

INTERRUPT OUTPUT MODE

When INT Mode is enabled (ALS Zone Information Register Bit [0] = 1), INT pin is configured as an interrupt output. INT is an open-drain output with an active pulldown of typically 66Ω. In INT Mode the INT output pulls low if the ALS interface is enabled, and the ALS input has changed zones. Reading back the ALS Zone Information while in this mode will clear the INT output and reset it to its open-drain state.

Fault Flags/Protection Features

The LM3533 contains both an LED open and LED short fault detection. These fault detections are designed to be used in production level testing and not normal operation. For the fault flags to operate, they must be enabled via the LED Fault Enable Register (see Table 48). The following sections detail the proper procedure for reading back open and short faults in both the HVLED and LVLED strings.

OPEN LED STRING (HVLED)

An open LED string is detected when the voltage at the input to any active high-voltage current sink has fallen below 200mV, and the boost output voltage has hit the OVP threshold. This test assumes that the HVLED string that is being detected for an open is connected to the LM3533's boost output (COUT+) (see Table 14). For an HVLED string not connected to the LM3533's boost output voltage, but connected to another voltage source, the boost output will not trigger the OVP flag. In this case an open LED string will not be detected.

The procedure for detecting an open fault in the HVLED current sinks (provided they are connected to the boost output voltage) is:

- Apply power to the LM3533
- Enable Open Fault (Register 0xB2, bit [0] = 1)
- Configure HVLED1 and HVLED2 for LED string anode connected to COUT (Register 0x25, bits[1:0] = (1,1)
- Set Bank A full-scale current to 20.2mA (Register 0x1F = 0x13)
- Set Bank A brightness to max (Register 0x40 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign HVLED1 and HVLED2 to Bank A (Register 0x10, Bits [1:0] = (0, 0)
- Enable Bank A (Register 0x27 Bit[0] = 1
- Wait 4ms
- Read back bits[1:0] of register 0xB0. Bit [0] = 1 (HVLED1 open). Bit [1] = 1 (HVLED2 open)
- Disable all banks (Register 0x27 = 0x00)

SHORTED LED STRING (HVLED)

The LM3533 features an LED short fault flag indicating one or more of the HVLED strings have experienced a short. The method for detecting a shorted HVLED strings is if the current sink is enabled and the string voltage (V_{OUT} - $V_{HVLED1/2}$) falls to below (V_{IN} - 1V) . This test must be performed on one HVLED string at a time. Performing the test with both current sinks enabled can result in a faulty reading if one of the strings is shorted and the other is not.

The procedure for detecting a short in an HVLED string is:

- Apply power to the LM3533
- Enable Short Fault (Register 0xB2, bit [1] = 1)
- Enable Feedback on the HVLED Current Sinks (Register 0x25 = 0xFF)
- Set Bank A full-scale current to 20.2mA (Register 0x1F = 0x13)
- Set Bank A brightness to max (Register 0x40 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign HVLED1 to Bank A (Register 0x10, Bits [1:0] = (1, 0)
- Enable Bank A (Register 0x27 Bit[0] = 1
- Wait 4ms
- Read back bits[0] of register 0xB1. 1 = HVLED1 open
- Disable all banks (Register 0x27 = 0x00)
- Repeat the procedure for the HVLED2 string

OPEN LED (LVLED)

The LM3533 features an open LED fault flag indicating one or more of the active LVLED strings are open. An open in an LVLED string is flagged if the voltage at the input to any active low-voltage current sink goes below 110mV.

Since the open LED detect is flagged when any active current sink input falls below 110mV, certain configurations can result in falsely triggering an open. These include:

1. LED anode tied to CPOUT, charge pump in 1X gain, and VIN drops low enough to bring any active LVLED current sink below 110mV.
2. LED anode not tied to CPOUT and VLED_ANODE goes low enough to bring any active LVLED current sink below 110mV.

The following list describes a test procedure that can be used in detecting an open in the LVLED strings:

- Apply power to the LM3533
- Enable Open Fault (Register 0xB2, bit [0] = 1)
- Configure all LVLED strings for Anode connected to CPOUT (register 0x25 bits[6:2] = 1)
- Force the Charge Pump into 2X gain (Register 0x26 Bits[2:1] = 11). Ensure that CPOUT and CP are in the circuit and that (V_{CPOUT} is > VF_{LVLED} + V_{HR_LV})
- Set Bank C full-scale Current to 20.2mA (Register 0x21 = 0x13)
- Set Bank C brightness to max (Register 0x42 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign LVLED1 - LVLED5 to Bank C (Register 0x11 = 0x00, Register 0x10 = 0x00)
- Enable Bank C (Register 0x27 Bit[2] = 1
- Wait 4ms
- Read back bits[6:2] of register 0xB0. 1 indicates an open and a 0 indicates normal operation (see Table 46)
- Disable all banks (Register 0x27 = 0x00)

SHORTED LED (LVLED)

The LM3533 features an LED short fault flag indicating when any active low-voltage LED is shorted (Anode to Cathode). A short in an LVLED is determined when the LED voltage (V_{CPOUT} - V_{HR}) falls below 1V.

A procedure for determining a short in an LVLED string is detailed below:

- Apply Power
- Enable Short Fault (Register 0xB2, bit [1] = 1)
- Enable Feedback on the LVLED Current Sinks (Register 0x25 = 0xFF)
- Set Bank C full-scale current to 20.2mA (Register 0x21 = 0x13)
- Set Bank C brightness to max (Register 0x42 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign LVLED1 to LVLED5 to Bank C (Register 0x11 = 0x00, Register 0x10 = 0x00)
- Set Charge Pump to 1X gain (Register 0x26 = 0x40)
- Enable Bank C (Register 0x27 Bit[2] = 1
- Wait 4ms
- Read bits[6:2] from register 0xB1. A 1 indicates short, and a 0 indicates normal (see Table 47).
- Disable all banks (Register 0x27 = 0x00)

OVER-VOLTAGE PROTECTION (INDUCTIVE BOOST)

The over-voltage protection threshold (OVP) on the LM3533 has 4 different programmable options (16V, 24V, 32V, and 40V). The OVP protects the device and associated circuitry from high voltages in the event the high-voltage LED string becomes open. During normal operation, the LM3533's inductive boost converter will boost the output up so as to maintain at least 400mV at the active, high-voltage (COUT connected) current sink inputs. When a high-voltage LED string becomes open, the feedback mechanism is broken, and the boost converter will over-boost the output. When the output voltage reaches the OVP threshold the boost converter will stop switching, thus allowing the output node to discharge. When the output discharges to V_{OVP} – 1V the boost converter will begin switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor's positive terminal.

For high-voltage current sinks that have the Anode Connect Register setting such that the high-voltage current sinks anodes are not connected to COUT (feedback is disabled), the over-voltage sense mechanism is not in place to protect the input to the high-voltage current sink. In this situation the application must ensure that the voltage at HVLED1 or HVLED2 doesn't exceed 40V.

The default setting for OVP is set at 16V. For applications that require higher than 16V at the boost output, the OVP threshold must be programmed to a higher level after powerup.

CURRENT LIMIT (INDUCTIVE BOOST)

The NMOS switch current limit for the LM3533's inductive boost is set at 1A. When the current through the LM3533's NFET switch hits this over-current protection threshold (OCP), the device turns the NFET off and the inductor's energy is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switching cycle. The result is that during high-output power conditions the device can continuously run in current limit. Under these conditions the LM3533's inductive boost converter stops regulating the headroom voltage across the high-voltage current sinks. This results in a drop in the LED current.

CURRENT LIMIT (CHARGE PUMP)

The LM3533's charge pump's output current limit is set high enough so that the device will support 29.8mA (max full-scale current) in all LVLED current sinks. This would typically be (29.5mA × 5 = 149mA. For 1X gain the output current limit is typically 350mA (VIN = 3.6V). For 2X gain the current limit is typically 240mA (output referred), with a typical limit on the input current of 480mA. The typical performance characteristic curves detail the charge pump current limit vs VIN at both 1X and 2X gain settings (see Typical Performance Characteristics).

I²C-Compatible Interface

START AND STOP CONDITIONS

The LM3533 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

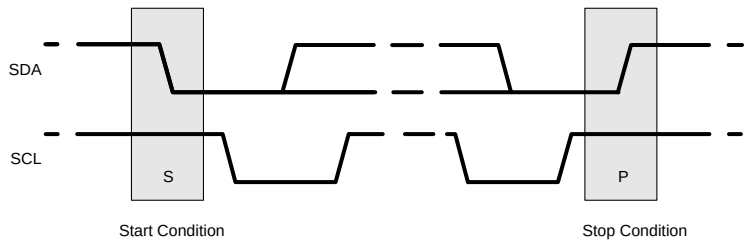


Figure 53. Start and Stop Sequences

I²C-COMPATIBLE ADDRESS

The chip address for the LM3533 is 0110110 (36h) for the -40 device and 0111000 (38h) for the -40A device. After the START condition, the I²C master sends the 7-bit chip address followed by an eighth read or write bit (R/W). R/W= 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data will be written. The third byte contains the data for the selected register.

TRANSFERRING DATA

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse. The LM3533 pulls down SDA during the 9th clock pulse signifying an acknowledge. An acknowledge is generated after each byte has been received.

Table 2 lists the available registers within the LM3533.

LM3533 Register Descriptions

Table 2. LM3533 REGISTER DEFINITIONS

Name	Address	Power On Reset
Current Sink Output Configuration 1	0x10	0x92
Current Sink Output Configuration 2	0x11	0x0F
Start Up/Shut Down Ramp Rates	0x12	0x00
Run Time Ramp Rates	0x13	0x00
Control Bank A PWM Configuration	0x14	0x38
Control Bank B PWM Configuration	0x15	0x38
Control Bank C PWM Configuration	0x16	0x38
Control Bank D PWM Configuration	0x17	0x38
Control Bank E PWM Configuration	0x18	0x38
Control Bank F PWM Configuration	0x19	0x38
Control Bank A/B Brightness Configuration	0x1A	0x00
Control Bank C Brightness Configuration	0x1B	0x00
Control Bank D Brightness Configuration	0x1C	0x00
Control Bank E Brightness Configuration	0x1D	0x00
Control Bank F Brightness Configuration	0x1E	0x00
Control Bank A Full-Scale Current	0x1F	0x13
Control Bank B Full-Scale Current	0x20	0x13
Control Bank C Full-Scale Current	0x21	0x13
Control Bank D Full-Scale Current	0x22	0x13
Control Bank E Full-Scale Current	0x23	0x13
Control Bank F Full-Scale Current	0x24	0x13
Anode Connect	0x25	0x7F
Charge Pump Control	0x26	0x00
Control Bank Enable	0x27	0x00
Pattern Generator Enable/ALS Scaling Control	0x28	0x00
ALS Pattern Scaler #1(Zones 5, 4)	0x29	0xFF
ALS Pattern Scaler #2 (Zones 3, 2)	0x2A	0xFF
ALS Pattern Scaler #3 (Zone 1)	0x2B	0xF0
OVP/Frequency/PWM Polarity	0x2C	0x08
R_ALS Select	0x30	0x00
ALS Configuration	0x31	0x20
ALS Algorithm Select	0x32	0x00

Table 2. LM3533 REGISTER DEFINITIONS (continued)

Name	Address	Power On Reset
ALS Down Delay Control	0x33	0x00
Read-Back ALS Zone	0x34	0x00
Read-Back Down Delay ALS Zone	0x35	0x00
Read-Back Up Only ALS Zone	0x36	0x00
Read-Back ADC	0x37	0x00
Read-Back Average ADC	0x38	0x00
Brightness Register A	0x40	0x00
Brightness Register B	0x41	0x00
Brightness Register C	0x42	0x00
Brightness Register D	0x43	0x00
Brightness Register E	0x44	0x00
Brightness Register F	0x45	0x00
ALS Zone Boundary 0 High	0x50	0x35
ALS Zone Boundary 0 Low	0x51	0x33
ALS Zone Boundary 1 High	0x52	0x6A
ALS Zone Boundary 1 Low	0x53	0x66
ALS Zone Boundary 2 High	0x54	0xA1
ALS Zone Boundary 2 Low	0x55	0x99
ALS Zone Boundary 3 High	0x56	0xDC
ALS Zone Boundary 3 Low	0x57	0xCC
ALS M1 Zone Target 0	0x60	0x33
ALS M1 Zone Target 1	0x61	0x66
ALS M1 Zone Target 2	0x62	0x99
ALS M1 Zone Target 3	0x63	0xCC
ALS M1 Zone Target 4	0x64	0xFF
ALS M2 Zone Target 0	0x65	0x33
ALS M2 Zone Target 1	0x66	0x66
ALS M2 Zone Target 2	0x67	0x99
ALS M2 Zone Target 3	0x68	0xCC
ALS M2 Zone Target 4	0x69	0xFF
ALS M3 Zone Target 0	0x6A	0x33
ALS M3 Zone Target 1	0x6B	0x66
ALS M3 Zone Target 2	0x6C	0x99
ALS M3 Zone Target 3	0x6D	0xCC
ALS M3 Zone Target 4	0x6E	0xFF
Pattern Generator 1 Delay	0x70	0x00
Pattern Generator 1 Low Time	0x71	0x00
Pattern Generator 1 High Time	0x72	0x00
Pattern Generator 1 Low Level Brightness	0x73	0x00
Pattern Generator 1 Rise Time	0x74	0x00
Pattern Generator 1 Fall Time	0x75	0x00
Pattern Generator 2 Delay	0x80	0x00
Pattern Generator 2 Low Time	0x81	0x00
Pattern Generator 2 High Time	0x82	0x00
Pattern Generator 2 Low Level Brightness	0x83	0x00
Pattern Generator 2 Rise Time	0x84	0x00
Pattern Generator 2 Fall Time	0x85	0x00

Table 2. LM3533 REGISTER DEFINITIONS (continued)

Name	Address	Power On Reset
Pattern Generator 3 Delay	0x90	0x00
Pattern Generator 3 Low Time	0x91	0x00
Pattern Generator 3 High Time	0x92	0x00
Pattern Generator 3 Low Level Brightness	0x93	0x00
Pattern Generator 3 Rise Time	0x94	0x00
Pattern Generator 3 Fall Time	0x95	0x00
Pattern Generator 4 Delay	0xA0	0x00
Pattern Generator 4 Low Time	0xA1	0x00
Pattern Generator 4 High Time	0xA2	0x00
Pattern Generator 4 Low Level Brightness	0xA3	0x00
Pattern Generator 4 Rise Time	0xA4	0x00
Pattern Generator 4 Fall Time	0xA5	0x00
LED Open Fault Read Back	0xB0	0x00
LED Short Fault Read Back	0xB1	0x00
LED Fault Enables	0xB2	0x00

Table 3. OUTPUT CONFIGURATION REGISTER 1 (ADDRESS 0x10)

Bit [7:6] LVLED3 Configuration	Bits [5:4] LVLED2 Configuration	Bits [3:2] LVLED1 Configuration	Bit [1] HVLED2 Configuration	Bit 0 HVLED1 Configuration
00 = LVLED3 is controlled by Control Bank C	00 = LVLED2 is controlled by Control Bank C	00 = LVLED1 is controlled by Control Bank C **(Default)**	0 = HVLED2 is controlled by Control Bank A	0 = HVLED1 is controlled by Control Bank A **(Default)**
01 = LVLED3 is controlled by Control Bank D	01 = LVLED2 is controlled by Control Bank D **(Default)**	01 = LVLED1 is controlled by Control Bank D	1 = HVLED2 is controlled by Control Bank B **(Default)**	1 = HVLED1 is controlled by Control Bank B
10 = LVLED3 is controlled by Control Bank E **(Default)**	10 = LVLED2 is controlled by Control Bank E	10 = LVLED1 is controlled by Control Bank E		
11 = LVLED3 is controlled by Control Bank F	11 = LVLED2 is controlled by Control Bank F	11 = LVLED1 is controlled by Control Bank F		

Table 4. OUTPUT CONFIGURATION REGISTER 2 (ADDRESS 0x11)

Bits [7:4] Not used	Bits [3:2] LVLED5 Configuration	Bits [1:0] LVLED4 Configuration
	00 = LVLED5 is controlled by Control Bank C	00 = LVLED4 is controlled by Control Bank C
	01 = LVLED5 is controlled by Control Bank D	01 = LVLED4 is controlled by Control Bank D
	10 = LVLED5 is controlled by Control Bank E	10 = LVLED4 is controlled by Control Bank E
	11 = LVLED5 is controlled by Control Bank F **(Default)**	11 = LVLED4 is controlled by Control Bank F **(Default)**

Table 5. LED CURRENT STARTUP/SHUTDOWN TRANSITION TIME REGISTER (ADDRESS 0x12)

Bits [7:6]	Bits [5:3] Startup Transition Time	Bits [2:0] Shutdown Transition Time
Not Used	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s Startup time is from when the device is enabled via I^2C to when the initial target current is reached.	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s Shutdown ramp time is from when the device is shutdown via I^2C until the current sink ramps to 0.

Table 6. LED CURRENT RUN-TIME TRANSITION TIME REGISTER (ADDRESS 0x13)

Bits [7:6]	Bits [5:3] Transition Time Ramp Up	Bits [2:0] Transition Time Ramp Down
Not Used	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s

Table 7. CONTROL BANK PWM CONFIGURATION REGISTERS (ADDRESS 0x14 - 0x19)

Address	Function
0x14	Control Bank A PWM Configuration Register
0x15	Control Bank B PWM Configuration Register
0x16	Control Bank C PWM Configuration Register
0x17	Control Bank D PWM Configuration Register
0x18	Control Bank E PWM Configuration Register
0x19	Control Bank F PWM Configuration Register

Table 8. CONTROL BANK PWM CONFIGURATION REGISTER BIT SETTINGS

[Bit 7:6] Not Used	Bit 5 Zone 4 PWM Enabled	Bit 4 Zone 3 PWM Enabled	Bit 3 Zone 2 PWM Enabled	Bit 2 Zone 1 PWM Enabled	Bit 1 Zone 0 PWM Enabled	Bit 0 PWM Enabled
	0 = PWM input is disabled in Zone 4	0 = PWM input is disabled in Zone 3	0 = PWM input is disabled in Zone 2	0 = PWM input is disabled in Zone 1 **(Default)**	0 = PWM input is disabled in Zone 0 **(Default)**	0 = PWM Input is disabled **(Default)**
	1 = PWM input is enabled in Zone 4 **(Default)**	1 = PWM input is enabled in Zone 3 **(Default)**	1 = PWM input is enabled in Zone 2 **(Default)**	1 = PWM input is enabled in Zone 1	1 = PWM input is enabled in Zone 0	1 = PWM Input is enabled

Table 9. CONTROL BANK A/B BRIGHTNESS CONFIGURATION REGISTER (ADDRESS 0x1A)

Bits [7:4] Not Used	Bit 3 Control Bank B Mapping Mode	Bit 2 BREGB/ALSM2 Control	Bit 1 Control Bank A Mapping Mode	Bit 0 BREGA/ALSM1 Control
	0 = Exponential Mapping **(Default)**	0 = Control Bank B is configured for Brightness Register Current Control **(Default)**	0 = Exponential Mapping **(Default)**	0 = Control Bank A is configured for Brightness Register Current Control **(Default)**
	1 = Linear Mapping	1 = Control Bank B is configured for ALS current control via the ALSM2 Zone Target Registers	1 = Linear Mapping	1 = Control Bank A is configured for ALS current control via the ALSM1 Zone Target Registers

Table 10. LOW-VOLTAGE CONTROL BANK BRIGHTNESS CONFIGURATION REGISTERS (ADDRESS 0X1B, 0X1C, 0X1D, 0X1E)

Address	Function
0x1B	Control Bank C Brightness Configuration Register
0x1C	Control Bank D Brightness Configuration Register
0x1D	Control Bank E Brightness Configuration Register
0x1E	Control Bank F Brightness Configuration Register

Table 11. LOW-VOLTAGE CONTROL BANK BRIGHTNESS CONFIGURATION REGISTER BIT SETTINGS

Bits [7:4] Not Used	Bit 3 Pattern Generator Enable	Bit 2 Mapping Mode	Bits [1:0] Current Control
	0 = Pattern Generator is disabled for Control Bank_ **(Default)**	0 = Exponential Mapping **(Default)**	0X = Control Bank_ is configured for Brightness Register Current Control via the respective Brightness Register **(Default)**
	1 = Pattern Generator is enabled for Control Bank_	1 = Linear Mapping	10 = Control Bank_ is configured for ALS current control via the ALSM2 Zone Target Registers
			11 = Control Bank_ is configured for ALS current control via the ALSM3 Zone Target Registers

Table 12. CONTROL BANK FULL-SCALE CURRENT REGISTERS (ADDRESS 0x1F, 0x20, 0x21, 0x22, 0x23, 0x24)

Address	Function
0x1F	Control Bank A Full-Scale Current Register
0x20	Control Bank B Full-Scale Current Register
0x21	Control Bank C Full-Scale Current Register
0x22	Control Bank D Full-Scale Current Register
0x23	Control Bank E Full-Scale Current Register
0x24	Control Bank F Full-Scale Current Register

Table 13. CONTROL BANK FULL-SCALE CURRENT REGISTER BIT SETTINGS

Bits [7:5] Not Used	Bits [4:0] Control A Full-Scale Current Select Bits
N/A	00000 = 5mA
	:
	:
	10011 = 20.2mA **(Default)**
	:
	:
	11111 = 29.8mA The full-scale Current vs code is given by the following equation: ILED FULLSCALE = 5 mA + Code x 0.8 mA (7)

Table 14. ANODE CONNECT REGISTER (ADDRESS 0x25)

Bits [7] Not Used	Bit 6 LVLED5 Anode Connect	Bit 5 LVLED4 Anode Connec	Bit 4 LVLED3 Anode Connect	Bit 3 LVLED2 Anode Connect	Bit 2 LVLED1 Anode Connect	Bit 1 HVLED2 Anode Connect	Bit 0 HVLED1 Anode Connect
	0 = LVLED5 LED anode is not connected to CPOUT	0 = LVLED4 LED anode is not connected to CPOUT	0 = LVLED3 LED anode is not connected to CPOUT	0 = LVLED2 LED anode is not connected to CPOUT	0 = LVLED1 LED anode is not connected to CPOUT	0 = HVLED2 LED string anode is not connected to COUT	0 = HVLED1 LED string anode is not connected to COUT
	1 = LVLED5 LED anode is connected to CPOUT **(Default)**	1 = LVLED4 LED anode is connected to CPOUT **(Default)**	1 = LVLED3 LED anode is connected to CPOUT **(Default)**	1 = LVLED2 LED anode is connected to CPOUT **(Default)**	1 = LVLED1 LED anode is connected to CPOUT **(Default)**	1 = HVLED2 LED string anode is connected to COUT **(Default)**	1 = HVLED1 LED string anode is connected to COUT **(Default)**

Table 15. CHARGE PUMP CONTROL REGISTER (ADDRESS 0x26)

Bits [7:3] Not Used	Bits [2:1] Gain Select	Bit 0 Charge Pump Disable
N/A	0X = Automatic gain select **(Default)** 10 = Gain set at 1x 11 = Gain set at 2x	0 = Charge pump enabled **(Default)** 1 = Charge pump disabled; charge pump is high impedance from IN to CPOUT.

Table 16. CONTROL BANK ENABLE REGISTER (ADDRESS 0x27)

Bits [7:6] Not Used	Bit 5 Control F Enable	Bit 4 Control E Enable	Bit 3 Control D Enable	Bit 2 Control C Enable	Bit 1 Control B Enable	Bit 0 Control A Enable
	0 = Control Bank F is disabled **(Default)**	0 = Control Bank E is disabled **(Default)**	0 = Control Bank D is disabled **(Default)**	0 = Control Bank C is disabled **(Default)**	0 = Control Bank B is disabled **(Default)**	0 = Control Bank A is disabled **(Default)**
	1 = Control Bank F is enabled	1 = Control Bank E is enabled	1 = Control Bank D is enabled	1 = Control Bank C is enabled	1 = Control Bank B is enabled	1 = Control Bank A is enabled

Table 17. PATTERN GENERATOR ENABLE/ALS SCALING CONTROL (ADDRESS 0X28)

Bit 7 Pattern 4 ALS Scaling Enable	Bit 6 Pattern 4 Enable	Bit 5 Pattern 3 ALS Scaling Enable	Bit 4 Pattern 3 Enable	Bit 3 Pattern 2 ALS Scaling Enable	Bit 2 Pattern 2 Enable	Bit 1 Pattern 1 ALS Scaling Enable	Bit 0 Pattern 1 Enable
0 = Pattern 4 Scaling Disabled **(Default)**	0 = Pattern 4 Disabled **(Default)**	0 = Pattern 3 Scaling Disabled **(Default)**	0 = Pattern 3 Disabled **(Default)**	0 = Pattern 2 Scaling Disabled **(Default)**	0 = Pattern 2 Disabled **(Default)**	0 = Pattern 1 Scaling Disabled **(Default)**	0 = Pattern 1 Disabled **(Default)**
1 = Pattern 4 Scaling Enabled	1 = Pattern 4 Enabled	1 = Pattern 3 Scaling Enabled	1 = Pattern 3 Enabled	1 = Pattern 2 Scaling Enabled	1 = Pattern 2 Enabled	1 = Pattern 1 Scaling Enabled	1 = Pattern 1 Enabled

Note: If a low-voltage control bank is set to receive its brightness information from either ALSM2 or ALSM3, and then a pattern generator is enabled for that Control Bank, the Control Bank will ignore the ALSM2 or ALSM3 zone target information. This prevents conflicts from ALSM2/ALSM3 zone targets and ALS controlled pattern currents.

Table 18. ALS ZONE PATTERN SCALER #1 (ADDRESS 0x29)

Bits [7:4] ALS Pattern Scaler (Zone 4)	Bits [3:0] ALS Pattern Scaler (Zone 3)
0000 = 1/16	0000 = 1/16
0001 = 2/16	0001 = 2/16
:	:
1111 = 16/16 **(Default)**	1111 = 16/16 **(Default)**

Table 19. ALS ZONE PATTERN SCALER #2 (ADDRESS 0x2A)

Bits [7:4] ALS Pattern Scaler (Zone 2)	Bits [3:0] ALS Pattern Scaler (Zone 1)
0000 = 1/16	0000 = 1/16
0001 = 2/16	0001 = 2/16
:	:
1111 = 16/16 **(Default)**	1111 = 16/16h **(Default)**

Table 20. ALS ZONE PATTERN SCALER #3 (ADDRESS 0x2B)

Bits [7:4] Not Used	Bits [3:0] ALS Pattern Scaler (Zone 0)
	0000 = 1/16 **(Default)**
	0001 = 2/16

Table 20. ALS ZONE PATTERN SCALER #3 (ADDRESS 0x2B) (continued)

Bits [7:4] Not Used	Bits [3:0] ALS Pattern Scaler (Zone 0)
	:
	1111 = 16/16

Table 21. OVP/BOOST FREQUENCY/PWM POLARITY SELECT (ADDRESS 0x2C)

Bits [7:4] Not Used	Bit 3 PWM Polarity	Bit [2:1] Boost OVP Select	Bit 1 Boost Frequency Select
	0 = Active Low Polarity 1 = Active High Polarity **(Default)**	00 = 16V **(Default)** 01 = 24V 10 = 32V 11 = 40V	0 = 500 kHz **(Default)** 1 = 1MHz

Table 22. R_ALS SELECT REGISTER (ADDRESS 0x30)

Bit 7 Not Used	Bits [6:0] ALS Resistor Select Code
	0000000 = ALS input is high impedance **(Default)**
	0000001 = 200kΩ (10µA at 2V full-scale)
	0000010 = 100kΩ (20µA at 2V full-scale)
	:
	:
	:
	1111110 = 1.587kΩ (1.26mA at 2V full-scale)
	1111111 = 1.575kΩ (1.27mA at 2V full-scale)

The selectable codes are available which give a linear step in currents of 10uA per code based upon 2V/R_ALS. This gives a code to resistance relationship of:

$$R_{ALS} = \frac{2V}{10\ \mu A\ x\ Code(D)} \quad (8)$$

Table 23. ALS CONFIGURATION REGISTER (ADDRESS 0x31)

Bit [7:6] Not Used	Bits [5:3] ALS Average Times	Bit 2 Fast startup Enable/Disable	Bit 1 ALS Input Mode	Bit 0 ALS Enable/Disable
	000 = 17.92 ms 001 = 35.84ms 010 = 71.68ms 011 = 143.36ms 100 = 286.72ms **(Default)** 101 = 573.44ms 110 = 1146.88ms 111 = 2293.76ms	0 = ALS fast startup is enabled **(Default)** 1 = ALS fast startup is disabled	0 = ALS is set for Analog Sensor Input Mode **(Default)** 1 = ALS is set for PWM Sensor Input Mode	0 = ALS is disabled **(Default)** 1 = ALS is enabled

Table 24. ALS ALGORITHM SELECT REGISTER (ADDRESS 0X32)

Bits [7:6] ALS Pattern Generator Zone Algorithm Select	Bits [5:4] ALSM3 zone Algorithm Select	Bits [3:2] ALSM2 zone Algorithm Select	Bits [1:0] ALSM1 zone Algorithm Select
00 = Direct Control **(Default)**	00 = Direct Control **(Default)**	00 = Direct Control **(Default)**(Default)	00 = Direct Control (default)
01 = Up Only Control	01 = Up Only Control	01 = Up Only	01 = Up Only
1X = Down Delay Control	1X = Down Delay Control	1X = Down Delay	1X = Down Delay

Table 25. ALS DOWN DELAY CONTROL REGISTER (ADDRESS 0x33)

Bits [7:4] Not Used	Bits [4:0] Down Delay Settings (# Indicates total average periods required to force a change in the down direction)
	00000 = 6 **(Default)**
	:
	:
	:
	11111 = 37

Table 26. ALS ZONE INFORMATION REGISTER (ADDRESS 0x34)

Bits [7:5] Not Used	Bits [4:2] Average Zone Information Bits	Bit 1 Zone Change Bit	Bit 0 Interrupt Enable Bit
	000 = Zone 0 **(Default)** 001 = Zone 1 010 = Zone 2 011 = Zone 3 1XX = Zone 4	0 = no change in the ALS zone since the last read back of this register **(Default)** 1 = the ALS zone has changed. A read back of this	0 = INT Mode Disabled **(Default)** 1 = INT Mode Enabled

Table 27. READ-BACK ADC REGISTER (ADDRESS 0x37)

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Data	Data	Data	Data	Data	Data	Data	Data

This register contains the ADC data from the internal 8-bit ADC. This is a read-only register. When the ALS Interface is enabled this register is updated with the digitized ALS information every 140µs.

Table 28. READ-AVERAGE ADC REGISTER (ADDRESS 0x38)

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Data	Data	Data	Data	Data	Data	Data	Data

This register is updated after each average period.

Table 29. BRIGHTNESS REGISTERS (ADDRESSES 0x40, 0x41, 0x42, 0x43, 0x44, 0x45)

Address	Function
0x40	Control Bank A Brightness Register (BREGA)
0x41	Control Bank B Brightness Register (BREGB)
0x42	Control Bank C High Brightness Register (BREGHC)
0x43	Control Bank D High Brightness Register (BREGHD)
0x44	Control Bank E High Brightness Register (BREGHE)
0x45	Control Bank F High Brightness Register (BREGHF)

Table 30. BRIGHTNESS REGISTERS BIT DESCRIPTION

Brightness Code Bits[7:0}
When the Mapping Mode is set for exponential mapping (Control Bank_Brightness Configuration Register Bit [2] = 0), the current approximates the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]} \quad (9)$$

Table 30. BRIGHTNESS REGISTERS BIT DESCRIPTION (continued)

Brightness Code Bits[7:0}
When the Mapping Mode is set for linear mapping (Control Bank_Brightness Configuration Register Bit [2] = 1), the current approximates the equation: $$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \quad (10)$$

Table 31. ALS ZONE BOUNDARY HIGH AND LOW REGISTERS (ADDRESS 0x50 - 0x57)

Address	Function
0x50	ALS Zone Boundary 0 High
0x51	ALS Zone Boundary 0 Low
0x52	ALS Zone Boundary 1 High
0x53	ALS Zone Boundary 1 Low
0x54	ALS Zone Boundary 2 High
0x55	ALS Zone Boundary 2 Low
0x56	ALS Zone Boundary 3 High
0x57	ALS Zone Boundary 3 Low

Note: Each Zone Boundary register is 8 bits with a maximum voltage of 2V. This gives a step size for each Zone Boundary Register bit of:

$$ZoneBoundaryLSB = \frac{2V}{255} = 7.8\ mV \quad (11)$$

Table 32. ALSM1 ZONE TARGET REGISTERS (ADDRESS 0x60 - 0x64)

Address	Function
0x60	ALSM1 Zone Target 0
0x61	ALSM1 Zone Target 1
0x62	ALSM1 Zone Target 2
0x63	ALSM1 Zone Target 3
0x64	ALSM1 Zone Target 4

Table 33. ALSM2 ZONE TARGET REGISTERS (ADDRESS 0x65 - 0x69)

Address	Function
0x65	ALSM2 Zone Target 0
0x66	ALSM2 Zone Target 1
0x67	ALSM2 Zone Target 2
0x68	ALSM2 Zone Target 3
0x69	ALSM2 Zone Target 4

Table 34. ALSM3 ZONE TARGET REGISTERS (ADDRESS 0x6A - 0x6E)

Address	Function
0x6A	ALSM3 Zone Target 0
0x6B	ALSM3 Zone Target 1
0x6C	ALSM3 Zone Target 2
0x6D	ALSM3 Zone Target 3
0x6E	ALSM3 Zone Target 4

When the Mapping Mode is set for exponential mapping (Control Bank_Brightness Configuration Register Bit [2] = 0), the current approximates the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]} \quad (12)$$

When the Mapping Mode is set for linear mapping (Control Bank_Brightness Configuration Register Bit [2] = 1), the current approximates the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \quad (13)$$

PATTERN GENERATOR REGISTERS

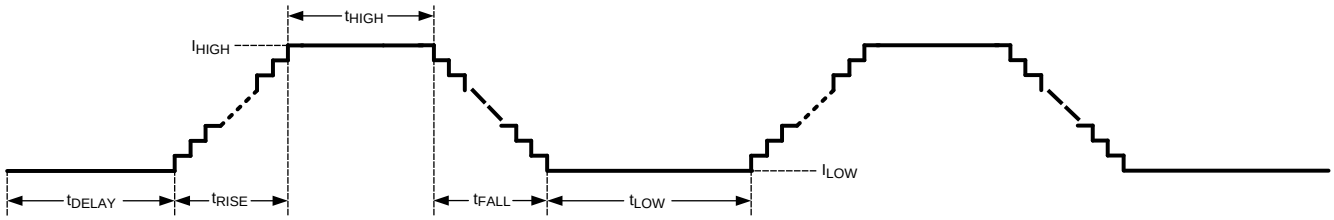


Figure 54. Pattern Generator Timing

Table 35. PATTERN GENERATOR DELAY REGISTERS (ADDRESS 0x70, 0x80, 0x90, 0xA0)

Address	Function
0x70	Pattern Generator 1 Delay Register
0x80	Pattern Generator 2 Delay Register
0x90	Pattern Generator 3 Delay Register
0xA0	Pattern Generator 4 Delay Register

Table 36. PATTERN GENERATOR DELAY REGISTER BIT DESCRIPTION

Bit 7 Not Used	Bit [6:0] t_{DELAY} times
	0x00 = 16.384ms (16.384ms/step) **(Default)**
	0x01 = 32.768ms
	:
	:
	0x3B = 983.05ms
	0x3C = 999.424ms
	0x3D = 1130.496ms (131.072ms/step)
	0x3E = 1261.568ms
	:
	:
	0x7F = 9781.248ms

Table 37. PATTERN GENERATOR LOW-TIME REGISTERS (ADDRESS 0x71, 0x81, 0x91, 0xA1)

Address	Function
0x71	Pattern Generator 1 Low-Time Register
0x81	Pattern Generator 2 Low-Time Register
0x91	Pattern Generator 3 Low-Time Register
0xA1	Pattern Generator 4 Low-Time Register

Table 38. PATTERN GENERATOR LOW-TIME REGISTER BIT DESCRIPTION

Bit [7:0]
t_{LOW} times
0x00 = 16.384ms (16.384ms/step) **(Default)**
0x01 = 32.768ms
:
:
0x3B = 983.05ms
0x3C = 999.424ms
0x3D = 1130.496ms (131.072ms/step)
0x3E = 1261.568ms
:
:
0x7F = 9781.248ms
0x80 = 10.305536s (524.288ms/step)
:
:
0xFF = 76.890112s

Table 39. PATTERN GENERATOR HIGH-TIME REGISTERS (ADDRESS 0x72, 0x82, 0x92, 0xA2)

Address	Function
0x72	Pattern Generator 1 High-Time Register
0x82	Pattern Generator 2 High-Time Register
0x92	Pattern Generator 3 High-Time Register
0xA2	Pattern Generator 4 High-Time Register

Table 40. PATTERN GENERATOR HIGH-TIME REGISTER BIT DESCRIPTION

Bit 7 Not Used	Bit [6:0] t_{HIGH} times
	0x00 = 16.384ms (16.384ms/step) **(Default)**
	0x01 = 32.768ms
	:
	:
	0x3B = 983.05ms
	0x3C = 999.424ms
	0x3D = 1130.496ms (131.072ms/step)
	0x3E = 1261.568ms
	:
	:
	0x7F = 9781.248ms

Table 41. PATTERN GENERATOR LOW-LEVEL BRIGHTNESS REGISTERS (ADDRESS 0x73, 0x83, 0x93, 0xA3)

Address	Function
0x73	Pattern Generator 1 Low-Level Brightness Register (BREGCL)
0x83	Pattern Generator 2 Low-Level Brightness Register (BREGDL)
0x93	Pattern Generator 3 Low-Level Brightness Register (BREGEL)
0xA3	Pattern Generator 4 Low-Level Brightness Register (BREGFL)

For Exponential Mapping Mode the low-level current becomes:

$$I_{LED\_LOW\_LEVEL} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]} \quad (14)$$

For Linear Mapping Mode the low-level current becomes:

$$I_{LED\_LOW\_LEVEL} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \quad (15)$$

Note: The Pattern Generator high level brightness setting is set through the Control Bank Brightness Registers (see Table 29).

Table 42. PATTERN GENERATOR RISE-TIME REGISTERS (ADDRESS 0x74, 0x84, 0x94, 0xA4)

Address	Function
0x74	Pattern Generator 1 Rise-Time Register
0x84	Pattern Generator 2 Rise-Time Register
0x94	Pattern Generator 3 Rise-Time Register
0xA4	Pattern Generator 4 Rise-TimeRegister

Table 43. PATTERN GENERATOR RISE-TIME REGISTER BIT SETTINGS

Bits [7:3] Not Used	Bits [2:0] t_{RISE} (from I_{LOW} to I_{HIGH})
	000 = 2048µs **(Default)**
	001 = 262ms
	010 = 524ms
	011 = 1.049s
	100 = 2.097s
	101 = 4.194s
	110 = 8.389s
	111 = 16.78s

Table 44. PATTERN GENERATOR FALL-TIME REGISTERS (ADDRESS 0x75, 0x85, 0x95, 0xA5)

Address	Function
0x75	Pattern Generator 1 Fall-Time Register
0x85	Pattern Generator 2 Fall-Time Register
0x95	Pattern Generator 3 Fall-Time Register
0xA5	Pattern Generator 4 Fall-Time Register

Table 45. PATTERN GENERATOR FALL-TIME REGISTER BIT SETTINGS

Bits [7:3] Not Used	Bits [2:0] t_{FALL} (from I_{HIGH} to I_{LOW})
	000 = 2048µs **(Default)**
	001 = 262ms
	010 = 524ms
	011 = 1.049s
	100 = 2.097s
	101 = 4.194s
	110 = 8.389s
	111 = 16.78s

Table 46. LED STRING OPEN FAULT READBACK REGISTER (ADDRESS 0xB0)

Bit 7 (Not Used)	Bit 6 (LVLED5 Open)	Bit 5 (LVLED4 Open)	Bit 4 (LVLED3 Open)	Bit 3 (LVLED2 Open)	Bit 2 (LVLED1 Open)	Bit 1 (HVLED2 Open)	Bit 0 (HVLED1 Open)
	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open

Table 47. LED STRING SHORT FAULT READBACK REGISTER (ADDRESS 0xB1)

Bit 7 (Not Used)	Bit 6 (LVLED5 Short)	Bit 5 (LVLED4 Short)	Bit 4 (LVLED3 Short)	Bit 3 (LVLED2 Short)	Bit 2 (LVLED1 Short)	Bit 1 (HVLED2 Short)	Bit 0 (HVLED1 Short)
	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short

Table 48. LED FAULT ENABLE (ADDRESS 0xB2)

Bits [7:2] Not Used	Bits [1] LED Short Fault Enable	Bit 0 LED Open Fault Enable
N/A	0 = Short Faults Disabled **(Default)** 1 = Short Faults Enabled	0 = Open Faults Disabled **(Default)** 1 = Open Faults Enabled

APPLICATIONS INFORMATION

BOOST CONVERTER MAXIMUM OUTPUT POWER (BOOST)

The LM3533's maximum output power is governed by two factors: the peak current limit (I_{CL} = 880mA min), and the maximum output voltage (V_{OVP}). When the application causes either of these limits to be reached it is possible that the proper current regulation and matching between LED current strings will not be met.

PEAK CURRENT LIMITED

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3533's current limit, the NFET switch turns off for the remainder of the switching period. If this happens each switching cycle the LM3533 will regulate the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the boost output connected current sinks, and the LED current dropping below its programmed level.

The peak current in a boost converter is dependent on the value of the inductor, total LED current in the boost (IOUT), the boost output voltage (VOUT) (which is the highest voltage LED string + 0.4V regulated headroom voltage), the input voltage (VIN), the switching frequency, and the efficiency (Output Power/Input Power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM), or discontinuous (DCM) where it goes to 0 before the switching period ends. For Continuous Conduction Mode the peak inductor current is given by:

$$IPEAK = \frac{IOUT \times VOUT}{VIN \times efficiency} + \left[\frac{VIN}{2 \times f_{SW} \times L} \times \left(1 - \frac{VIN \times efficiency}{VOUT}\right)\right] \quad (16)$$

For Discontinuous Conduction Mode the peak inductor current is given by:

$$I_{PEAK} = \sqrt{\frac{2 \times I_{OUT}}{f_{SW} \times L \times efficiency} \times \left(V_{OUT} - V_{IN} \times efficiency\right)} \quad (17)$$

To determine which mode the circuit is operating in (CCM or DCM) it is necessary to perform a calculation to test whether the inductor current ripple is less than the anticipated input current (I_{IN}). If ΔI_L is less than I_{IN} then the device will be operating in CCM. If ΔI_L is greater than I_{IN} then the device is operating in DCM.

$$\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times efficiency} > \frac{V_{IN}}{f_{SW} \times L} \times \left(1 - \frac{V_{IN} \times efficiency}{V_{OUT}}\right) \quad (18)$$

Typically at currents high enough to reach the LM3533's peak current limit, the device will be operating in CCM. When choosing the switching frequency and the inductor value, Equation 16 and Equation 17 should be used to ensure that I_{PEAK} stays below I_{CL_MIN} (see Electrical Characteristics).

OUTPUT VOLTAGE LIMITED

In the case of a output voltage limited situation, when the boost output voltage hits the LM3533's OVP threshold, the NFET turns off and stays off until the output voltage falls below the hysteresis level (typically 1V below the OVP threshold). This results in the boost converter regulating the output voltage to the programmed OVP threshold (16V, 24V, 32V, or 40V), causing the current sinks to go into dropout. The default OVP threshold is set at 16V. For LED strings higher than typically 4 series LEDs, the OVP will have to be programmed higher after power-up or after a HWEN reset.

MAXIMUM OUTPUT POWER (CHARGE PUMP)

The maximum output power available from the LM3533's charge pump is determined by the maximum output voltage available from the charge pump. In 1X gain the charge pump operates in Pass Mode so that the voltage at CPOUT tracks VIN (less the drop across the charge pumps pass switch). In this case the maximum output power is given as:

$$P_{OUT\_MAX} = I_{LVLED\_TOTAL} \times (V_{IN} - I_{LVLED\_TOTAL} \times R_{CP}) \quad (19)$$

where R_{CP} is the resistance from IN to CPOUT and I_{LVLED_TOTAL} is the maximum programmed current in the LVLED strings.

In 2X gain the voltage at CPOUT (V_{CPOUT_2X}) is regulated to typically 4.4V. In this case the maximum output power is given by:

$$P_{OUT\_MAX} = I_{LVLED\_TOTAL} \times V_{CPOUT\_2X} \quad (20)$$

Both equations assume there is sufficient headroom at the top side of the low-voltage current sinks to ensure the LED current remains in regulation (V_{HR_LV}) in the Electrical Characteristics.

LAYOUT GUIDELINES AND COMPONENT SELECTION (BOOST)

The LM3533 inductive boost converter sees a high switched voltage (up to 40V) at the SW pin, and a step current (up to 1A) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OVP pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 55 highlights these two noise-generating components.

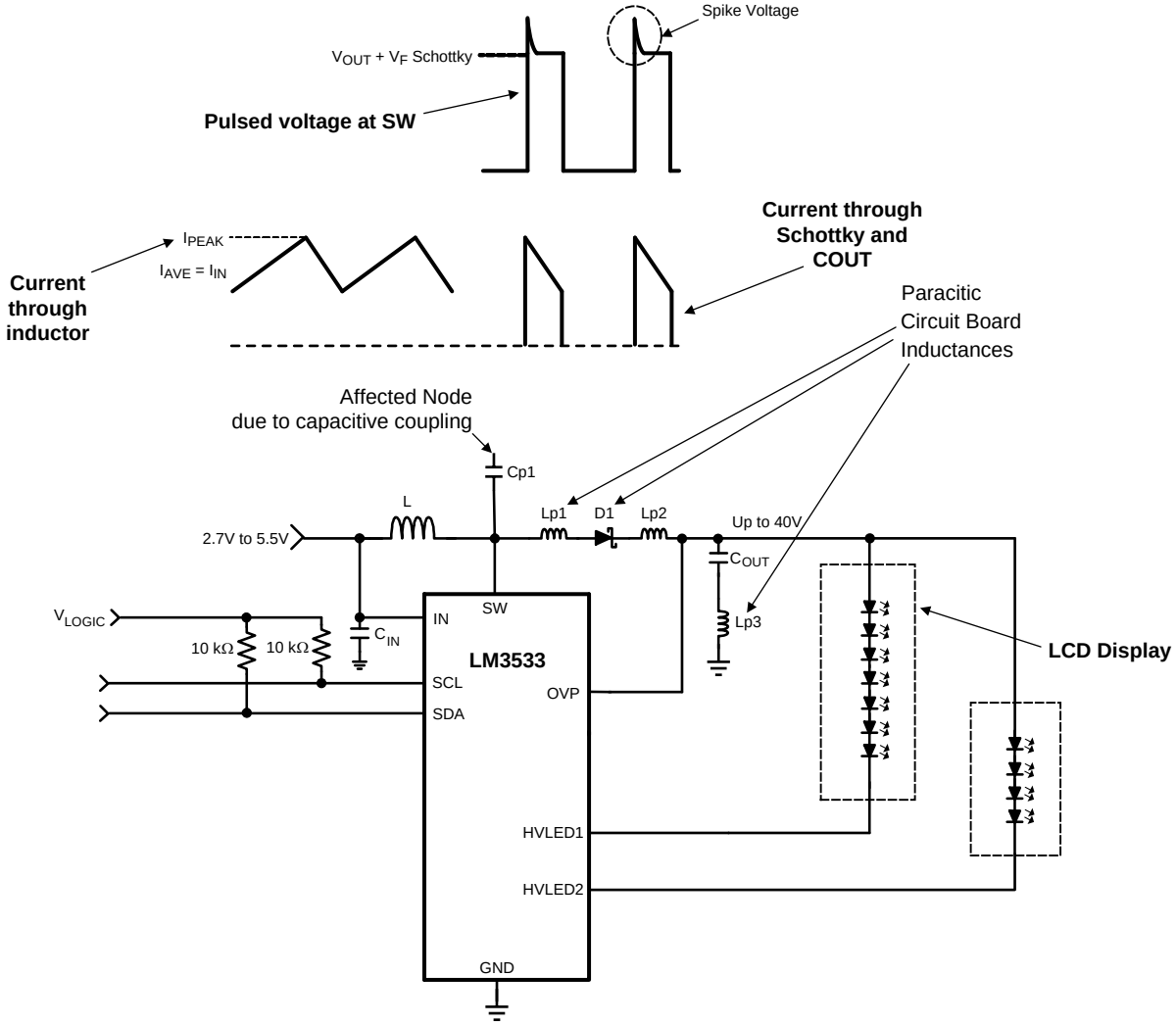


Figure 55. LM3533's Inductive Boost Converter Showing Pulsed Voltage at SW (High dV/dt) and Current Through Schottky and COUT (High dI/dt)

The following list details the main (layout sensitive) areas of the LM3533's inductive boost converter in order of decreasing importance:

1. **Output Capacitor**
   - Schottky Cathode to COUT+
   - COUT− to GND
2. **Schottky Diode**
   - SW Pin to Schottky Anode
   - Schottky Cathode to COUT+
3. **Inductor**
   - SW Node PCB capacitance to other traces
4. **Input Capacitor**
   - CIN+ to IN pin

Boost Output Capacitor Selection and Placement

The LM3533's inductive boost converter requires a 1µF output capacitor. The voltage rating of the capacitor depends on the selected OVP setting. For the 16V setting a 16V capacitor must be used. For the 24V setting a 25V capacitor must be used. For the 32V setting, a 35V capacitor must be used. For the 40V setting a 50V capacitor must be used. Pay careful attention to the capacitor's tolerance and DC bias response. For proper operation the degradation in capacitance due to tolerance, DC bias, and temperature, should stay above 0.4µF. This might require placing two devices in parallel in order to maintain the required output capacitance over the device operating range, and series LED configuration.

Because the output capacitor is in the path of the inductor current discharge path it will see a high-current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through COUT and back into the LM3533's GND pin will contribute to voltage spikes (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. These spikes can potentially over-voltage the SW pin, or feed through to GND. To avoid this, COUT+ must be connected as close as possible to the Cathode of the Schottky diode, and COUT− must be connected as close as possible to the LM3533's GND bump. The best placement for COUT is on the same layer as the LM3533 so as to avoid any vias that can add excessive series inductance.

Schottky Diode Placement

The Schottky diode must have a reverse breakdown voltage greater than the LM3533's maximum output voltage (see OVER-VOLTAGE PROTECTION (INDUCTIVE BOOST) section). Additionally, the diode must have an average current rating high enough to handle the LM3533's maximum output current, and at the same time the diode's peak current rating must be high enough to handle the peak inductor current. Schottky diodes are required due to their lower forward voltage drop (0.3V to 0.5V) and their fast recovery time.

In the LM3533's boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode will cause a voltage spike (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to VOUT and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to COUT+ will reduce the inductance (LP_) and minimize these voltage spikes.

Inductor Placement

The node where the inductor connects to the LM3533's SW bump has 2 issues. First, a large switched voltage (0 to VOUT + VF_SCHOTTKY) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range.

To reduce the capacitive coupling of the signal on SW into nearby traces, the SW bump-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high-impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as SCL, SDA, HWEN, PWM, and possibly ALS. A GND plane placed directly below SW will dramatically reduce the capacitance from SW into nearby traces.

Lastly, limit the trace resistance of the VBATT-to-inductor connection and from the inductor-to-SW connection, by use of short, wide traces.

Boost Input Capacitor Selection and Placement

The input capacitor on the LM3533 filters the voltage ripple due to the switching action of the inductive boost and the capacitive charge pump doubler. A ceramic capacitor of at least 2.2µF must be used.

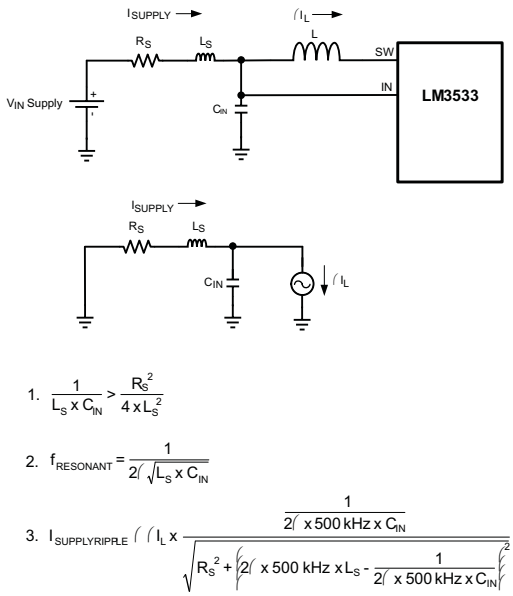
For the LM3533's boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turn on of the internal power switch. The driver current requirement can range from 50mA at 2.7V to over 200mA at 5.5V with fast durations of approximately 10ns to 20ns. This will appear as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical since any series inductance between IN and CIN+ or CIN− and GND can create voltage spikes that could appear on the VIN supply line and in the GND plane.

Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM3533, form a series RLC circuit. If the output resistance from the source (RS) is low enough the circuit will be underdamped and will have a resonant frequency (typically the case). Depending on the size of LS the resonant frequency could occur below, close to, or above the LM3533's switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM3533's switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; or
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency. Figure 56 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor.

The circuit is redrawn for the AC case where the VIN supply is replaced with a short to GND and the LM3533 + Inductor is replaced with a current source (ΔIL). Equation 1 is the criteria for an underdamped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of LS, RS, and CIN.

As an example, consider a 3.6V supply with 0.1Ω of series resistance connected to C_{IN} through 50nH of connecting traces. This results in an under-damped input-filter circuit with a resonant frequency of 712kHz. Since both the 1MHz and 500kHz switching frequency options lie close to the resonant frequency of the input filter, the supply current ripple is probably larger than the inductor current ripple. In this case, using equation 3, the supply current ripple can be approximated as 1.68 times the inductor current ripple (using a 500kHz switching frequency) and 0.86 times the inductor current ripple using a 1MHz switching frequency. Increasing the series inductance (LS) to 500nH causes the resonant frequency to move to around 225kHz, and the supply current ripple to be approximately 0.25 times the inductor current ripple (500kHz switching frequency) and 0.053 times for a 1MHz switching frequency.



1. $\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$

2. $f_{RESONANT} = \frac{1}{2\pi\sqrt{L_S \times C_{IN}}}$

3. $I_{SUPPLYRIPPLE} \approx I_L \times \frac{\frac{1}{2\pi \times 500\,kHz \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times 500\,kHz \times L_S - \frac{1}{2\pi \times 500\,kHz \times C_{IN}}\right)^2}}$

Figure 56. Input RLC Network

LAYOUT GUIDELINES (CHARGE PUMP)

The charge pump basically has three areas of concern regarding component placement:

1. The flying capacitor (CP)
2. The output capacitor (CPOUT)
3. The input capacitor

Flying Capacitor (CP)

The charge pump flying capacitor must quickly charge up to the input voltage and then supply the current to the output every switching cycle. Since the charge pump switching frequency is 1MHz, the capacitor must be a low-inductance and low-resistive ceramic. Additionally, there must be a low-inductive connection from CP to the LM3533's flying capacitor terminals C+ and C−. This is accomplished by placing CP as close as possible to the LM3533 and on the same layer to avoid vias.

Output Capacitor (CPOUT)

The charge pump output capacitor sees the switched charge from the flying capacitor every switching cycle (1MHz). This fast switching action requires that a low inductive and low resistive capacitor (ceramic) be used and that CPOUT be connected to the LM3533's CPOUT terminal with a low inductive connection. This is done by placing CPOUT as close as possible to the CPOUT and GND terminals of the LM3533 and on the same layer as the LM3533 to avoid vias.

Charge Pump Input Capacitor Placement

The input capacitor for the LM3533's charge pump is the same one used for the LM3533's inductive boost converter (see Boost Input Capacitor Selection and Placement section).

LM3533 Example Layout

Figure 57 details an example layout for the LM3533.

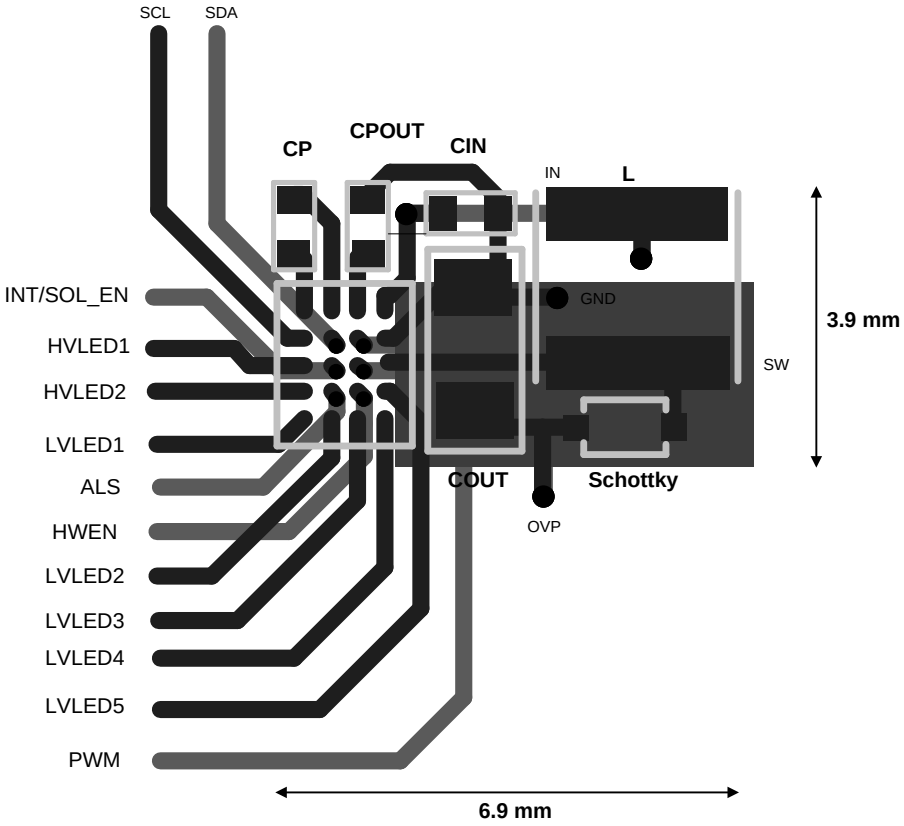


Figure 57. LM3533 Example Layout

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	55

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3533TME-40/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D72B	Samples
LM3533TME-40A/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D74B	Samples
LM3533TMX-40/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D72B	Samples
LM3533TMX-40A/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D74B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

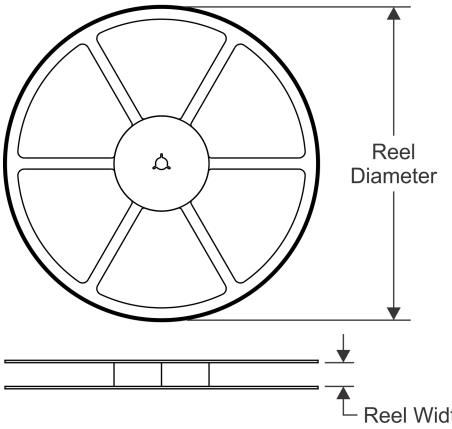
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

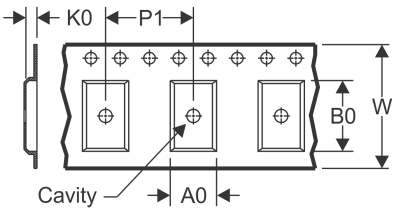
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

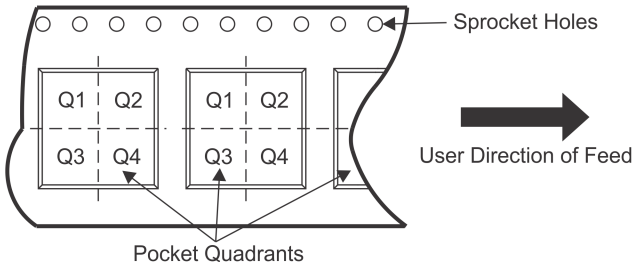


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

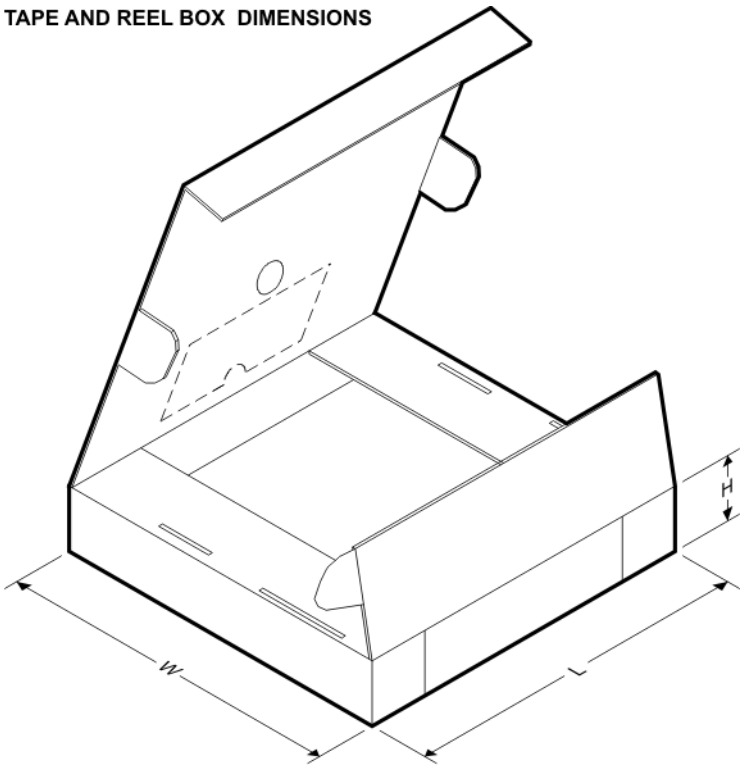
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3533TME-40/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
LM3533TME-40A/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
LM3533TMX-40/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1
LM3533TMX-40A/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.89	2.2	0.69	4.0	8.0	Q1

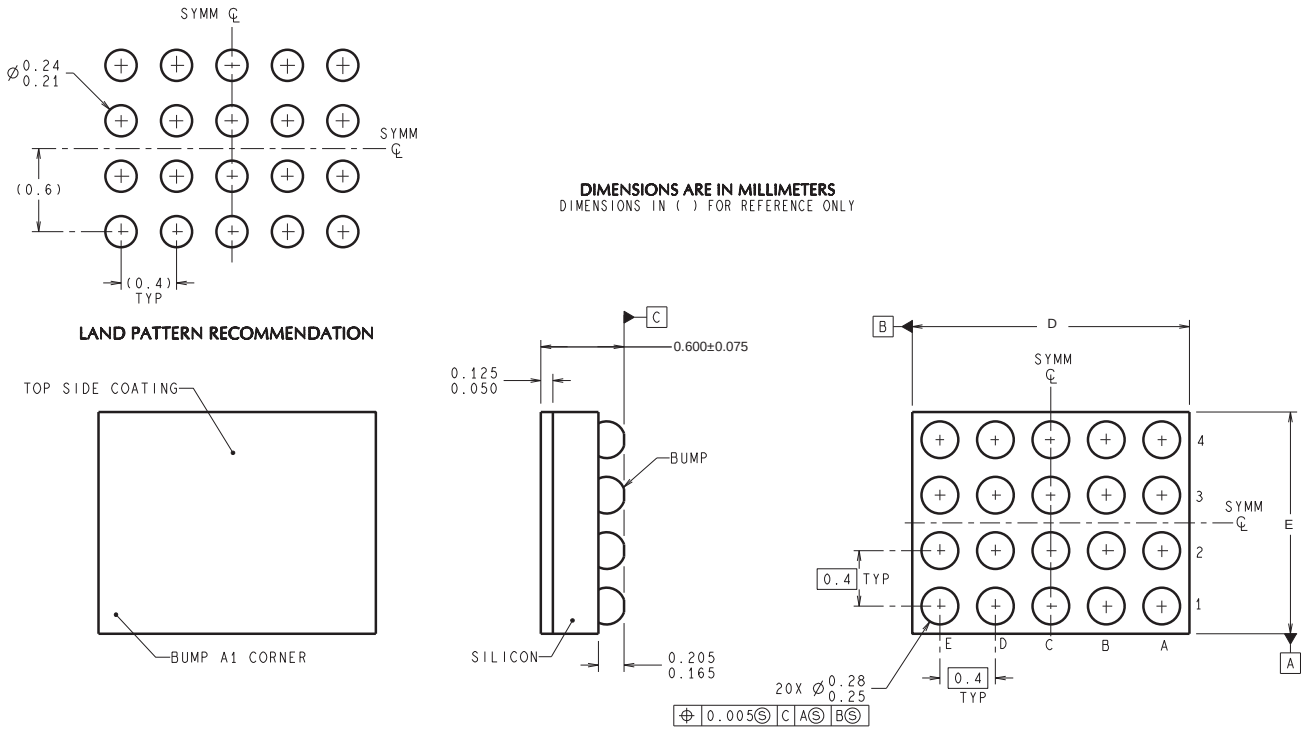
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3533TME-40/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0
LM3533TME-40A/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0
LM3533TMX-40/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0
LM3533TMX-40A/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0

YFQ0020



D: Max = 2.04 mm, Min = 1.98 mm

E: Max = 1.78 mm, Min = 1.72 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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