LM3550 5A Flash LED Driver with Automatic V_{LED} and ESR Detection for Mobile Camera Systems

Check for Samples: LM3550

FEATURES

- **Up to 5A Flash Current**
- **4 Selectable Super-Capacitor Charge Voltage Levels (4.5V, 5.0V, 5.3V, Optimized)**
- **Flash Optimized Charge Mode for Optimal Efficiency**
  - **33% Faster Charge Time Using Optimal Mode**
  - **49% Less Power Dissipated in Current Source using Optimal Charge Mode**
- **Fast Super-Capacitor Charger with 500 mA Input Current Limit**
- **Adjustable Torch Current (60 mA to 200 mA)**
- **Ambient Light or LED Thermal Sensing with Current Scaleback**
- **End-of-Charge Output ($\overline{EOC}$)**
- **Dedicated Indicator LED Current Source**
- **No Inductor Required**
- **Manual Flash Enable via Strobe Pin Input**
- **Programmable Flash Pulse Duration, and Torch and Flash Currents via I^2C-compatible Interface**
- **True Shutdown (LED Disconnect)**
- **Flash Time-Out Protection**
- **LED Temperature Protection or Ambient Light Sensing Pin**
- **Low Profile 20-Pin UQFN Package (3.0 mm × 2.5 mm × 0.8 mm)**

APPLICATIONS

- **Camera Phones**
- **Digital Still Camera**
- **Voltage Rail Management**

DESCRIPTION

LM3550 is a low-noise, switched-capacitor DC/DC converter designed to operate as a current-limited and adjustable (up to 5.3V) super-capacitor charger. LM3550 features user-selectable super-capacitor charge-termination voltages and an optimal charge-termination mode that maximizes flash-energy efficiency by accounting for flash element losses. Additionally, the device provides one adjustable constant current output (up to 200 mA) and one NFET controller ideal for driving one or more high-current LEDs either in a high-power flash mode or a low-power torch mode.

Typical Application Circuit

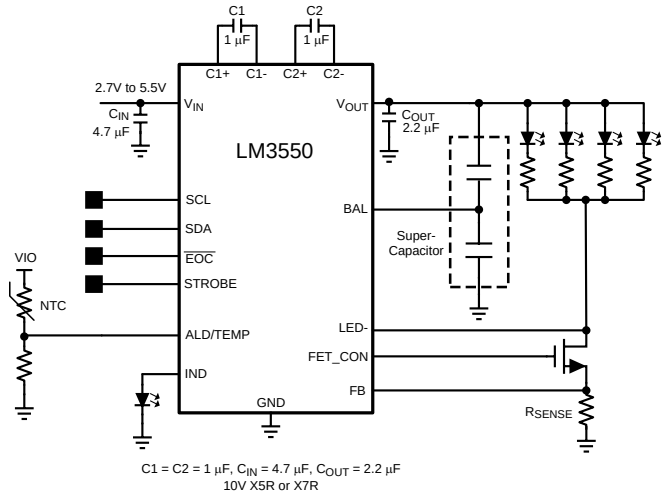

Figure 1.

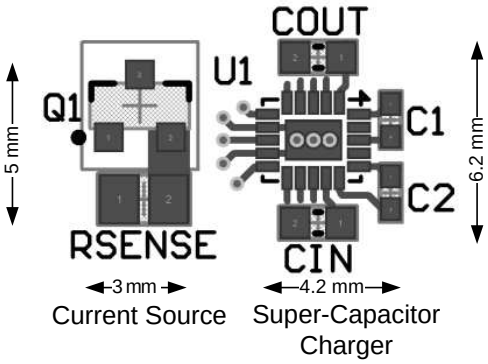

Figure 2. Solution Size

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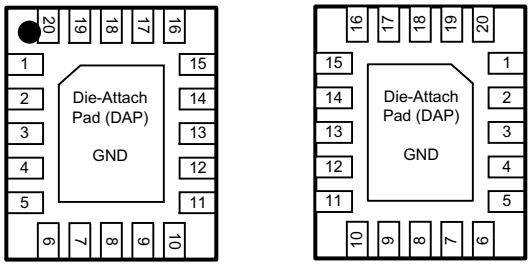
DESCRIPTION (CONTINUED)

The LM3550 can be configured to utilize a proprietary super-capacitor charging scheme (Optimal Charge Mode), allowing faster charging times (0 to Target Voltage) and lower current-source power dissipation. Optimal Charge Mode adapts to changes in the flash LEDs forward voltage as well as the super-capacitor's ESR ensuring that the super-capacitor is charged to the ideal voltage required to sustain constant current-flash operation.

The LED current and Flash pulse duration of the LM3550 can be programmed via an I^2C-compatible interface. The STROBE pin allows the Flash to be toggled via a flash-enable signal from a camera module. The $\overline{EOC}$ pin sinks current when the output voltage reaches 95% of the final value.

The ALD/TEMP input pin allows either a light sensor to adjust the flash-current level based on the ambient light conditions, or it allows for over-temperature detection and protection of the LED during high-power operation or high ambient-temperature conditions by connecting an NTC thermistor temperature monitoring circuit to the pin.

Connection Diagram



Top View Bottom View

PIN DESCRIPTIONS

Pin #	Name	Description
14	V_{IN}	Input voltage connection. A 1 µF ceramic capacitor is required from V_{IN} to GND.
1	V_{OUT}	Charge pump output. A 1 µF ceramic capacitor is required from V_{OUT} to GND. Connect the Flash LED anodes and Super-Capacitor to this pin.
20	C1+	Flying capacitor pins. 1 µF ceramic capacitor should be connected from C1+ to C1− and C2+ to C2−.
18	C1-	
15	C2+	
16	C2-	
3	LED-	Regulated current sink input, for Torch Mode.
4	FET_CON	External FET controller. Connect gate of flash NFET to this pin.
5	FB	Programmable Feedback Voltage pin.
10	SCL	I^2C Serial Clock pin.
8	SDA	I^2C Serial Data I/O pin.
13	IND	Indicator LED Current Source. Drives one red LED with a 5 mA current.
6	$\overline{EOC}$	End-of-charge output/ flash ready. The $\overline{EOC}$ pin will transition from high to low when an end of charge state has been reached
11	STROBE	Manual Flash enable pin. The Strobe pin can be configured to be rising edge sensitive with the flash timing controlled internally, or level sensitive with the flash timing being controlled externally.
2	BAL	Super-capacitor active Balance pin.
12	ALD/TEMP	Ambient Light Sensor or Temperature Monitoring pin. For ambient light sensing, connect a light sensor / photo-diode and a resistor to this pin. For temperature monitoring, connect a NTC thermistor from VCC to the NTC pin and a resistor from the NTC pin to ground.
7,9,17,19, DAP	GND	Ground pins. These pins should be connected directly to a low impedance ground plane.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

V_{IN} to GND		−0.3V to 6V
V_{OUT}, LED−, FB to GND		−0.3V to 6V
SDA, SCL, STROBE, FET_CON, $\overline{EOC}$, ALD/TEMP, IND to GND		−0.3V to 6V
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature (T_{J-MAX})		150°C
Storage Temperature Range		−65°C to +150
Maximum Lead Temperature (Soldering, 10s)		See(5)
ESD Rating(6)	Human Body Model	2 kV
	Machine Model(7)	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 145ºC (typ.) and disengages at T_J = 125ºC (typ.). The thermal shutdown is specified by design.
(5) For detailed soldering specifications and information, please refer to Texas Instruments Application Note: AN-1187 (SNOA401) for Recommended Soldering Profiles.
(6) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged through a 0Ω (nominal) resistor into each pin.(MIL-STD-883 3015.7). Texas Instruments recommends that all integrated circuits be handled with appropriate ESD precautions. Failure to observe proper ESD handling techniques can result in damage to the device.
(7) The LED− pin has a machine model ESD rating of 150V.

Operating Ratings(1)(2)

Input Voltage Range	2.7V to 5.5V
Junction Temperature Range (T_J)(3)	−30°C to 125°C
Ambient Temperature Range (T_A)(4)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
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Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA})(1)	57°C/W

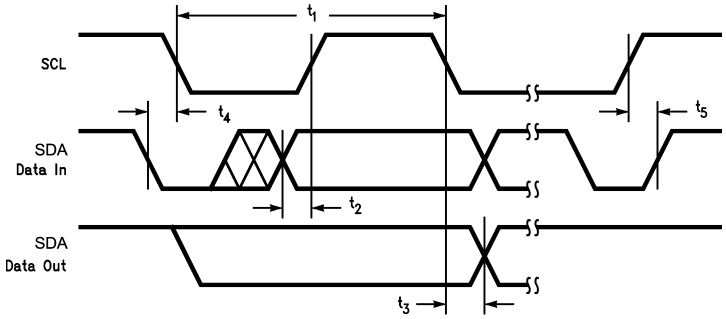
(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Electrical Characteristics[1][2]

Limits in standard typeface are for T_J = +25°C. Limits in **boldface type** apply over the full ambient junction temperature range (−30°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to the LM3550 Typical Application Circuit with: : V_{IN} = 3.6V, C_{IN} = 4.7µF, C_{OUT} = 2.2µF, C_1 = C_2 = 1 µF.

Symbol	Parameter	Conditions		Min[3]	Typ	Max[3]	Units
I_{LED-}	Current Sink Accuracy	2.7V ≤ V_{IN} ≤ 5.5V 3.0V ≤ V_{OUT} ≤ 5.5V		**54**	60	**66**	mA
				90	100	**110**	
				180	200	**220**	
V_{OVP}	Output Over Voltage Protection	2.7V ≤ V_{IN} ≤ 5.5V	Going into OVP		5.3	**5.479**	V
			Hysteresis		0.2		
V_{OUT}	Output Voltage Regulation	2.7V ≤ V_{IN} ≤ 5.5V I_{OUT} = 0 mA		**4.275**	4.5	**4.666**	V
				4.75	5	**5.169**	
				5.035	5.3	**5.479**	
V_{BAL}	BAL Pin Voltage Regulation	2.7V ≤ V_{IN} ≤ 5.5V			V_{OUT} / 2		V
I_{IND}	IND Pin Current Regulation	2.7V ≤ V_{IN} ≤ 5.5V V_{IND} = 2.0V		**3.3**	4.8	**6.3**	mA
f_{SW}	Switching Frequency	2.7V ≤ V_{IN} ≤ 5.5V		**0.882**	1	**1.153**	MHz
V_{FB}	Feedback Pin Regulation Voltage	2.7V ≤ V_{IN} ≤ 5.5V V_{OUT} = 4.6V		**94**	100	**106**	mV
$V_{ALD/TEMP}$	ALD/TEMP Pin Reference Voltage	2.7V ≤ V_{IN} ≤ 5.5V		**0.95**	1	**1.05**	V
$V_{\overline{EOC}}$	$\overline{EOC}$ Pin Output Logic Low	I_{LOAD} = 3 mA				**400**	mV
I_{IN-CL}	Input Current Limit	V_{OUT} = 0V			534	**610**	mA
I_{SD}	Shutdown Supply Current	Device Disabled 2.7V ≤ V_{IN} ≤ 5.5V			1.8	**4**	µA
I_Q	Quiescent Supply Current	2.7V ≤ V_{IN} ≤ 5.5V I_{OUT} = 0 mA 5V Charge Mode Non-Switching			168	**240**	µA
V_{STROBE}	Strobe Logic Thresholds	2.7V ≤ V_{IN} ≤ 5.5V	High	**1.23**		**V_{IN}**	V
			Low	**0**		**0.7**	
I^2C-Compatible Voltage Specifications (SCL, SDA)							
V_{IL}	Input Logic Low	2.7V ≤ V_{IN} ≤ 5.5V		**0**		**0.7**	V
V_{IH}	Input Logic High	2.7V ≤ V_{IN} ≤ 5.5V		**1.23**		**V_{IN}**	V
V_{OL}	Output Logic Low	I_{LOAD} = 3 mA				**400**	mV
I^2C-Compatible Timing Specifications (SCL, SDA)							
t_1	SCL (Clock Period)			**294**			ns
t_2	Data In Setup Time to SCL High	f_{SCL} = 400 kHz.		**100**			ns
t_3	Data Out Stable After SCL Low	f_{SCL} = 400 kHz.		**0**			ns
t_4	SDA Low Setup Time to SCL Low (Start)	f_{SCL} = 400 kHz.		**100**			ns
t_5	SDA High Hold Time After SCL High (Stop)	f_{SCL} = 400 kHz.		**100**			ns

(1) All voltages are with respect to the potential at the GND pin.
(2) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/36 µm (1.5oz/1oz/1oz/1.5oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W.
(3) Min and Max limits are specified by design, test, or statistical analysis. Typical (typ.) numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = 3.6V and T_A = 25ºC.


t1
SCL
t4
t5
SDA
Data In
t2
SDA
Data Out
t3

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN} = 4. 7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super-Capacitor = 0.5F TDK EDLC272020-501-2F-50,

Output Voltage vs. Output Current 5.3V Mode

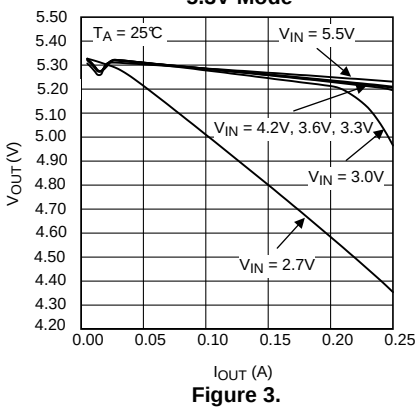


Figure 3.

Output Voltage vs. Output Current 5.3V Mode, Tri-Temp

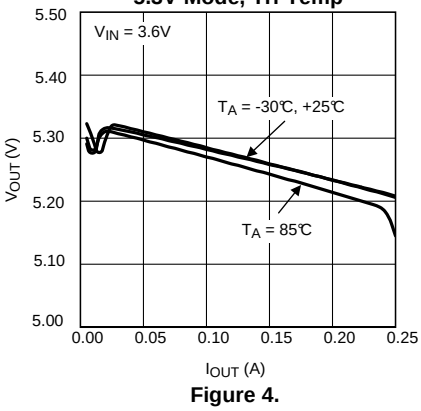


Figure 4.

Output Voltage vs. Output Current 5.0V Mode

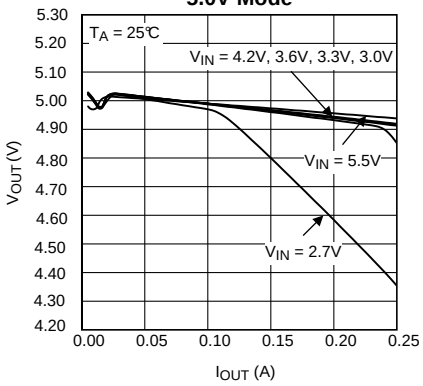


Figure 5.

Output Voltage vs. Output Current 5.0V Mode, Tri-Temp

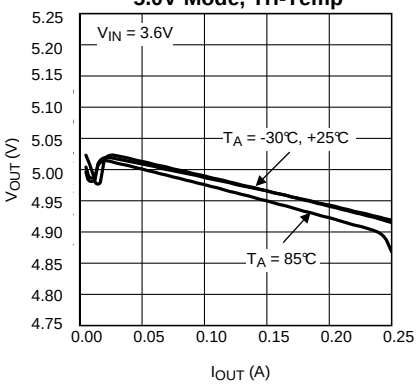


Figure 6.

Output Voltage vs. Output Current 4.5V Mode

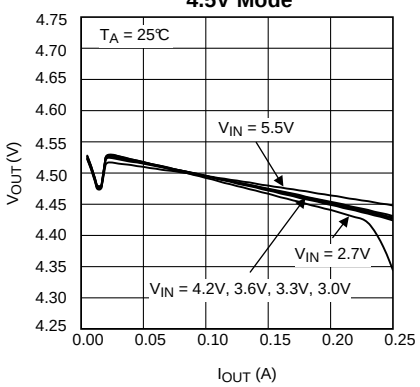


Figure 7.

Output Voltage vs. Output Current 4.5V Mode, Tri-Temp

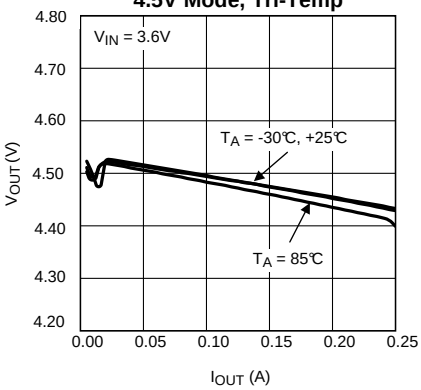


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN} = 4. 7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super-Capacitor = 0.5F TDK EDLC272020-501-2F-50,

Input Current Limit vs. Output Voltage

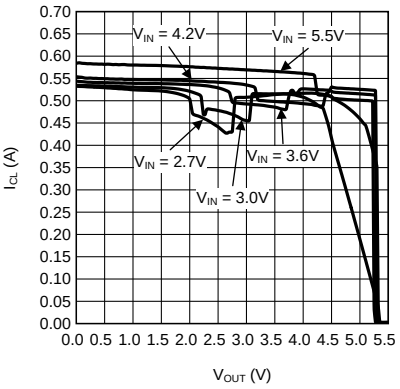


Figure 9.

Input Current Limit vs. Output Voltage Tri-Temp

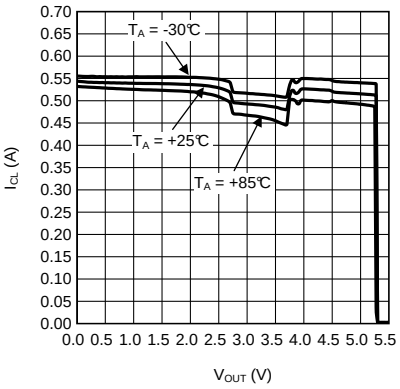


Figure 10.

Converter Efficiency vs. Input Voltage 5.3V Mode

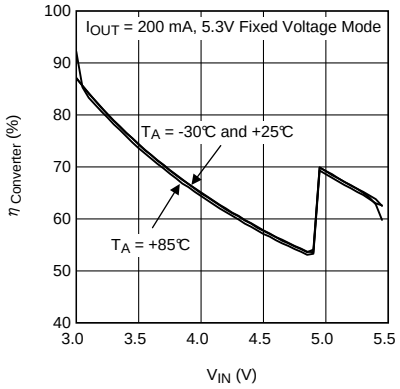


Figure 11.

Converter Efficiency vs. Input Voltage 5.0V Mode

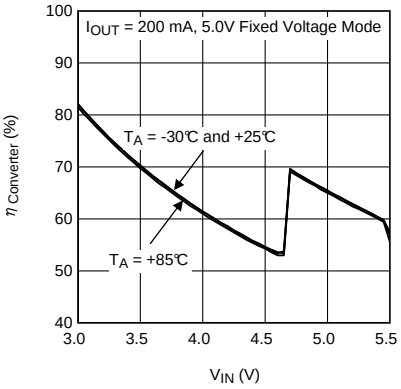


Figure 12.

Converter Efficiency vs. Input Voltage 4.5V Mode

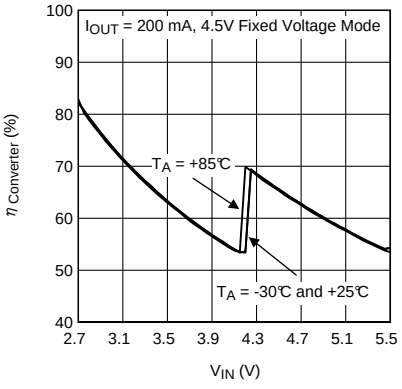


Figure 13.

Input Current vs. Input Voltage 5.3V Mode

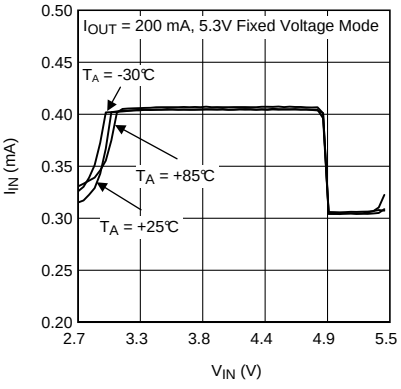


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN} = 4. 7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super-Capacitor = 0.5F TDK EDLC272020-501-2F-50,

Input Current vs. Input Voltage 5.0V Mode

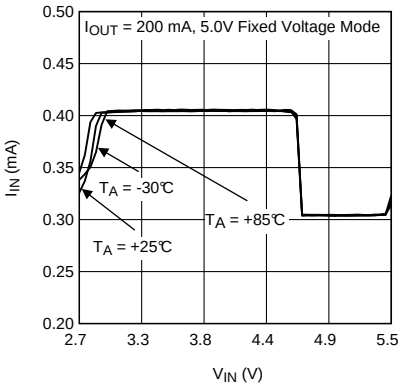


Figure 15.

Input Current vs. Input Voltage 4.5V Mode

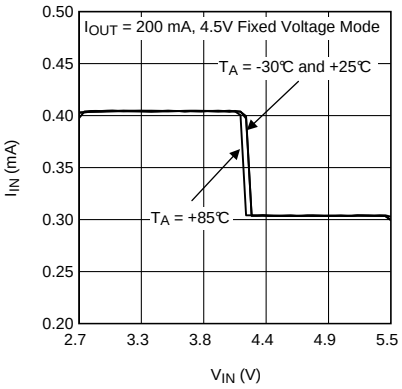


Figure 16.

LED Efficiency vs. Input Voltage Torch Mode, 100 mA

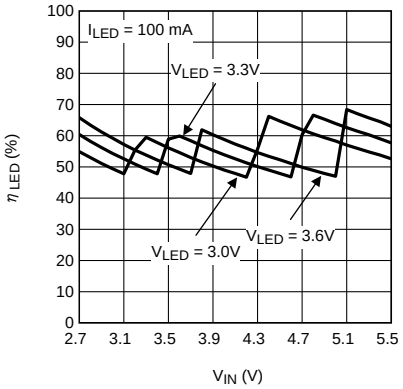


Figure 17.

LED Efficiency vs. Input Voltage Torch Mode, 200 mA

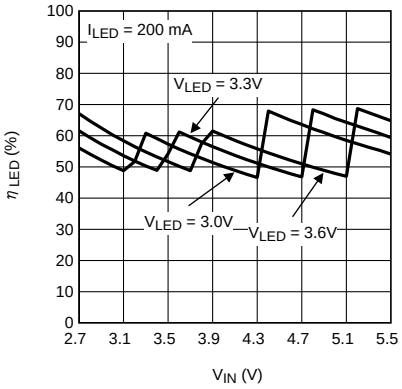


Figure 18.

Torch Current vs. Brightness Code

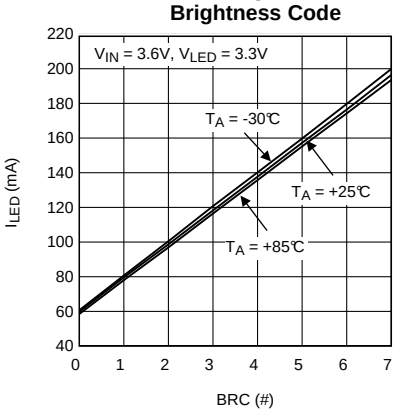


Figure 19.

Torch Current vs. Input Voltage Code = 0

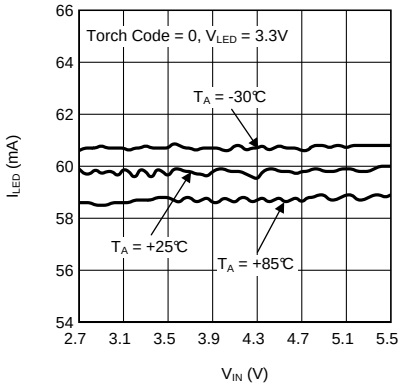


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN} = 4. 7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super-Capacitor = 0.5F TDK EDLC272020-501-2F-50,

Torch Current vs. Input Voltage Code = 1

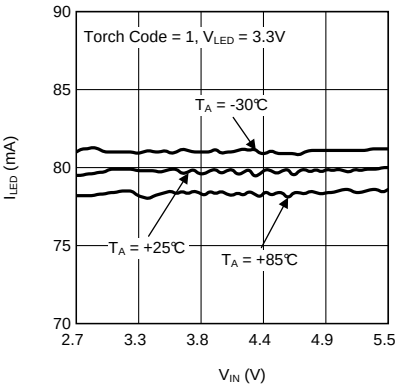


Figure 21.

Torch Current vs. Input Voltage Code = 2

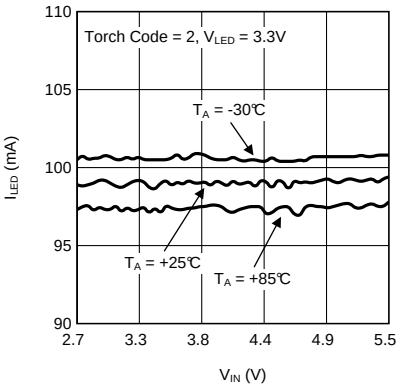


Figure 22.

Torch Current vs. Input Voltage Code = 3

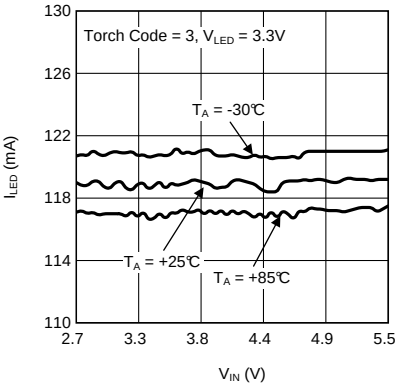


Figure 23.

Torch Current vs. Input Voltage Code = 4

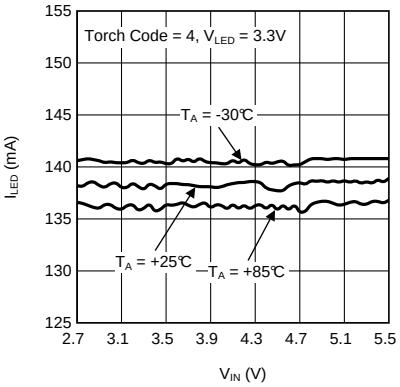


Figure 24.

Torch Current vs. Input Voltage Code = 5

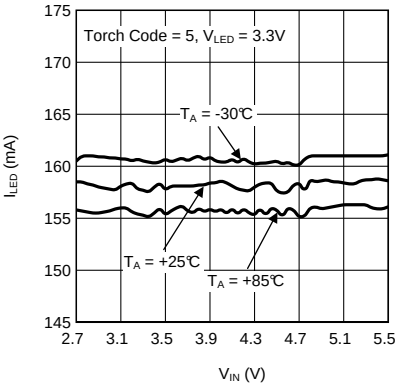


Figure 25.

Torch Current vs. Input Voltage Code = 6

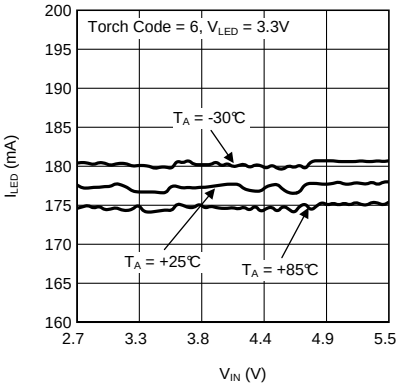


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN} = 4. 7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super-Capacitor = 0.5F TDK EDLC272020-501-2F-50,

Torch Current vs. Input Voltage Code = 7

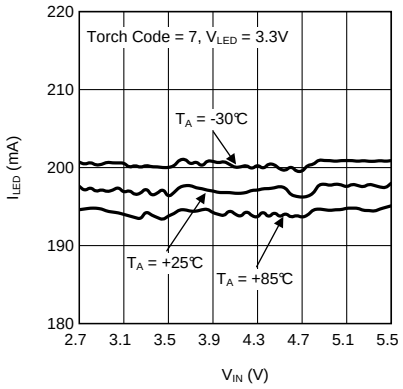


Figure 27.

Torch Current vs. Input Voltage Different V_{LED}

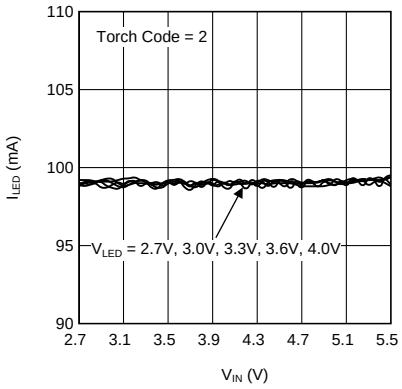


Figure 28.

Feedback Voltage vs. Input Voltage

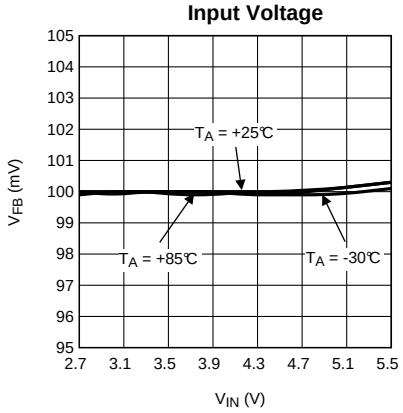


Figure 29.

Oscillator Frequency vs. Input Voltage

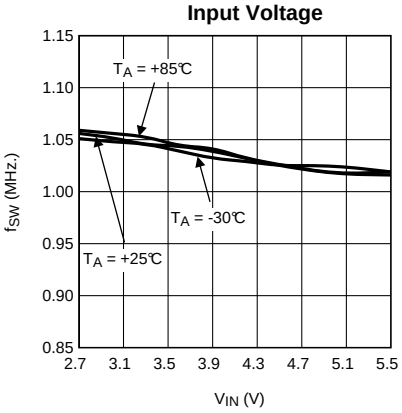


Figure 30.

Shutdown Current vs. Input Voltage

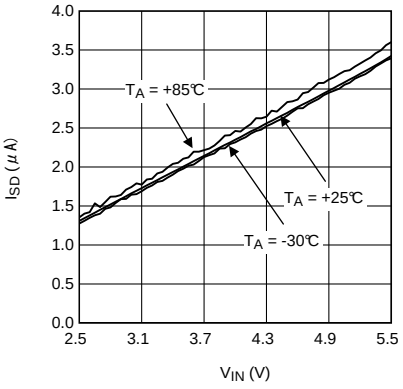


Figure 31.

Indicator Current vs. Input Voltage Different VLED

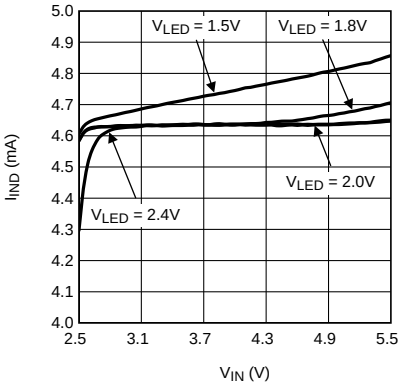


Figure 32.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN} = 4. 7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super-Capacitor = 0.5F TDK EDLC272020-501-2F-50,

Indicator Current vs. Input Voltage Tri-Temp

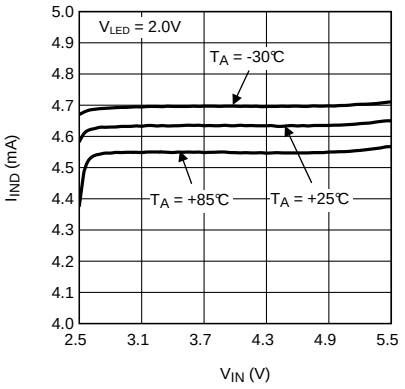


Figure 33.

5.3V Mode Super Capacitor Charge

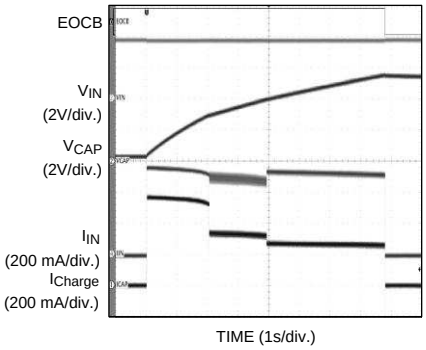


Figure 34.

2 LED, 3A Flash (1.5A each)

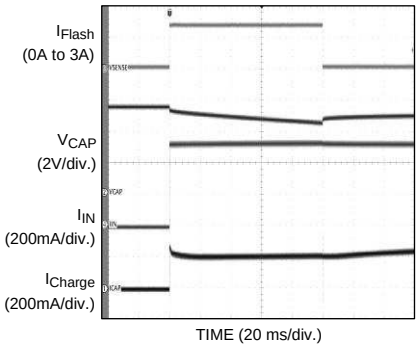


Figure 35.

5.3V Mode Super Capacitor Recharge

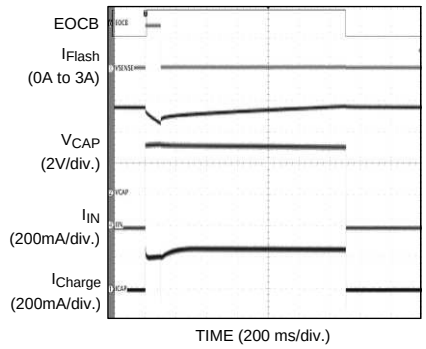


Figure 36.

Strobe to Flash Delay

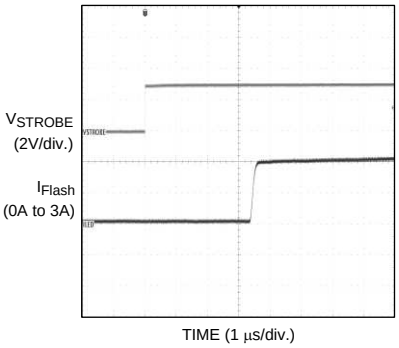


Figure 37.

Edge-Sensitive Strobe

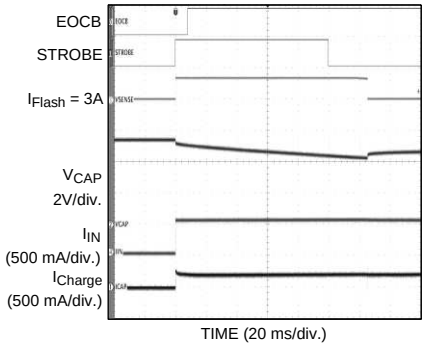


Figure 38.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN} = 4. 7 µF, C_{OUT} = 2.2 µF, C1 = C2 = 1 µF. Super-Capacitor = 0.5F TDK EDLC272020-501-2F-50,

Level-Sensitive Strobe

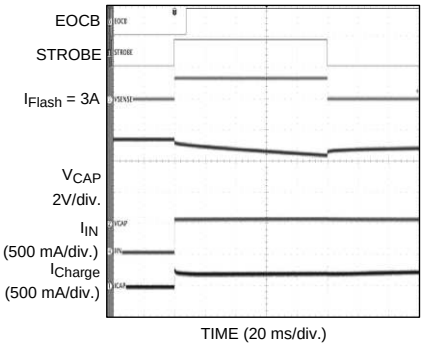


Figure 39.

Flash with $\overline{FGATE}$ = 0

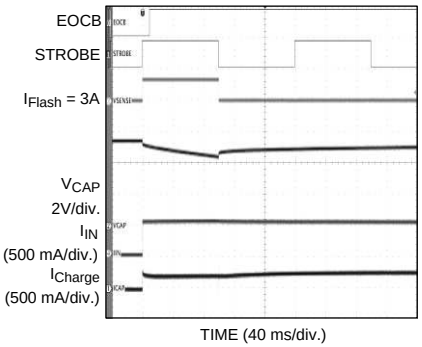


Figure 40.

Flash with $\overline{FGATE}$ = 1

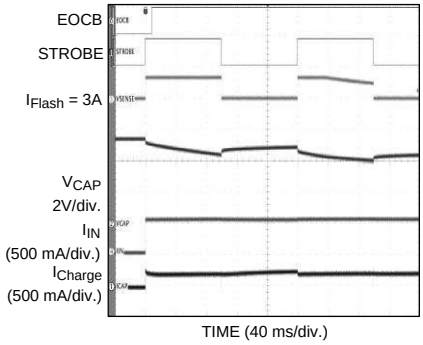


Figure 41.

ALS DETECT
Zone 0, V_{ALS} = 100 mV

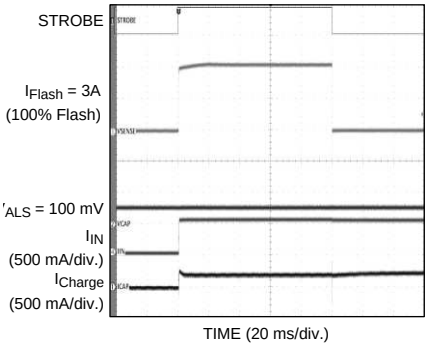


Figure 42.

ALS DETECT
Zone 1, V_{ALS} = 500 mV

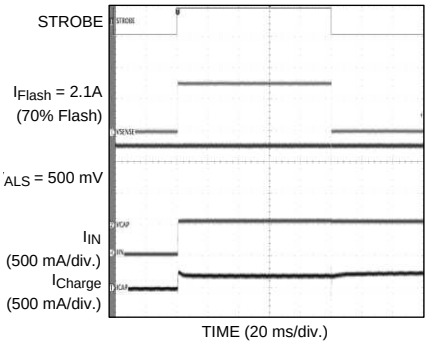


Figure 43.

ALS DETECT
Zone 2, V_{ALS} = 1V

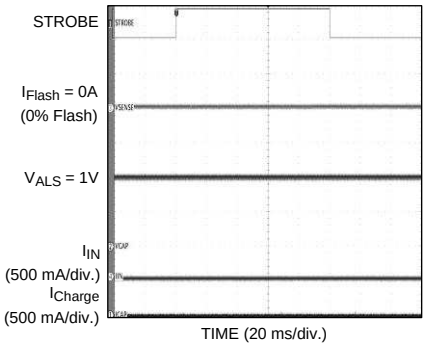
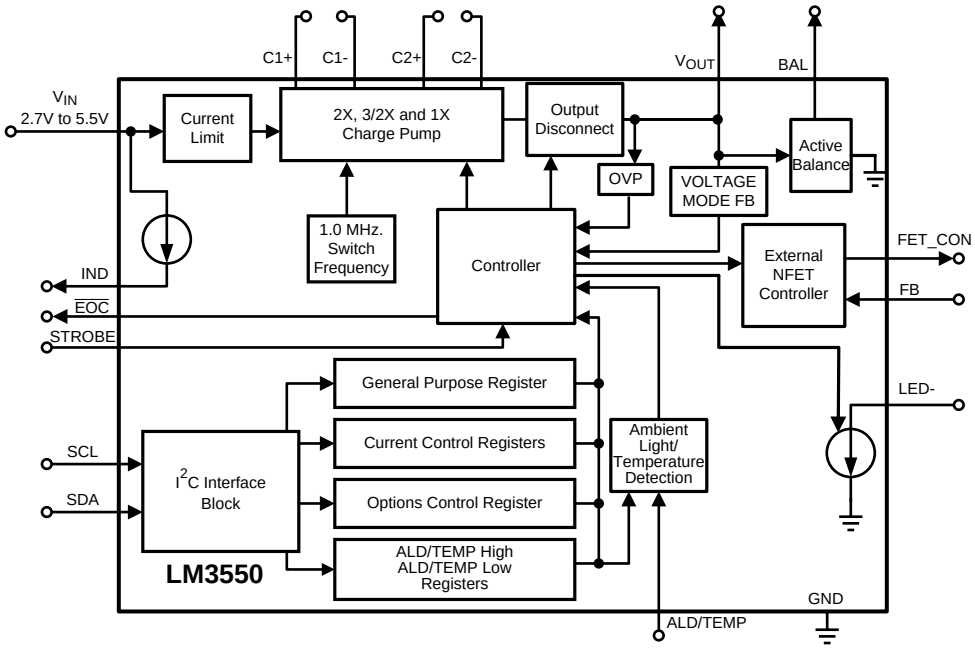


Figure 44.

Block Diagram



CIRCUIT DESCRIPTION

BASIC OPERATION

The LM3550 is a super-capacitor charger and high current-flash controller based upon a switched capacitor boost converter. On the charging end of the application, the LM3550 has a 534 mA (typ.) input current limit that prevents the part from drawing an excessive current when the super-capacitor voltage is below the target charge voltage. During the charge phase the LM3550 will run in current limit and adaptively change gains (1X, 1.5X, 2X) until the super-capacitor reaches its target charge voltage. Integrated into the LM3550 is an external NFET controller that allows the flash current drawn from the super-capacitor to remain regulated throughout the flash cycle. Flash timing and current level can be changed through the I^2C-compatible interface.

DETAILED PIN DESCRIPTION

Strobe Pin

The STROBE pin on the LM3550 provides an external method of flash triggering. This allows a direct connection between a camera/imager and the LM3550 to be made avoiding any latency added due to communication delays in the micro-controller/micro-processor (µC/µP). The STROBE pin can be configured to be rising-edge sensitive (default) or level sensitive. In the rising-edge sensitive mode, the flash duration is controlled internally and will use the value stored in the FLASH duration bits (Options Control Register bits 3:0) to determine the pulse length. If Level Sensitive Mode is selected (Options Control Register bit 7 = '1'), the flash-pulse duration can be controlled externally. In this mode, when the STROBE pin is high, the flash will remain on as long as the duration does not exceed the value stored in the FLASH duration control bits. If the timing does exceed the internal flash-duration value, the LM3550 will automatically disable the flash current.

End of Charge Pin ($\overline{EOC}$)

The $\overline{EOC}$ pin provides an external flag alerting the micro-controller/micro-processor that the super-capacitor has reached the end of charging. When the super-capacitor has reached the desired end-of-charge level, the $\overline{EOC}$ pin will transition from its default state (logic '1') to the EOC state (logic '0'). The $\overline{EOC}$ pin utilizes an open-drain driver that allows the $\overline{EOC}$ logic levels to be compatible with many of the common controller input/output (I/O) levels. Connecting a resistor between the system I/O supply and the $\overline{EOC}$ pin on the LM3550 ensures the proper voltage levels are utilized.

The state of the $\overline{EOC}$ pin can change during a flash event, or any other event whenever the super-capacitor voltage drops below 95% of the target charge voltage.

ALD/TEMP Pin

The ALD/TEMP pin allows the LM3550 to monitor the ambient light or ambient temperature and adjust the flash current through the LED/LEDs without requiring the µC/µP to issue commands through the control interface.

For ambient light detection, a reverse-biased photosensor/diode and a resistor are required. For ambient temperature sensing, a negative temperature coefficient (NTC) thermistor and a resistor are required. Internal to the LM3550 are two comparators (based on a 1V reference) connected to the ALD/TEMP pin that provide three user-selectable regions of flash current adjustment. The trip-point thresholds are selectable in the ALD/TEMP Sense High and Low Registers.

If the ambient light or ambient temperature are sufficiently low (LM3550 in low region) the full-scale flash current will be allowed. As the lighting conditions or temperature increase, the LM3550 ALD/TEMP detection circuit transitions to the second level that limits the flash current to 70% or the full-scale value. For conditions where a flash is not required (Ambient Detection) or if the ambient temperature is too high to flash safely, placing the ALD/TEMP circuit in the high-detection level, the LM3550 will prevent a flash event from occurring. The functionality of the ALD/TEMP pin can be enabled or disabled through General Purpose Register (bit 6). These macro-functions, when enabled, off-load the µC/µP and provide significant system-power savings.

To help filter out the 50 to 60 Hz noise caused by indoor lighting, a 1 µF ceramic capacitor tied between the ALD/TEMP pin and GND is recommended.

IND Pin

The Indicator pin (IND) consists of a current source that is capable of driving a red indicator LED with 5 mA of drive current. This indicator LED can be turned on and off by toggling bit 7 in the General Purpose Register.

BAL Pin

The Balance pin (BAL), when connected to a super-capacitor (if needed), regulates the two sections of the super-capacitor so that voltage on either cell is equal to ½ the output voltage. This ensures that an over-voltage condition on either cap section does not occur.

State Machine Description

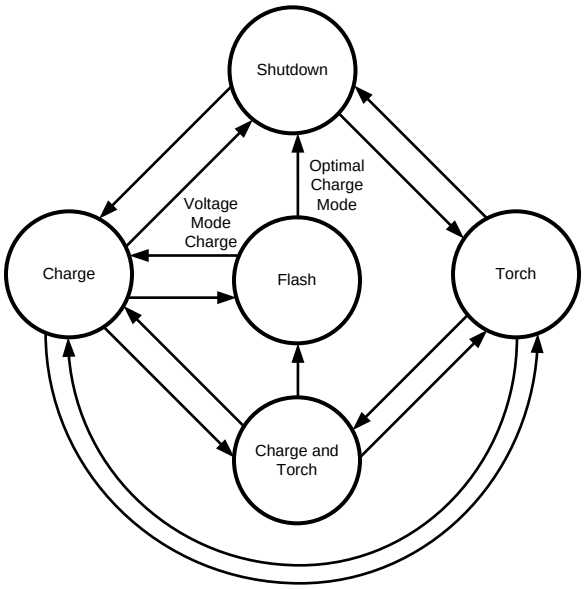


Figure 45. Default State Diagram

BASIC DESCRIPTION

The state machine for the LM3550 involves five different states: Shutdown, Torch, Charge, Charge and Torch, and Flash.

The Shutdown state, or standby state, places the LM3550 in a low-power mode that will typically draw 1.8 µA of current from the power supply.

The Torch state charges the super-capacitor up to V_{LED} + V_{TREG} (V_{TREG} ≈ 300 mV) and utilizes the internal current sink to drive the flash LEDs with a current up to 200 mA.

The Charge state places the LM3550 into a dedicated charge mode that provides the fastest means of charging the super-capacitor up to the target level (4.5V, 5.0V, 5.3V or Optimal).

The Charge and Torch State combines the functionality of both the Torch state and Charge state. This state allows the flash LEDs to be on during the charging of the super-capacitor. During the initial charging, the torch current is limited to 60 mA to allow the majority of the output current to be utilized in the super-capacitor charging. Once the target capacitor voltage is reached, the torch-current levels become fully adjustable.

The Flash state is responsible for driving the flash LEDs at the desired flash current. This state can be entered either through I^2C-controlled event or through an external Strobe event.

SHUTDOWN STATE

The Shutdown state is the default power-up state. The LM3550 will enter the shutdown state when the STROBE pin is held low without a flash event occurring, and when the FLASH, TORCH and CHARGE bits in the General Purpose Register are equal to '0'.

TORCH STATE

The Torch state of the LM3550 provides the flash LED / LEDs with a constant current level that is safe for continuous operation. This state is useful in low light conditions when an imager is placed in movie / video mode. The Torch state is enabled when the Torch bit in the General Purpose Register is set to a '1' and the Flash and Charge bits are set to '0'. The desired torch current level (8 total levels between 60 mA and 200 mA) is set in the Current Control Register.

Enabling the torch bit will start up the LM3550 and begin charging the capacitor. Before a torch event can occur, the super-capacitor must be charged to a voltage greater than 3.0V. Once the super-capacitor reaches a voltage of 3.0V, the LED− pin will begin sinking current. In order for the torch current to be properly regulated, the super-capacitor must be charged up to a value that is greater than V_{LED} + V_{TREG} (V_{TREG} ≈ 300 mV).

When in the Torch state, the LM3550 will regulate the proper output voltage (either 3.0V or V_{LED} + V_{REG}) utilizing a pulsed regulation scheme (PFM). During this mode, the part will operate in current limit until the output voltage reaches the target level. At that point, the charge-pump will turn off, and the super-capacitor will supply the load. Once the super-capacitor voltage drops below the turn-on threshold due to the loading caused by the torch current, the charge-pump will turn on again and re-charge the super-capacitor.

CHARGE STATE

The Charge state of the LM3550 provides the fastest charge time when compared to the other states of operation. In this state, the user has the option of charging the super-capacitor to a voltage equal to 4.5V, 5.0V, 5.3V or to an optimal voltage. The Charge state is enabled through the I^2C interface by setting the Charge Bit to a '1' and setting the Flash and Torch Bits to a '0' in the General Purpose Register. The charge voltage is selectable by setting the two charge-mode bits (CM1 and CM0) also found in the General Purpose Register.

Depending on the input voltage and output voltage conditions, the LM3550 will deliver different charge currents to the super-capacitor. Charge current is dependent on the charge-pump gain.

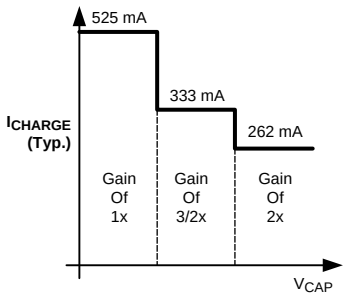


Figure 46. Charge Current vs. Output Voltage

Fixed Voltage Charge Mode

During the Charge state, the LM3550 will operate in current limit until the target voltage is reached. For the 4.5V, 5.0V and 5.3V charge modes, the LM3550 will operate in a constant-frequency mode once the target voltage is reached for load currents greater than 60 mA. This allows the LM3550 to draw only the required current from the power source when the load current is less than the maximum. When the average output current exceeds the maximum of the LM3550, the part will return to the current limited operation until the target voltage is reached. If the output current is less than 60 mA, the LM3550 will operate in a PFM-burst mode.

Optimal Charge Mode

For the Optimal Charge Mode, the current-limited, pulsed regulation scheme (PFM) is used to maintain the target voltage. In Optimal Charge Mode, the LM3550 charges the super-capacitor to a level that is required to sustain a flash for a given period of time. Optimal Charge Mode compensates for variations in LED forward voltage and super-capacitor ESR by charging the capacitor to an optimal voltage that minimizes the power dissipated in the external current source during the flash. The user must calculate the required overhead voltage and select this value in the Options Control Register. For more information regarding the optimal charge mode, please see the **Optimal vs. Fixed Charge Mode** description in the Application Information section of this datasheet.

NOTE

When the LM3550 is placed into Optimal Charge Mode, the flash LEDs will begin to glow once the super-capacitor voltage exceeds 3.0V. The LEDs will continue to glow until the part is placed into shutdown, into the flash state, or into one of the fixed voltage charge modes.

TORCH AND CHARGE STATE

The Torch and Charge state provides the ability to utilize the torch functionality while charging to the selected target voltage. The Torch and Charge state is entered by setting the Torch bit and Charge bit to a '1' and by setting the Flash bit to a '0' in the General Purpose Register. Additionally, the CM1 and CM0 bits can be configured to define the target charge voltage.

During the initial charging of the super-capacitor, the Torch functionality will not be enabled until the capacitor voltage reaches 3.0V. Additionally, the Torch current is limited to 60 mA until the target voltage is reached. Once the output reaches the target, the current level specified in the Current Control Register is allowed.

In the event that the total output current exceeds the capacitor charge current ($I_{CHARGE} = I_{MAX} - I_{TORCH} - I_{EXTERNAL}$), causing the super-capacitor to drop below the target voltage, the LM3550 will automatically set the T2 bit in the Current Control Register to a '0', decreasing the torch current.

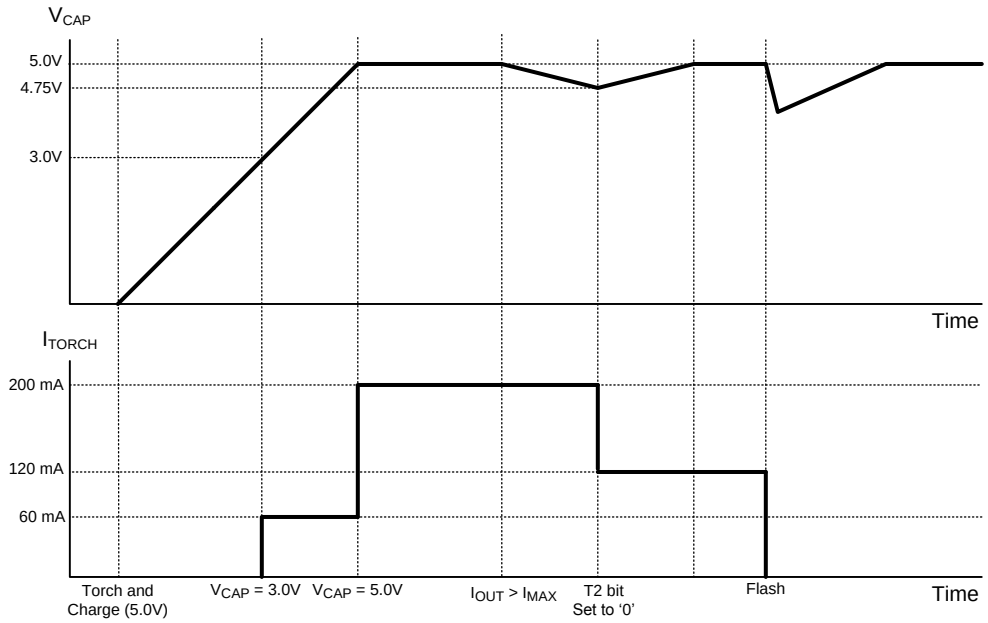


Figure 47. Torch Current Diagram

FLASH STATE

When entered, the LM3550's Flash state delivers a high-current burst of current to the Flash LEDs. To enter the Flash state, the Flash bit in the General Purpose Register must be set to a '1' or the STROBE pin must be pulled high (edge or level sensitive). The flash duration and current level are user adjustable via the I^2C interface (F2-F0 in Current Control and FD3-FD0 in Options).

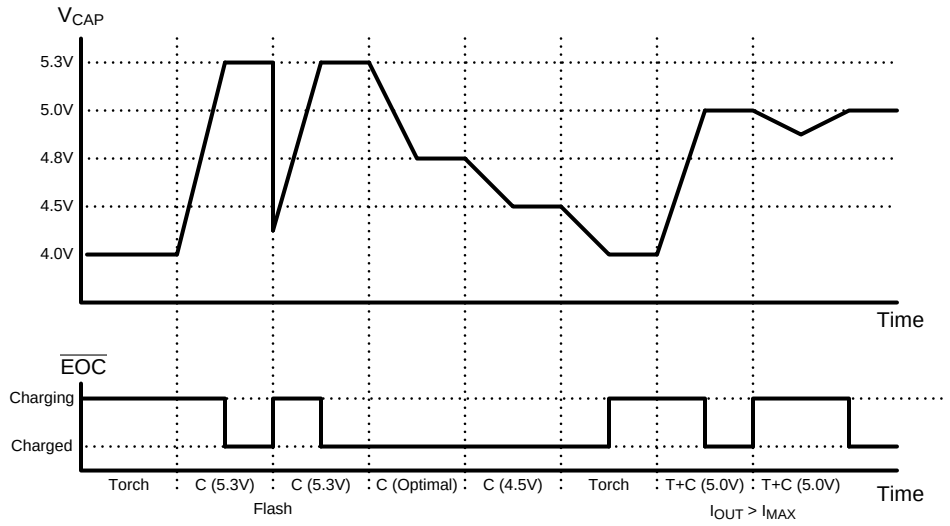
By default, a flash will not occur if the super-capacitor is not fully charged (i.e., the end-of-charge flag ($\overline{EOC}$ pin) must transition low). If the Flash state was entered via the I^2C interface (Flash bit = '1'), the LM3550 will automatically reset the Flash bit and the Torch bit to '0' upon completion of the flash. Additionally, after the flash event has occurred, the LM3550 will return to the charge state/mode that was in operation before the flash event with the exception of Optimal Charge Mode. (If Optimal Charge Mode was used before a flash, all charging is halted after the flash.)

$\overline{\text{EOC}}$ FUNCTIONALITY

The LM3550's $\overline{\text{EOC}}$ provides an indicator alerting the controller that the super-capacitor has reached its target voltage. The $\overline{\text{EOC}}$ pin will transition low once the capacitor reaches 95% of the target voltage for the 4.5V, 5.0V and 5.3V modes or once the capacitor has reached the optimal charge voltage in Optimal Charge Mode.

During operation, the LM3550 will continue to monitor the voltage on the super-capacitor and will update the $\overline{\text{EOC}}$ pin when needed. Any time a mode transition occurs during Charge mode or Charge and Torch mode, the EOC state will be re-evaluated.

During Torch Mode, the $\overline{\text{EOC}}$ will always indicate a charging state ($\overline{\text{EOC}}$ = '1') .



STATE DIAGRAM $\overline{\text{FGATE}}$ = '1'

By default, the LM3550 will prevent a flash event from occurring if the super-capacitor has not reached the target voltage ($\overline{\text{EOC}}$ = '0'). In the event that this restriction is not desired, the flash gate bit ($\overline{\text{FGATE}}$ in the General Purpose Register) can be set to a '1' disabling the end-of-charge requirement. Setting $\overline{\text{FGATE}}$ to a '1' allows the Flash state to be entered at anytime. If the super-capacitor is not charged to the proper voltage before the $\overline{\text{EOC}}$ pin indicates a full charge, the perceived duration and flash level could be lower than desired.

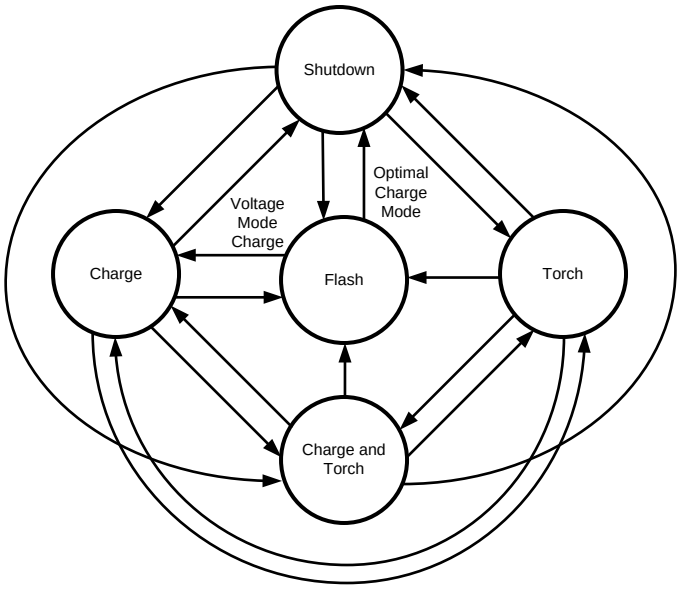


Figure 48. $\overline{\text{FGATE}}$ = '1' State Diagram

I²C-Compatible Interface

DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.

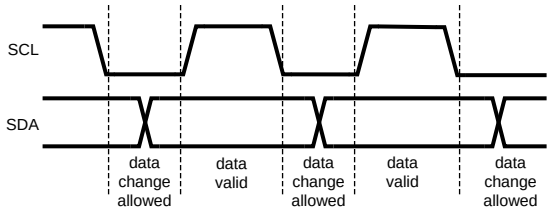


Figure 49. Data Validity Diagram

A pull-up resistor between VIO (Logic Power Supply) and SDA must be greater than [**(VIO − V_{OL}) / 3.0 mA**] to meet the V_{OL} requirement on SDA. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when SCL is LOW.

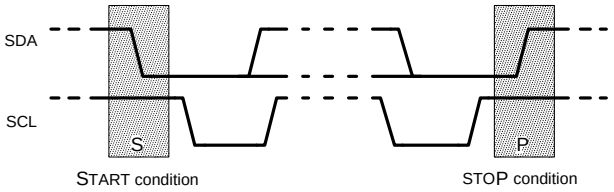
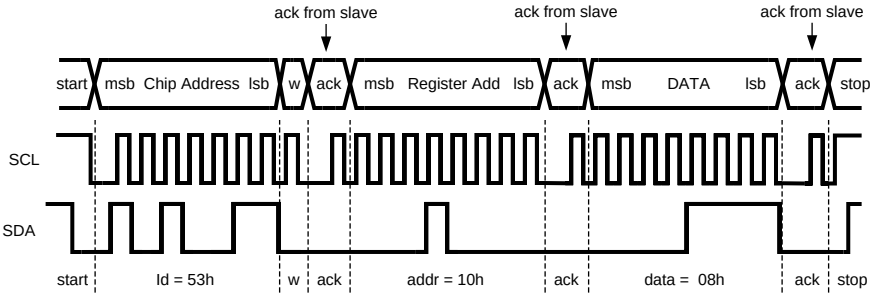


Figure 50. Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3550 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3550 generates an acknowledge after each byte has been received.

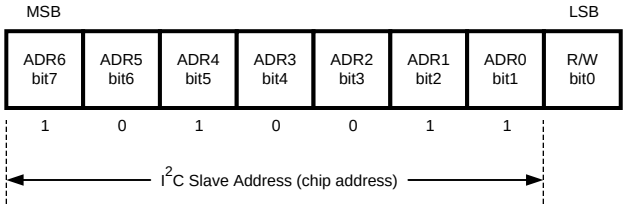
After the START condition, the I^2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3550 address is 53h. For the eighth bit, a '0' indicates a WRITE and a '1' indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



w = write (SDA = "0")
ack = acknowledge (SDA pulled down by the slave)
id = chip address, 53h for LM3550

Figure 51. Write Cycle

I^2C-COMPATIBLE CHILD ADDRESS: 0x53



INTERNAL REGISTERS

Register	Internal Hex Address	Power On Value
General Purpose	0x10	0000 0000
Current Control	0xA0	1111 1000
Options	0xB0	1000 0000
ALD/TEMP Sense High	0xC0	1111 1001
ALD/TEMP Sense Low	0xD0	1100 0110

General Purpose Register Description

General Purpose Register
Register Address: 0x10

MSB							LSB
IND EN bit7	A/T EN bit6	$\overline{\text{FGATE}}$ bit5	CM1 bit4	CM0 bit3	FLASH bit2	CHARGE bit1	TORCH bit0

FLASH, CHARGE, and TORCH: Mode Bits (see Table 1 below).

CM0–CM1: Capacitor Charge Mode (see Table 2 below).

$\overline{\text{FGATE}}$: Flash Gate Bit. If $\overline{\text{FGATE}}$ is a '0', then an end-of-charge condition must occur before a flash can take place. If $\overline{\text{FGATE}}$ is a '1', then an end-of-charge condition does not have to occur before a flash can take place.

A/T EN: ALD/TEMP Enable Bit

IND EN: Enable Indicator Current Source ('0' = Indicator Off, '1' = Indicator On)

Table 1. Control Modes

Flash	Charge	Torch	Mode
0	0	0	Disabled
0	0	1	Torch
0	1	0	Charge
0	1	1	Charge and Torch
1	x	x	Flash

Table 2. Capacitor Charge Level

CM1	CM0	Level
0	0	Optimal Charge Mode
0	1	4.5
1	0	5.0V
1	1	5.3V

Table 3. Gated Flash Control

$\overline{\text{FGATE}}$ Bit	Result
0	Flash only allowed after EOC reached
1	Flash allowed without EOC reached

Table 4. ALD/TEMP Control

A/T EN Bit	Result
0	ALD MODE DISABLED
1	ALD MODE ENABLED

Current Control Register Description

Current Control Register
Register Address: 0xA0

MSB							LSB
1 bit7	1 bit6	F2 bit5	F1 bit4	F0 bit3	T2 bit2	T1 bit1	T0 bit0

Table 5. Torch Level Table

T2	T1	T0	Level
0	0	0	60 mA
0	0	1	80 mA

Table 5. Torch Level Table (continued)

T2	T1	T0	Level
0	1	0	100 mA
0	1	1	120 mA
1	0	0	140 mA
1	0	1	160 mA
1	1	0	180 mA
1	1	1	200 mA

Table 6. Flash Level Table

F2	F1	F0	FB Voltage Level
0	0	0	30 mV
0	0	1	40 mV
0	1	0	50 mV
0	1	1	60 mV
1	0	0	70 mV
1	0	1	80 mV
1	1	0	90 mV
1	1	1	100 mV

Options Control Register Description

Options Register
Register Address: 0xB0

MSB							LSB
SLE bit7	OH2 bit6	OH1 bit5	OH0 bit4	FD3 bit3	FD2 bit2	FD1 bit1	FD0 bit0

SLE: Strobe Level or Edge Sensitivity. '0' = Edge Sensitive, '1' = Level Sensitive

FD0-FD3: Flash Duration control bits (see Table 7).

OH0-OH2: Overhead Charge Voltage control bits (see Table 8).

Table 7. Time-out Duration Table

FD3	FD2	FD1	FD0	Time (msec)
0	0	0	0	16
0	0	0	1	32
0	0	1	0	48
0	0	1	1	64
0	1	0	0	80
0	1	0	1	96
0	1	1	0	112
0	1	1	1	128
1	0	0	0	144
1	0	0	1	160
1	0	1	0	176
1	0	1	1	192
1	1	0	0	208
1	1	0	1	224
1	1	1	0	240
1	1	1	1	512

Table 8. Overhead Charge Voltage Table

OH2	OH1	OH0	Level
0	0	0	300 mV
0	0	1	400 mV
0	1	0	500 mV
0	1	1	600 mV
1	0	0	700 mV
1	0	1	800 mV
1	1	0	900 mV
1	1	1	1V

ALD/TEMP Sense High/Low Registers

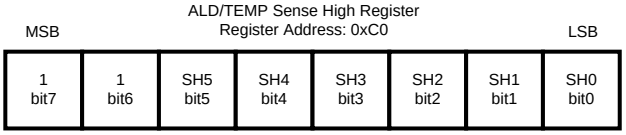


Figure 52. ALD/TEMP Sense High Register

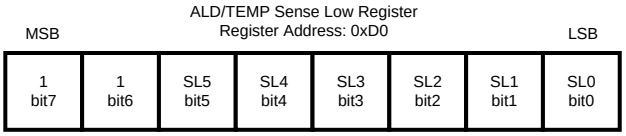


Figure 53. ALD/TEMP Sense Low Register

For ALD/TEMP Sense High and ALD/TEMP Sense Low, the trip levels are set by the following equation:

$$\text{Sense High/Low} = 1V \times N/(2^6 - 1) \quad (1)$$

where N is the decimal equivalent of the value stored in the ALD/TEMP Sense High/Low registers. $N_{SENSEHIGH}$ must be greater than $N_{SENSELOW}$.

Application Information

Super-Capacitor Flash Variable Definitions:

V_{BATT} Voltage supplying charger circuit.

V_{CAP} Super-capacitor voltage at the end of the charge cycle and before a flash.

I_{CL} Maximum current allowed to be drawn from the battery.

I_{FLASH} LED current during the flash event.

t_{FLASH} Desired flash duration.

C_{SC} Super capacitor value.

V_{LED} Flash diode forward voltage at I_{FLASH}.

V_{HR} The headroom required across the FET and the Sense resistor to maintain current sink regulation.

V_{FB} The degeneration resistor R_{SENSE} regulation voltage that in part sets I_{FLASH}.

R_{DSON} On-Resistance of NFET.

V_{RDSON} The voltage drop across the current source FET.

V_{PUMP} The initial SC voltage required for the Flash.

R_{SENSE} Current set resistor.

V_{DROOP} Voltage droop on the super-capacitor during a flash of duration t_{FLASH}.
$= I_{FLASH} \times t_{FLASH} / C_{SC}$

R_{ESR} Super-capacitor ESR value.

V_{ESR} Voltage drop due to SC ESR.

V_{BAL} Voltage drop due to LED ballast resistors

V_{OH} Overhead charge voltage required for constant current regulation during the entire flash duration.

V_{PUMP} $V_{OH} + V_{LED} + V_{ESR} = V_{FB} + V_{RDSON} + V_{ESR} + V_{LED} + V_{DROOP} + V_{BAL}$

V_{HR} $V_{FB} + V_{RDSON}$

SUPER-CAPACITOR CHARGING TIME

The time it takes the LM3550 to charge a super-capacitor from 0V to the target voltage is highly dependent on the input voltage, output-voltage target, and super-capacitor capacitance value.

- The LM3550 will charge up a capacitor faster with higher input voltage and slower with lower input voltages. This is due to the LM3550 staying in the lower gains for longer periods of time.
- The LM3550 will charge up a capacitor faster if the target output voltage is lower and slower if the target output voltage is higher. For a given charge profile, a lower capacitor voltage will be reached faster than a higher voltage level.
- The LM3550 will charge up a capacitor having a lower capacitance value faster than a capacitor having a higher capacitance level.

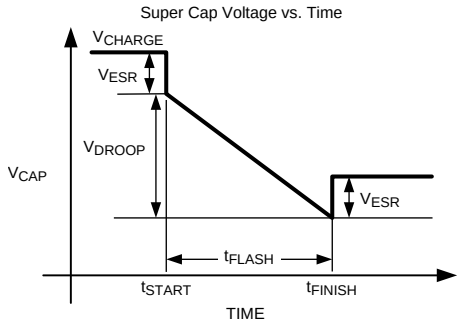
Table 9. Super-Capacitor Charging Times
0.5F Capacitor, 0V to Target

	Opt. MODE(1)	FIXED VOLTAGE MODE		
VIN	**4.38V**	**4.5V**	**5.0V**	**5.3V**
4.2V	4.565s	5.087s	6.314s	7.014s
3.6V	5.207s	5.765s	6.978s	7.832s
3.0V	6.090s	6.446s	7.870s	8.904s

(1) Optimal Mode Flash = 2 LEDs @ 3A (1.5A Each) for 48 ms. Super-Capacitor Part#: TDK EDLC272020-501-2F-50

SUPER-CAPACITOR VOLTAGE PROFILE

When a constant load current is drawn from the charged super-capacitor, the voltage on the capacitor will change. The capacitor ESR and capacitance both affect the discharge profile.



At the beginning of the flash (t_{START}), the super-capacitor voltage will drop due to the super-capacitor's ESR. The magnitude of the drop is equal to the flash current (I_{FLASH}) multiplied by the ESR (R_{ESR}).

$$V_{ESR} = I_{FLASH} \times R_{ESR} \quad (2)$$

Once the initial voltage drop occurs (V_{ESR}) the super-capacitor voltage will decay at a constant rate until the flash ends (t_{FINISH}). The voltage droop (V_{DROOP}) during the flash event is equal to flash current (I_{FLASH}) multiplied by the flash duration (t_{FLASH}) divided by the capacitance value of the super-capacitor (C_{SC}).

$$V_{DROOP} = (I_{FLASH} \times t_{FLASH}) / C_{SC} \quad (3)$$

After the flash event has finished, the voltage on the super-capacitor will increase due to the absence of current flowing through the ESR of the super-capacitor. This step-up is equal to

$$V_{ESR} = I_{FLASH} \times R_{ESR} \quad (4)$$

PEAK FLASH CURRENT

To set the peak flash current controlled by the LM3550, a current setting resistor must be placed between the source of the current source and ground (FB to GND). The LM3550 will regulate the voltage across the resistor to a value between 100 mV and 30 mV depending on the setting in the Current Control Register. Using the 100 mV setting, the peak flash current can be found using the following equation:

$$I_{FLASH} = V_{FB} / R_{SENSE} \quad (5)$$

The LM3550 provides eight feedback voltage levels allowing eight different current settings. The current ranges from 100% of Full-Scale (100 mV setting) down to 30% of Full-Scale (30 mV setting) in 10% steps.

MAXIMUM FLASH DURATION

Several factors determine the maximum achievable flash pulse duration. The flash current magnitude, feedback voltage, R_{DSON} of the current source FET, super-capacitor capacitance (C_{SC}), super-capacitor ESR (R_{ESR}) and super-capacitor charge voltage (V_{CAP}) determine the LM3550's ability to regulate the flash current for a given amount of time.

$$t_{FLASH}\ (max.) = (C_{SC} \times V_{DROOP}) / I_{FLASH}$$

where

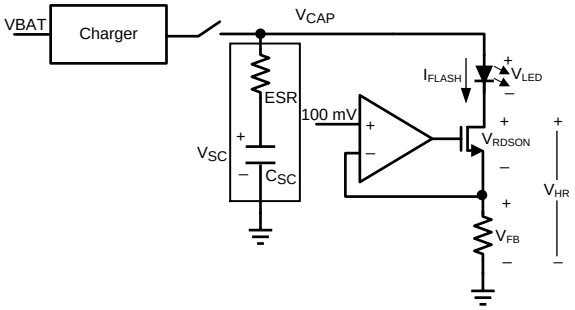
- $V_{DROOP} = V_{CAP} - V_{LED} - [I_{FLASH} \times (R_{ESR} + R_{DSON} + \{R_{BAL}/N)\}] - V_{FB}$
- N = # of Flash LEDs

(6)

Example:

If V_{CAP} = 5.3V, V_{LED} = 4V (@1.5A), I_{FLASH} (total) = 3A, C_{SC} = 0.5F, R_{ESR} = 50 mΩ,R_{DSON} = 40mΩ, V_{FB} = 100 mV, and R_{BAL} = 75 mΩ

Then V_{DROOP} = 0.82V and t_{FLASH} (max.) = 136 ms



OPTIMAL CHARGE MODE VS. FIXED VOLTAGE MODE

The LM3550 provides two types of super-capacitor charging modes: Fixed Voltage and Optimal Charge.

In Fixed Voltage Mode, the LM3550 will charge and regulate the super-capacitor to either 4.5V, 5V or 5.3V. This mode is useful if the LM3550 is going to be used for both flash and fixed-rail applications (power supply for audio or PA sub-systems).

If the LM3550 is only going to be used as a super-capacitor charger and flash controller, the Optimal Charge Mode provides many advantages over the Fixed Voltage Mode. Optimal Charge Mode will charge the super-capacitor to the minimum voltage that is required to sustain a flash pulse compensating for variations in super-capacitor ESR and LED forward voltage due to temperature and process. To properly use the Optimal Charge Mode, the Overhead Voltage (V_{OH}) must be determined. The Overhead Voltage is equal to the voltage required to maintain current source regulation (V_{HR}) plus the voltage droop (V_{DROOP}) on the super-capacitor due to the flash event.

$$V_{OH} = V_{DROOP} + V_{HR} = (I_{FLASH} \times t_{FLASH} / C_{SC}) + V_{FB} + (I_{FLASH} \times R_{DSDON}) \quad (7)$$

and

$$V_{CAP} = V_{OH} + V_{LED} + [I_{FLASH} \times (R_{ESR}+R_{BAL}/ N)] \quad (8)$$

where

- N = Number of Flash LEDs

Example:

If V_{LED} (peak)= 4.1V (@1.5A), I_{FLASH} (total) = 3A, C_{SC} = 0.5F, R_{ESR} = 50 mΩ, R_{DSON} = 40 mΩ, V_{FB} = 100 mV, R_{BAL} = 75 mΩ, and t_{FLASH} = 64 ms

Then V_{OH} = 0.604V and V_{CAP} = 4.97V

NOTE

V_{LED} (peak) is equal to the LED voltage before self-heating occurs. Once current flows through the LED, the LED will heat up, and the forward voltage will decrease until it reaches a steady-state level. This voltage drop is dependent on the LED and the PCB layout.

Based on this calculation, setting the Overhead Voltage to 600 mV in the Current Control Register should ensure a regulated 3A flash pulse over the entire flash duration.

Unlike Fixed Voltage Mode, Optimal Charge Mode will adjust the super-capacitor voltage upon changes in LED forward voltage and variation in super-capacitor ESR, ensuring that the super-capacitor does not charge to a voltage higher than needed. By charging optimally, the LM3550 can potentially charge the super-capacitor to its EOC state faster due to the target voltage being lower, and it helps ease the thermal loading on the current source FET during the flash.

Power-Saving Example

Optimal Charge vs. Fixed Voltage Charge

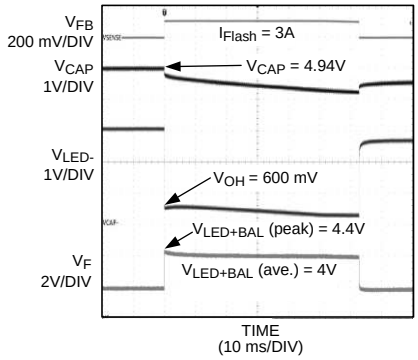


Figure 54. Optimal Charge Mode

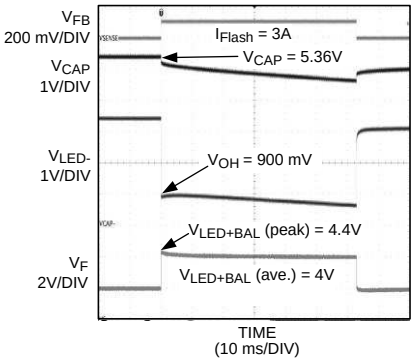


Figure 55. 5.3V Fixed Voltage Charge Mode

Peak Power Dissipation Across Current Source FET

P_{NFET} (max.) = I_{FLASH} × (V_{OH} − V_{FB})

where

- Optimal Mode = 1.5W, Fixed Voltage Mode (5.3V) = 2.4W (9)

Average Power Dissipation Across Current Source FET (64 ms Pulse)

P_{NFET} (avg.) = I_{FLASH} × [V_{OH} − (V_{DROOP}÷2) − V_{FB}]

where

- Optimal Mode = 936 mW, Fixed Voltage Mode (5.3V) = 1.824W (10)

COMPONENT SELECTION

Super-Capacitor

Super-capacitors, or electrochemical double-layer capacitors (EDLC's), have a very high energy density compared to other capacitor types. Most super-capacitors aimed at applications requiring voltages higher than 3V are three-terminal devices (two super-capacitor cells stacked in series). Special care must be taken to ensure that the voltage on each cell of the super-capacitor does not exceed the maximum rating (typically 2.75V to 2.85V, depending on the manufacturer). The LM3550 is capable of safely charging super-capacitors of many different capacitances up to a V_{OUT}(max.) = 5.3V typ.

The capacitor balance pin (BAL) on the LM3550 ensures that the voltage on each cell is equal to half of the output voltage to prevent an over-voltage condition on either cell. If either cell fails as a short, the BAL pin will not prevent the second cell from being damaged.

NOTE

The LM3550 is not designed to work with low-voltage, single-cell super-capacitors.

Boost Capacitors

The LM3550 requires 4 external capacitors for proper operation (C_1 = C_2 = 1µF; C_{IN} = 4.7 µF; C_{OUT} = 2.2 µF). Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20 mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM3550 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM3550. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over −55°C to 125°C; X5R: ±15% over −55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM3550. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, −20%) and vary significantly over temperature (Y5V: +22%, −82% over −30°C to +85°C range; Z5U: +22%, −56% over +10°C to +85°C range). Under some conditions, a nominal 1µF Y5V or Z5U capacitor could have a capacitance of only 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM3550.

The recommended voltage rating for the capacitors is 10V to account for DC bias capacitance losses.

Current Source FET

Choosing the proper current source MOSFET is required to ensure accurate flash current delivery. N-Channel MOSFETs (NFET) with allowed drain-to-source voltages (V_{DS}) greater than 5.5V are required. In order to prevent damage to the current source NFET, special attention must be given to the pulsed-current rating of the MOSFET. The NFET must be sized appropriately to handle the desired flash current and flash duration. Most MOSFET manufacturers provide curves showing the NFET's pulsed performance in the electrical characteristics section of their datasheets. A MOSFET's performance rating at temperature, primarily temperatures greater than 40°C, must also be investigated to ensure NFET does not become thermally damaged during a flash pulse. An NFET possessing low R_{DSON} values helps improve the efficiency of the flash pulse.

ALD/TEMP Components

NTC SELECTION

NTC thermistors have a temperature-to-resistance relationship of:

$$R(T) = R_{25°C} \times e^{\left[\beta\left(\frac{1}{T°C+273} - \frac{1}{298}\right)\right]} \tag{11}$$

where β is given in the thermistor datasheet and $R_{25°C}$ is the thermistor's value at +25°C. R1 in is chosen so that it is equal to:

$$R1 = \frac{V_{TRIP} R_{T(TRIP)}}{(V_{BIAS} - V_{TRIP})} \tag{12}$$

where $R_{T(TRIP)}$ is the thermistors value at the temperature trip point, V_{BIAS} is shown in the Thermistor Resistive Divider Response vs. Temperature graph below, and V_{TRIP} = 800 mV (typ.). Choosing R1 here gives a more linear response around the temperature trip voltage. For example, with V_{BIAS} = 1.8V and a thermistor whose nominal value at +25°C is 100 kΩ and a β = 4500K, the trip point is chosen to be +85°C. The value of R(T) at 85°C is:

$$R(T) = 100\ k\Omega \times e^{\left[\beta\left(\frac{1}{85+273} - \frac{1}{298}\right)\right]} = 7.959\ k\Omega$$

$$R1 \text{ is then: } \frac{0.8V \times 7.959\ k\Omega}{1.8V - 0.8V} = 6.367\ k\Omega \tag{13}$$

Setting the ALD/TEMP Sense High Register to N = 50 or hex 0x32 will place the upper trip point to approx. 800 mV. Voltages higher than 800 mV will prevent the flash LED from turning on. Based on the curve, the Sense Low Register can be set to a lower code to give a second LED current threshold (70% flash). Voltages lower than the value stored in the Sense Low Register will allow a full current flash.

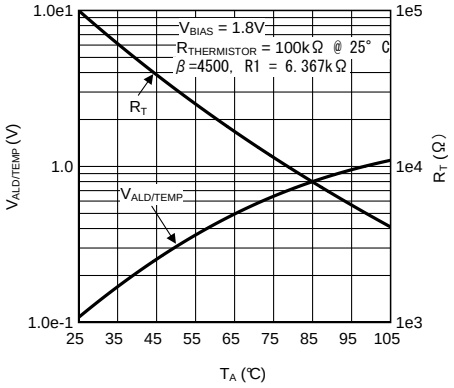


Figure 56. Thermistor Resistive Divider Response vs Temperature

If the temperature changes during a flash event, meaning $V_{ALS/TEMP}$ crosses the Sense High and/or Sense Low values, the current will scale to the appropriate zone current.

The thermistor should be placed as close to the Flash LEDs as possible. This will provide the best thermal coupling (lowest thermal resistance).

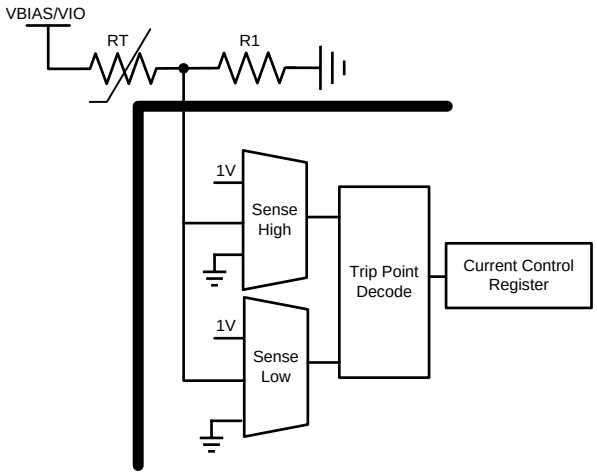
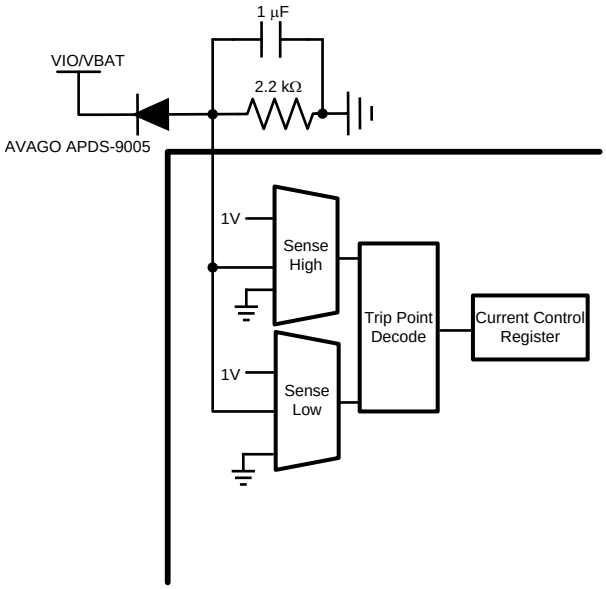


Figure 57. Thermistor Voltage Divider and Sensing Circuit

AMBIENT LIGHT SENSOR

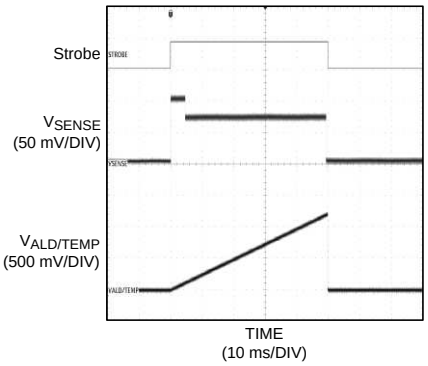
If the ALD/TEMP pin is not used for ambient/LED temperature monitoring, it can be used for ambient light detection. The LM3550 provides three regions of current control based upon ambient conditions. The three regions are defined using the Sense High and Sense Low Registers to set the zone boundaries (user-configurable from 0 to 1V). Most ambient light sensors are reverse-biased diodes that leak current proportional to the amount of ambient light reaching the sensor. This current is then translated into a voltage by using a resistor in series with the light sensor. The voltage-setting resistor will vary based upon the desired ambient detection range and manufacturer.



Default TRIP POINTS

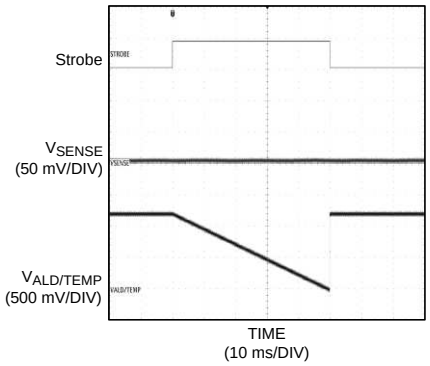
1000 LUX for Bright Ambient (900 mV) (Bright Outdoor Lighting)	No Flash
100 to 1000 LUX for Indoor Ambient (90 mV) (Office Lighting)	70% Full-Scale Flash
0 to 100 LUX for Low Ambient (Night or Movie Theater)	Full-Scale Flash

Most ambient light sensors suggest placing a capacitor in parallel with the voltage-setting resistor in order to help filter the 50/60 Hz. noise generated by fluorescent overhead lighting. This capacitor can range from no capacitor up to 10 µF. The key is to filter the noise so that the peak-to-peak voltage is less than 16 mV (LSB size of the ALD/TEMP Sense High and Sense Low settings). Please refer to the ambient light sensor's datasheet for the recommended capacitor value.



The Flash current drops to 70% of the peak once the voltage on the ALD/TEMP pin exceeds the Sense Low trip point.

Figure 58. Effect of ALD/TEMP Voltage Rising during a Flash



The Flash event is not allowed to start if the voltage on ALD/TEMP is higher that the Sense High Trip point.

Figure 59. Effect of ALD/TEMP Voltage Dropping during a Flash

LAYOUT CONSIDERATIONS

The UQFN is a leadless package with very good thermal properties. This package has an exposed DAP (die attach pad) at the underside center of the package measuring 1.86 mm x 2.2 mm. The main advantage of this exposed DAP is to offer low thermal resistance when soldered to the thermal ground pad on the PCB. For good PCB layout a 1:1 ratio between the package and the PCB thermal land is recommended. To further enhance thermal conductivity, the PCB thermal ground pad may include vias to a 2nd layer ground plane. For more detailed instructions on mounting UQFN packages, please refer to Texas Instruments Application Note AN-1187 (SNOA401).

The proceeding steps must be followed to ensure stable operation and proper current source regulation.

1. Bypass V_{IN} with at least a 4.7 µF ceramic capacitor. Connect the positive terminal of this capacitor as close as possible to V_{IN}.
2. Connect C_{OUT} as close to the VOUT pin as possible with at least a 2.2 µF capacitor.
3. Connect the return terminals of the input capacitor and the output capacitor as close as possible to the exposed DAP and GND pins through low impedance traces.
4. Place the two 1 µF flying capacitors (C1 and C2) as close to the LM3550 C1+/− and C2+/− pins as possible.
5. To minimize losses during the flash pulse, it is recommended that the flash LEDs, the current source NFET, and current-setting resistor be placed as close to the super capacitor as possible.

THERMAL PROTECTION

Internal thermal protection circuitry disables the LM3550 when the junction temperature exceeds 145°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below 125°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	31

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3550SP/NOPB	ACTIVE	UQFN	NHU	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-30 to 85	3550	Samples
LM3550SPX/NOPB	ACTIVE	UQFN	NHU	20	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-30 to 85	3550	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

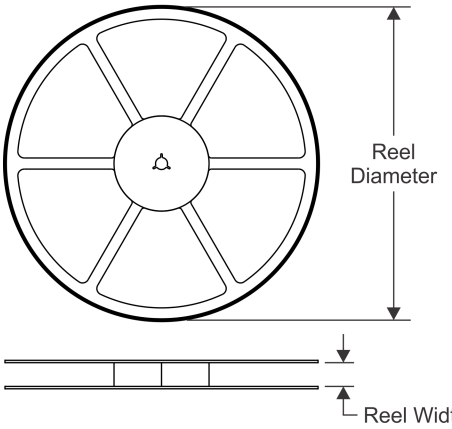
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

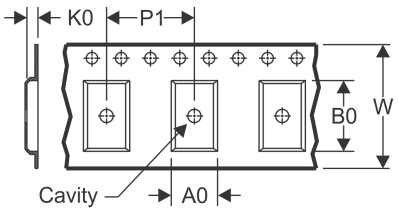
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

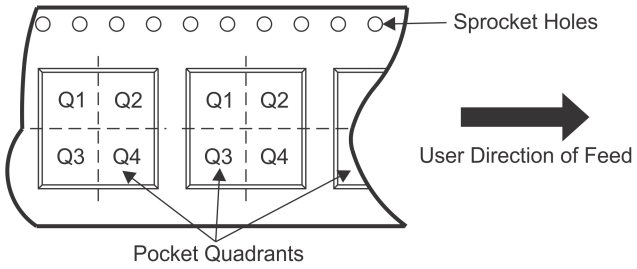


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

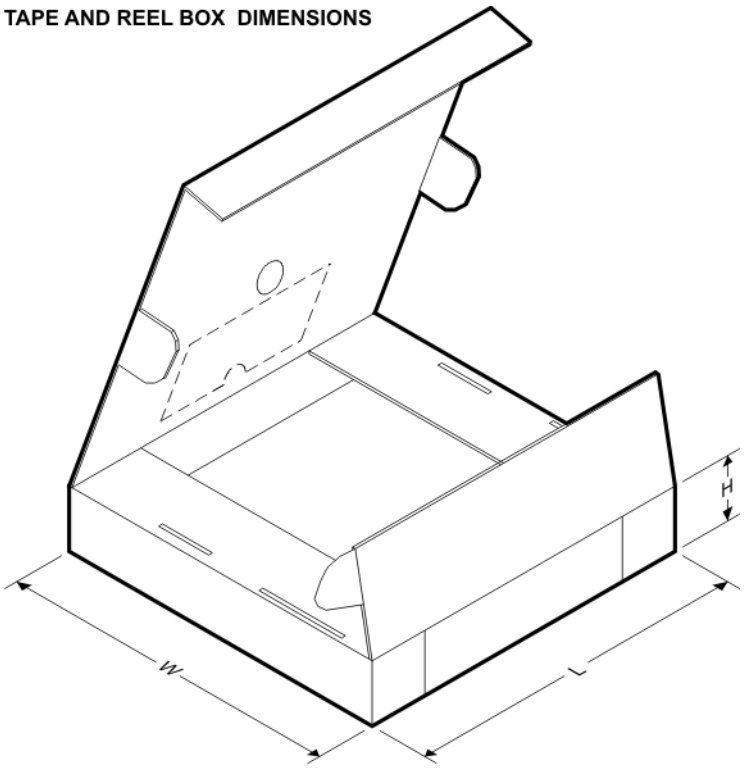
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3550SP/NOPB	UQFN	NHU	20	1000	178.0	12.4	2.7	3.2	0.8	8.0	12.0	Q1
LM3550SPX/NOPB	UQFN	NHU	20	4500	330.0	12.4	2.7	3.2	0.8	8.0	12.0	Q1

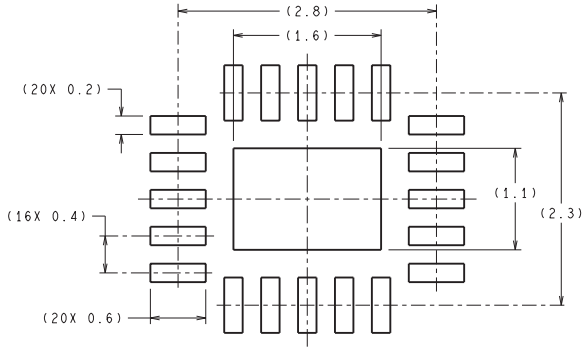
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

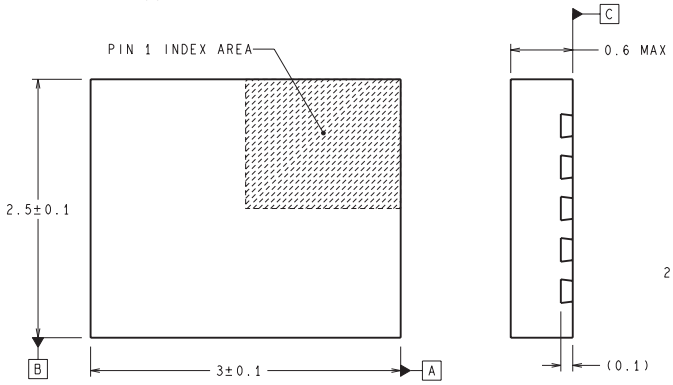
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3550SP/NOPB	UQFN	NHU	20	1000	213.0	191.0	55.0
LM3550SPX/NOPB	UQFN	NHU	20	4500	367.0	367.0	35.0

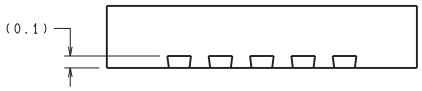
NHU0020A

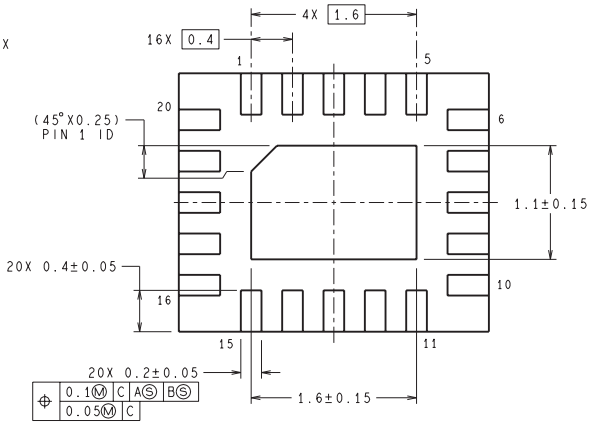


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SPF20A (Rev B)

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