# LM3674 2MHz, 600mA Step-Down DC-DC Converter in SOT-23

**Check for Samples: LM3674**

## FEATURES

- **600mA Max Load Current**
- **Input Voltage Range from 2.7V to 5.5V**
- **Available in Fixed and Adjustable Output Voltages Ranging from 1.0V to 3.3V**
- **Operates from a Single Li-Ion Cell Battery**
- **Internal Synchronous Rectification for High Efficiency**
- **Internal Soft Start**
- **0.01 µA Typical Shutdown Current**
- **2 MHz PWM Fixed Switching Frequency (typ)**
- **5-Pin SOT-23 Package**
- **Current Overload Protection and Thermal Shutdown Protection**

## APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **MP3 Players**
- **Portable Instruments**
- **W-LAN**
- **Digital Still Cameras**
- **Portable Hard Disk Drives**

## DESCRIPTION

The LM3674 step-down DC-DC converter is optimized for powering low voltage circuits from a single Li-Ion cell battery and input voltage rails from 2.7V to 5.5V. It provides up to 600mA load current, over the entire input voltage range. There are several fixed output voltages and adjustable output voltage versions.

The device offers superior features and performance for mobile phones and similar portable systems. During PWM mode, the device operates at a fixed-frequency of 2 MHz (typ). Internal synchronous rectification provides high efficiency during Pulse Width Modulation (PWM) mode operation. In shutdown mode, the device turns off and reduces battery consumption to 0.01 µA (typ).

The LM3674 is available in a 5-pin SOT-23 package in leaded (PB) and lead-free (NO PB) versions. A high switching frequency of 2 MHz (typ) allows use of only three tiny external surface-mount components, an inductor and two ceramic capacitors.

## TYPICAL APPLICATION CIRCUITS

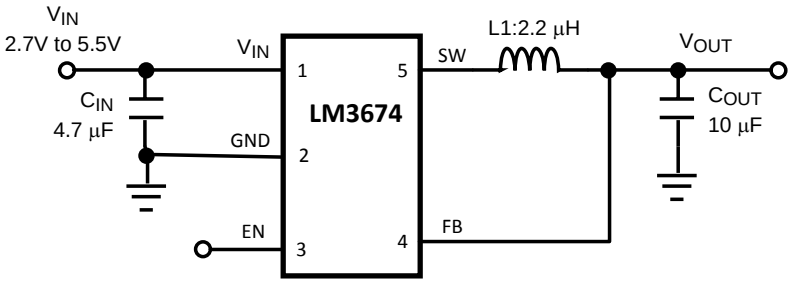



**Figure 1. Typical Application Circuit**

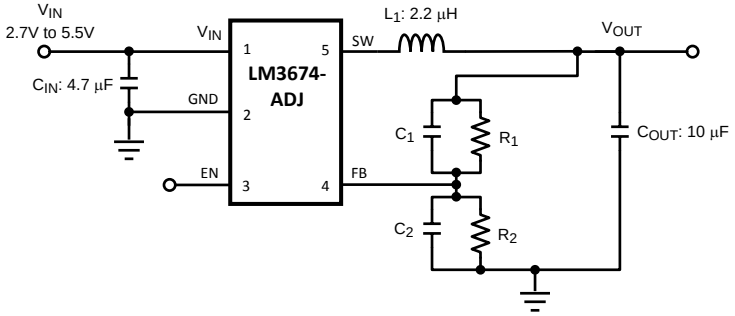



**Figure 2. Typical Application Circuit for Adjustable Voltage Option**

## PIN DIAGRAM

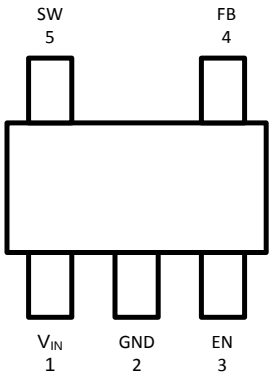



**Figure 3. Top View**
**5-Pin SOT-23 Package**
**See Package Number DBV0005A**

**Note:** The actual physical placement of the package marking will vary from part to part.

## PIN DESCRIPTIONS

| Pin Number | Name | Description |
|---|---|---|
| 1 | $V_{IN}$ | Power supply input. Connect to the input filter capacitor ( Figure 1). |
| 2 | GND | Ground pin. |
| 3 | EN | Enable input. The device is in shutdown mode when voltage to this pin is <0.4V and enable when >1.0V. Do not leave this pin floating. |
| 4 | FB | Feedback analog input. Connect to the output filter capacitor for fixed voltage versions. For adjustable version external resistor dividers are required ( Figure 2). The internal resistor dividers are disabled for the adjustable version. |
| 5 | SW | Switching node connection to the internal PFET switch and NFET synchronous rectifier. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)(2)

| LM3674 (5 Pin SOT-23) | |
|---|---|
| **Ordering Information** | **Voltage Option (V)** |
| LM3674MF-1.2 | 1.2 |
| LM3674MFX-1.2 | |
| LM3674MF-1.2/NOPB | |
| LM3674MFX-1.2/NOPB | |
| LM3674MF-1.5 | 1.5 |
| LM3674MFX-1.5 | |
| LM3674MF-1.5/NOPB | |
| LM3674MFX-1.5/NOPB | |
| LM3674MF-1.6 | 1.6 |
| LM3674MFX-1.6 | |
| LM3674MF-1.6/NOPB | |
| LM3674MFX-1.6/NOPB | |
| LM3674MF-1.8 | 1.8 |
| LM3674MFX-1.8 | |
| LM3674MF-1.8/NOPB | |
| LM3674MFX-1.8/NOPB | |
| LM3674MF-1.875 | 1.875 |
| LM3674MFX-1.875 | |
| LM3674MF-1.875/NOPB | |
| LM3674MFX-1.875/NOPB | |
| LM3674MF-2.8 | 2.8 |
| LM3674MFX-2.8 | |
| LM3674MF-2.8/NOPB | |
| LM3674MFX-2.8/NOPB | |
| LM3674MF-ADJ | Adjustable |
| LM3674MFX-ADJ | |
| LM3674MF-ADJ/NOPB | |
| LM3674MFX-ADJ/NOPB | |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## Absolute Maximum Ratings[1][2]

| | |
|---|---|
| $V_{IN}$ Pin: Voltage to GND | −0.2V to 6.0V |
| EN, FB, SW Pin: | (GND−0.2V) to ($V_{IN}$ + 0.2V) |
| Continuous Power Dissipation[3] | Internally Limited |
| Junction Temperature ($T_{J-MAX}$) | +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Lead Temperature (Soldering, 10 sec.) | 260°C |
| ESD Rating[4] Human Body model: All Pins | 2 kV |
| Machine Model: All Pins | 200V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings may not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) In Applications where high power dissipation and /or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ($T_{J-MAX}$ ), the maximum power dissipation of the device in the application ($P_{D-MAX}$ ) and the junction to ambient thermal resistance of the package ($\theta_{JA}$) in the application, as given by the following equation: $T_{A-MAX} = T_{J-MAX}$- ($\theta_{JA}$ x $P_{D-MAX}$). Refer to Dissipation ration table for $P_{D-MAX}$ values at different ambient temperatures.
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin (MIL-STD-883 3015.7). National Semiconductor recommends that all intergrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling techniques can result in damage.

## Operating Ratings[1][2][3]

| | |
|---|---|
| Input Voltage Range[4] | 2.7V to 5.5V |
| Recommended Load Current | 0A to 600 mA |
| Junction Temperature ($T_J$) Range | −30°C to +125°C |
| Ambient Temperature ($T_A$) Range | −30°C to +85°C |

(1) In Applications where high power dissipation and /or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ($T_{J-MAX}$ ), the maximum power dissipation of the device in the application ($P_{D-MAX}$ ) and the junction to ambient thermal resistance of the package ($\theta_{JA}$) in the application, as given by the following equation: $T_{A-MAX} = T_{J-MAX}$- ($\theta_{JA}$ x $P_{D-MAX}$). Refer to Dissipation ration table for $P_{D-MAX}$ values at different ambient temperatures.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings may not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) All voltages are with respect to the potential at the GND pin.
(4) Input voltage range recommended for ideal applications performance for the specified output voltages are given below
$V_{IN}$ = 2.7V to 5.5V for 1.0V ≤ $V_{OUT}$ < 1.8V
$V_{IN}$ = ( $V_{OUT}$ + $V_{DROP\ OUT}$) to 5.5V for 1.8 ≤ $V_{OUT}$≤ 3.3V Where $V_{DROP\ OUT}$ = $I_{LOAD}$ * ($R_{DSON\ (P)}$ + $R_{INDUCTOR}$)

## Thermal Properties[1]

over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) (SOT-23) for a 2 layer board [2] | 250°C/W |
| Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) (SOT-23) for a 4 layer board [2] | 130°C/W |

(1) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J$ = 150°C (typ.) and disengages at $T_J$ = 130°C
(2) Junction to ambient thermal resistance ($\theta_{JA}$) is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design. Value specified here 250°C/W is based on measurement results using a 2 layer, 4" X 3", 2 oz. Cu board as per JEDEC standards. The $\theta_{JA}$ is 130°C/W if a 4 layer, 4" X 3", 2/1/1/2 oz. Cu board as per JEDEC standards is used.

## Electrical Characteristics (1)(2)(3)

Limits in standard typeface are for $T_J$ = 25°C. Limits in **boldface** type apply over the full operating junction temperature range (−30°C ≤ $T_J$ ≤ 125°C). Unless otherwise noted, specifications apply to the LM3674 with $V_{IN}$ = EN = 3.6V

| Parameter | | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback Voltage (4)(5) | $I_O$ = 10mA | **-4** | | **+4** | % |
| | Line Regulation | 2.7V ≤ $V_{IN}$ ≤ 5.5V<br>$I_O$ = 100 mA | | 0.083 | | %/V |
| | Load Regulation | 100 mA ≤ $I_O$ ≤ 600 mA<br>$V_{IN}$ = 3.6V | | 0.0010 | | %/mA |
| $V_{REF}$ | Internal Reference Voltage | See (6) | | 0.5 | | V |
| $I_{SHDN}$ | Shutdown Supply Current | EN = 0V | | 0.01 | **1** | µA |
| $I_Q$ | DC Bias Current into $V_{IN}$ | No load, device is not switching (FB=0V) | | 300 | **600** | µA |
| $R_{DSON\ (P)}$ | Pin-Pin Resistance for PFET | $I_{SW}$ = 200mA | | 380 | 500 | mΩ |
| $R_{DSON\ (N)}$ | Pin-Pin Resistance for NFET | $I_{SW}$ = 200mA | | 250 | 400 | mΩ |
| $I_{LIM}$ | Switch Peak Current Limit | Open Loop (7) | **830** | 1020 | **1200** | mA |
| $V_{IH}$ | Logic High Input | | **1.0** | | | V |
| $V_{IL}$ | Logic Low Input | | | | **0.4** | V |
| $I_{EN}$ | Enable (EN) Input Current | | | 0.01 | **1** | µA |
| $F_{OSC}$ | Internal Oscillator Frequency | PWM Mode | **1.6** | 2 | **2.6** | MHz |

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested at $V_{IN}$ = 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) ADJ configured to 1.5V output.
(5) For $V_{OUT}$ less than 2.5V, $V_{IN}$ = 3.6V, for $V_{OUT}$ greater than or equal to 2.5V, $V_{IN}$ = $V_{OUT}$ +1.
(6) For the ADJ version the resistor dividers should be selected such that at the desired output voltage, the voltage at the FB pin is 0.5V.
(7) Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB=0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

## Dissipation Rating

over operating free-air temperature range (unless otherwise noted)

| $\theta_{JA}$ | $T_A$ ≤ 25°C (Power Rating) | $T_A$ = 60°C (Power Rating) | $T_A$ = 85°C (Power Rating) |
|---|---|---|---|
| 250°C/W (2 layer board) | 400mW | 260mW | 160mW |
| 130°C/W (4 layer board) | 770mW | 500mW | 310mW |

## Block Diagram

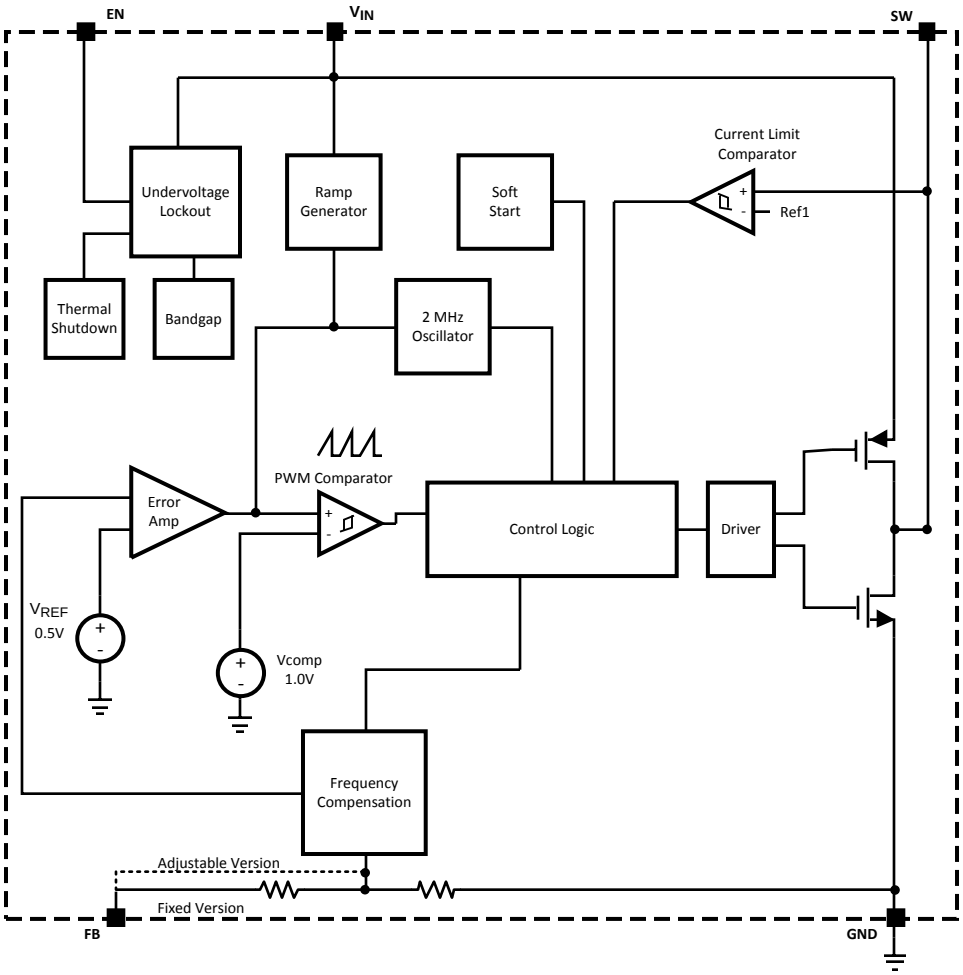



**Figure 4. Simplified Functional Block Diagram**

## Typical Performance Characteristics

(unless otherwise stated: $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.5V, $T_A$ = 25°C)

**Quiescent Current vs. Supply Voltage (FB = 0V, No Switching)**

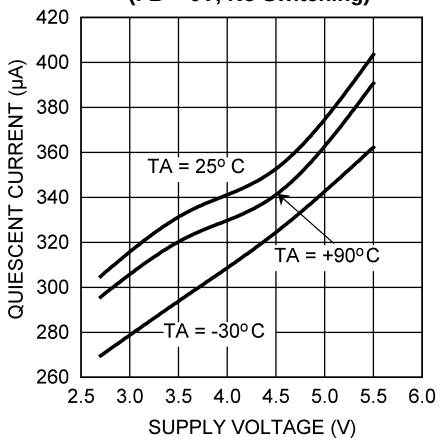



**Figure 5.**

**$I_Q$ Shutdown vs. Temp**

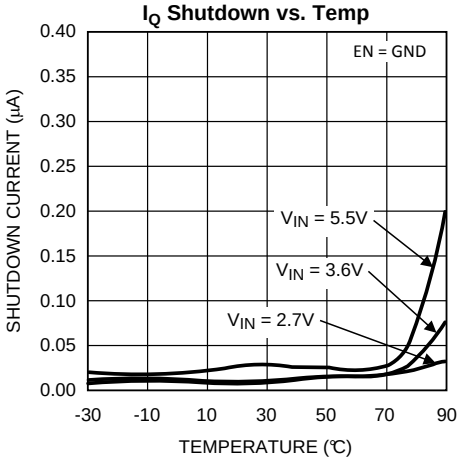



**Figure 6.**

**Feedback Bias Current vs. Temp**

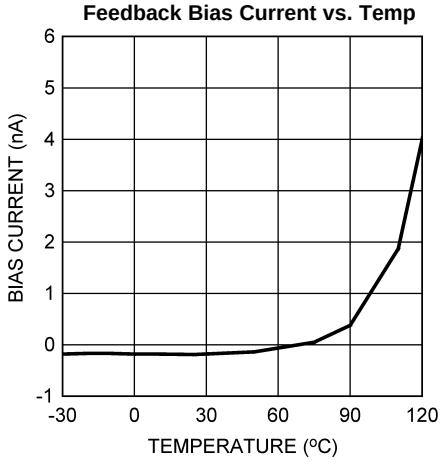



**Figure 7.**

**Output Voltage vs. Supply Voltage**

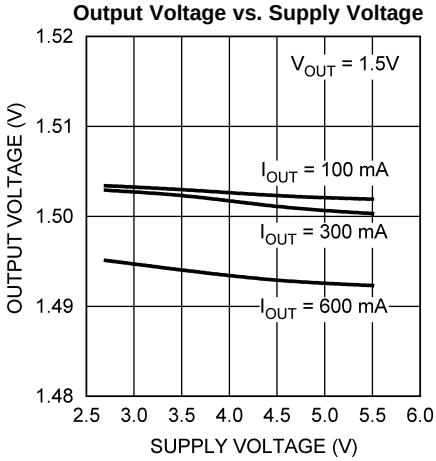



**Figure 8.**

**Output Voltage vs. Temperature**

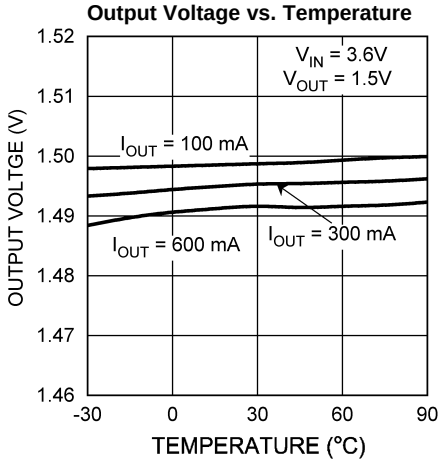



**Figure 9.**

**Output Voltage vs. Output Current**

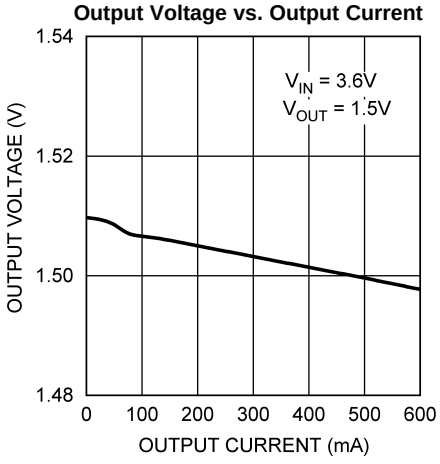



**Figure 10.**

## Typical Performance Characteristics (continued)

(unless otherwise stated: $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.5V, $T_A$ = 25°C)

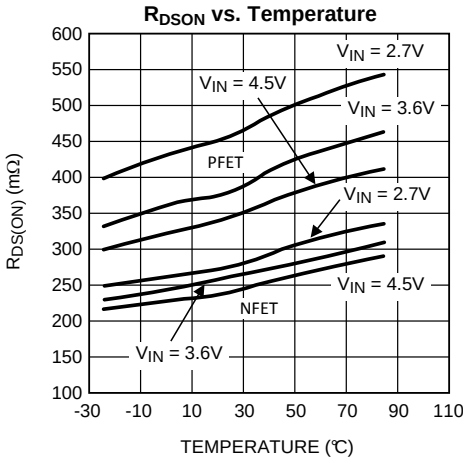



**Figure 11.**

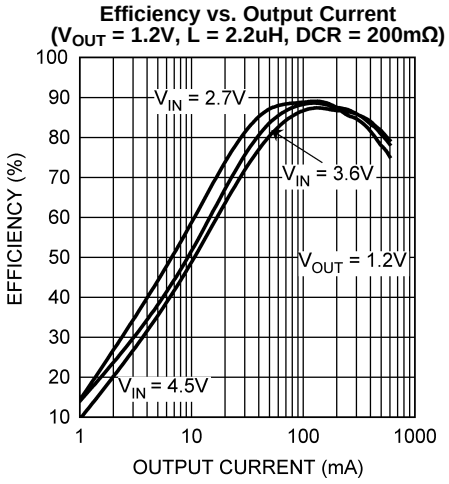



**Figure 12.**

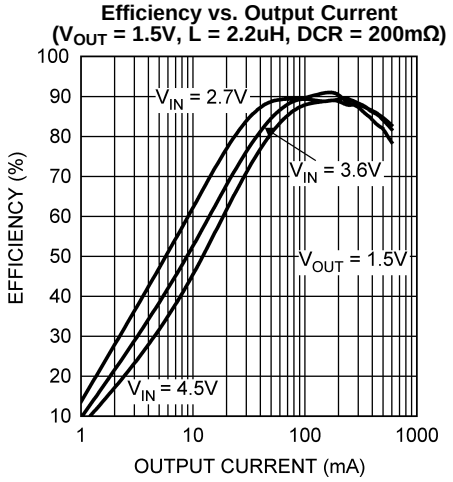



**Figure 13.**

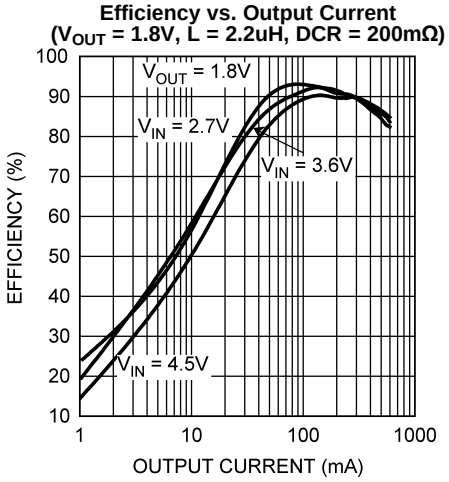



**Figure 14.**

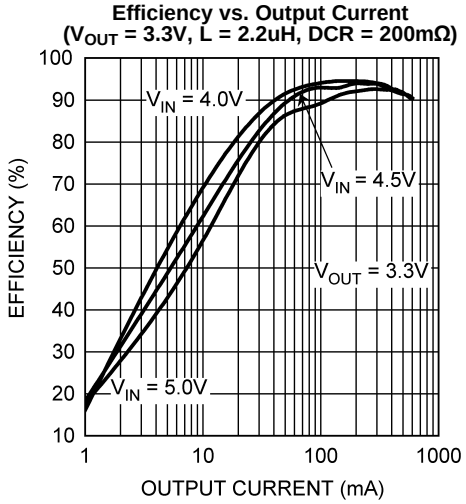



**Figure 15.**

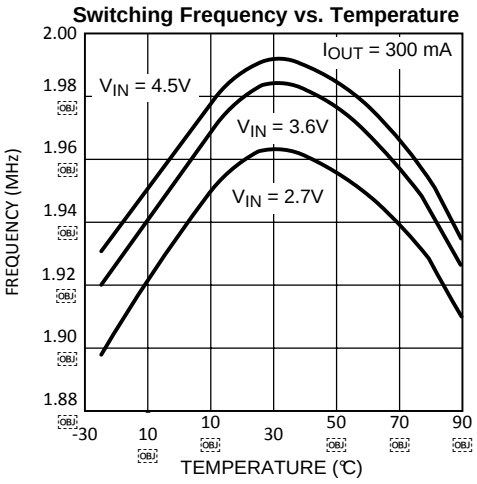



**Figure 16.**

## Typical Performance Characteristics (continued)

(unless otherwise stated: $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.5V, $T_A$ = 25°C)

**Open/Closed Loop Current Limit vs. Temperature**

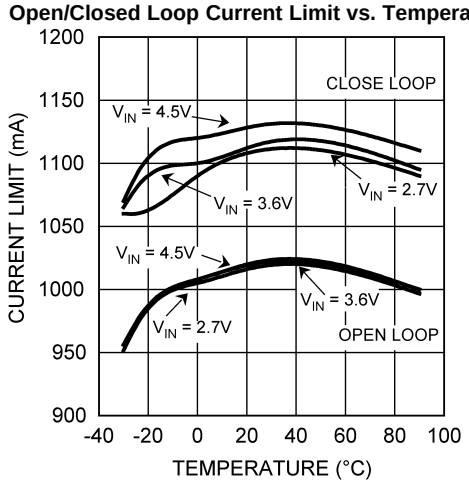



**Figure 17.**

**Line Transient Response**

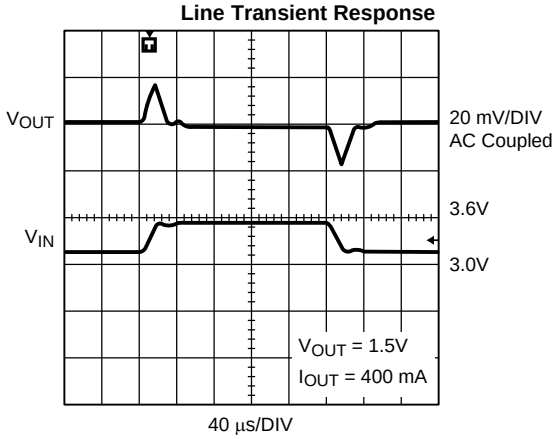



**Figure 18.**

**Load Transient**

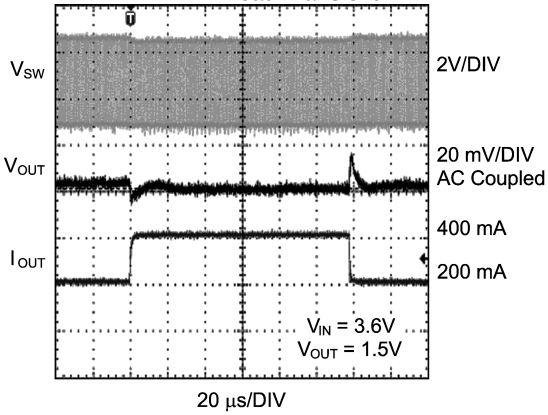



**Figure 19.**

**Start Up (Output Current = 300mA)**

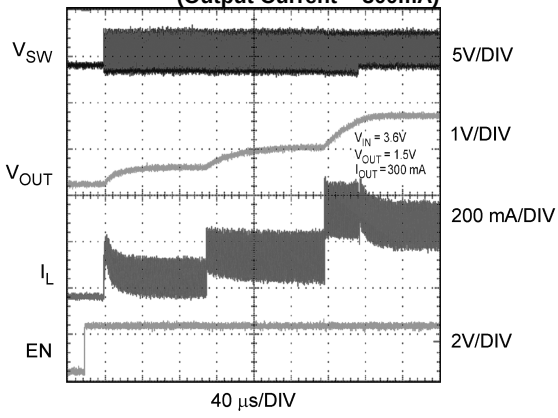



**Figure 20.**

**Start Up (Output Current = 10mA)**

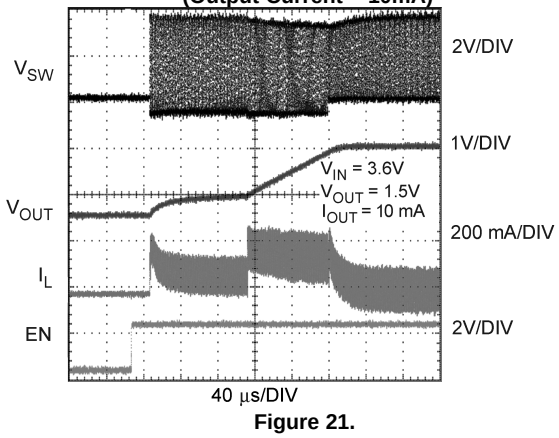



**Figure 21.**

# OPERATION DESCRIPTION

## DEVICE INFORMATION

The LM3674, a high efficiency step down DC-DC switching buck converter, delivers a constant voltage from a single Li-Ion battery and input voltage rails from 2.7V to 5.5V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3674 has the ability to deliver up to 600 mA depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

There are two modes of operation depending on the current required - Pulse Width Modulation (PWM), and shutdown. The device operates in PWM throughout the $I_{OUT}$ range. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.01 µA typ).

Additional features include soft-start, under voltage protection, current overload protection, and thermal overload protection. As shown in Figure 1, only three external power components are required for implementation.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 2.7V or higher.

## CIRCUIT OPERATION

During the first portion of each switching cycle, the control block in the LM3674 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of:

$$\frac{V_{IN}-V_{OUT}}{L} \quad (1)$$

by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of:

$$\frac{-V_{OUT}}{L} \quad (2)$$

The output filter stores charge when the inductor current is high, and releases it when the inductor current is low, smoothing the voltage across the load.

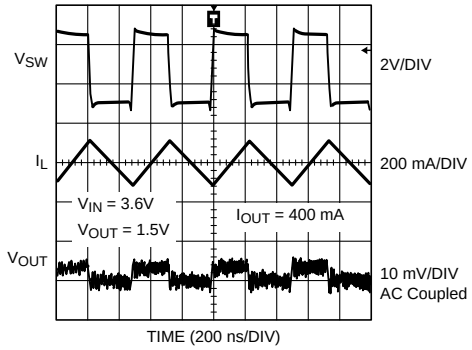
The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

## PWM OPERATION

During Pulse Width Modulation (PWM) operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.




### Internal Synchronous Rectification

While in PWM mode, the LM3674 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

### Current Limiting

A current limit feature allows the LM3674 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1020 mA (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

## SOFT-START

The LM3674 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after Vin reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 70mA, 140mA, 280mA, and 1020mA (typ. switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with 10µF output capacitor and 300mA load current is 350µs and with 10mA load current is 240µs.

## LDO - LOW DROP OUT OPERATION

The LM3674-ADJ can operate at 100% duty cycle (no switching, PMOS switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, the output voltage supply ripple is slightly higher, approximately 25mV.

The minimum input voltage needed to support the output voltage is:

$$V_{IN,MIN} = I_{LOAD} * (R_{DSON\ (P)} + R_{INDUCTOR}) + V_{OUT} \quad (3)$$

| | |
|---|---|
| $I_{LOAD}$ | Load current |
| $R_{DSON\ (P)}$ | Drain to source resistance of PFET switch in the triode region |
| $R_{INDUCTOR}$ | Inductor resistance |

## APPLICATION INFORMATION

### OUTPUT VOLTAGE SELECTION FOR ADJUSTABLE (LM3674-ADJ)

The output voltage of the adjustable parts can be programmed through the resistor network connected from $V_{OUT}$ to FB then to GND. $V_{OUT}$ will be adjusted to make FB equal to 0.5V. The resistor from FB to GND (R2) should be 200 kΩ to keep the current drawn through this network small but large enough that it is not susceptible to noise. If $R_2$ is 200KΩ, and given the $V_{FB}$ is 0.5V, then the current through the resistor feedback network will be 2.5µA. The output voltage formula is:

$$V_{OUT} = V_{FB} * (\frac{R_1}{R_2} + 1) \quad (4)$$

- $V_{OUT}$ = Output Voltage (V)
- $V_{FB}$ = Feedback Voltage (0.5V typ)
- $R_1$ = Resistor from $V_{OUT}$ to FB (Ω)
- $R_2$ = Resistor from FB to GND (Ω)

For any output voltage greater than or equal to 1.0V a frequency zero must be added at 45KHz for stability. The formula is:

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times 45\ kHz} \quad (5)$$

For output voltages greater than or equal to 2.5V, a pole must also be placed at 45KHz as well. If the pole and zero are at the same frequency the formula for calculation of C2 is:

$$C_2 = \frac{1}{2 \times \pi \times R_2 \times 45\ kHz} \quad (6)$$

The formula for location of zero and pole frequency created by adding C1,C2 are given below. It can be seen that by adding C1, a zero as well as a higher frequency pole is introduced.

$$Fz = \frac{1}{(2 * \pi * R1 * C1)} \quad Fp = \frac{1}{2 * \pi * (R1 \| R2) * (C1+C2)} \quad (7)$$

See the LM3674-ADJ Configurations for Various $V_{OUT}$ table. Table 1

**Table 1. Adjustable LM3674 Configurations for Various $V_{OUT}$**

| VOUT (V) | R1 (KΩ) | R2 (KΩ) | C1 (pF) | C2 (pF) | L (µH) | CIN (µF) | COUT (µF) |
|---|---|---|---|---|---|---|---|
| 1.0 | 200 | 200 | 18 | None | 2.2 | 4.7 | 10 |
| 1.1 | 191 | 158 | 18 | None | 2.2 | 4.7 | 10 |
| 1.2 | 280 | 200 | 12 | None | 2.2 | 4.7 | 10 |
| 1.5 | 357 | 178 | 10 | None | 2.2 | 4.7 | 10 |
| 1.6 | 442 | 200 | 8.2 | None | 2.2 | 4.7 | 10 |
| 1.7 | 432 | 178 | 8.2 | None | 2.2 | 4.7 | 10 |
| 1.8 | 464 | 178 | 8.2 | None | 2.2 | 4.7 | 10 |
| 1.875 | 523 | 191 | 6.8 | None | 2.2 | 4.7 | 10 |
| 2.5 | 402 | 100 | 8.2 | None | 2.2 | 4.7 | 10 |
| 2.8 | 464 | 100 | 8.2 | 33 | 2.2 | 4.7 | 10 |
| 3.3 | 562 | 100 | 6.8 | 33 | 2.2 | 4.7 | 10 |

## INDUCTOR SELECTION

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. **The minimum value of inductance to ensure good performance is 1.76µH at $I_{LIM}$ (typ) dc current over the ambient temperature range.** Shielded inductors radiate less noise and should be preferred.

There are two methods to choose the inductor saturation current rating.

### Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE} \quad (8)$$

$$\text{where} \quad I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}\right) \tag{9}$$

- $I_{Ripple}$ : average to peak inductor current
- $I_{outmax}$: maximum load current (600mA)
- $V_{IN}$: maximum input voltage in application
- L: min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f: minimum switching frequency (1.6 MHz)
- $V_{OUT}$: output voltage

**Method 2:**

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the max current limit of 1200 mA.

A 2.2 µH inductor with a saturation current rating of at least 1200 mA is recommended for most applications. The inductor's resistance should be less than around 0.3Ω for good efficiency. Table 2 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

**Table 2. Suggested Inductors and Their Suppliers**

| Model | Vendor | Dimensions LxWxH (mm) | D.C.R (max) |
|---|---|---|---|
| DO3314-222MX | Coilcraft | 3.3 x 3.3 x 1.4 | 200 mΩ |
| LPO3310-222MX | Coilcraft | 3.3 x 3.3 x 1.0 | 150 mΩ |
| ELL5GM2R2N | Panasonic | 5.2 x 5.2 x 1.5 | 53 mΩ |
| CDRH2D14NP-2R2NC | Sumida | 3.2 x 3.2 x 1.55 | 94 mΩ |

## INPUT CAPACITOR SELECTION

A ceramic input capacitor of 4.7 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the $V_{IN}$ pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. **The minimum input capacitance to ensure good performance is 2.2µF at 3V dc bias; 1.5µF at 5V dc bias including tolerances and over ambient temperature range.** The input filter capacitor supplies current to the PFET switch of the LM3674 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f \times I_{OUTMAX} \times V_{IN}} \qquad \text{The worst case is when } V_{IN} = 2 \times V_{OUT} \tag{10}$$

## OUTPUT CAPACITOR SELECTION

A ceramic output capacitor of 10 µF, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

**The minimum output capacitance to ensure good performance is 5.75µF at 1.8V dc bias including tolerances and over ambient temperature range.** The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the $R_{ESR}$ and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follow:

$$V_{PP-C} = \frac{I_{ripple}}{f \times 4 \times C} \quad (11)$$

Voltage peak-to-peak ripple due to ESR =

$$V_{OUT} = V_{PP-ESR} = I_{PP} * R_{ESR} \quad (12)$$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared =

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2} \quad (13)$$

Note that the output ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor ($R_{ESR}$).

The $R_{ESR}$ is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

**Table 3. Suggested Capacitors and Their Suppliers**

| Model | Type | Vendor | Voltage Rating | Case size inch (mm) |
|---|---|---|---|---|
| **10 µF for $C_{OUT}$** | | | | |
| GRM21BR60J106K | Ceramic, X5R | Murata | 6.3V | 0805 (2012) |
| C2012X5R0J106K | Ceramic, X5R | TDK | 6.3V | 0805 (2012) |
| JMK212BJ106K | Ceramic, X5R | Taiyo-Yuden | 6.3V | 0805 (2012) |
| **4.7 µF for $C_{IN}$** | | | | |
| GRM21BR60J475K | Ceramic, X5R | Murata | 6.3V | 0805 (2012) |
| JMK212BJ475K | Ceramic, X5R | Taiyo-Yuden | 6.3V | 0805 (2012) |
| C2012X5R0J475K | Ceramic, X5R | TDK | 6.3V | 0805 (2012) |

## BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

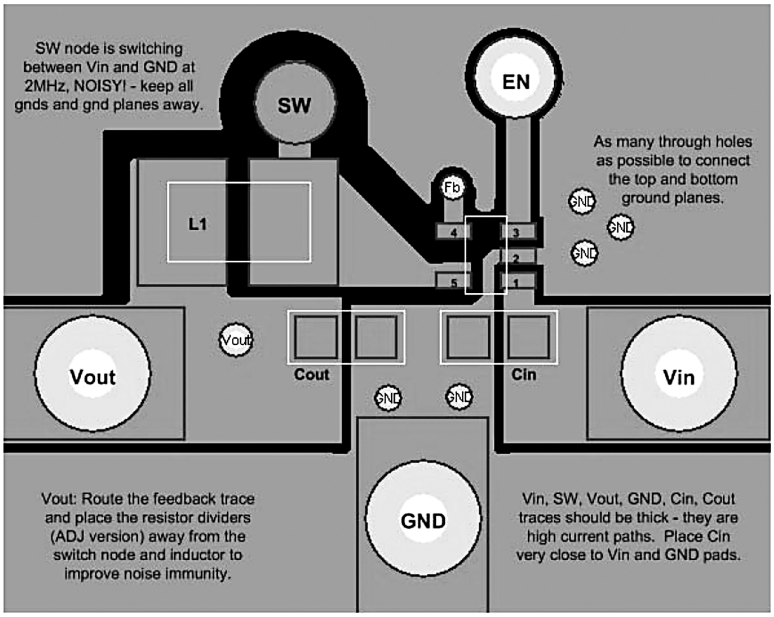



**Figure 22. Board Layout Design Rules for the LM3674**

Good layout for the LM3674 can be implemented by following a few simple design rules, as illustrated in .

1. *Place the LM3674, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must by given to place the input filter capacitor very close to the $V_{IN}$ and GND pin.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor, through the LM3674 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3674 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the LM3674, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3674 by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3674 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

## REVISION HISTORY

| Changes from Revision E (April 2013) to Revision F | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 15 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3674MF-1.2 | NRND | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -30 to 85 | SLRB | |
| LM3674MF-1.2/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLRB | Samples |
| LM3674MF-1.5/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLSB | Samples |
| LM3674MF-1.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLHB | Samples |
| LM3674MF-1.875/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SNNB | Samples |
| LM3674MF-2.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLZB | Samples |
| LM3674MF-ADJ | NRND | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -30 to 85 | SLTB | |
| LM3674MF-ADJ/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLTB | Samples |
| LM3674MFX-1.2/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLRB | Samples |
| LM3674MFX-1.5/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLSB | Samples |
| LM3674MFX-1.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLHB | Samples |
| LM3674MFX-1.875/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SNNB | Samples |
| LM3674MFX-2.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLZB | Samples |
| LM3674MFX-ADJ/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -30 to 85 | SLTB | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

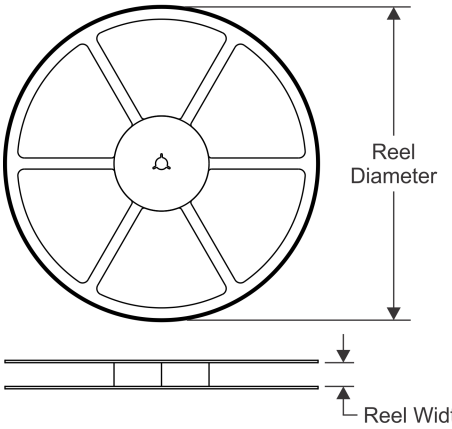
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

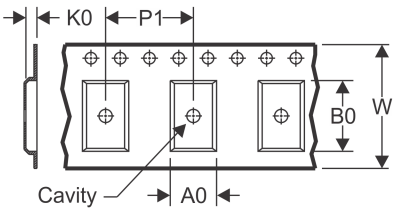
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

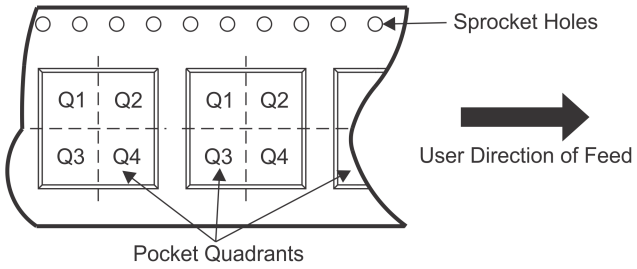



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

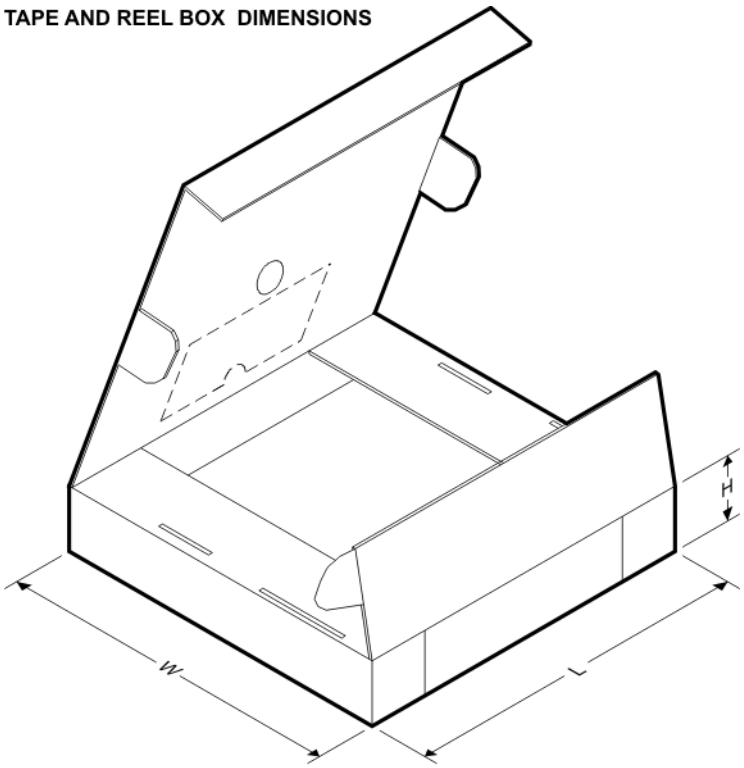
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3674MF-1.2 | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MF-1.2/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MF-1.5/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MF-1.8/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MF-1.875/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MF-2.8/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MF-ADJ | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MF-ADJ/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MFX-1.2/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MFX-1.5/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MFX-1.8/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MFX-1.875/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MFX-2.8/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LM3674MFX-ADJ/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

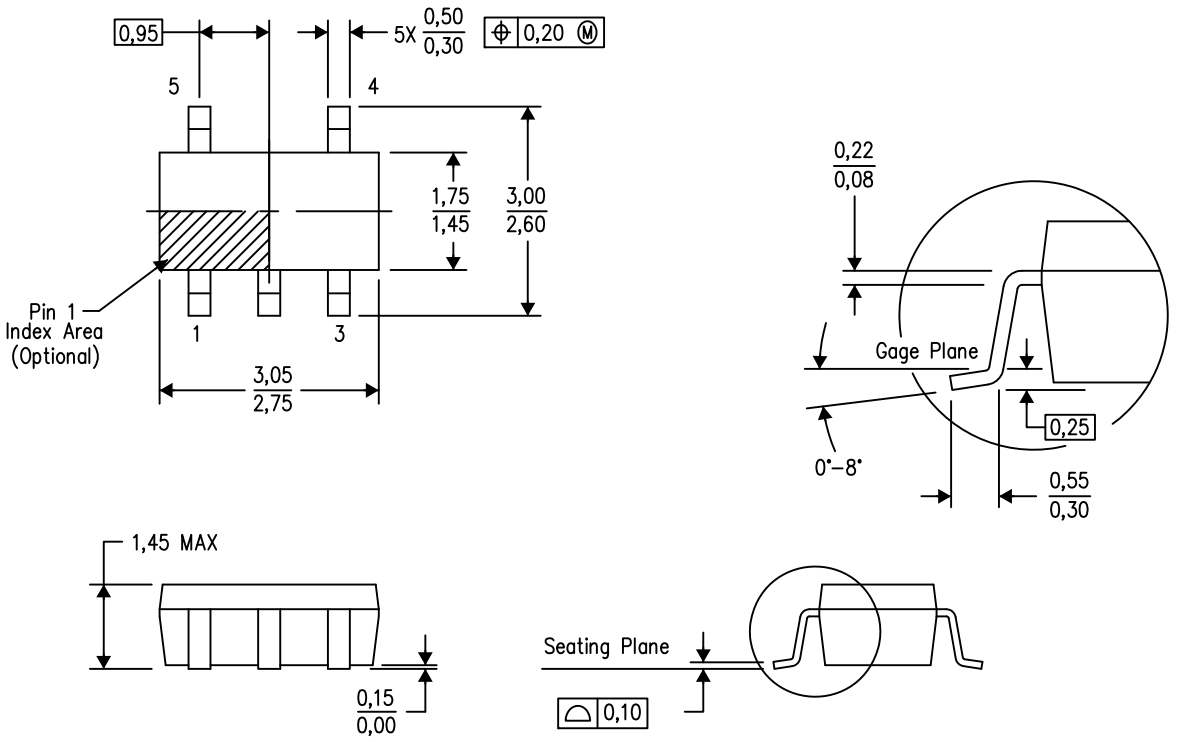
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM3674MF-1.2 | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MF-1.2/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MF-1.5/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MF-1.8/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MF-1.875/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MF-2.8/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MF-ADJ | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MF-ADJ/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LM3674MFX-1.2/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LM3674MFX-1.5/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LM3674MFX-1.8/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LM3674MFX-1.875/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LM3674MFX-2.8/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LM3674MFX-ADJ/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

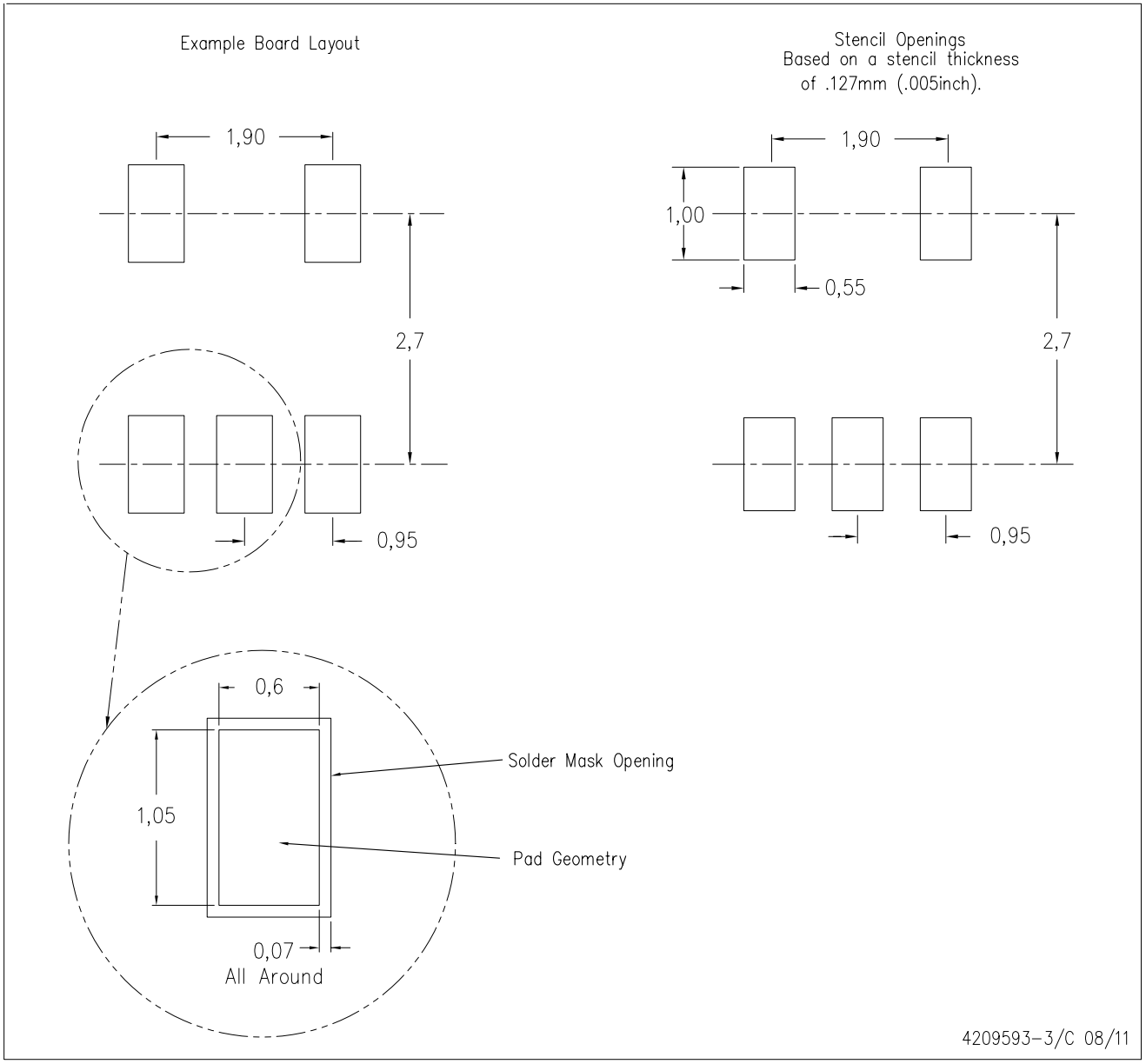
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/L 08/2013

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

## IMPORTANT NOTICE

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