LM3708/LM3709 Microprocessor Supervisory Circuits with Low Line Output, Manual Reset and Watchdog Timer

Check for Samples: LM3708, LM3709

FEATURES

- **Standard Reset Threshold Voltage: 3.08V**
- **Custom Reset Threshold Voltages: For Other Voltages between 2.2V and 5.0V in 10mV Increments, Contact TI.**
- **No External Components Required**
- **Manual-Reset Input**
- **$\overline{\text{RESET}}$ (LM3708) or RESET (LM3709) Outputs**
- **Precision Supply Voltage Monitor**
- **Factory Programmable Reset and Watchdog Timeout Delays**
- **Available in DSBGA Package for Minimum Footprint**
- **±0.5% Reset Threshold Accuracy at Room Temperature**
- **±2% Reset Threshold Accuracy Over Temperature Extremes**
- **Reset Assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ Option Only)**
- **28 µA V_{CC} Supply Current**

APPLICATIONS

- **Embedded Controllers and Processors**
- **Intelligent Instruments**
- **Automotive Systems**
- **Critical µP Power Monitoring**

DESCRIPTION

The LM3708/LM3709 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3708/LM3709 series are available in a 9-bump DSBGA package.

Built-in features include the following:

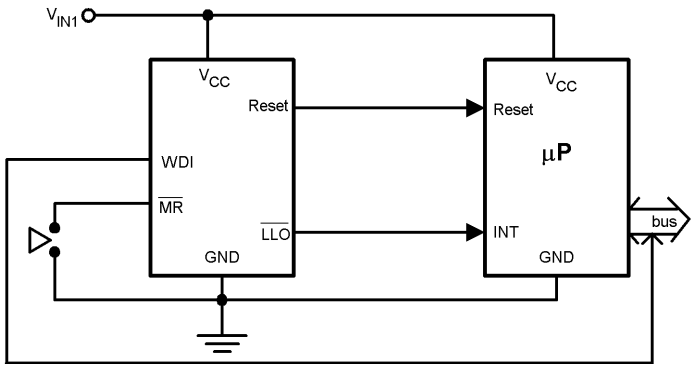
Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is specified down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Watchdog Timer: The WDI (Watchdog Input) monitors one of the µP's output lines for activity. If no output transition occurs during the watchdog timeout period, reset is activated.

Typical Application



Connection Diagram

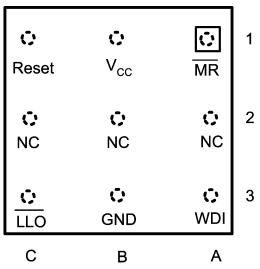


Figure 1. Top View
(looking from the coating side)
DSBGA 9 Bump Package
BPA09

PIN DESCRIPTIONS

Bump No.	Name	Function
A1	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
B1	V_{CC}	Power Supply input.
C1	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3708 only).
	RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3709 only).
C3	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
B3	GND	Ground reference for all signals.
A3	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), reset is engaged.
A2, C2	NC	No Connect.
B2	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram

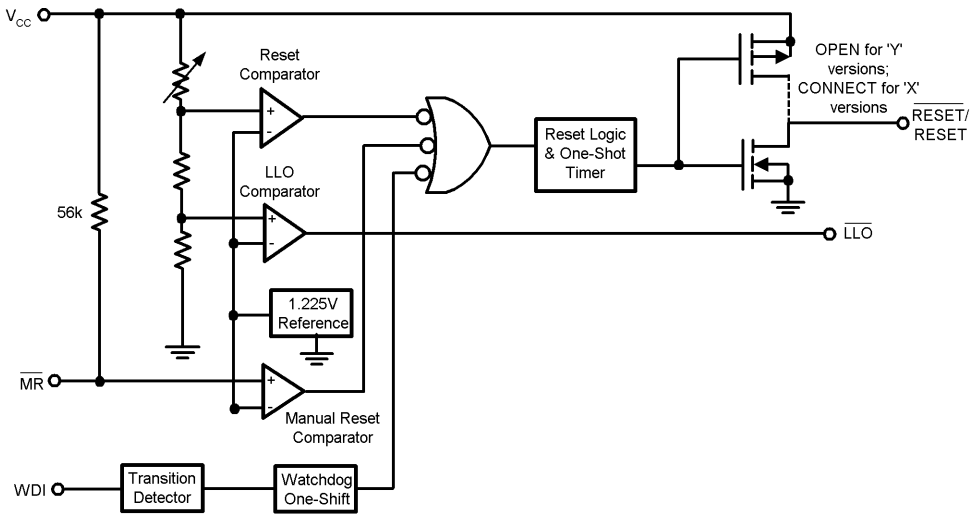


Table 1. Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Watchdog Timeout Period	Manual Reset	Low Line Output
LM3708	x		X, Y(1)	Customized	Customized	x	x
LM3709		x	X	Customized	Customized	x	x

(1) = available upon request. Contact TI

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{CC})		−0.3V to 6.0V
All Other Inputs		−0.3V to V_{CC} + 0.3V
ESD Ratings(3)	Human Body Model	1.5kV
	Machine Model	150V
Power Dissipation		See(4)

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

(3) The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

(4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperture is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of θ_{J-A} for the DSBGA package is 220°C/W.

OPERATING RATINGS(1)

Temperature Range	−40°C ≤ T_J ≤ 85°C

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

LM3708/LM3709 SERIES ELECTRICAL CHARACTERISTICS

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range: V_{CC}	LM3708	**1.0**		**5.5**	V
		LM3709	**1.2**		**5.5**	
I_{CC}	V_{CC} Supply Current	All inputs = V_{CC}; all outputs floating		28	**50**	µA
RESET THRESHOLD						
V_{RST}	Reset Threshold	V_{CC} falling	−0.5 **−2**	V_{RST}	+0.5 **+2**	%
		V_{CC} falling: T_A = 0°C to 70°C	**−1.5**		**+1.5**	
V_{RSTH}	Reset Threshold Hysteresis			0.0032•V_{RST}		mV
t_{RP}	Reset Timeout Period	Reset Timeout Period = E, J, N, S Reset Timeout Period = F, K, P, T Reset Timeout Period = G, L, Q, U Reset Timeout Period = H, M, R, V	**1** **20** **140** **1120**	1.4 28 200 1600	**2** **40** **280** **2240**	ms
t_{RD}	V_{CC} to Reset Delay	V_{CC} falling at 1mV/µs		20		µs
RESET (LM3709)						
V_{OL}	RESET	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	RESET	V_{CC} > 1.2V, I_{SOURCE} = 50µA	**0.8 V_{CC}**			V
		V_{CC} > 1.8V, I_{SOURCE} = 150µA	**0.8 V_{CC}**			
		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
I_{LKG}	Output Leakage Current	V_{RESET} = 5.5V			**1.0**	µA
$\overline{\text{RESET}}$ (LM3708)						
V_{OL}	$\overline{\text{RESET}}$	V_{CC} > 1.0V, I_{SINK} = 50µA			**0.3**	V
		V_{CC} > 1.2V, I_{SINK} = 100µA			**0.3**	
		V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	$\overline{\text{RESET}}$	V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
WDI						
WDI	Watchdog Input Current		**−1**		**+1**	µA
WDI_T	Watchdog Input Threshold		**0.2•V_{CC}**	1.225	**0.8•V_{CC}**	V
t_{WD}	Watchdog Timeout Period	Watchdog Timeout Period = E, F, G, H Watchdog Timeout Period = J, K, L, M Watchdog Timeout Period = N, P, Q, R Watchdog Timeout Period = S, T, U, V	**4.3** **71** **1120** **17900**	6.2 102 1600 25600	**9.3** **153** **2400** **38400**	ms

LM3708/LM3709 SERIES ELECTRICAL CHARACTERISTICS (continued)

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\overline{MR}$						
V_{MRT}	$\overline{MR}$ Input Threshold	$\overline{MR}$, Low			**0.8**	V
		$\overline{MR}$, High	**2.0**			
V_{MRTH}	$\overline{MR}$ Threshold Hysteresis	$\overline{MR}$ falling: V_{CC} = $V_{RST\ MAX}$ to 5.5V		0.0032•V_{RST}		mV
R_{MR}	$\overline{MR}$ Pull-up Resistance		**35**	56	**75**	kΩ
t_{MD}	$\overline{MR}$ to Reset Delay			12		µS
t_{MR}	$\overline{MR}$ Pulse Width		**25**			µS
$\overline{LLO}$						
V_{OL}	$\overline{LLO}$ Output Voltage	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
$\overline{LLO}$ OUTPUT						
V_{LLOT}	$\overline{LLO}$ Output Threshold ($V_{\overline{LLO}}$ − V_{RST}, V_{CC} falling)		**1.01•V_{RST}**	1.02•V_{RST}	**1.03•V_{RST}**	V
V_{LLOTH}	Low-Line Comparator Hysteresis			0.0032•V_{RST}		mV
t_{CD}	Low-Line Comparator Delay	V_{CC} falling at 1mV/µs		20		µs

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage

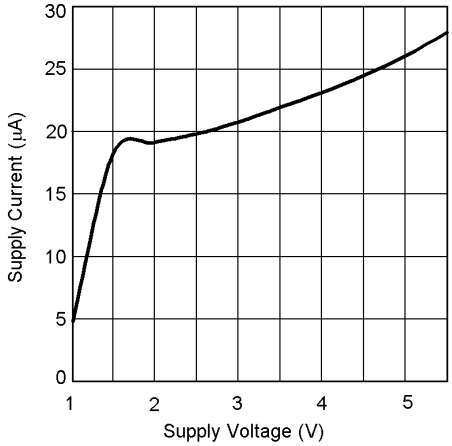


Figure 2.

3.3V Supply Current vs Temperature

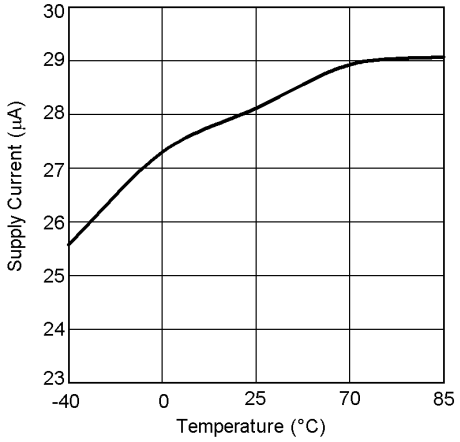


Figure 3.

Normalized Reset Threshold Voltage vs Temperature

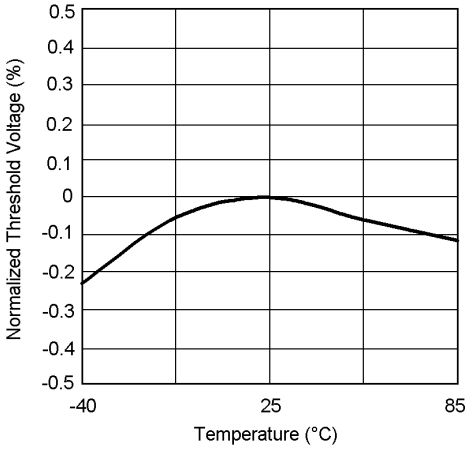


Figure 4.

Reset Timeout Period vs V_{CC}

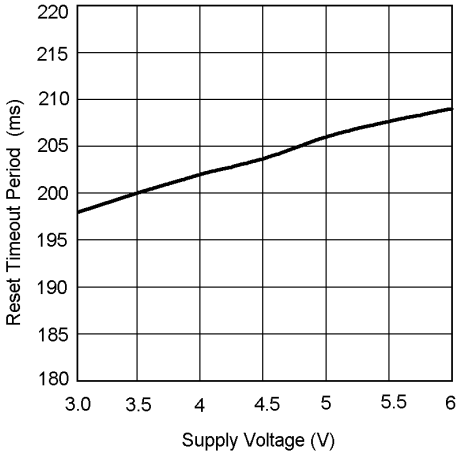


Figure 5.

Reset Timeout Period vs Temperature

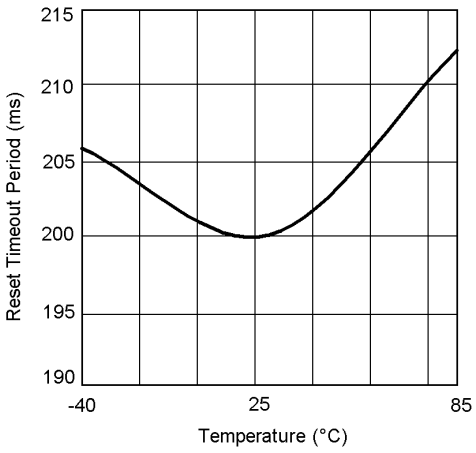


Figure 6.

Max. Transient Duration vs Reset Comparator Overdrive (V_{CC} = 3.3V)

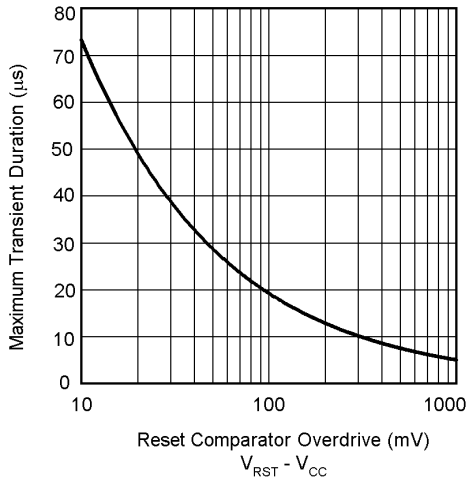


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Watchdog Timeout Period vs Temperature (t_{WD} programmed as 6.2ms)

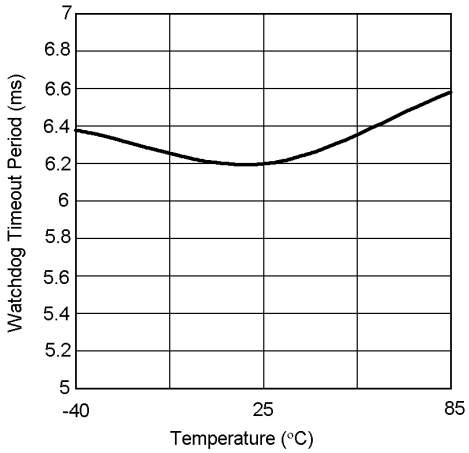


Figure 8.

Low-Line Comparator Propagation Delay vs Temperature

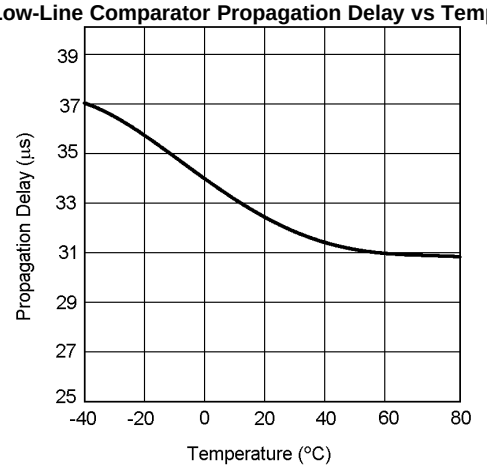


Figure 9.

CIRCUIT INFORMATION

Reset Output

The Reset input of a µP initializes the device into a known state. The LM3708/LM3709 microprocessor supervisory circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is ensured valid for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM3708 offers an active-low $\overline{\text{RESET}}$; The LM3709 offers an active-high RESET.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input ($\overline{\text{MR}}$) will initiate a forced reset also. See the Manual Reset Input ($\overline{\text{MR}}$) section.

Reset Threshold

The LM3708/LM3709 family is available with a reset voltage of 3.08V. Other reset thresholds in the 2.20V to 5.0V range, in steps of 10 mV, are available; contact TI for details.

Manual Reset Input ($\overline{\text{MR}}$)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{\text{MR}}$ input is fully debounced and provides an internal 56 kΩ pull-up. When the $\overline{\text{MR}}$ input is pulled below V_{MRT} (1.225V) for more than 25 µs, reset is asserted after a typical delay of 12 µs. Reset remains active as long as $\overline{\text{MR}}$ is held low, and releases after the reset timeout period expires after $\overline{\text{MR}}$ rises above V_{MRT}. Use $\overline{\text{MR}}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

Low-Line Output ($\overline{\text{LLO}}$)

The low-line output comparator is typically used to provide a non-maskable interrupt to a µP when V_{CC} begins falling. $\overline{\text{LLO}}$ monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically 1.02 • V_{RST}) with hysteresis of 0.0032 • V_{RST}.

Watchdog Timer Input (WDI)

The watchdog timer input monitors one of the microprocessor's output lines for activity. Each time a transition occurs on this monitored line, the watchdog counter is reset. However, if no transition occurs and the timeout period is reached, the LM3708/LM3709 assumes that the microprocessor has locked up and the reset output is activated.

WDI is a high impedance input.

Special Precautions for the DSBGA Package

As with most integrated circuits, the LM3708 and LM3709 are sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the DSBGA package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

DSBGA Mounting

The DSBGA package requires specific mounting techniques which are detailed in TI Application Note AN-1112. Referring to the section ***Surface Mount Technology (SMT) Assembly Considerations***, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

Timing Diagrams

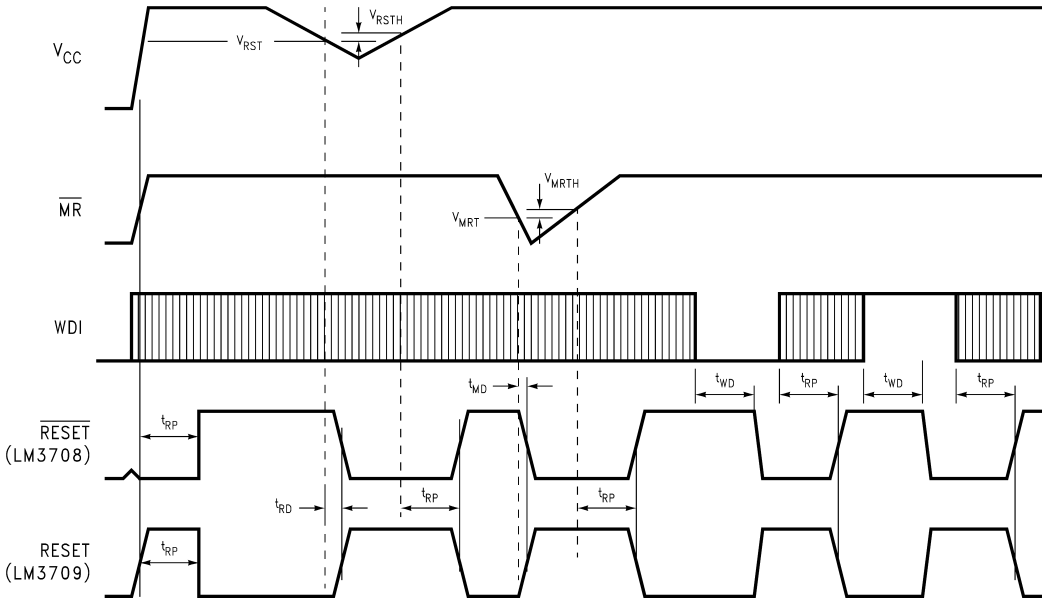


Figure 10. LM3708 Reset Time with $\overline{MR}$ and WDI

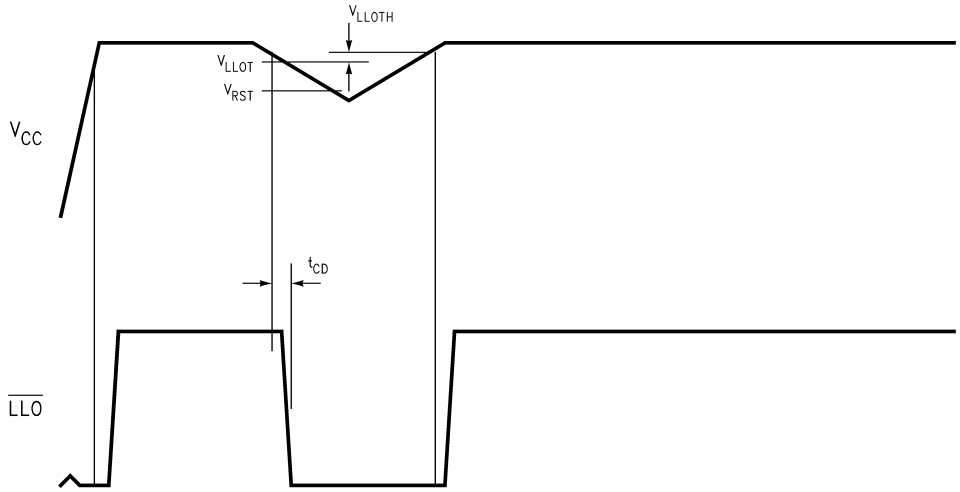


Figure 11. $\overline{LLO}$ Output

Typical Application Circuit

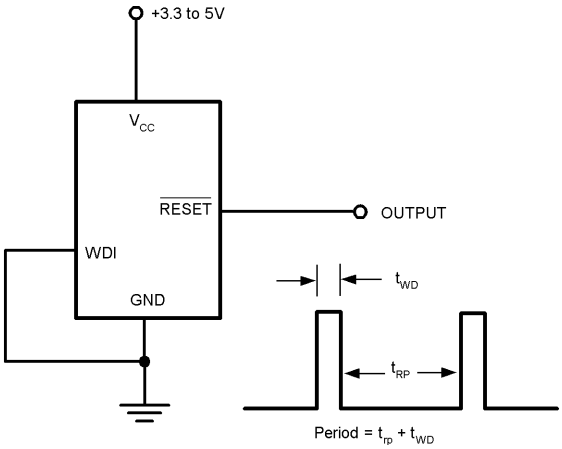


Figure 12. Long Delay Timer/Oscillator

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 10

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