LM5050-1/LM5050-1-Q1 High Side OR-ing FET Controller

Check for Samples: LM5050-1, LM5050-1-Q1

FEATURES

- **Available in Standard and AEC-Q100 Qualified Versions LM5050Q0MK-1 (up to 150°C T_J) and LM5050Q1MK-1 (up to 125°C T_J)**
- **Wide Operating Input Voltage Range, V_{IN}: 5V to 75V**
- **+100 Volt Transient Capability**
- **Charge Pump Gate Driver for External N-Channel MOSFET**
- **Fast 50ns Response to Current Reversal**
- **2A Peak Gate Turn-Off Current**
- **Minimum V_{DS} Clamp for Faster Turn-Off**
- **Package: SOT-6 (Thin SOT-23-6)**

APPLICATIONS

- **Active OR-ing of Redundant (N+1) Power Supplies**

DESCRIPTION

The LM5050-1 High Side OR-ing FET Controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

The LM5050-1 controller provides charge pump gate drive for an external N-Channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5050-1 can connect power supplies ranging from +5V to +75V and can withstand transients up to +100V.

Typical Application Circuits

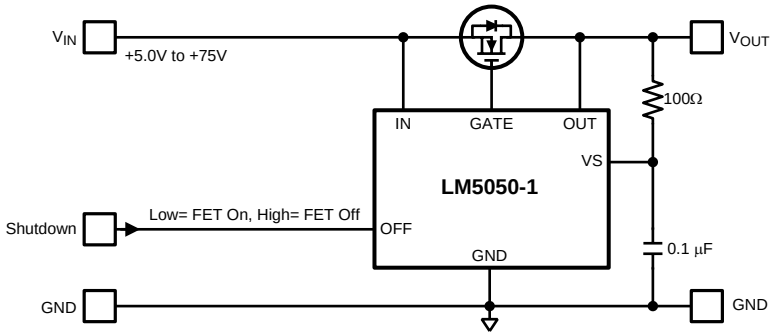

Figure 1. Full Application

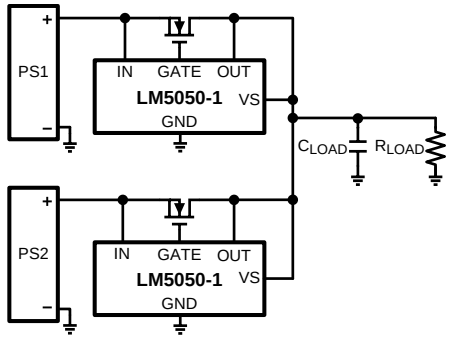

Figure 2. Typical Redundant Supply Configuration

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Connection Diagram

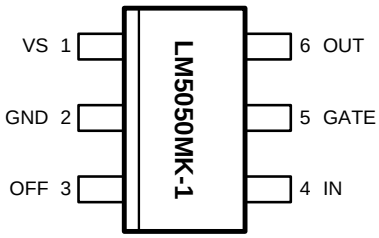

Figure 3. LM5050MK-1
Top View
SOT-6 Package
Package Number DDC0006A

PIN DESCRIPTIONS

Pin No.	Name	Function
1	VS	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either V_{OUT} or V_{IN}, a separate supply can also be used.
2	GND	Ground return for the controller
3	OFF	A logic high state at the OFF pin will pull the GATE pin low and turn off the external MOSFET.
4	IN	Voltage sense connection to the external MOSFET Source pin.
5	GATE	Connection to the external MOSFET Gate.
6	OUT	Voltage sense connection to the external MOSFET Drain pin.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

IN, OUT Pins to Ground(2)		-0.3V to 100V
GATE Pin to Ground(2)		-0.3V to 100V
VS Pin to Ground		-0.3V to 100V
OFF Pin to Ground		-0.3V to 7V
Storage Temperature Range		−65°C to 150°C
ESD	HBM(3)	2 kV
	MM(4)	150V
Peak Reflow Temperature(5)		260°C, 30sec

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including in-operability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For ensured specifications and conditions, see the Electrical Characteristics table.
(2) The GATE pin voltage is typically 12V above the IN pin voltage when the LM5050-1 is enabled (i.e. OFF Pin is Open or Low, and $V_{IN} > V_{OUT}$). Therefore, the Absolute Maximum Rating for the IN pin voltage applies only when the LM5050-1 is disabled (i.e. OFF Pin is logic high), or for a momentary surge to that voltage since the Absolute Maximum Rating for the GATE pin is also 100V
(3) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Applicable test standard is JESD-22-A114-C.
(4) The Machine Model (MM) is a 200 pF capacitor discharged through a 0Ω resistor (i.e. directly) into each pin. Applicable test standard is JESD-A115-A.
(5) For soldering specifications see the LM5050-1 Product Folder at www.ti.com, general information at www.ti.com/packaging, and reflow information in literature number SNOA549.

OPERATING RATINGS(1)

IN, OUT, VS Pins		5.0V to 75V
OFF Pin		0.0V to 5.5V
Junction Temperature Range (T_J)	Standard Grade	−40°C to +125°C
	LM5050Q0MK-1	−40°C to +150°C
	LM5050Q1MK-1	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including in-operability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For ensured specifications and conditions, see the Electrical Characteristics table.

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the appropriate operating junction temperature (T_J) range of **-40°C to +125°C** (LM5050MK-1, LM5050Q1MK-1) or **-40°C to +150°C** (LM5050Q0MK-1). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12.0V, $V_{VS} = V_{IN}$, $V_{OUT} = V_{IN}$, V_{OFF} = 0.0V, C_{GATE}= 47 nF, and T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VS Pin						
V_{VS}	Operating Supply Voltage Range	-	**5.0**	-	**75.0**	V
I_{VS}	Operating Supply Current	V_{VS}= 5.0V, V_{IN} = 5.0V $V_{OUT} = V_{IN}$ - 100 mV	-	75	**105**	µA
		V_{VS}= 12.0V, V_{IN} = 12.0V $V_{OUT} = V_{IN}$ - 100 mV	-	100	**147**	
		V_{VS}= 75.0V, V_{IN} = 75.0V $V_{OUT} = V_{IN}$ - 100 mV	-	130	**288**	
IN Pin						
V_{IN}	Operating Input Voltage Range	-	**5.0**	-	**75.0**	V

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ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the appropriate operating junction temperature (T_J) range of **-40°C to +125°C** (LM5050MK-1, LM5050Q1MK-1) or **-40°C to +150°C** (LM5050Q0MK-1). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12.0V, V_{VS} = V_{IN}, V_{OUT} = V_{IN}, V_{OFF} = 0.0V, C_{GATE}= 47 nF, and T_J = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IN}	IN Pin current	V_{IN} = 5.0V V_{VS}= V_{IN} V_{OUT} = V_{IN} - 100 mV GATE = Open		**32**	190	**305**	µA
		V_{IN} = 12.0V to 75.0V V_{VS}= V_{IN} V_{OUT} = V_{IN} - 100 mV GATE = Open	LM5050MK-1, LM5050Q1MK-1	**233**	320	**400**	
			LM5050Q0MK-1	**233**	320	**475**	
OUT Pin							
V_{OUT}	Operating Output Voltage Range	-		**5.0**	-	**75.0**	V
I_{OUT}	OUT Pin Current	V_{IN} = 5.0V to 75.0V V_{VS}= V_{IN} V_{OUT} = V_{IN} - 100 mV		-	3.2	**8**	µA
GATE Pin							
$I_{GATE(ON)}$	Gate Pin Source Current	V_{IN} = 5.0V V_{VS} = V_{IN} V_{GATE} = V_{IN} V_{OUT} = V_{IN} - 175 mV		**12**	30	**41**	µA
		V_{IN} = 12.0V to 75.0V V_{VS} = V_{IN} V_{GATE} = V_{IN} V_{OUT} = V_{IN} - 175 mV		**20**	32	**41**	
V_{GS}	V_{GATE} - V_{IN} in Forward Operation(1)	V_{IN} = 5.0V V_{VS} = V_{IN} V_{OUT} = V_{IN} - 175 mV		**4.0**	7	**9.0**	V
		V_{IN} = 12.0V to 75.0V V_{VS} = V_{IN} V_{OUT} = V_{IN} - 175 mV		**9.0**	12	**14.0**	
$t_{GATE(REV)}$	Gate Capacitance Discharge Time at Forward to Reverse Transition See Figure 4	C_{GATE} = 0(2)		-	25	**85**	ns
		C_{GATE} = 10 nF(2)		-	60	-	
		C_{GATE} = 47 nF(2)		-	180	**350**	
$t_{GATE(OFF)}$	Gate Capacitance DischargeTime at OFF pin Low to High Transition See Figure 5	C_{GATE} = 47 nF(3)		-	486	-	ns
$I_{GATE(OFF)}$	Gate Pin Sink Current	V_{GATE} = V_{IN} + 3V V_{OUT} > V_{IN} + 100 mV t ≤ 10ms	LM5050MK-1, LM5050Q1MK-1	**1.8**	2.8	-	A
			LM5050Q0MK-1	**1.4**	2.8		
$V_{SD(REV)}$	Reverse V_{SD} Threshold V_{IN} < V_{OUT}	V_{IN} - V_{OUT}		**-41**	-28	**-16**	mV
$\Delta V_{SD(REV)}$	Reverse V_{SD} Hysteresis			-	10	-	mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold V_{IN} > V_{OUT}	V_{IN} = 5.0V V_{VS} = V_{IN} V_{IN} - V_{OUT}	LM5050MK-1, LM5050Q1MK-1	**1**	19	**37**	mV
			LM5050Q0MK-1	**1**	19	**60**	
		V_{IN} = 12.0V V_{VS} = V_{IN} V_{IN} - V_{OUT}	LM5050MK-1, LM5050Q1MK-1	**4.4**	22	**37**	
			LM5050Q0MK-1	**4.4**	22	**60**	

(1) Measurement of V_{GS} voltage (i.e. V_{GATE} - V_{IN}) includes 1 MΩ in parallel with C_{GATE}.
(2) Time from V_{IN}-V_{OUT} voltage transition from 200 mV to -500 mV until GATE pin voltage falls to V_{IN} + 1V. See Figure 4.
(3) Time from V_{OFF} voltage transition from 0.0V to 5.0V until GATE pin voltage falls to V_{IN} + 1V. See Figure 5

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ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the appropriate operating junction temperature (T_J) range of **-40°C to +125°C** (LM5050MK-1, LM5050Q1MK-1) or **-40°C to +150°C** (LM5050Q0MK-1). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12.0V, V_{VS} = V_{IN}, V_{OUT} = V_{IN}, V_{OFF} = 0.0V, C_{GATE}= 47 nF, and T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF Pin						
$V_{OFF(IH)}$	OFF Input High Threshold Voltage	V_{OUT} = V_{IN}-500 mV V_{OFF} Rising	-	1.56	**1.75**	V
$V_{OFF(IL)}$	OFF Input Low Threshold Voltage	V_{OUT} = V_{IN} - 500 mV V_{OFF} Falling	**1.10**	1.40	-	
ΔV_{OFF}	OFF Threshold Voltage Hysteresis	$V_{OFF(IH)}$ - $V_{OFF(IL)}$	-	155	-	mV
I_{OFF}	OFF Pin Internal Pull-down	V_{OFF} = 4.5V	**3.0**	5	**7.0**	µA
		V_{OFF} = 5.0V	-	8	-	

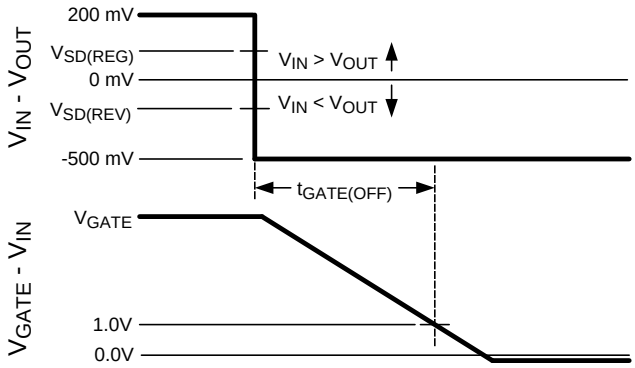


Figure 4. Gate Off Timing for Forward to Reverse Transition

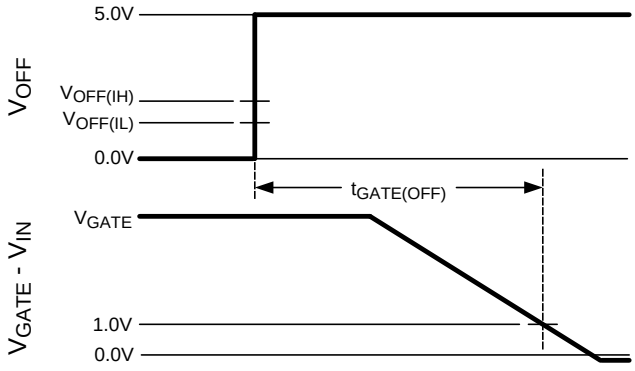
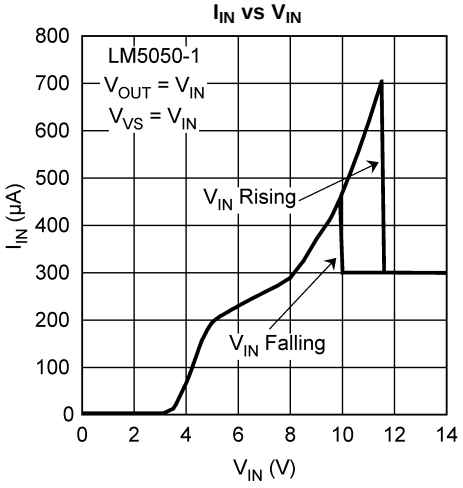


Figure 5. Gate Off Timing for OFF pin Low to High Transition

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise stated: V_{VS} = 12V, V_{IN} = 12V, V_{OFF} = 0.0V, and T_J = 25°C



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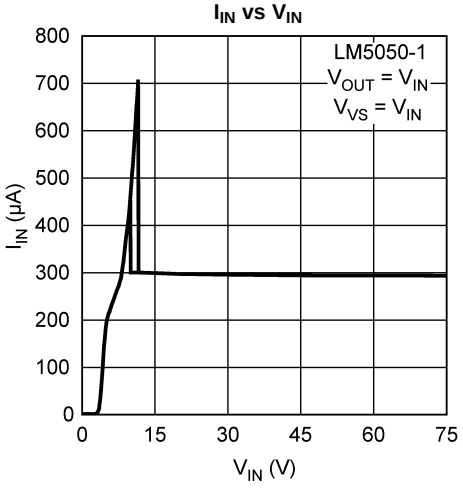

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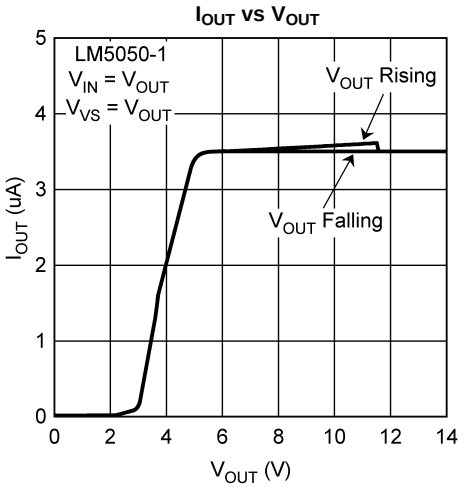

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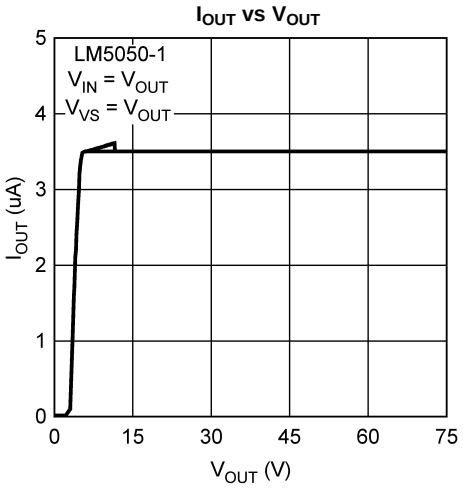

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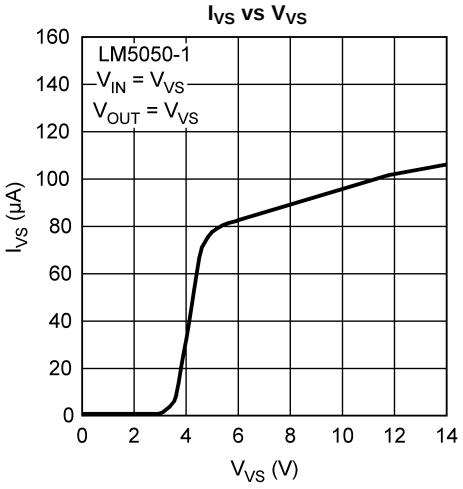

Figure 10.

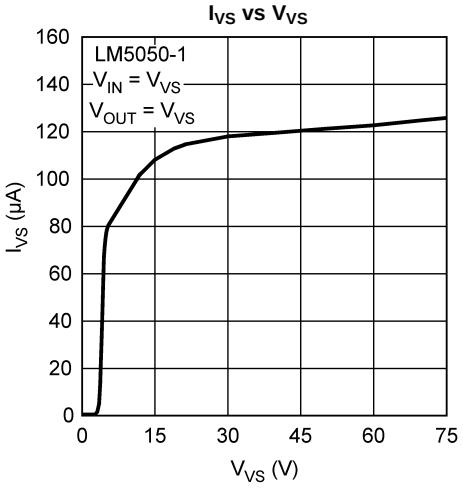

Figure 11.

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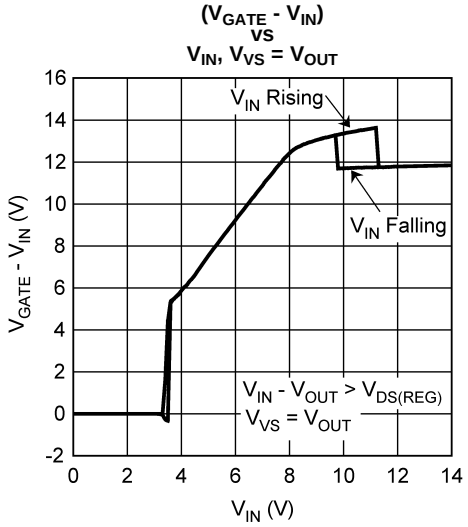
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise stated: V_{VS} = 12V, V_{IN} = 12V, V_{OFF} = 0.0V, and T_J = 25°C



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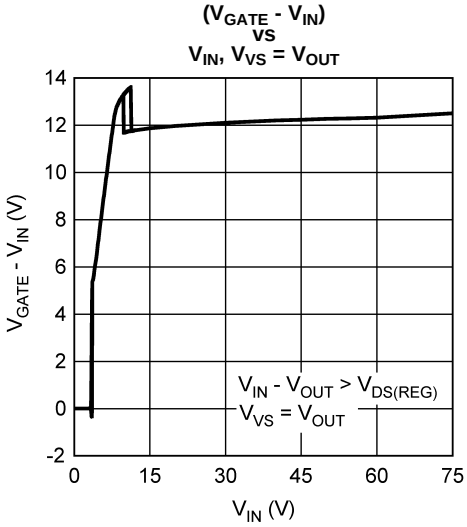

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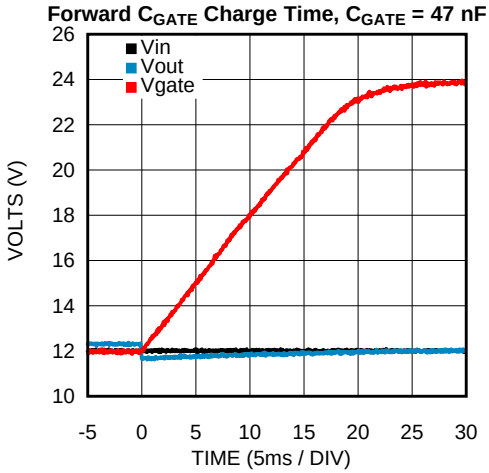
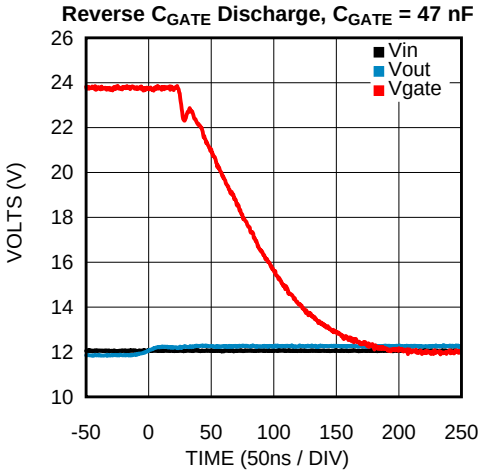


Figure 14.



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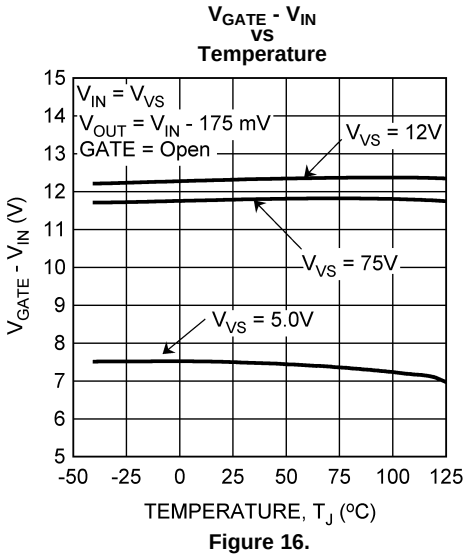

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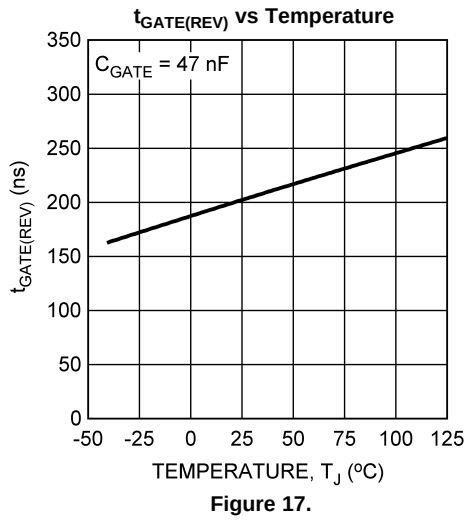

Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise stated: V_{VS} = 12V, V_{IN} = 12V, V_{OFF} = 0.0V, and T_J = 25°C

OFF Pin Thresholds vs Temperature

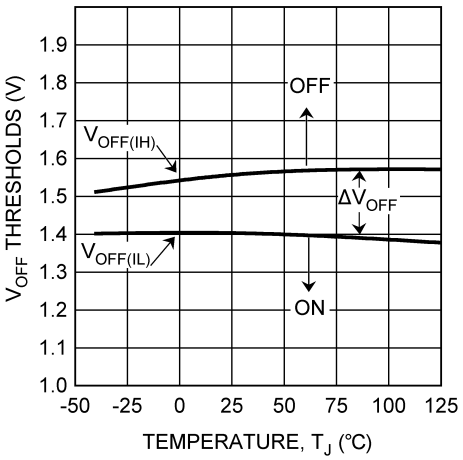

Figure 18.

OFF Pin Pull-Down vs Temperature

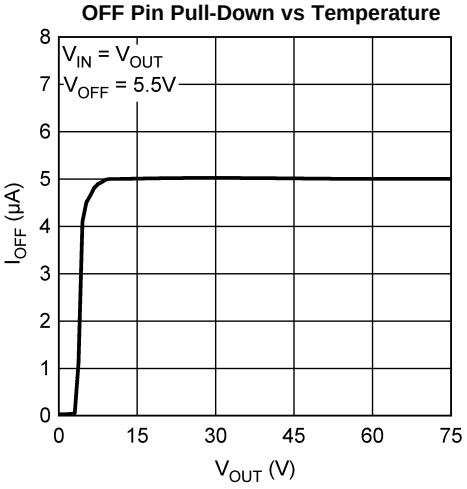

Figure 19.

C_{GATE} Charge and Discharge vs OFF Pin

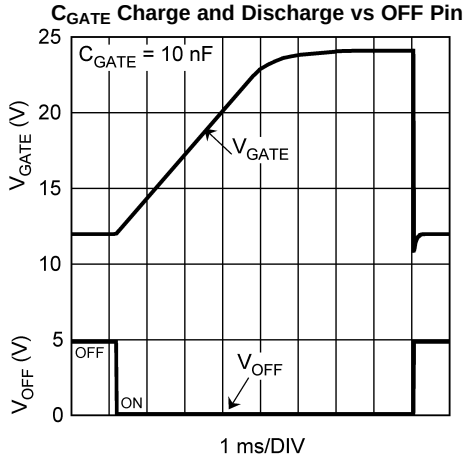

Figure 20.

OFF Pin, On to Off Transition

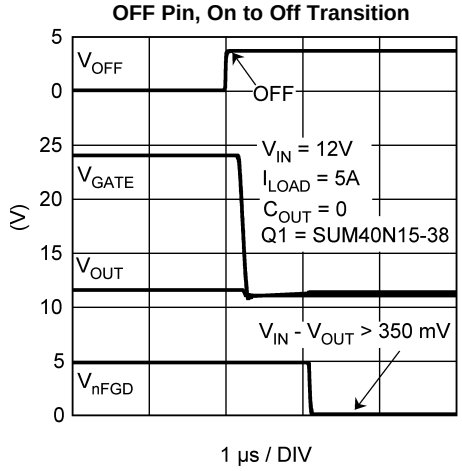

Figure 21.

OFF Pin, Off to On Transition

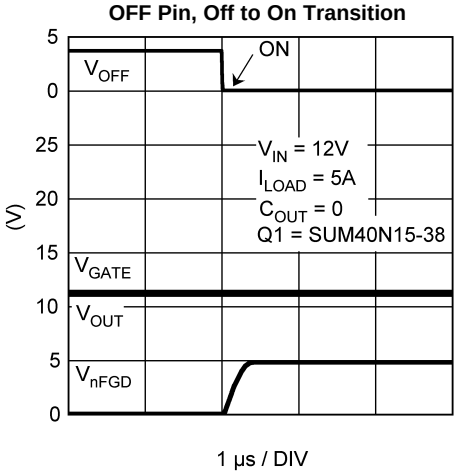

Figure 22.

GATE Pin vs ($R_{DS(ON)}$ x I_{DS})

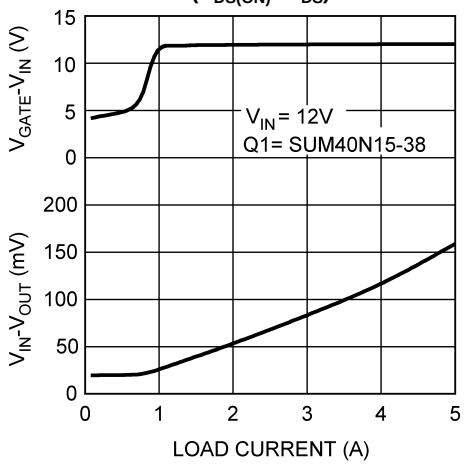

Figure 23.

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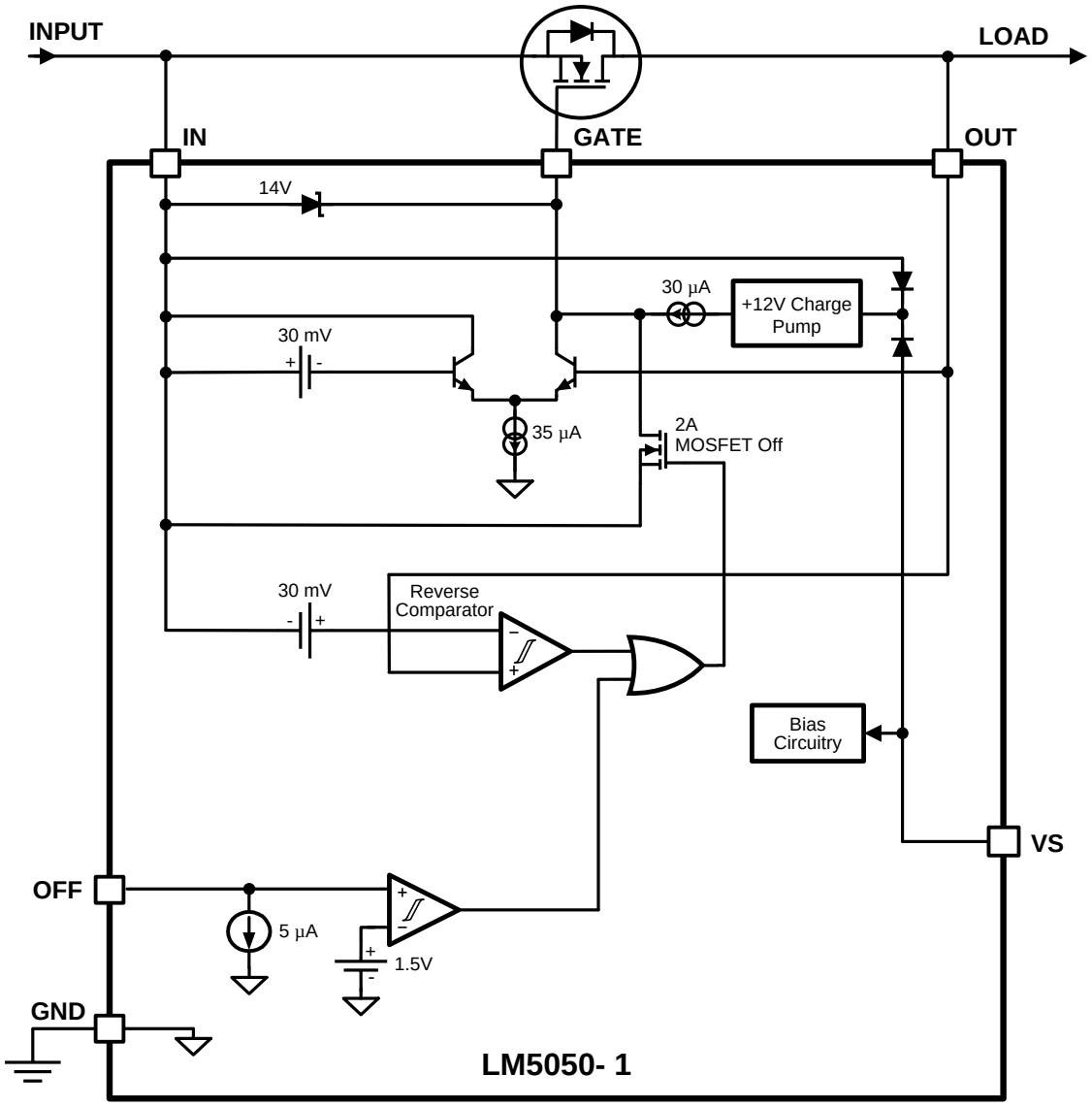
BLOCK DIAGRAM



APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.

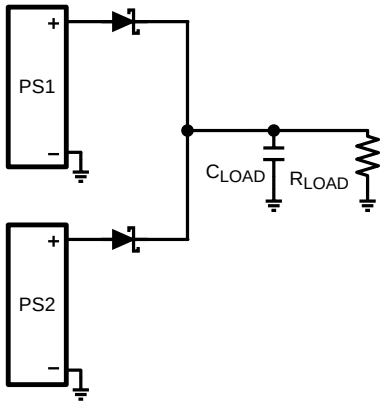


Figure 24. OR-ing with Diodes

The LM5050-1 is a positive voltage (i.e. high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the LM5050-1 at the IN and OUT pins, while the GATE pin drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.

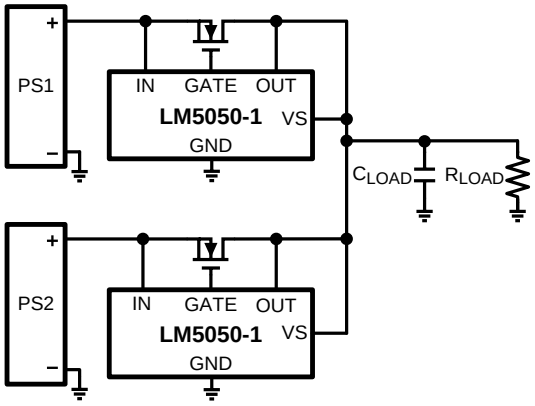


Figure 25. OR-ing with MOSFETs

IN, GATE AND OUT PINS

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. The resulting voltage across the body diode will be detected at the LM5050-1 IN and OUT pins which then begins charging the MOSFET gate through a 32 µA (typical) charge pump current source . In normal operation, the gate of the MOSFET is charged until it reaches the clamping voltage of the 12V GATE to IN pin zener diode internal to the LM5050-1.

The LM5050-1 is designed to regulate the MOSFET gate- to -source voltage if the voltage across the MOSFET source and drain pins falls below the $V_{SD(REG)}$ voltage of 22 mV (typical).

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If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 27 mV (typical), the GATE pin voltage will be decreased until the voltage across the MOSFET is regulated at 22 mV. If the drain-to-source voltage is greater than $V_{SD(REG)}$ voltage the gate-to-source will increase, eventually reaching the 12V GATE to IN zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the LM5050-1 IN and OUT pins is more negative than the $V_{SD(REV)}$ voltage of -28 mV (typical), the LM5050-1 will quickly discharge the MOSFET gate through a strong GATE to IN pin discharge transistor.

If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The LM5050-1 responds to a voltage reversal condition typically within 25 ns. The actual time required to turn off the MOSFET will depend on the charge held by gate capacitance of the MOSFET being used. A MOSFET with 47 nF of effective gate capacitance can be turned off in typically 180 ns. This fast turn off time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

VS PIN

The LM5050-1 VS pin is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

For typical LM5050-1 applications, where the input voltage is above 5.0V, the VS pin can be connected directly to the OUT pin. In situations where the input voltage is close to, but not less than, the 5.0V minimum, it may be helpful to connect the VS pin to the OUT pin through an RC Low-Pass filter to reduce the possibility of erratic behavior due to spurious voltage spikes that may appear on the OUT and IN pins. The series resistor value should be low enough to keep the VS voltage drop at a minimum. A typical series resistor value is 100Ω. The capacitor value should be the lowest value that produces acceptable filtering of the voltage noise.

Alternately, it is possible to operate the LM5050-1 with V_{IN} values less than 1V if the VS pin is powered from a separate supply. This separate VS supply must be between 5.0V and 75V. See Figure 28.

OFF PIN

The OFF pin is a logic level input pin that is used to control the gate drive to the external MOSFET. The maximum operating voltage on this pin is 5.5V.

When the OFF pin is high, the MOSFET is turned off (independent of the sensed IN and OUT voltages). In this mode, load current will flow through the body diode of the MOSFET. The voltage difference between the IN pin and OUT pins will be approximately 700 mV if the MOSFET is operating normally through the body diode.

The OFF pin has an internal pull-down of 5 µA (typical). If the OFF function is not required the pin may be left open or connected to ground.

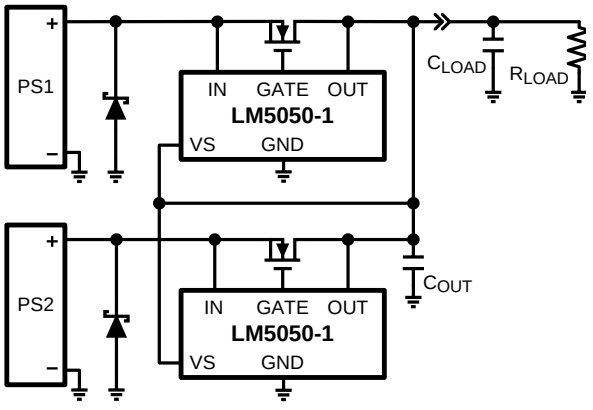

Figure 26.

SHORT CIRCUIT FAILURE OF AN INPUT SUPPLY

An abrupt zero ohm short circuit across the input supply will cause the highest possible reverse current to flow while the internal LM5050-1 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator will react, and will start the process of discharging the Gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the LM5050-1 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both. In low voltage applications, the MOSFET drainto- source breakdown voltage rating may be adequate to protect the OUT pin (i.e. $V_{IN} + V_{(BR)DSS(MAX)} < 75V$), but most MOSFET datasheets do not ensure the maximum breakdown rating, so this method should be used with caution.

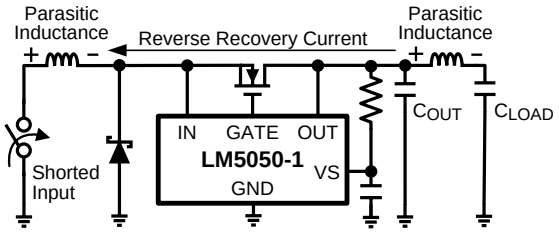

Figure 27.

MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (i.e. body diode) I_S, the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source On resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$.

$$\text{Gate Charge Time} = Q_g / I_{GATE(ON)} \quad (3)$$

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.

The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.

The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the LM5050-1 gate drive capabilities. Logic level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 5V, are recommended, but sub-Logic level MOSFETs having $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 2.5V, can also be used. Standard level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 10V, are not recommended.

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The dominate MOSFET loss for the LM5050-1 active OR-ing controller is conduction loss due to source-to-drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

1. Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the LM5050-1 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turn-off condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.
2. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (i.e. reverse) without activating the LM5050-1 Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.
3. Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.

Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the LM5050-1 can provide as it attempts to drive the Drain to Source voltage down to the $V_{SD(REG)}$ of 22 mV typical. This increased Gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.

As a guideline, it is suggest that $R_{DS(ON)}$ be selected to provide at least 22 mV, and no more than 100 mV, at the nominal load current.

$$(22\ mV / I_D) \le R_{DS(ON)} \le (100mV / I_D) \quad (4)$$

The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET in order to ensure that the junction temperature (T_J) is reasonably well controlled, since the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

$$P_{DISS} = I_D^2 \times (R_{DS(ON)}) \quad (5)$$

Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10A, and an $R_{DS(ON)}$ of 10 mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating (θ_{JA}) would need to be:

$$\theta_{JA} \le (T_{J(MAX)} - T_{A(MAX)})/(I_D^2 \times R_{DS(ON)})$$
$$\theta_{JA} \le (100°C - 35°C)/(10A \times 10A \times 0.01\Omega)$$
$$\theta_{JA} \le 65°C/W \quad (6)$$

Typical Applications

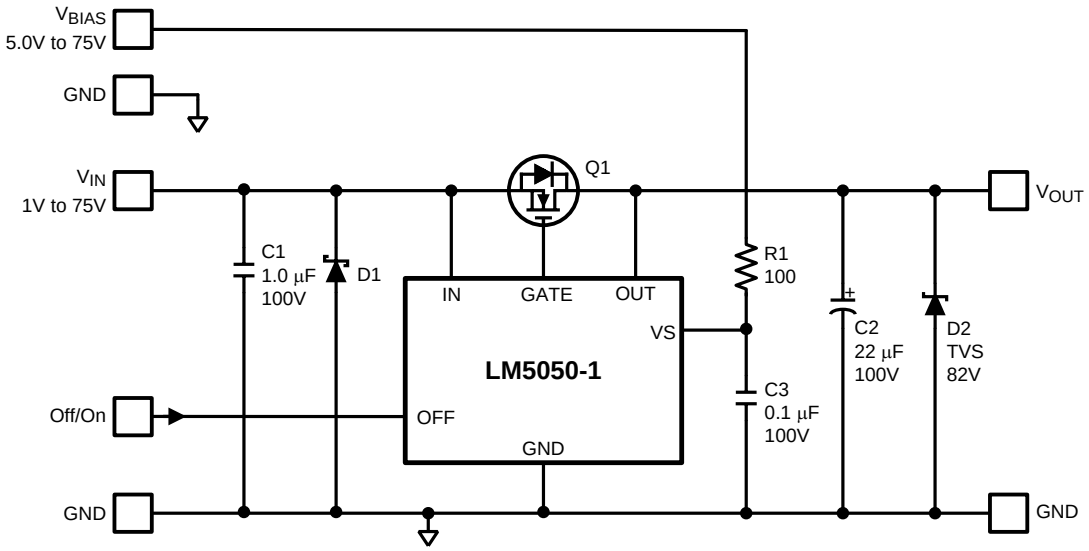

Figure 28. Using a Separate VS Supply For Low Vin Operation

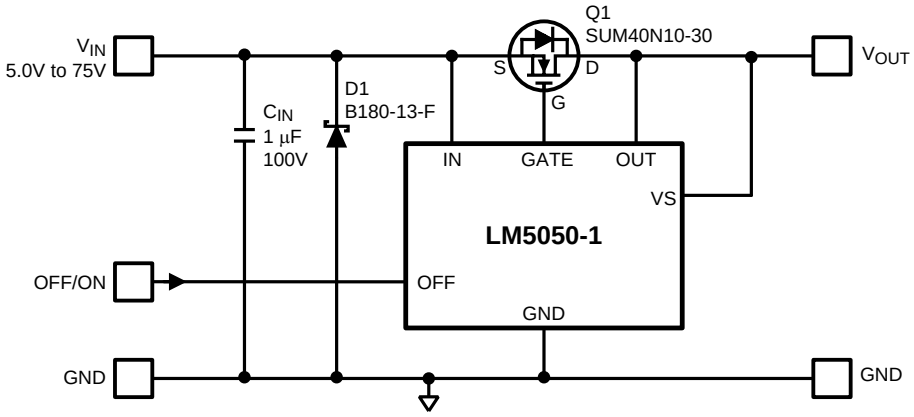

Figure 29. Basic Application with Input Transient Protection

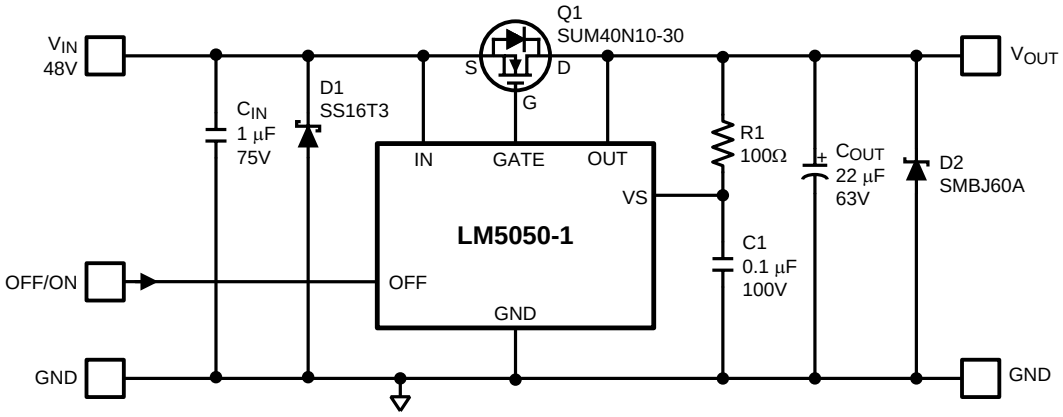

Figure 30. Typical Application with Input and Output Transient Protection

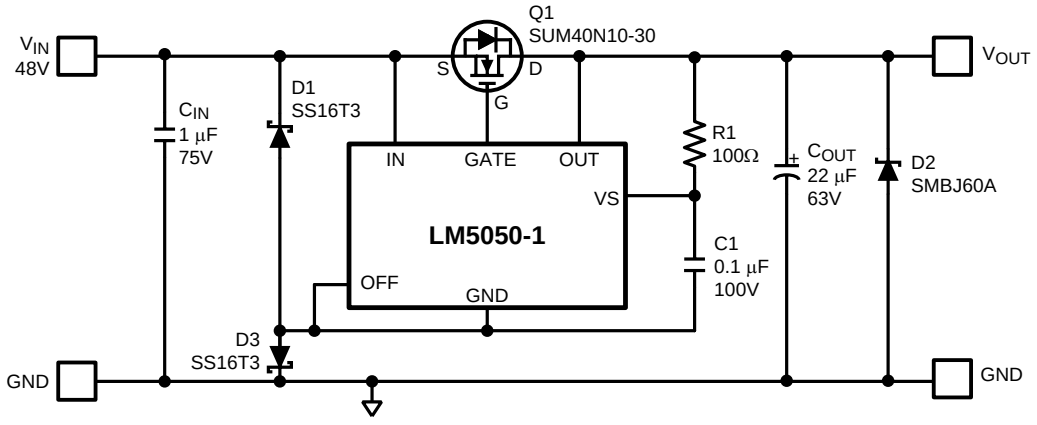

Figure 31. +48V Application with Reverse Input Voltage (V_{IN} = -48V) Protection

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5050MK-1/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SZHB	Samples
LM5050MKX-1/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SZHB	Samples
LM5050Q0MK-1/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 150	SL5B	Samples
LM5050Q0MKX-1/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 150	SL5B	Samples
LM5050Q1MK-1/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SP3B	Samples
LM5050Q1MKX-1/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SP3B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF LM5050-1, LM5050-1-Q1 :

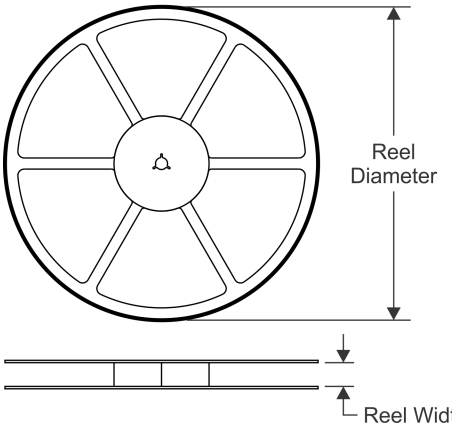
- Catalog: LM5050-1
- Automotive: LM5050-1-Q1

NOTE: Qualified Version Definitions:

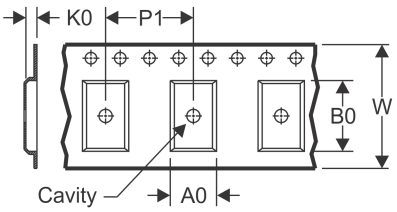
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

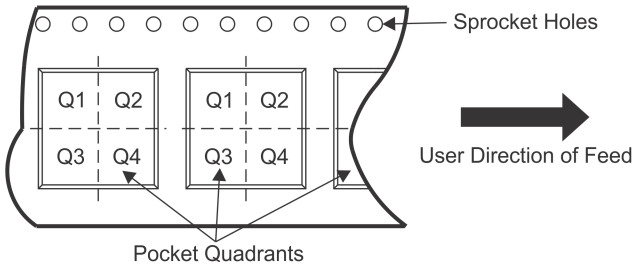


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

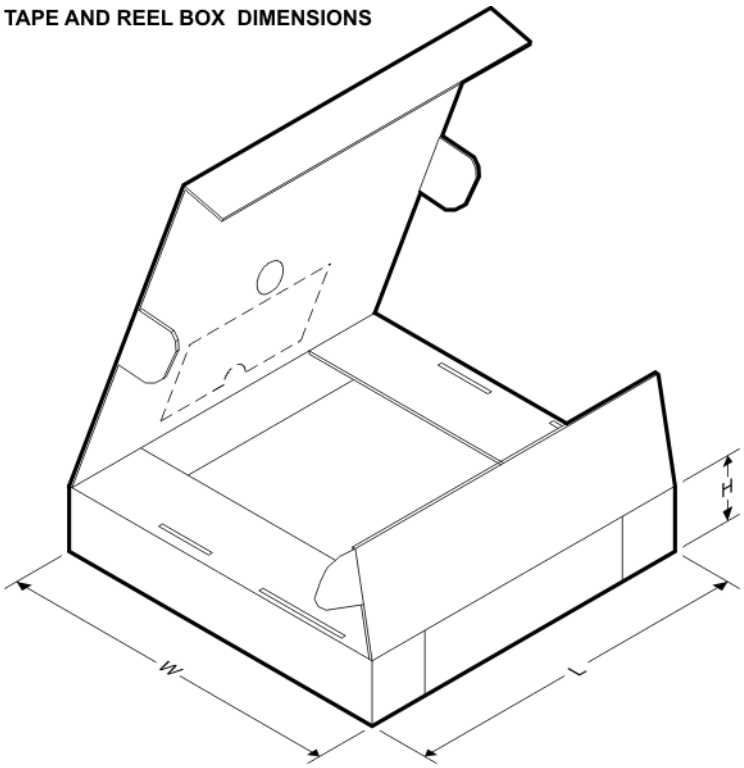
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5050MK-1/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050MKX-1/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q0MK-1/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q0MKX-1/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q1MK-1/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050Q1MKX-1/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

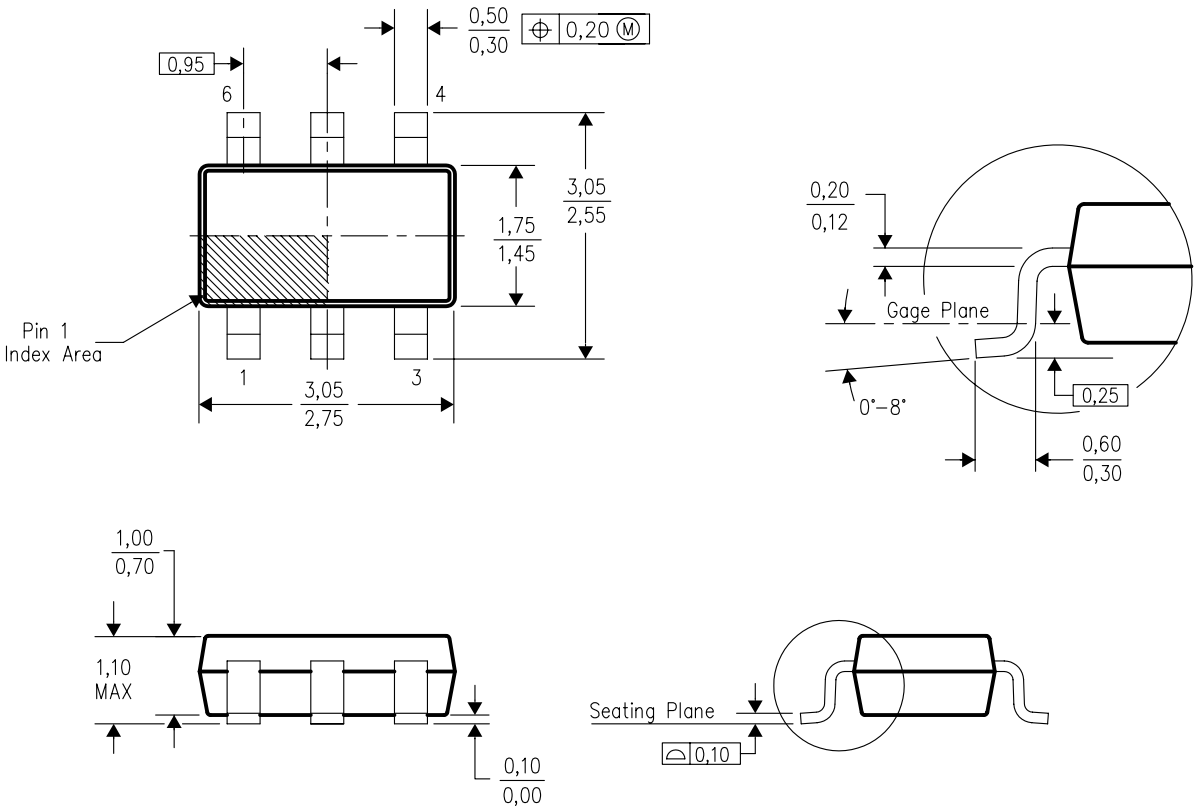
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5050MK-1/NOPB	SOT	DDC	6	1000	210.0	185.0	35.0
LM5050MKX-1/NOPB	SOT	DDC	6	3000	210.0	185.0	35.0
LM5050Q0MK-1/NOPB	SOT	DDC	6	1000	210.0	185.0	35.0
LM5050Q0MKX-1/NOPB	SOT	DDC	6	3000	210.0	185.0	35.0
LM5050Q1MK-1/NOPB	SOT	DDC	6	1000	210.0	185.0	35.0
LM5050Q1MKX-1/NOPB	SOT	DDC	6	3000	210.0	185.0	35.0

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



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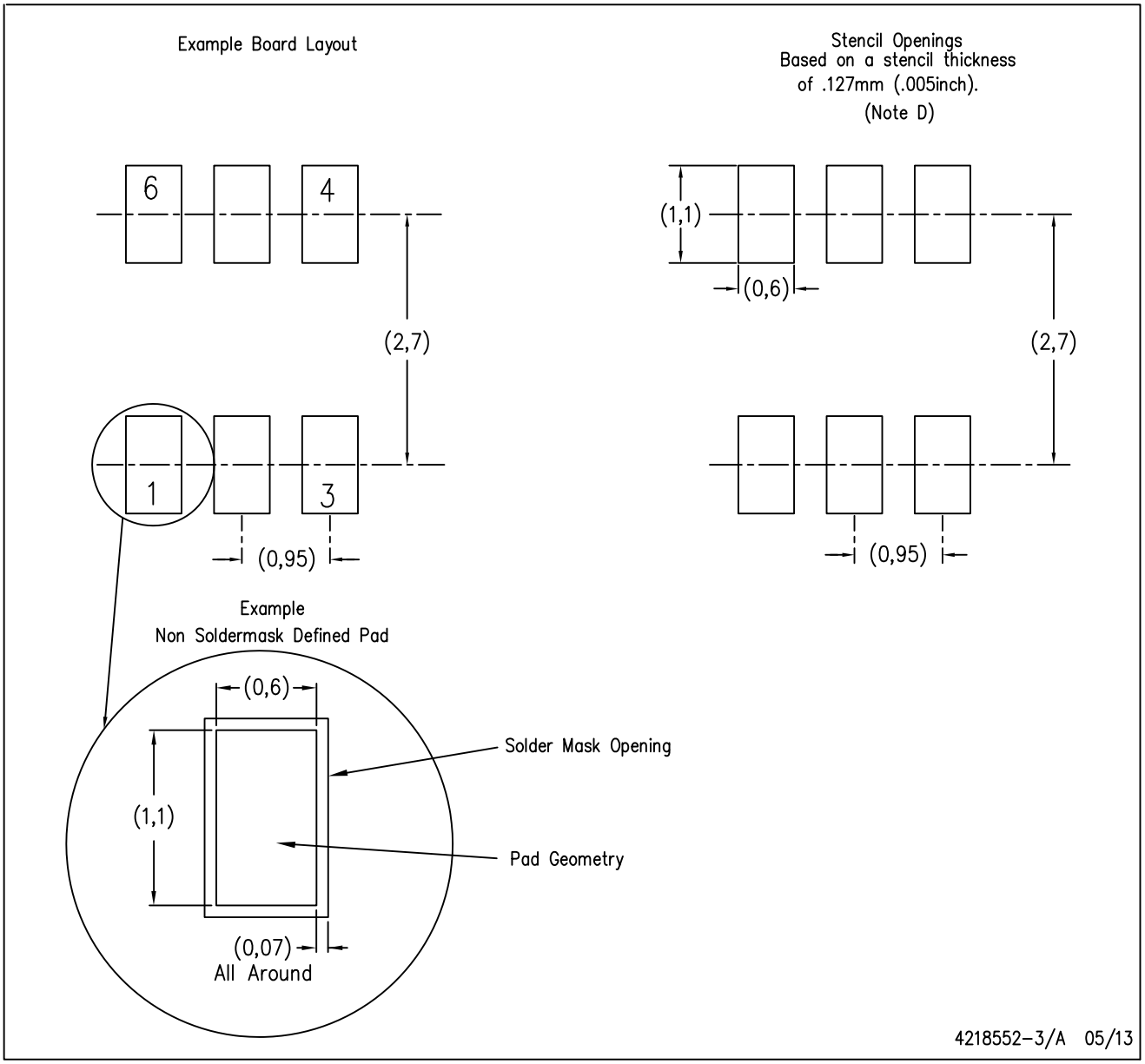
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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