Single 7.6A Peak Current Low-Side Gate Driver with a PILOT Output

Check for Samples: LM5134

FEATURES

- **7.6A/4.5A Peak Sink/Source Drive Current for Main Output**
- **820mA/660mA Peak Sink/Source Current for PILOT Output**
- **+4V to +12.6V Single Power Supply**
- **Matching Delay Time Between Inverting and Non-Inverting Inputs**
- **TTL/CMOS Logic Inputs**
- **Up to +14V Logic Inputs (Regardless of VDD Voltage)**
- **-40°C to 125°C Junction Temperature Range**

TYPICAL APPLICATIONS

- **Motor Drive**
- **Solid-State Power Controller**
- **Power Factor Correction Converter**

PACKAGE

- **SOT23-6**
- **WSON (3mm x 3mm)**

DESCRIPTION

The LM5134 is a high-speed single low-side driver capable of sinking and sourcing 7.6A/4.5A peak currents. The LM5134 has inverting and non-inverting inputs that give the user greater flexibility in controlling the FET. The LM5134 features one main output, OUT, and an extra gate drive output, PILOT. The PILOT pin logic is complementary to the OUT pin, and can be used to drive a small MOSFET located close to the main power FET. This configuration minimizes the turn-off loop and reduces the consequent parasitic inductance. It is particularly useful for driving high-speed FETs or multiple FETs in parallel. The LM5134 is available in the SOT23 6-pin package and the WSON-6 package with an exposed pad to aid thermal dissipation.

Block Diagram

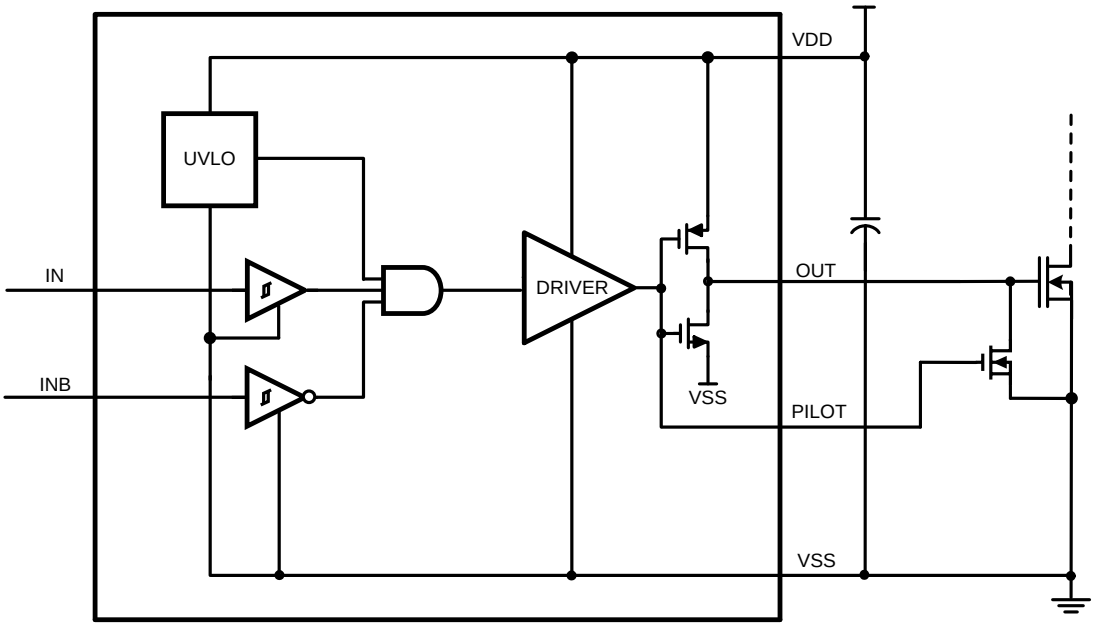


Figure 1. Block Diagram

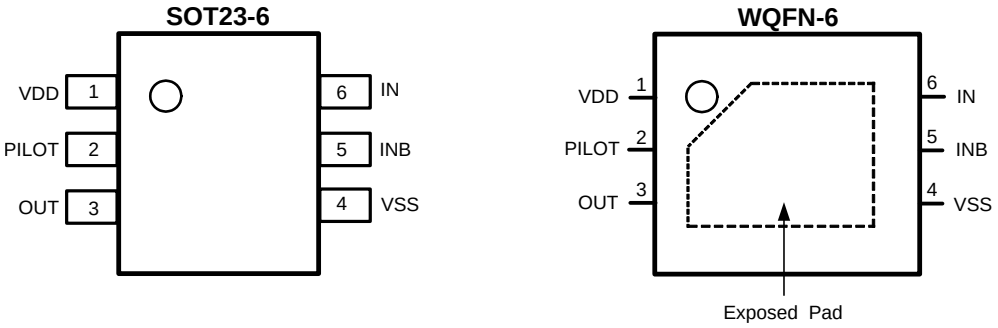
Input/Output Options

Base Part Number	Logic Input
LM5134A	CMOS
LM5134B	TTL

Truth Table

IN	INB	OUT	PILOT
L	L	L	H
L	H	L	H
H	L	H	L
H	H	L	H

Connection Diagram



PIN DESCRIPTIONS

Pin No.	Name	Description	Applications Information
1	VDD	Gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close as possible to the IC.
2	PILOT	Gate drive output for an external turn-off FET	Connect to the gate of a small turn-off MOSFET with a short, low inductance path. The turn-off FET provides a local turn-off path.
3	OUT	Gate drive output for the power FET	Connect to the gate of the power FET with a short, low inductance path. A gate resistor can be used to eliminate potential gate oscillations.
4	VSS	Ground	All signals are referenced to this ground.
5	INB	Inverting logic input	Connect to VSS when not used.
6	IN	Non-inverting logic input	Connect to VDD when not used.
EP	EP	Exposed Pad	It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PC board, and that ground plane extend out from beneath the IC to help dissipate heat.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

VDD to VSS	−0.3V to 14V
IN, INB to VSS	−0.3V to 14V
Storage Temperature Range	−55°C to +150°C
Junction Temperature	+150°C
ESD Rating HBM	2kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.

Recommended Operating Conditions

VDD	+4.0V to 12.6V
Operating Junction Temperature	−40°C to +125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, VDD = +12V(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
VDD	VDD Operating Voltage		**4.0**		**12.6**	V
UVLO	VDD Undervoltage Lockout	VDD Rising	**3.25**	3.6	**4.00**	V
	VDD Undervoltage Lockout Hysteresis			0.36		V
	VDD Undervoltage lockout to Main output delay time	VDD Rising		500		ns
I_{DD}	VDD Quiescent Current	IN = INB = VDD		0.8	**2**	mA
OUTPUT						
R_{ON-DW} (SOT23-6)	Main output Resistance – Pulling Down	VDD = 10V, I_{OUT} = -100mA		0.15	**0.45**	Ω
		VDD = 4.5V, I_{OUT} = -100mA		0.2	**0.5**	Ω
R_{ON-DW} (WSON)	Main output Resistance – Pulling Down	VDD = 10V, I_{OUT} = -100mA		0.2	**0.5**	Ω
		VDD = 4.5V, I_{OUT} = -100mA		0.25	**0.55**	Ω
	Power-off Pull Down Resistance	VDD = 0V, I_{OUT} = -10mA		1.5	10	Ω
	Power-off Pull Down Clamp Voltage	VDD = 0V, I_{OUT} = -10mA		0.7	1.0	V
	Peak Sink Current	C_L = 10,000pF		7.6		A
R_{ON-UP} (SOT23-6)	Main output Resistance - Pulling Up	VDD = 10V, I_{OUT} = 50mA		0.7	**1.3**	Ω
		VDD = 4.5V, I_{OUT} = 50mA		1	**1.9**	Ω
R_{ON-UP} (WSON)	Main output Resistance - Pulling Up	VDD = 10V, I_{OUT} = 50mA		0.75	**1.2**	Ω
		VDD = 4.5V, I_{OUT} = 50mA		1.14	**1.85**	Ω
	Peak Source Current	C_L = 10,000pF		4.5		A
PILOT						
R_{ONP-DW}	PILOT Output Resistance – Pulling Down	VDD = 10V,I_{OUT} = -100mA		3.7	**9**	Ω
		VDD = 4.5V, I_{OUT} = -100mA		4.7	**12**	Ω
	Peak Sink Current	C_L = 330pF		820		mA

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, VDD = +12V(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{ONP-UP}	PILOT output Resistance – Pulling Up	VDD = 10V, I_{OUT} = 50mA		6	**11**	Ω
		VDD = 4.5V, I_{OUT} = 50mA		10.7	**20**	Ω
	Peak Source Current	C_L = 330pF		660		mA
LOGIC INPUT						
V_{IH}	Logic 1 Input Voltage	LM5134A	**0.67 x VDD**			V
		LM5134B	**2.4**			V
V_{IL}	Logic 0 Input Voltage	LM5134A			**0.33 x VDD**	V
		LM5134B			**0.8**	V
V_{HYS}	Logic-Input Hysteresis	LM5134A		0.9		V
		LM5134B		0.68		
	Logic-Input Current	INB = VDD or 0		0.001	**10**	µA
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	SOT23-6		90		°C/W
		WSON-6		60		°C/W
SWITCHING CHARACTERISTICS FOR VDD = +10V						
t_R	OUT Rise Time	C_L = 1000pF		3		ns
		C_L = 5000pF		10		ns
		C_L = 10,000pF		20		ns
t_F	OUT Fall Time	C_L = 1000pF		2		ns
		C_L = 5000pF		4.7		ns
		C_L = 10,000pF		7.2		ns
t_{D-ON}	OUT Turn-On Propagation Delay	C_L = 1000pF		17	**40**	ns
t_{D-OFF}	OUT Turn-Off Propagation Delay	C_L = 1000pF		12	**25**	ns
	Main Output Break-Before-Make Time			2.5		ns
t_{PR}	PILOT Rise Time	C_L = 330pF		5.3		ns
t_{PF}	PILOT Fall Time	C_L = 330pF		3.9		ns
t_{PD-ON}	OUT Turn-Off to PILOT Turn-On Propagation Delay	C_L = 330pF		4.2		ns
t_{PD-OFF}	PILOT Turn-Off to OUT Turn-On Propagation Delay	C_L = 330pF		6.4		ns
SWITCHING CHARACTERISTICS FOR VDD = +4.5V						
t_R	Rise Time	C_L = 1000pF		5		ns
		C_L = 5000pF		14		ns
		C_L = 10,000pF		24		ns
t_F	Fall Time	C_L = 1000pF		2.3		ns
		C_L = 5000pF		5.4		ns
		C_L = 10,000pF		7.2		ns
t_{D-ON}	OUT Turn-On Propagation Delay	C_L = 1000pF		26	**50**	ns
t_{D-OFF}	OUT Turn-Off Propagation Delay	C_L = 1000pF		20	**45**	ns
	Main output Break-Before-Make Time			4.2		ns
t_{PR}	PILOT Rise Time	C_L = 330pF		9.6		ns
t_{Pf}	PILOT Fall Time	C_L = 330pF		3.7		ns

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, VDD = +12V(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD-ON}	OUT Turn-Off to PILOT Turn-On Propagation Delay	C_L = 330pF		7.5		ns
t_{PD-OFF}	PILOT Turn-Off to OUT Turn-On Propagation Delay	C_L = 330pF		11.8		ns

TIMING DIAGRAM

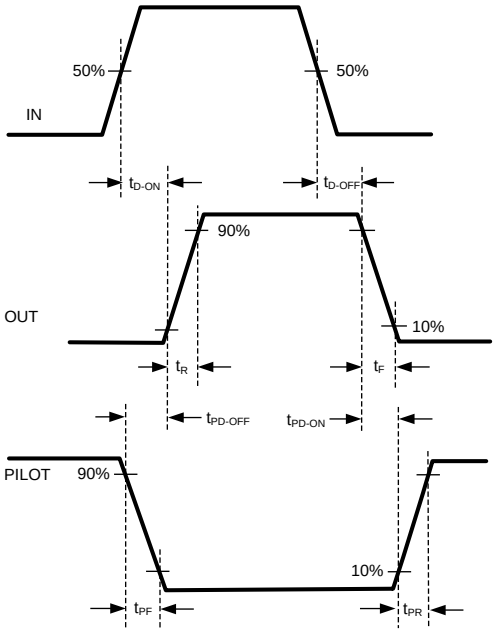


Figure 2.

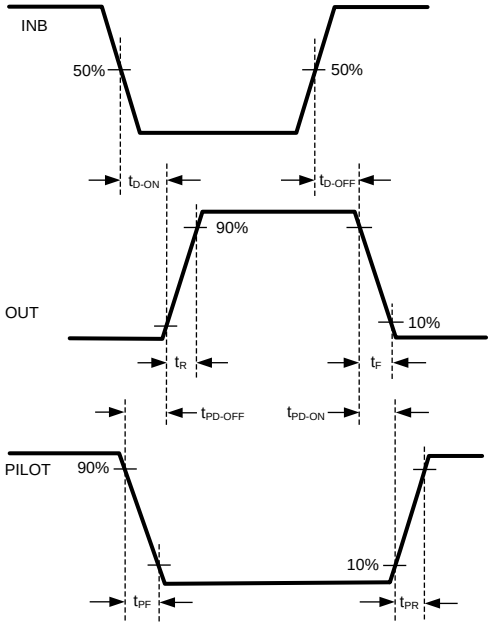


Figure 3.

Typical Performance Characteristics

OUT Source Current vs. OUT Voltage

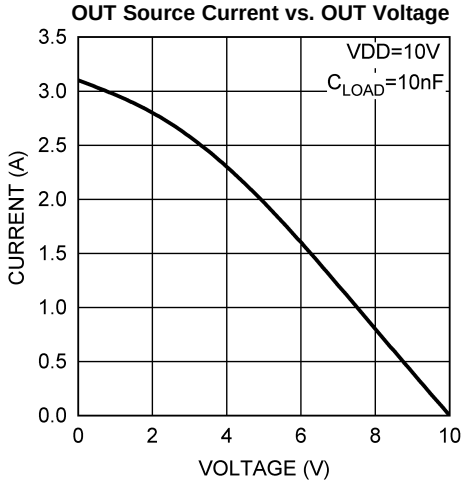


Figure 4.

OUT Sink Current vs. OUT Voltage

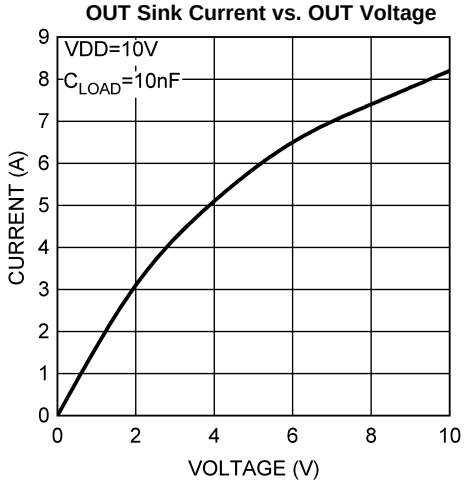


Figure 5.

OUT Peak Source Current vs. VDD Voltage

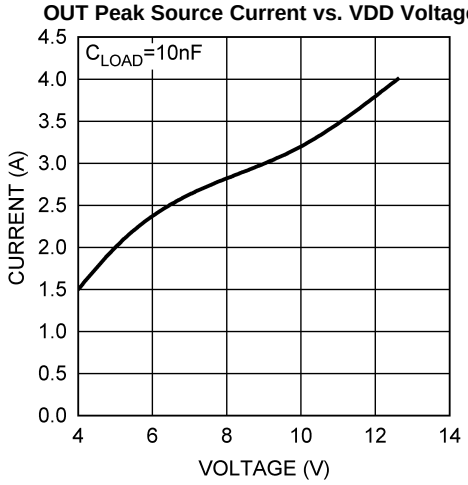


Figure 6.

OUT Peak Sink Current vs. VDD Voltage

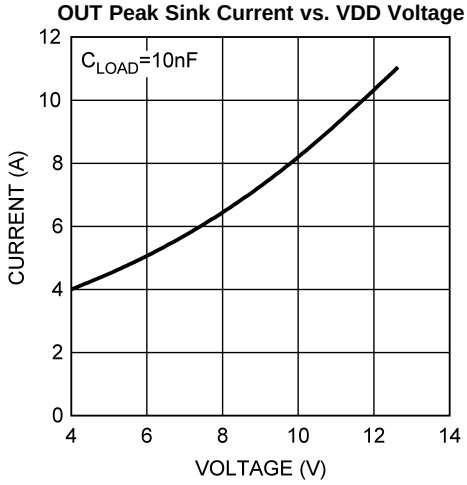


Figure 7.

PILOT Source Current vs. PILOT Voltage

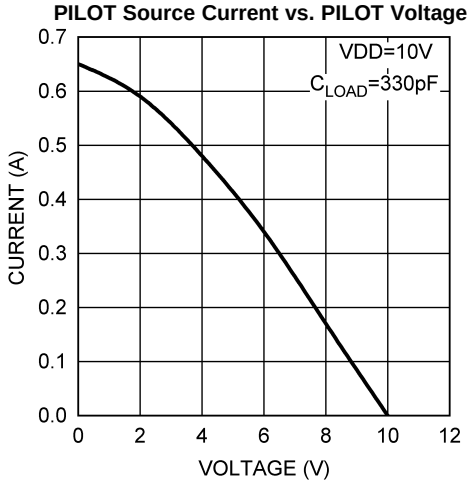


Figure 8.

PILOT Sink Current vs. PILOT Voltage

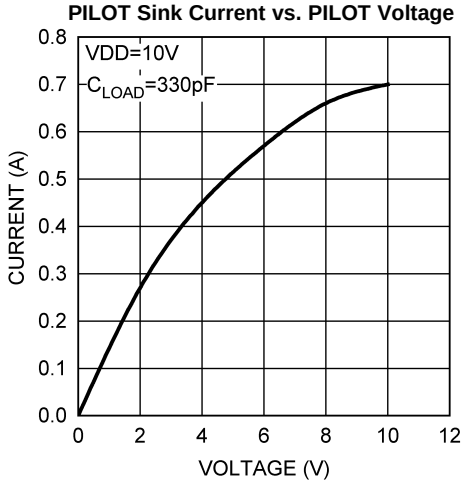


Figure 9.

Typical Performance Characteristics (continued)

PILOT Peak Source Current vs. VDD Voltage

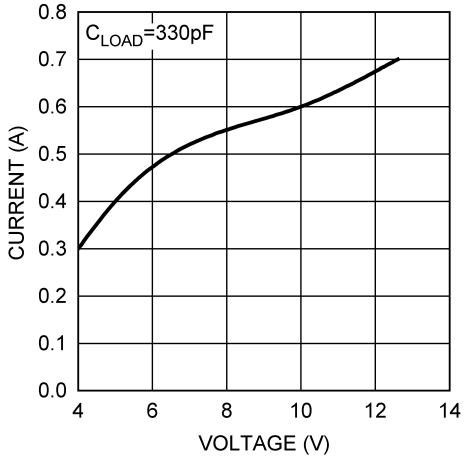


Figure 10.

PILOT Peak Sink Current vs. VDD Voltage

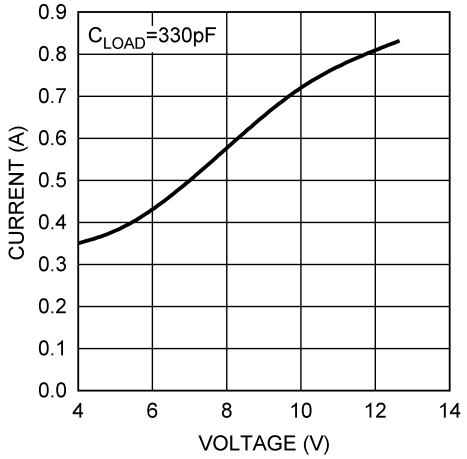


Figure 11.

OUT Turn-On Propagation Delay vs. VDD

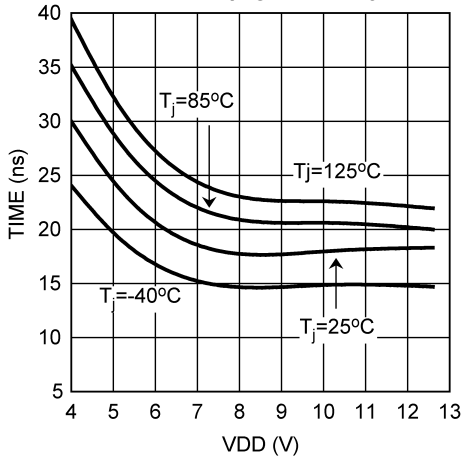


Figure 12.

OUT Turn-Off Propagation Delay vs. VDD

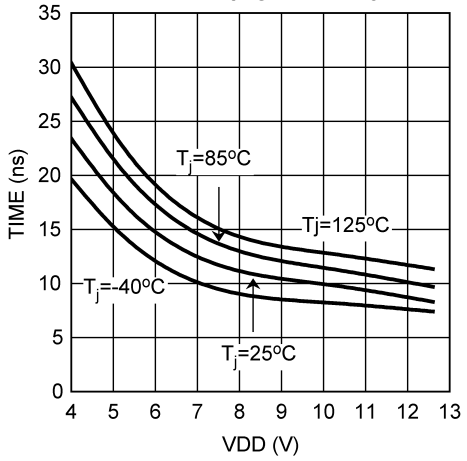


Figure 13.

OUT Turn-Off to PILOT Turn-On Propagation Delay vs. VDD

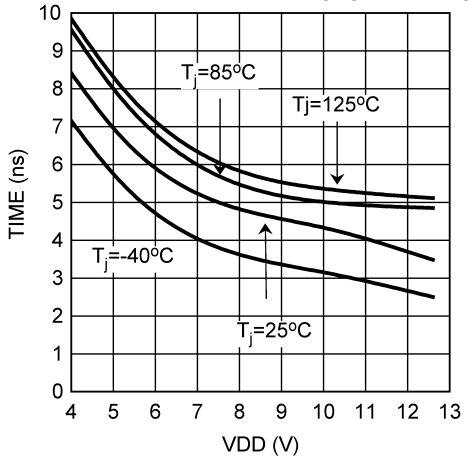


Figure 14.

PILOT Turn-Off to OUT Turn-On Propagation Delay vs. VDD

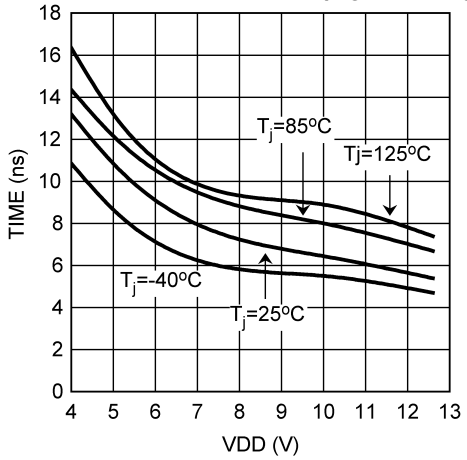


Figure 15.

Typical Performance Characteristics (continued)

Supply Current vs. OUT Capacitive Load

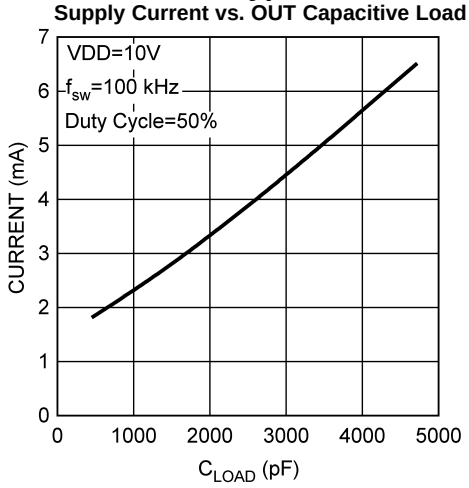


Figure 16.

Supply Current vs. PILOT Capacitive Load

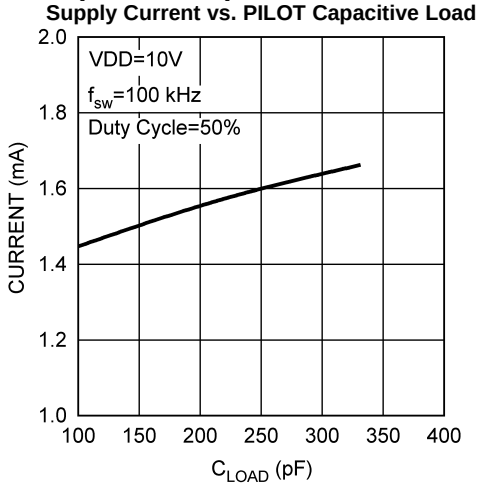


Figure 17.

Supply Current vs. Frequency

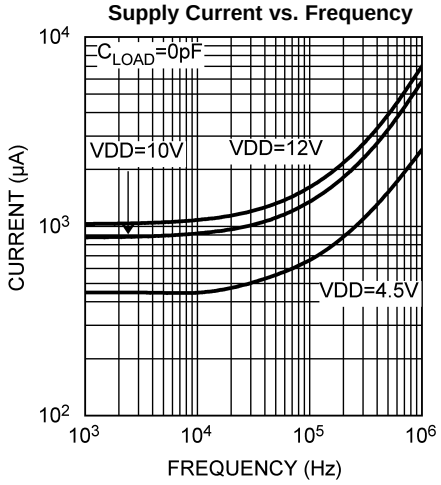


Figure 18.

Quiescent Current vs. Temperature

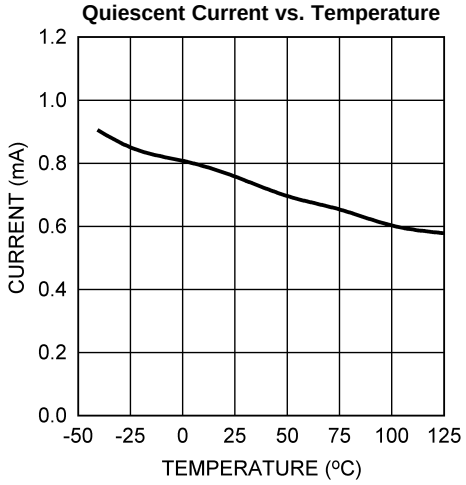


Figure 19.

LM5134A Input Threshold vs. Temperature

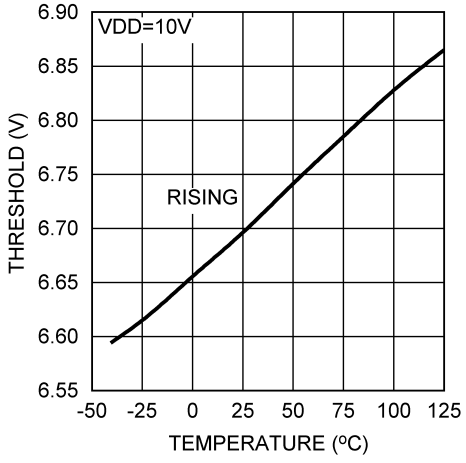


Figure 20.

LM5134A Input Threshold vs. Temperature

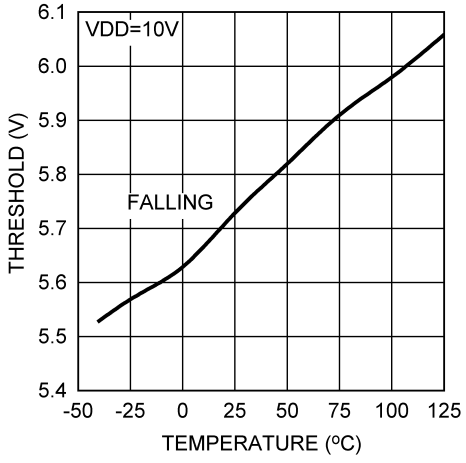


Figure 21.

Typical Performance Characteristics (continued)

LM5134B Input Threshold vs. Temperature

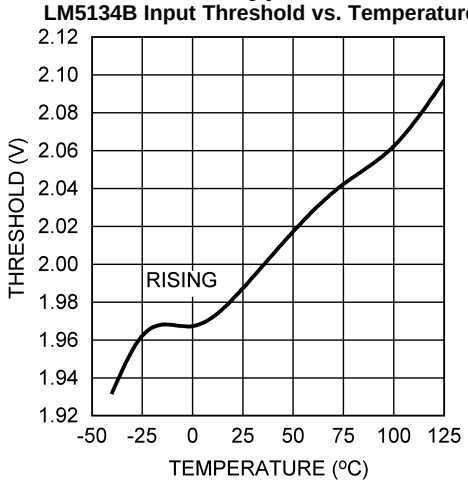


Figure 22.

LM5134B Input Threshold vs. Temperature

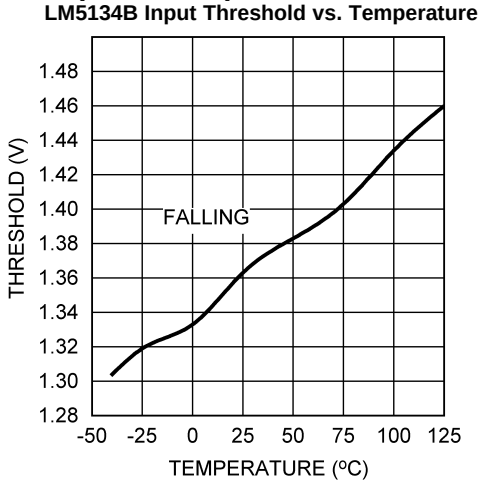


Figure 23.

UVLO Threshold vs. Temperature

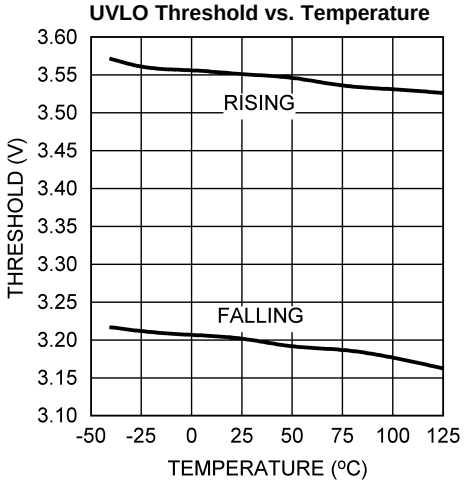


Figure 24.

DETAILED OPERATING DESCRIPTION

The LM5134 is a single low-side gate driver with one main output, OUT, and a complementary output PILOT. The OUT pin has high 7.6A/4.5A peak sink/source current and can be used to drive large power MOSFETs or multiple MOSFETs in parallel. The PILOT pin has 820mA/660mA peak sink/source current, and is intended to drive an external turn-off MOSFET, as shown in Figure 1. The external turn-off FET can be placed close to the power MOSFETs to minimize the loop inductance, and therefore helps eliminate stray inductance induced oscillations or undesired turn-on. This feature also provides the flexibility to adjust turn-on and turn-off speed independently.

When using the external turn-off switch, it is important to prevent the potential shoot-through between the external turn-off switch and the LM5134 internal pull-up switch. The propagation delay, T_{PD-ON} and T_{PD-OFF}, has been implemented in the LM5134 between the PILOT and the OUT pins, as depicted in the timing diagram. The turn-on delay T_{PD-ON} is designed to be shorter than the turn-off delay T_{PD-OFF} because the rising time of the external turn-off switch can attribute to the additional delay time. It is also desirable to minimize T_{PD-ON} to favor the fast turn-off of the power MOSFET.

The LM5134 offers both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive signals in a single device type. Inputs of the LM5134 are TTL and CMOS Logic compatible and can withstand input voltages up to 14V regardless of the VDD voltage. This allows inputs of the LM5134 to be connected directly to most PWM controllers.

The LM5134 includes an Under-voltage Lockout (UVLO) circuit. When the VDD voltage is below the UVLO threshold voltage, the IN and INB inputs are ignored, and if there is sufficient VDD voltage, the OUT is pulled low. In addition, the LM5134 has an internal PNP transistor in parallel with the output NMOS. Under the UVLO condition, the PNP transistor will be on and clamp the OUT voltage below 1V. This feature ensures the OUT remains low even with insufficient VDD voltage.

Application Information

PILOT MOSFET Selection

In general, a small sized 20V MOSFET with logic level gates can be used as the external turn-off switch. To achieve a fast switching speed and avoid the potential shoot-through, it is suggested to select a MOSFET with the total gate charge less than 3nC. It is good practice to verify that no shoot-through occurs for the entire operating temperature range. In addition, a small Rds(on) is preferred to obtain the strong sink current capability. The power losses of the PILOT MOSFET can be estimated as:

$$P_g = 1/2 \times Q_{go} \times VDD \times F_{SW}$$

where

- Q_{go} is the total input gate charge of the power MOSFET (1)

Power Dissipation

It is important to keep the power consumption of the driver below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation of the LM5134 is the sum of the gate charge losses and the losses in the driver due to the internal CMOS stages used to buffer the output as well as the power losses associated with the quiescent current.

The gate charge losses include the power MOSFET gate charge losses as well as the PILOT FET gate charge losses and can be calculated as follows:

$$P_g = (Q_{go} + Q_{gp}) \times VDD \times F_{SW} \quad (2)$$

Or

$$P_g = (C_o + C_p) \times VDD^2 \times F_{SW}$$

where

- F_{sw} is switching frequency
- Q_{go} is the total input gate charge of the power MOSFET
- Q_{gp} is the total input gate charge of the PILOT MOSFET (3)

C_o and C_p are the load capacitance at OUT and PILOT outputs respectively. It should be noted that due to the use of an external turn-off switch, part of the gate charge losses are dissipated in the external turn-off switch. Therefore, the actual gate charge losses dissipated in the LM5134 is less than predicted by the above expressions. However, they are a good conservative design estimate.

The power dissipation associated with the internal circuit operation of the driver can be estimated with the characterization curves of the LM5134. For a given ambient temperature, the maximum allowable power losses of the IC can be defined as:

$$P = \frac{\left(T_J - T_A \right)}{\theta_{JA}} \quad (4)$$

where

- P is the total power dissipation of the driver

Layout Considerations

Attention must be given to board layout when using LM5134. Some important considerations include:

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the FETs gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate.
2. To reduce the loop inductance, the driver should be placed as close as possible to the FETs. The gate trace to and from the FETs are recommended to be placed closely side by side, or directly on top of one another.
3. A low ESR/ESL ceramic capacitor must be connected close to the IC, between VDD and VSS pins to support the high peak current being drawn from VDD during turn-on of the FETs. It is most desirable to place the VDD decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.
4. The parasitic source inductance, along with the gate capacitor and the driver pull-down path, can form a LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5134AMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		SK7A	Samples
LM5134AMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		SK7A	Samples
LM5134ASD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5134A	Samples
LM5134ASDX/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5134A	Samples
LM5134BMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		SK7B	Samples
LM5134BMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		SK7B	Samples
LM5134BSD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5134B	Samples
LM5134BSDX/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5134B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

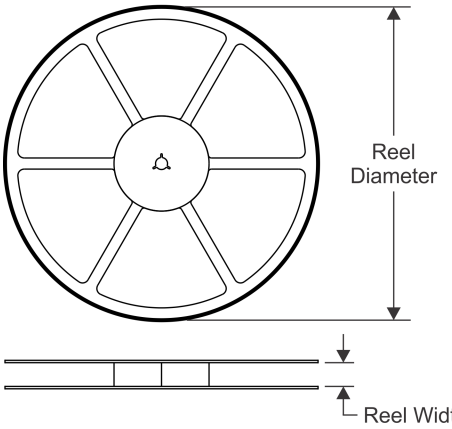
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

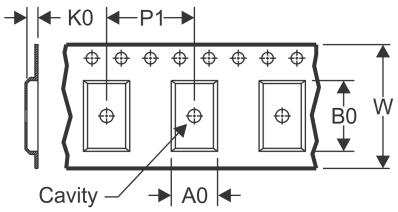
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

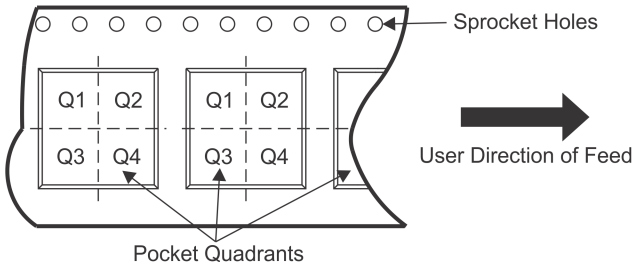


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

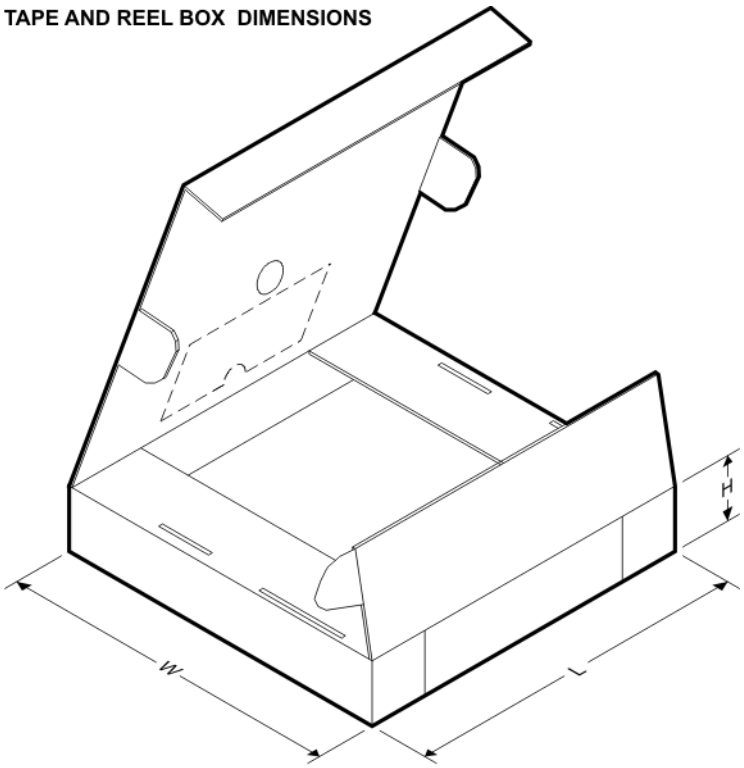
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5134AMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134AMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134ASD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5134ASDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5134BMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134BMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134BSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5134BSDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

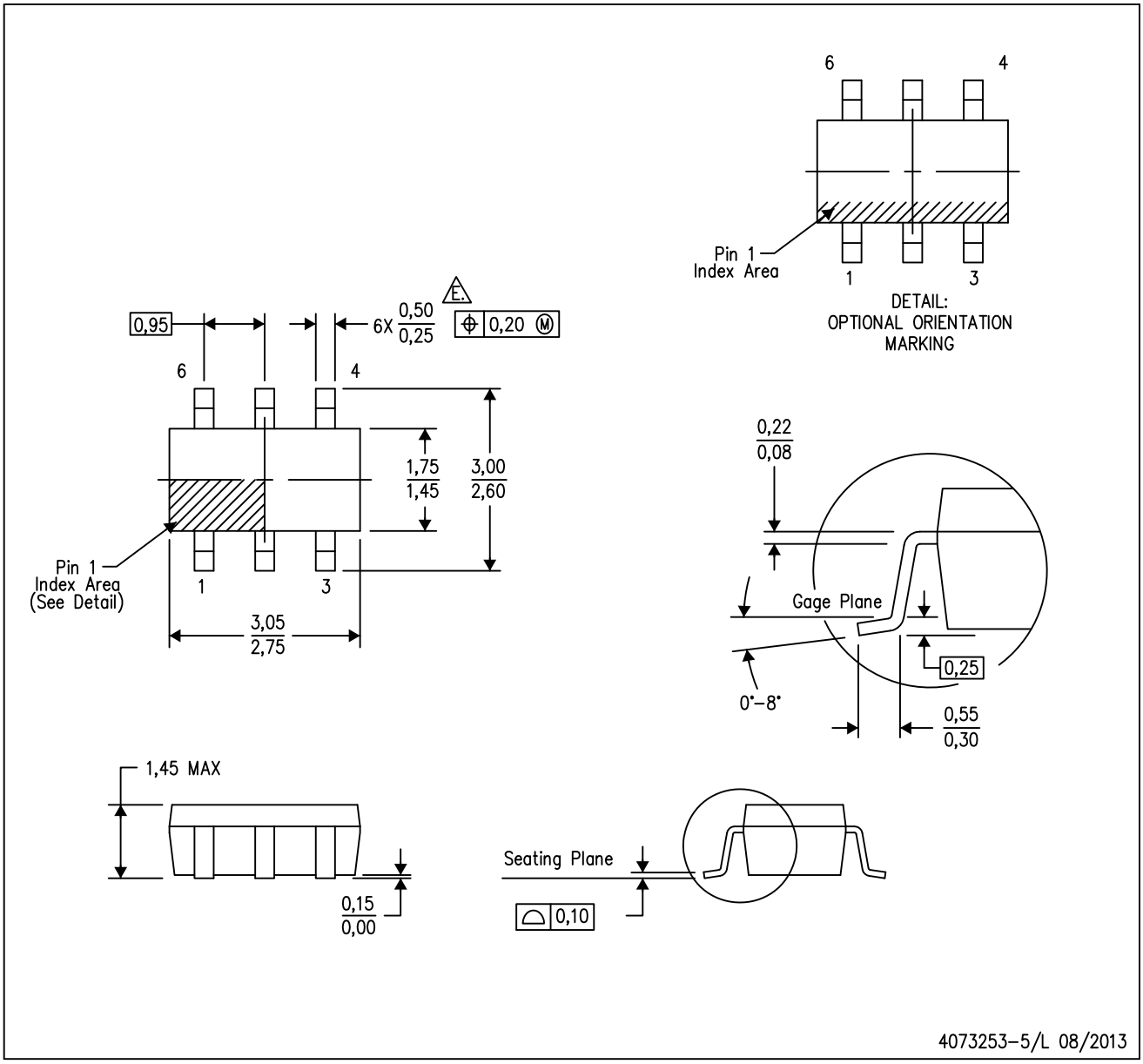
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

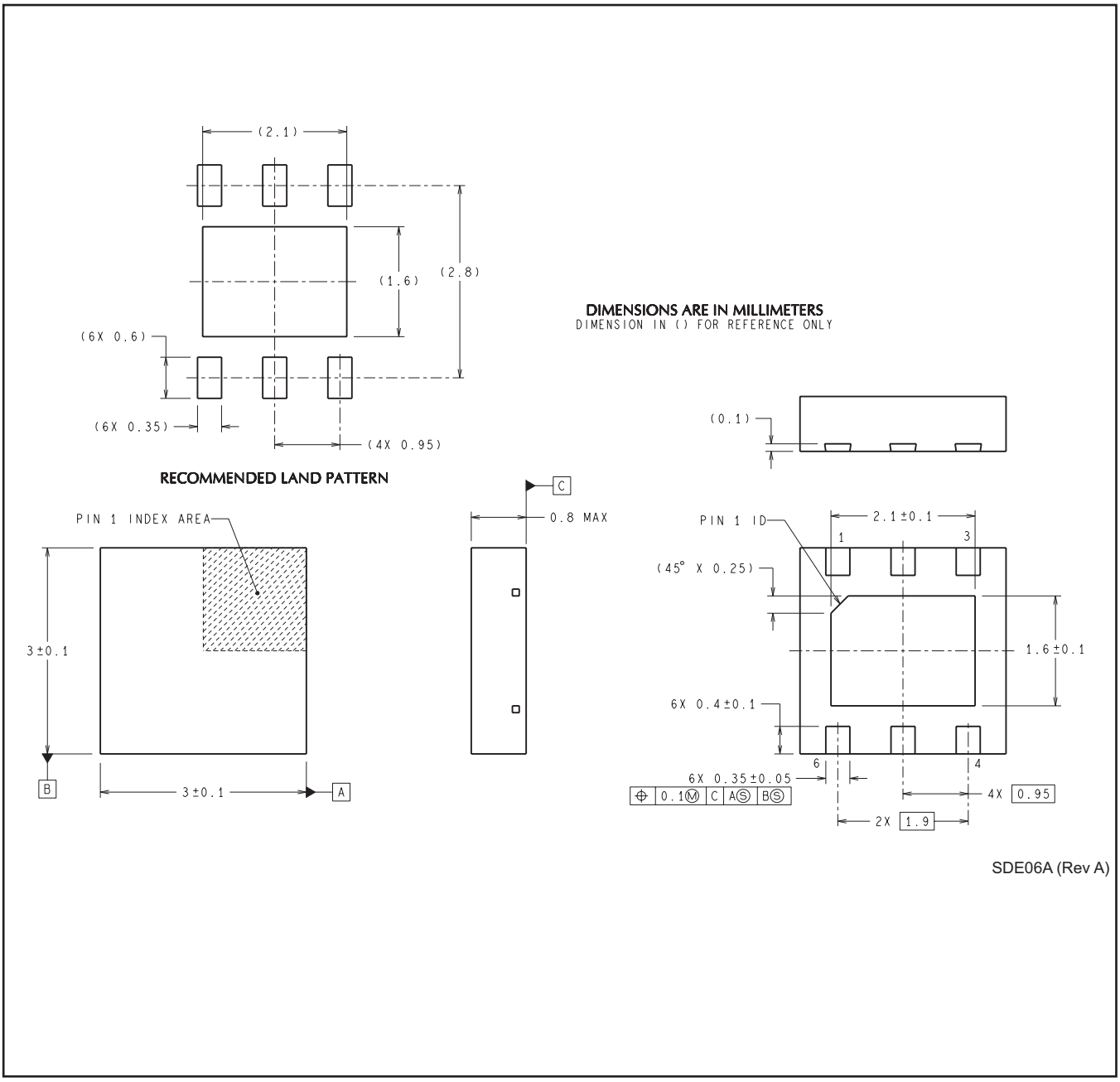
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5134AMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5134AMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5134ASD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM5134ASDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LM5134BMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5134BMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5134BSD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM5134BSDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

NGG0006A



SDE06A (Rev A)

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