LM6181 100 mA, 100 MHz Current Feedback Amplifier

Check for Samples: LM6181

FEATURES

- (Typical Unless Otherwise Noted)
- Slew Rate: 2000 V/μs
- Settling Time (0.1%): 50 ns
- Characterized for Supply Ranges: ±5V and ±15V
- Low Differential Gain and Phase Error: 0.05%, 0.04°
- High Output Drive: ±10V into 100Ω
- Ensured Bandwidth and Slew Rate
- Improved Performance Over EL2020, OP160, AD844, LT1223 and HA5004

APPLICATIONS

- Coax Cable Driver
- Video Amplifier
- Flash ADC Buffer
- High Frequency Filter
- Scanner and Imaging Systems

DESCRIPTION

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin PDIP high-speed amplifier making it ideal for video applications.

Built on TI's advanced high-speed VIP™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at A_V = −1, 60 MHz at A_V = −10. With a slew rate of 2000V/μs, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

Typical Application

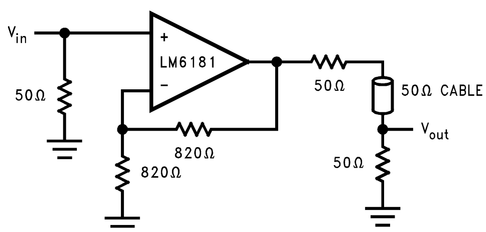
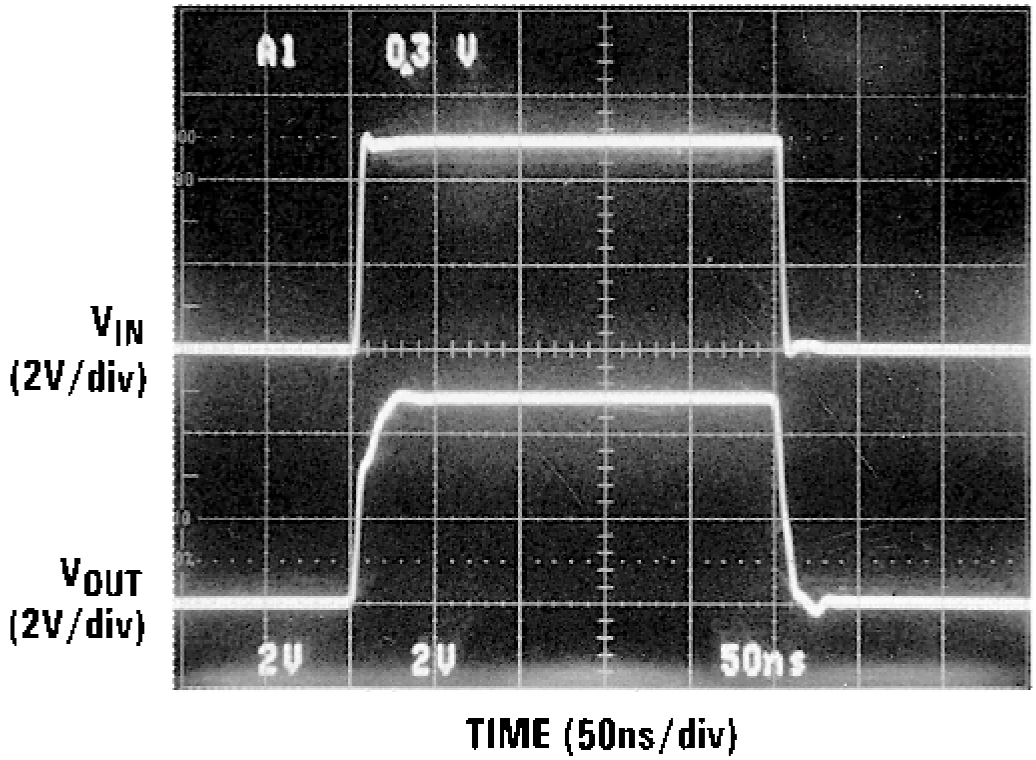


Figure 1. Cable Driver



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage			±18V
Differential Input Voltage			±6V
Input Voltage			±Supply Voltage
Inverting Input Current			15 mA
Soldering Information	PDIP Package (N)	Soldering (10 sec)	260°C
	SOIC Package (M)	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Output Short Circuit			See[3]
Storage Temperature Range			$-65°C \leq T_J \leq +150°C$
Maximum Junction Temperature			150°C
ESD Rating[4]			±3000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be ensured under these conditions. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±130 mA over a long term basis may adversely affect reliability.
(4) Human body model 100 pF and 1.5 kΩ.

Operating Ratings[1]

Supply Voltage Range		7V to 32V
Junction Temperature Range[2]	LM6181AM	$-55°C \leq T_J \leq +125°C$
	LM6181AI, LM6181I	$-40°C \leq T_J \leq +85°C$
Thermal Resistance (θ_{JA}, θ_{JC})	8-pin PDIP (N)	102°C/W, 42°C/W
	8-pin SOIC (M-8)	153°C/W, 42°C/W
	16-pin SOIC (M)	70°C/W, 38°C/W

(1) For ensured Military Temperature Range parameters see RETS6181X.
(2) The typical junction-to-ambient thermal resistance of the molded PDIP(N) package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the SOIC (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in^2 1 oz. copper trace. The 16-pin SOIC (M) package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V^- for proper operation. The typical junction-to-ambient thermal resistance of the SOIC (M-8) package soldered directly into a PC board is 153°C/W.

±15V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (1)	Limit (2)	Typical (1)	Limit (2)	Typical (1)	Limit (2)	
V_{OS}	Input Offset Voltage		2.0	3.0 **4.0**	2.0	3.0 **3.5**	3.5	5.0 **5.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		5.0		5.0		5.0		μV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	2.0	5.0 **12.0**	5.0	10 **17.0**	μA max
	Non-Inverting Input Bias Current		0.5	1.5 **3.0**	0.5	1.5 **3.0**	2.0	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		30		30		30		nA/°C
	Non-Inverting Input Bias Current Drift		10		10		10		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.3	0.5 **3.0**	0.3	0.5 **3.0**	0.3	0.75 **4.5**	μA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.05	0.5 **1.5**	0.05	0.5 **1.5**	0.05	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−10V ≤ V_{CM} ≤ +10V	0.3	0.5 **0.75**	0.3	0.5 **0.75**	0.3	0.75 **1.0**	
	Non-Inverting Input Bias Current Common Mode Rejection	−10V ≤ V_{CM} ≤ +10V	0.1	0.5 **0.5**	0.1	0.5 **0.5**	0.1	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	60	50 **50**	60	50 **50**	60	50 **50**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V, ±16V	80	70 **70**	80	70 **70**	80	70 **65**	dB min
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.2		0.2		0.2		Ω
R_{IN}	Non-Inverting Input Resistance		10		10		10		MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	12	11 **11**	12	11 **11**	12	11 **11**	V min
		R_L = 100Ω	11	10 **7.5**	11	10 **8.0**	11	10 **8.0**	
I_{SC}	Output Short Circuit Current		130	100 **75**	130	100 **85**	130	100 **85**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.5**	1.8	1.0 **0.5**	1.8	0.8 **0.4**	MΩ min
		R_L = 100Ω	1.4	0.8 **0.4**	1.4	0.8 **0.4**	1.4	0.7 **0.35**	
I_S	Supply Current	No Load, V_O = 0V	7.5	10 **10**	7.5	10 **10**	7.5	10 **10**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

±15V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, R_F = 820Ω, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (1)	Limit (2)	Typical (1)	Limit (2)	Typical (1)	Limit (2)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100		100		100		MHz min
		A_V = +10	80		80		80		
		A_V = −1	100	80	100	80	100	80	
		A_V = −10	60		60		60		
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60		60		60		
SR	Slew Rate	Overdriven	2000		2000		2000		V/µs min
		A_V = −1, V_O = ±10V, R_L = 150Ω (3)	1400	1000	1400	1000	1400	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5		5		5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6		6		6		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(−)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		pA/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−50		−50		−50		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−50		
	Differential Gain	R_L = 150Ω							%
		A_V = +2	0.05		0.05		0.05		
		NTSC							
	Differential Phase	R_L = 150Ω							Deg
		A_V = +2	0.04		0.04		0.04		
		NTSC							

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.
(3) Measured from +25% to +75% of output waveform.

±5V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (1)	Limit (2)	Typical (1)	Limit (2)	Typical (1)	Limit (2)	
V_{OS}	Input Offset Voltage		1.0	2.0 **3.0**	1.0	2.0 **2.5**	1.0	3.0 **3.5**	mV max
TC V_{OS}	Input Offset Voltage Drift		2.5		2.5		2.5		μV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	5.0	10 **22**	5.0	17.5 **27.0**	μA max
	Non-Inverting Input Bias Current		0.25	1.5 **1.5**	0.25	1.5 **1.5**	0.25	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		50		50		50		nA/°C
	Non-Inverting Input Bias Current Drift		3.0		3.0		3.0		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.3	0.5 **0.5**	0.3	0.5 **0.5**	0.3	1.0 **1.0**	μA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.05	0.5 **0.5**	0.05	0.5 **0.5**	0.05	0.5 **0.5**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.3	0.5 **1.0**	0.3	0.5 **1.0**	0.3	1.0 **1.5**	
	Non-Inverting Input Bias Current Common Mode Rejection	−2.5V ≤ V_{CM} ≤ +2.5V	0.12	0.5 **1.0**	0.12	0.5 **0.5**	0.12	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	−2.5V ≤ V_{CM} ≤ +2.5V	57	50 **47**	57	50 **47**	57	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.0V, ±6.0V	80	70 **70**	80	70 **70**	80	64 **64**	
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.25		0.25		0.25		Ω
R_{IN}	Non-Inverting Input Resistance		8		8		8		MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.2**	2.6	2.25 **2.25**	2.6	2.25 **2.25**	V min
		R_L = 100Ω	2.2	2.0 **2.0**	2.2	2.0 **2.0**	2.2	2.0 **2.0**	
I_{SC}	Output Short Circuit Current		100	75 **70**	100	75 **70**	100	75 **70**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.35**	1.4	0.75 **0.4**	1.0	0.6 **0.3**	MΩ min
		R_L = 100Ω	1.0	0.5 **0.25**	1.0	0.5 **0.25**	1.0	0.4 **0.2**	
I_S	Supply Current	No Load, V_O = 0V	6.5	8.5 **8.5**	6.5	8.5 **8.5**	6.5	8.5 **8.5**	mA max
V_{CM}	Input Common Mode Voltage Range		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V^+ − 1.7V V^- + 1.7V		V

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

±5V AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, R_F = 820Ω, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (1)	Limit (2)	Typical (1)	Limit (2)	Typical (1)	Limit (2)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50		50		50		MHz min
		A_V = +10	40		40		40		
		A_V = −1	55	35	55	35	55	35	
		A_V = −10	35		35		35		
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40		40		40		
SR	Slew Rate	A_V = −1, V_O = ±2V, R_L = 150Ω (3)	500	375	500	375	500	375	V/μs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5		8.5		8.5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8		8		8		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		pA/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−45		−45		−45		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−55		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.063		0.063		0.063		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.16		0.16		0.16		Deg

(1) Typical values represent the most likely parametric norm.
(2) All limits ensured at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.
(3) Measured from +25% to +75% of output waveform.

Typical Performance Characteristics

T_A = 25°C unless otherwise noted

CLOSED-LOOP FREQUENCY RESPONSE V_S = ±15V; R_f = 820Ω; R_L = 1 kΩ

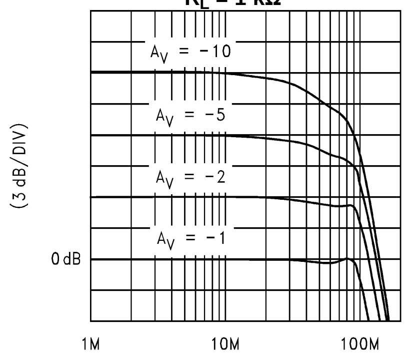


Figure 2.

CLOSED-LOOP FREQUENCY RESPONSE V_S = ±15V; R_f = 820Ω; R_L = 150Ω

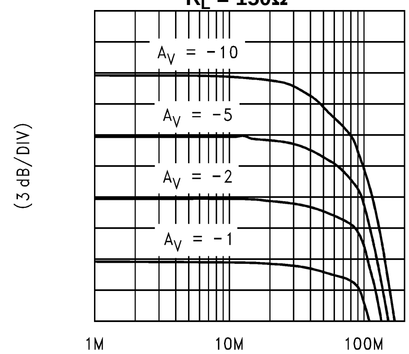


Figure 3.

UNITY GAIN FREQUENCY RESPONSE V_S = ±15V; A_V = +1; R_f = 820Ω

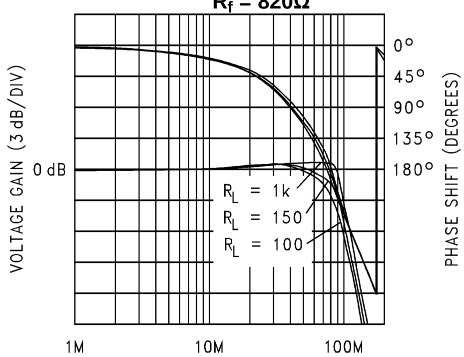


Figure 4.

UNIT GAIN FREQUENCY RESPONSE V_S = ±5V; A_V = +1; R_f = 820Ω

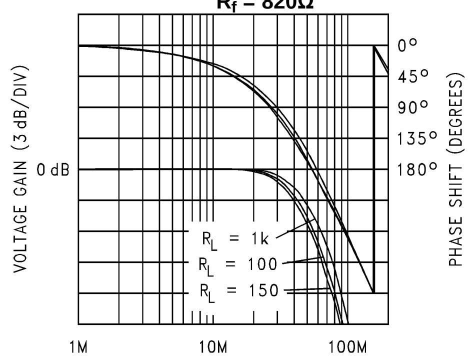


Figure 5.

FREQUENCY RESPONSE vs SUPPLY VOLTAGE A_V = −1; R_f = 820Ω; R_L = 1 kΩ

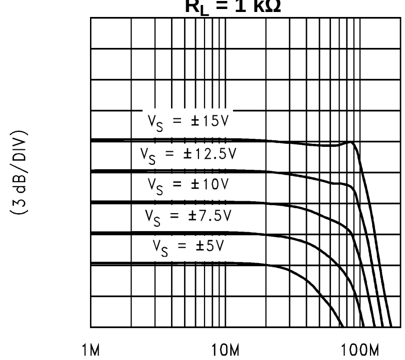


Figure 6.

FREQUENCY RESPONSE vs SUPPLY VOLTAGE A_V = −1; R_f = 820Ω; R_L = 150Ω

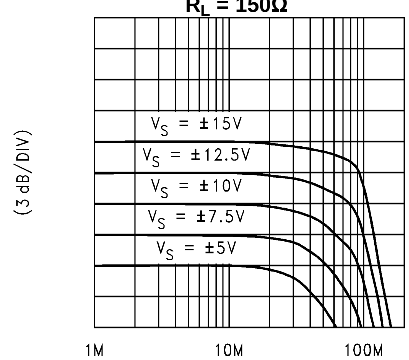


Figure 7.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

INVERTING GAIN FREQUENCY RESPONSE V_S = ±15V; A_V = −1; R_f = 820Ω

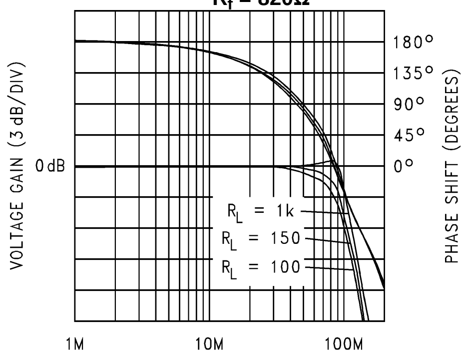


Figure 8.

INVERTING GAIN FREQUENCY RESPONSE V_S = ±5V; A_V = −1; R_f = 820Ω

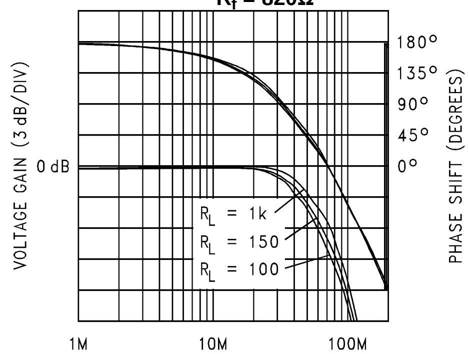


Figure 9.

NON-INVERTING GAIN FREQUENCY RESPONSE V_S = ±15V; A_V = +2; R_f = 820Ω

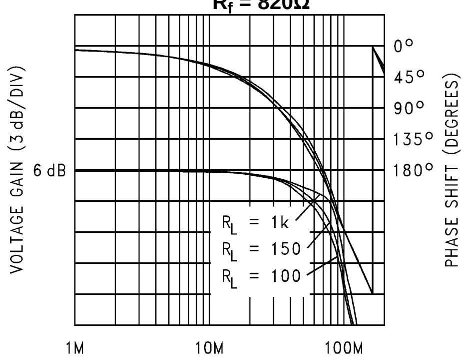


Figure 10.

NON-INVERTING GAIN FREQUENCY RESPONSE V_S = ±5V; A_V = +2; R_f = 820Ω

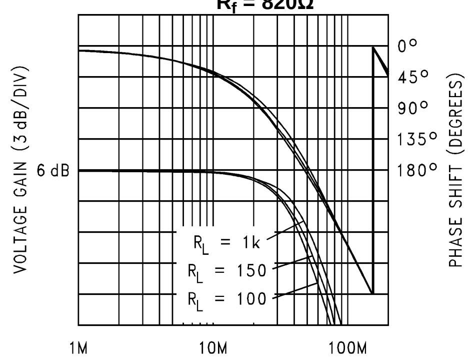


Figure 11.

INVERTING GAIN FREQUENCY RESPONSE V_S = ±15V; A_V = −10; R_f = 820Ω

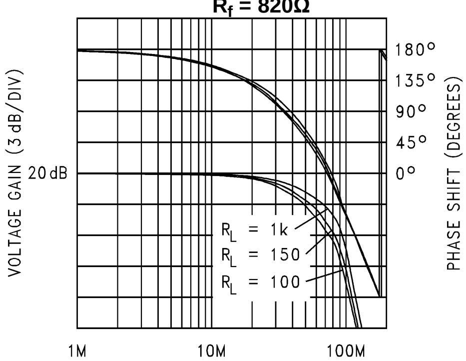


Figure 12.

INVERTING GAIN FREQUENCY RESPONSE V_S = ±5V; A_V = −10; R_f = 820Ω

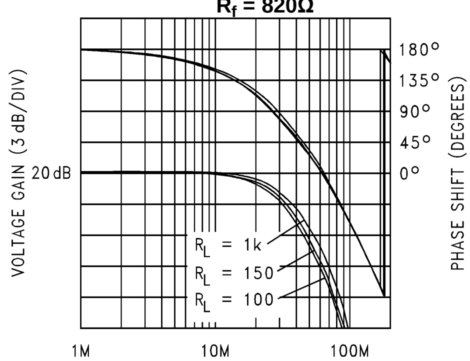


Figure 13.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

NON-INVERTING GAIN FREQUENCY RESPONSE V_S = ±15V; A_V = +10; R_f = 820Ω

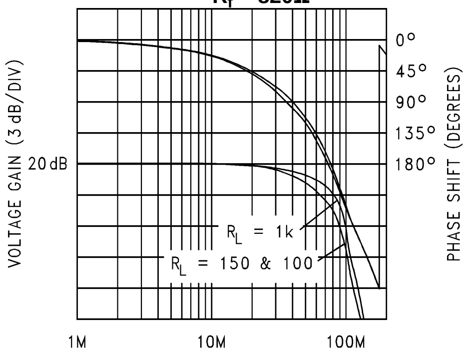


Figure 14.

NON-INVERTING GAIN FREQUENCY RESPONSE V_S = ±5V; A_V = +10; R_f = 820Ω

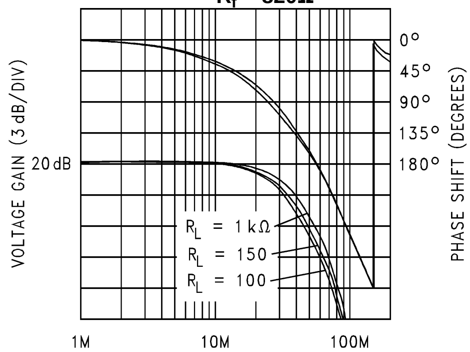


Figure 15.

NON-INVERTING GAIN FREQUENCY COMPENSATION V_S = ±15V; A_V = +2; R_L = 150Ω

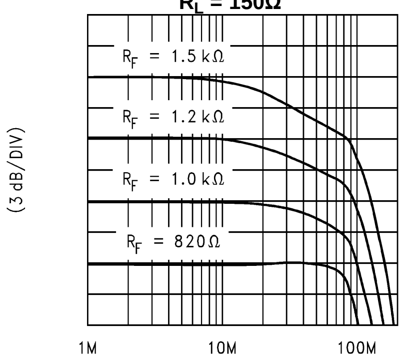


Figure 16.

BANDWIDTH vs R_f & R_S A_V = −1, R_L = 1 kΩ

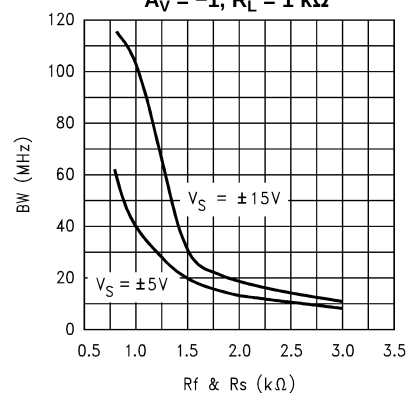


Figure 17.

OUTPUT SWING vs R_{LOAD} PULSED, V_S = ±15V, I_{IN} = ±200 µA, V_{IN+} = 0V

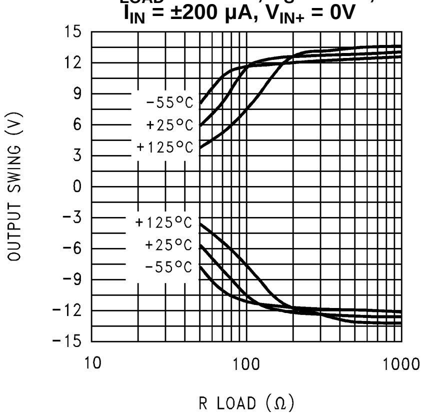


Figure 18.

TRANSIMPEDANCE vs FREQUENCY V_S = ±15V R_L = 1 kΩ

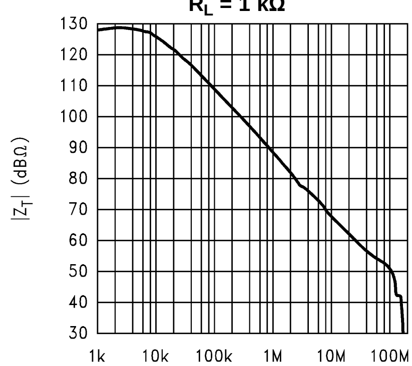


Figure 19.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

TRANSIMPEDANCE vs FREQUENCY
V_S = ±15V
R_L = 100Ω

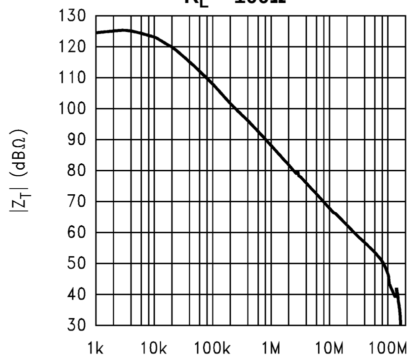


Figure 20.

TRANSIMPEDANCE vs FREQUENCY
V_S = ±5V
R_L = 1 kΩ

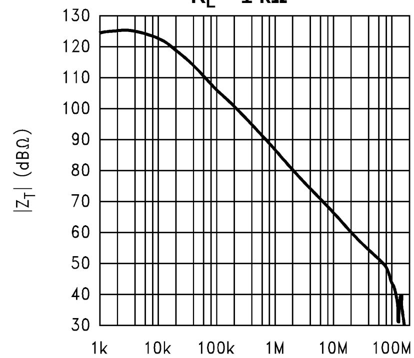


Figure 21.

SETTLING RESPONSE
V_S = ±15V; R_L = 150Ω;
V_O = ±5V; A_V = −1

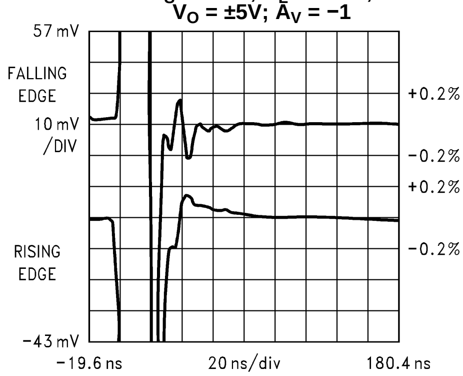


Figure 22.

SETTLING RESPONSE
V_S = ±5V; R_L = 150Ω;
V_O = ±2V; A_V = −1

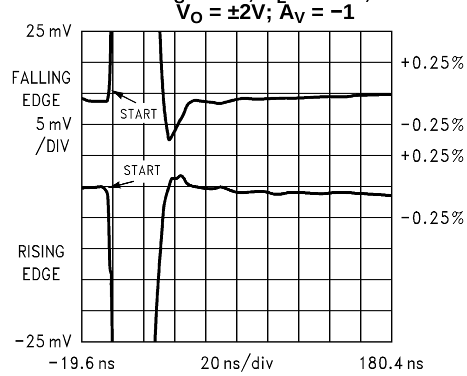


Figure 23.

SUGGESTED R_f and R_S for C_L
A_V = − 1; R_L = 150Ω

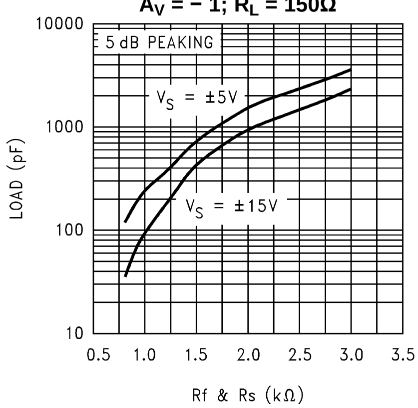


Figure 24.

TRANSIMPEDANCE vs FREQUENCY
V_S = ±5V
R_L = 100Ω

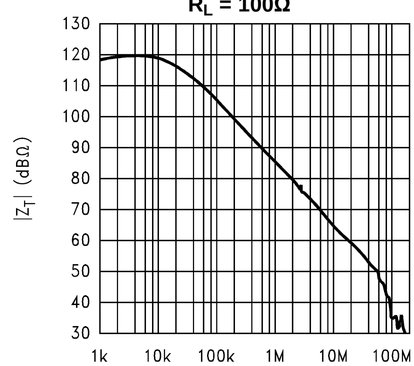


Figure 25.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

SUGGESTED R_f and R_S FOR C_L $A_V = -1$

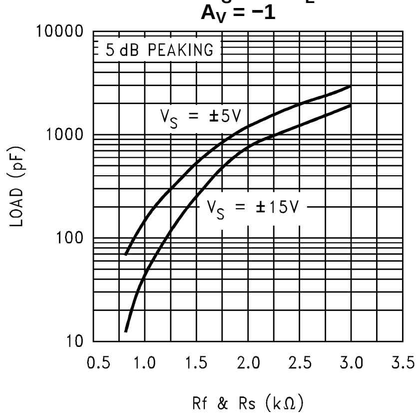


Figure 26.

SUGGESTED R_f and R_S FOR C_L $A_V = +2$; $R_L = 150\Omega$

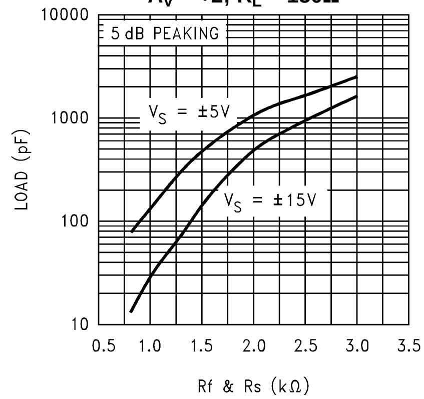


Figure 27.

SUGGESTED R_f and R_S FOR C_L $A_V = +2$

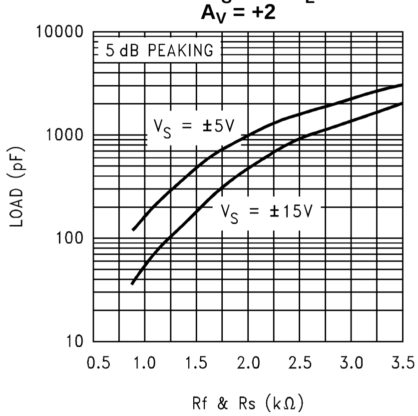


Figure 28.

OUTPUT IMPEDANCE vs FREQ $V_S = \pm15V$; $A_V = -1$ $R_f = 820\Omega$

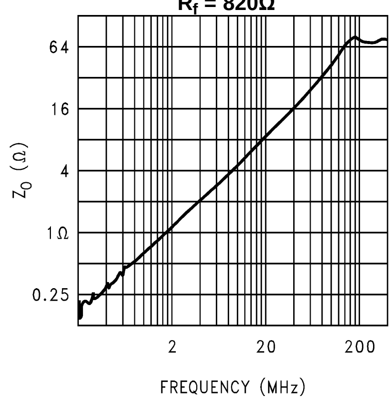


Figure 29.

OUTPUT IMPEDANCE vs FREQ $V_S = \pm5V$; $A_V = -1$ $R_f = 820\Omega$

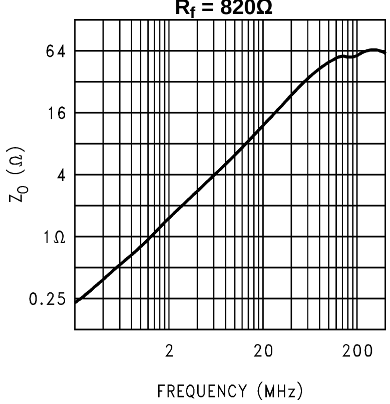


Figure 30.

PSRR (V_S^+) vs FREQUENCY

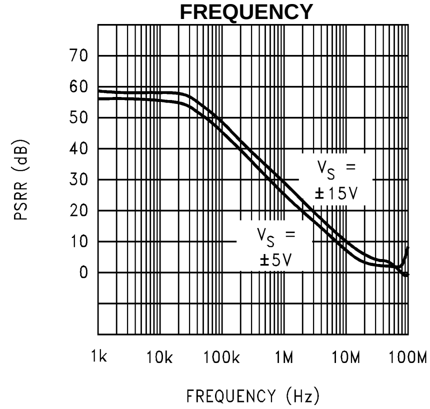


Figure 31.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

PSRR (V_S^-) vs FREQUENCY

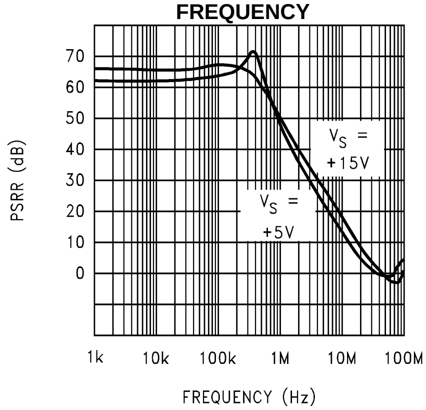


Figure 32.

CMRR vs FREQUENCY

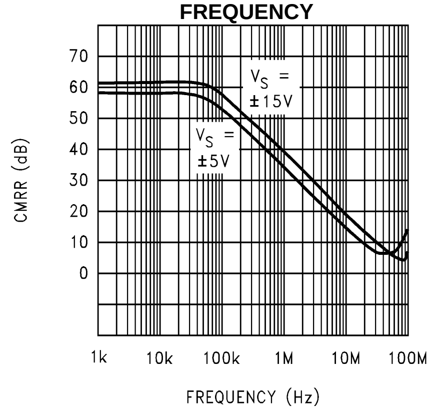


Figure 33.

INPUT VOLTAGE NOISE vs FREQUENCY

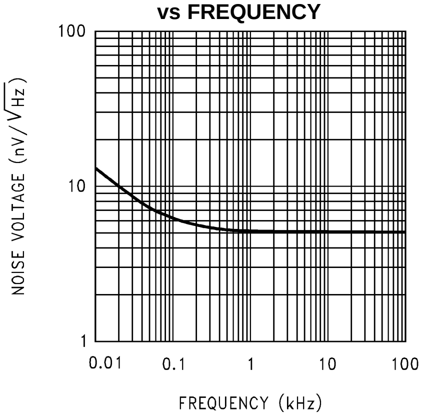


Figure 34.

INPUT CURRENT NOISE vs FREQUENCY

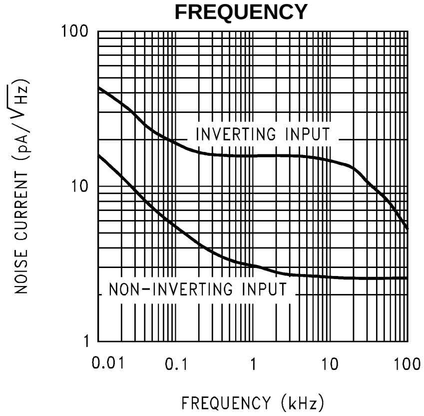


Figure 35.

SLEW RATE vs TEMPERATURE A_V = −1; R_L = 150Ω, V_S = ±15V

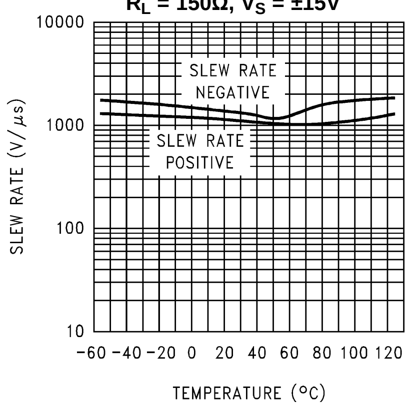


Figure 36.

SLEW RATE vs TEMPERATURE A_V = −1; R_L = 150Ω, V_S = ±5V

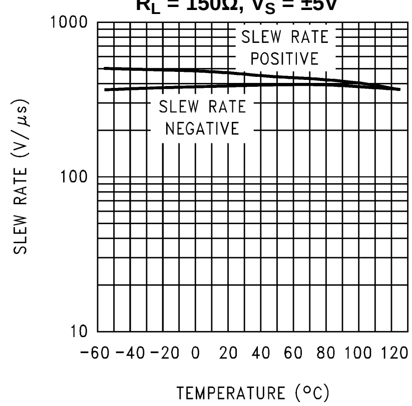


Figure 37.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

−3 dB BANDWIDTH vs TEMPERATURE $A_V = -1$

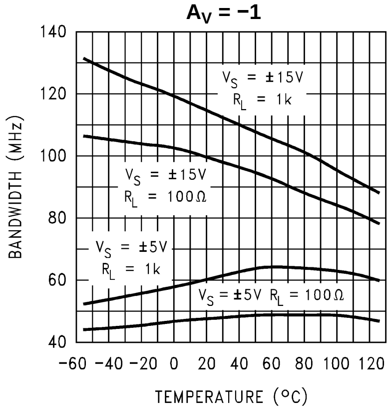


Figure 38.

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 1\ k\Omega$

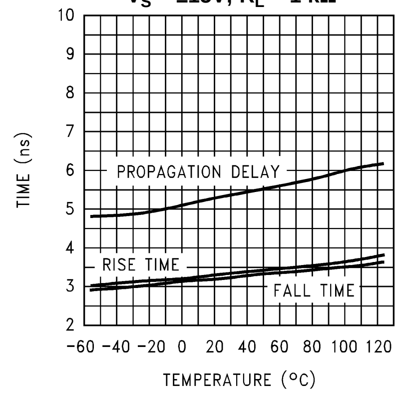


Figure 39.

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 100\Omega$

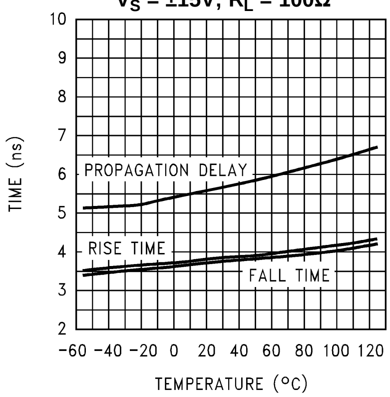


Figure 40.

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 1\ k\Omega$

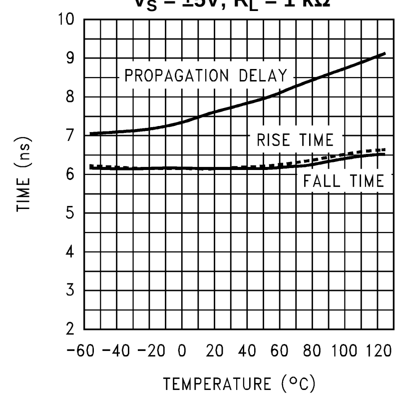


Figure 41.

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 100\Omega$

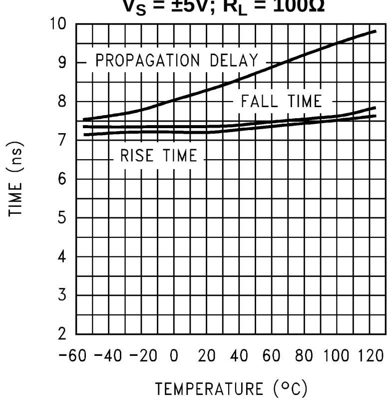


Figure 42.

SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm15V$; $R_L = 1\ k\Omega$

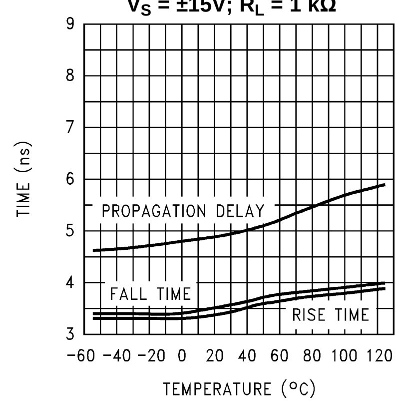


Figure 43.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −1, V_S = ±15V; R_L = 100Ω

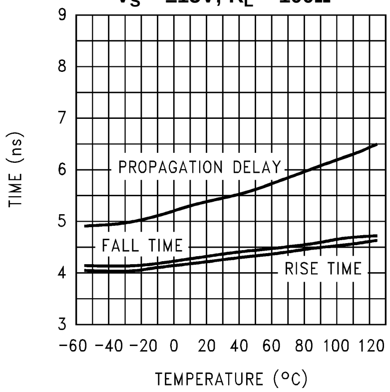


Figure 44.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −1, V_S = ±5V; R_L = 1 kΩ

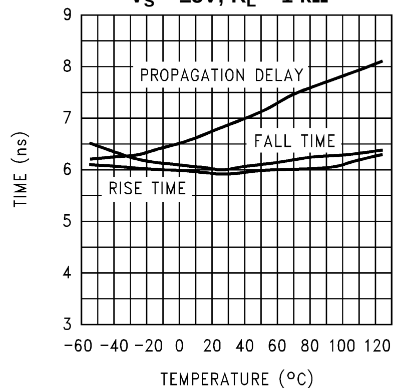


Figure 45.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −1, V_S = ±5V; R_L = 100Ω

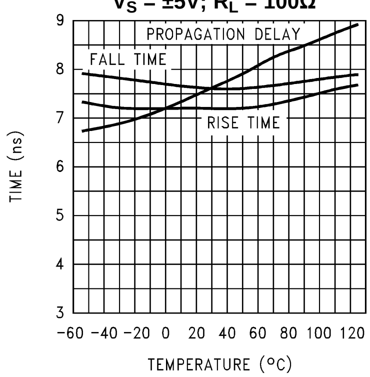


Figure 46.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2, V_S = ±15V; R_L = 1 kΩ

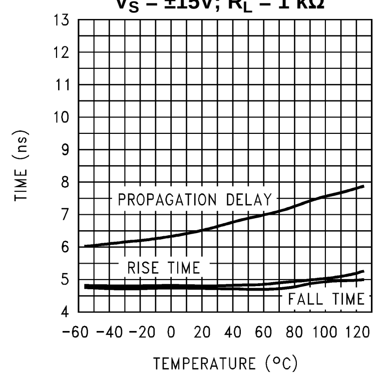


Figure 47.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2, V_S = ±15V; R_L = 100Ω

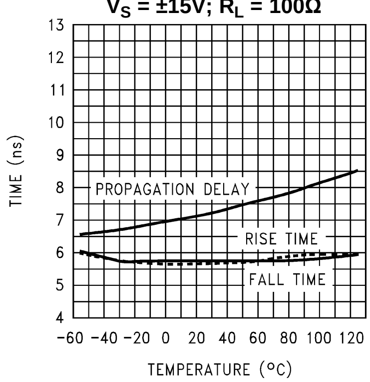


Figure 48.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2, V_S = ±5V; R_L = 1 kΩ

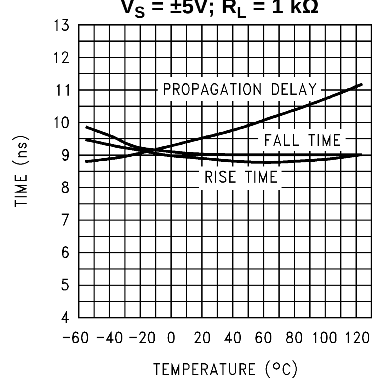


Figure 49.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +2 V_S = ±5V; R_L = 100Ω

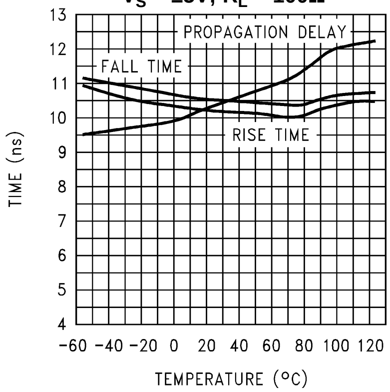


Figure 50.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10 V_S = ±15V; R_L = 1 kΩ

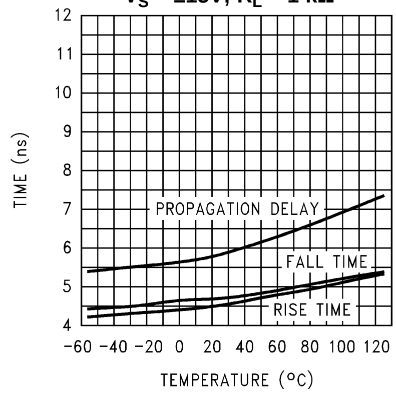


Figure 51.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10 V_S = ±15V; R_L = 100Ω

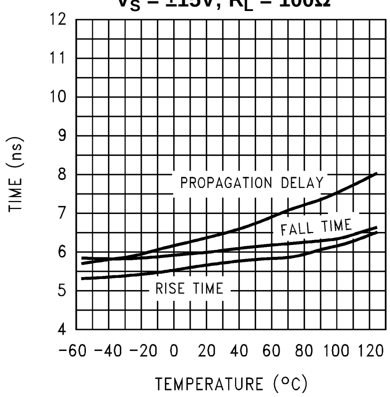


Figure 52.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10 V_S = ±5V; R_L = 1 kΩ

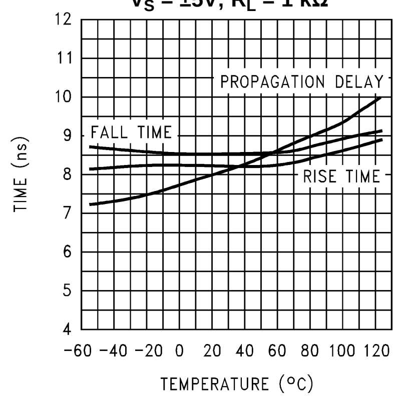


Figure 53.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = −10 V_S = ±5V; R_L = 100Ω

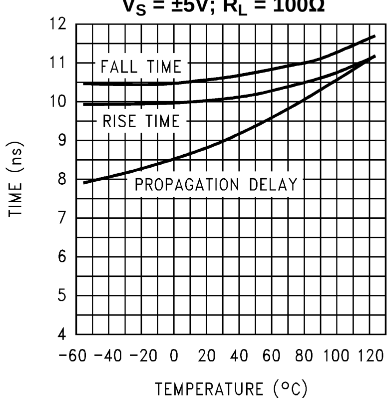


Figure 54.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10 V_S = ±15V; R_L = 1 kΩ

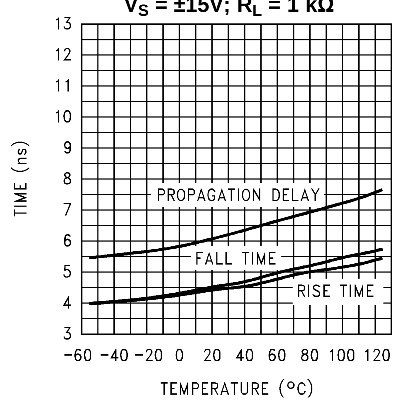


Figure 55.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10 V_S = ±15V; R_L = 100Ω

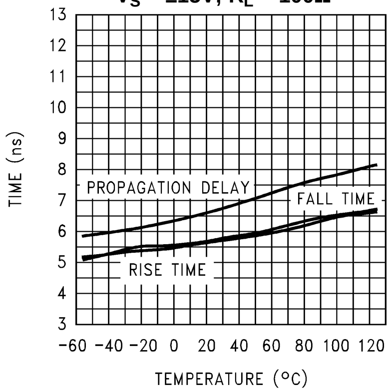


Figure 56.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10 V_S = ±5V; R_L = 1 kΩ

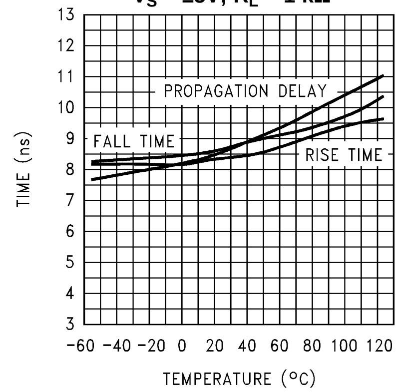


Figure 57.

SMALL SIGNAL PULSE RESPONSE vs TEMP, A_V = +10 V_S = ±5V; R_L = 100Ω

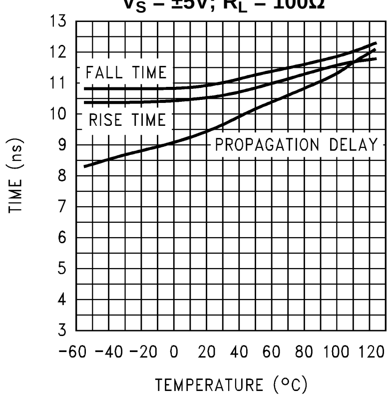


Figure 58.

OFFSET VOLTAGE vs TEMPERATURE

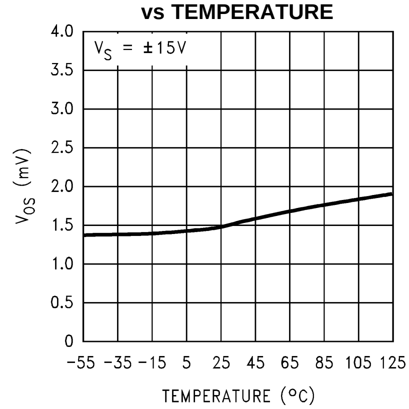


Figure 59.

OFFSET VOLTAGE vs TEMPERATURE

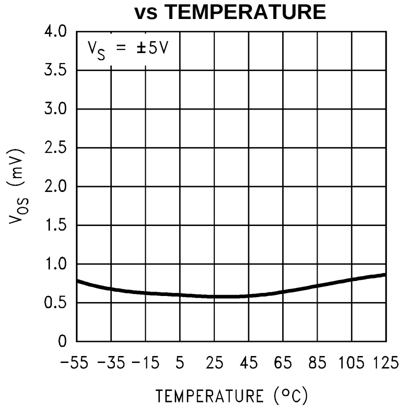


Figure 60.

TRANSIMPEDANCE vs TEMPERATURE

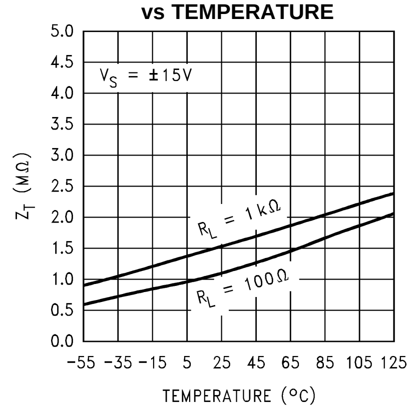


Figure 61.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

TRANSIMPEDANCE vs TEMPERATURE

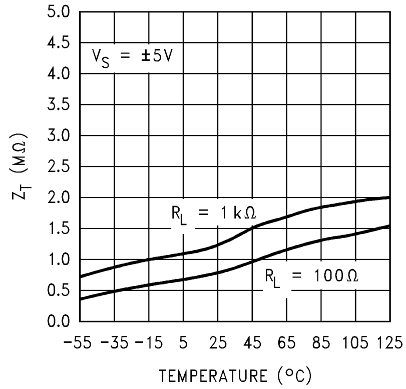


Figure 62.

QUIESCENT CURRENT vs TEMPERATURE

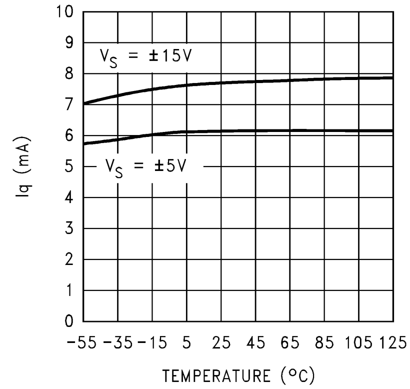


Figure 63.

PSRR vs TEMPERATURE

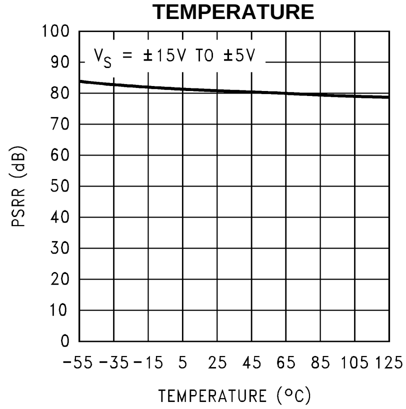


Figure 64.

CMRR vs TEMPERATURE

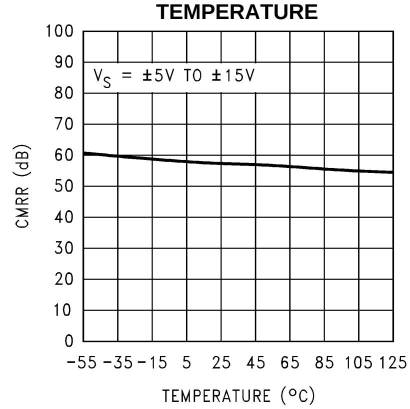


Figure 65.

NON-INVERTING BIAS CURRENT vs TEMPERATURE

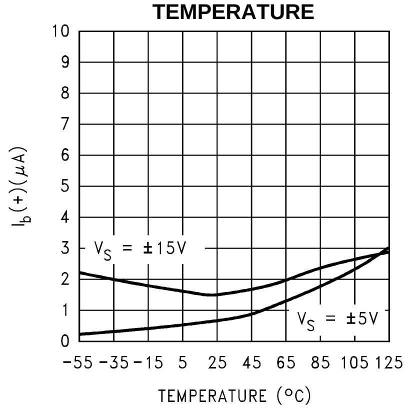


Figure 66.

INVERTING BIAS CURRENT vs TEMPERATURE

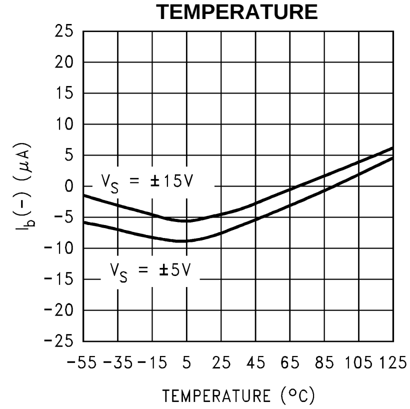


Figure 67.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

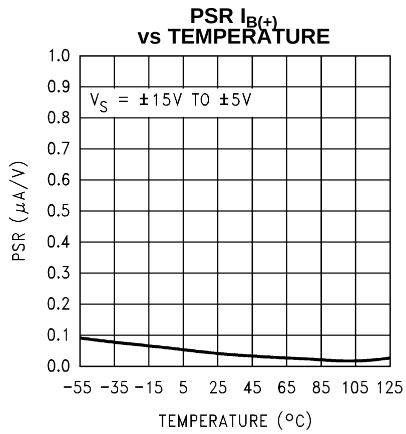


Figure 68.

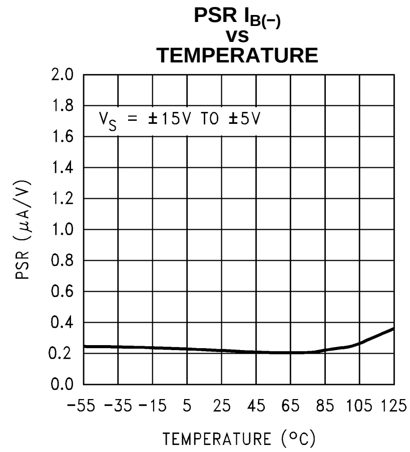


Figure 69.

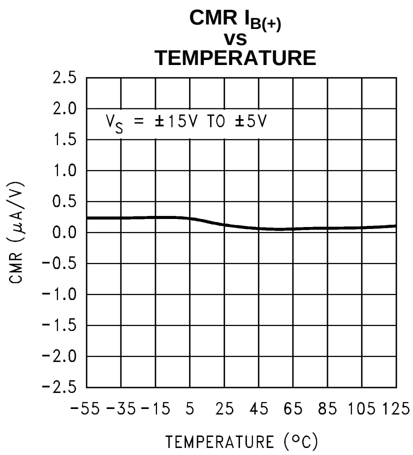


Figure 70.

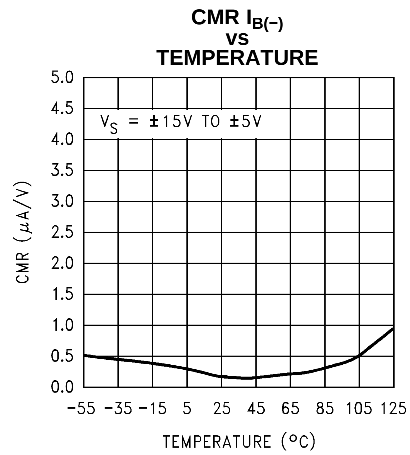


Figure 71.

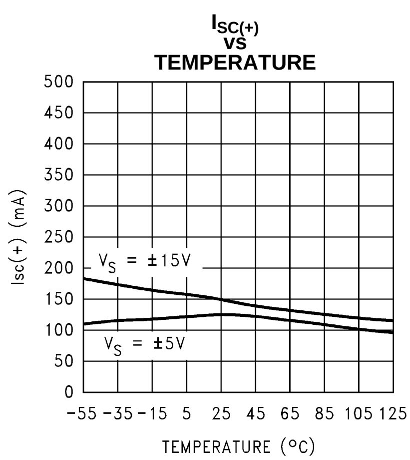


Figure .

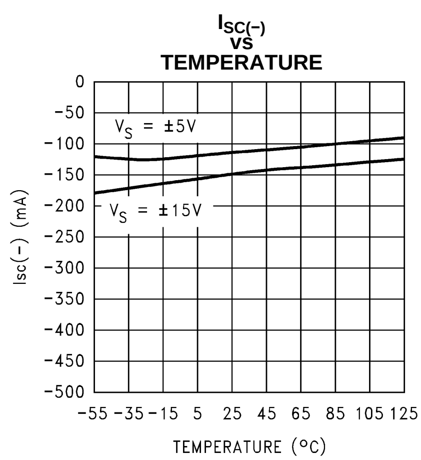


Figure 72.

Typical Performance Characteristics (continued)

T_A = 25°C unless otherwise noted

Absolute Maximum Power Derating Curves

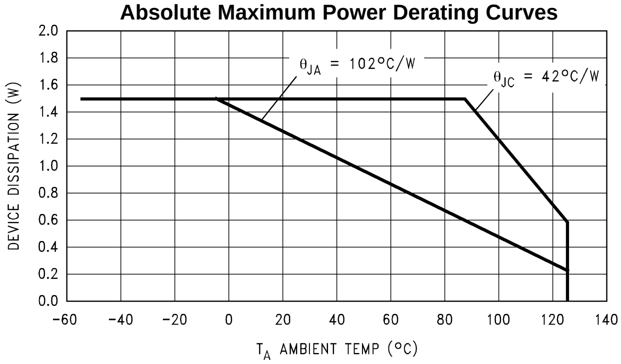
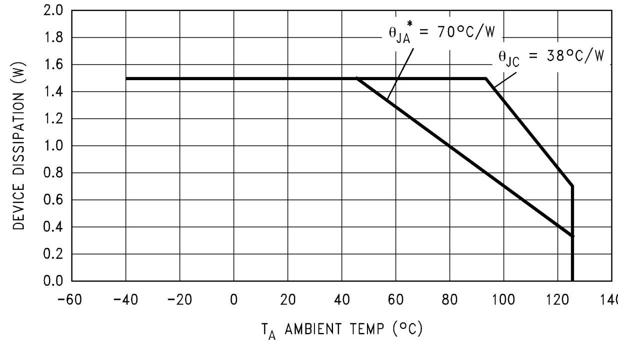


Figure 73. N-Package



*θ_{JA} = Thermal Resistance with 2 square inches of 1 ounce Copper tied to Pins 1, 8, 9 and 16.

Figure 74. M-Package

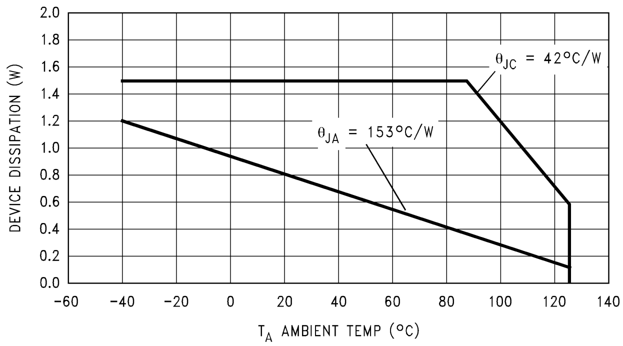


Figure 75. M-8 Package

Simplified Schematic

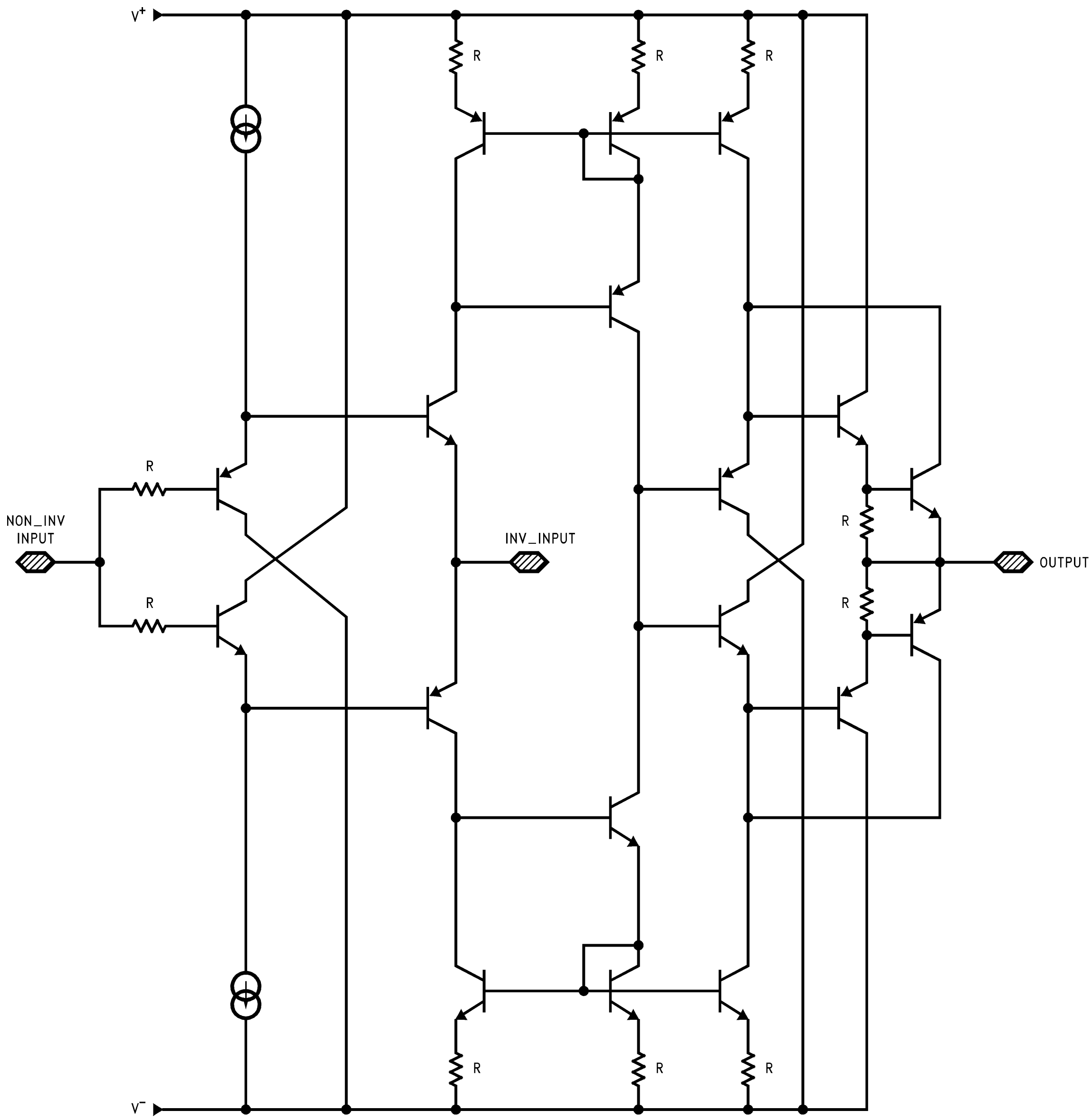


Figure 76.

TYPICAL APPLICATIONS

CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6181, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed-loop gain. Figure 77 and Figure 78 illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.

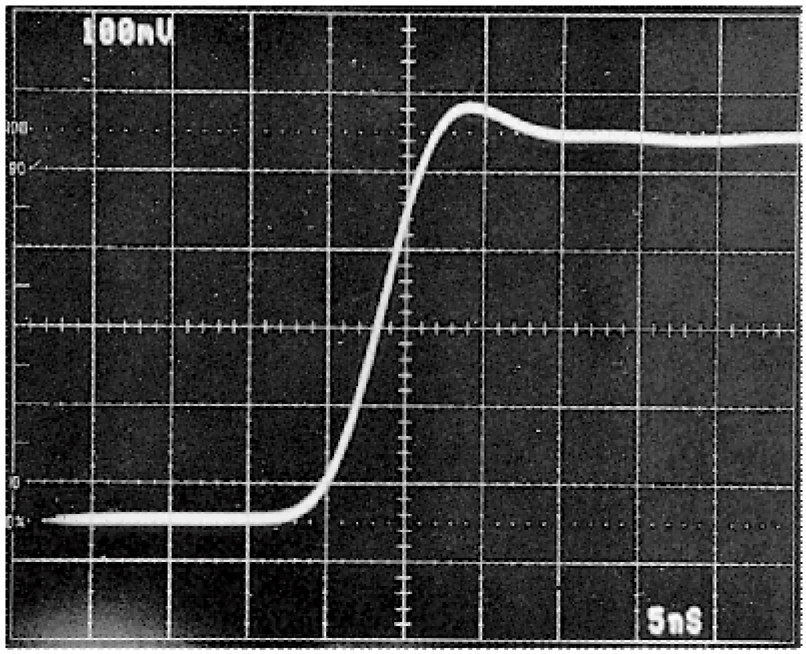
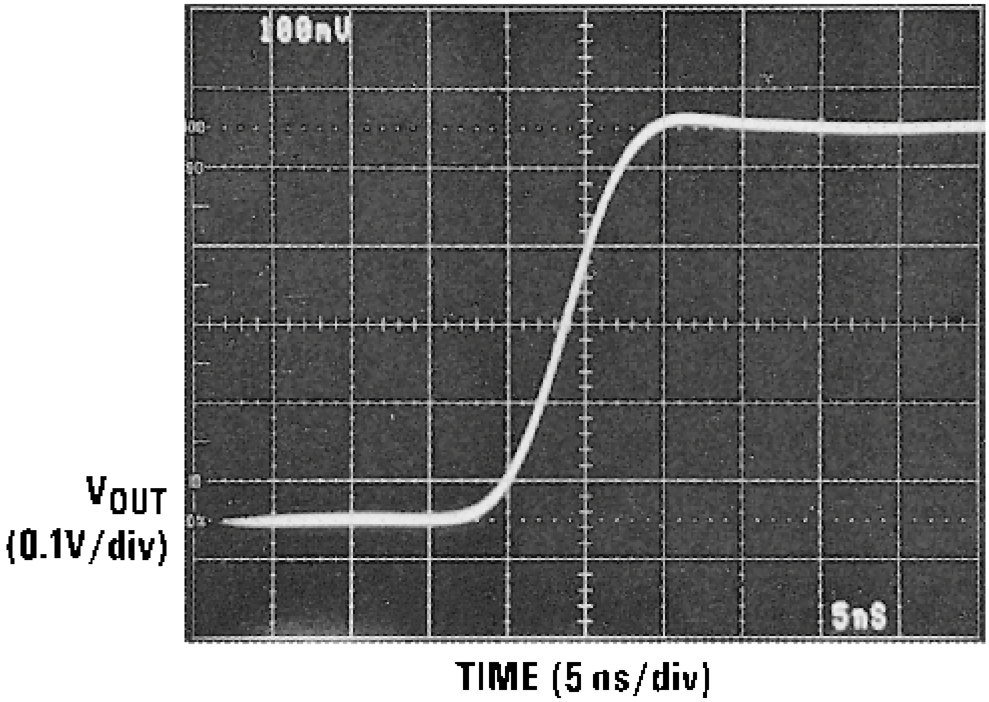


Figure 77.



Variation of Closed Loop Gain
from −1 to −5 Yields Similar Responses

Figure 78.

The closed-loop bandwidth of the LM6181 depends on the feedback resistance, R_f. Therefore, R_S and not R_f, must be varied to adjust for the desired closed-loop gain as in Figure 79.

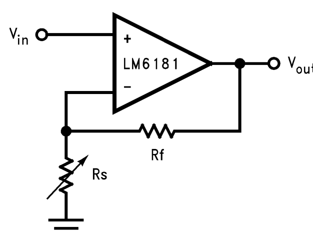


Figure 79. R_S Is Adjusted to Obtain the Desired Closed Loop Gain, A_{VCL}

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 10 μF tantalum and 0.1 μF ceramic bypass capacitors are recommended for each supply pin. The bypass capacitors should be placed as close to the amplifier pins as possible (0.5″ or less).

FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6181. For general applications the LM6181 will maintain specified performance with an 820Ω feedback resistor. Although this value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are 2 and the feedback resistors are 820Ω and 1640Ω, respectively. Figure 80 and Figure 81 illustrate the effect of increasing

R_f while maintaining the same closed-loop gain—the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6181 (see −3 dB bandwidth vs R_f typical curves) and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed loop gains, due to 2nd order effects. For example Figure 82 illustrates reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed loop gain of 25.

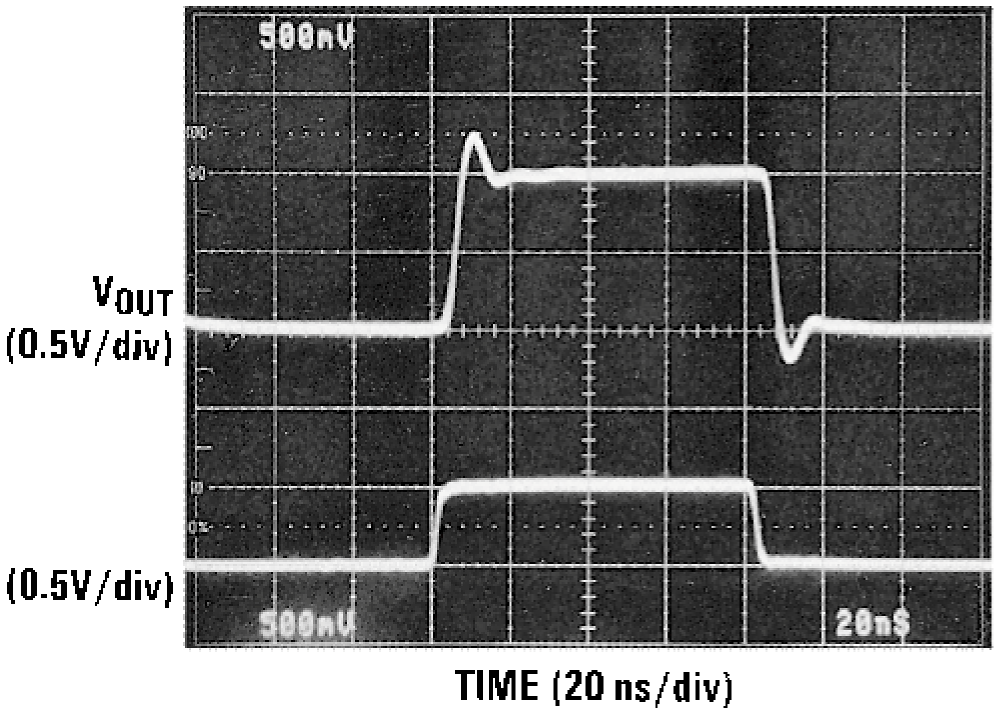
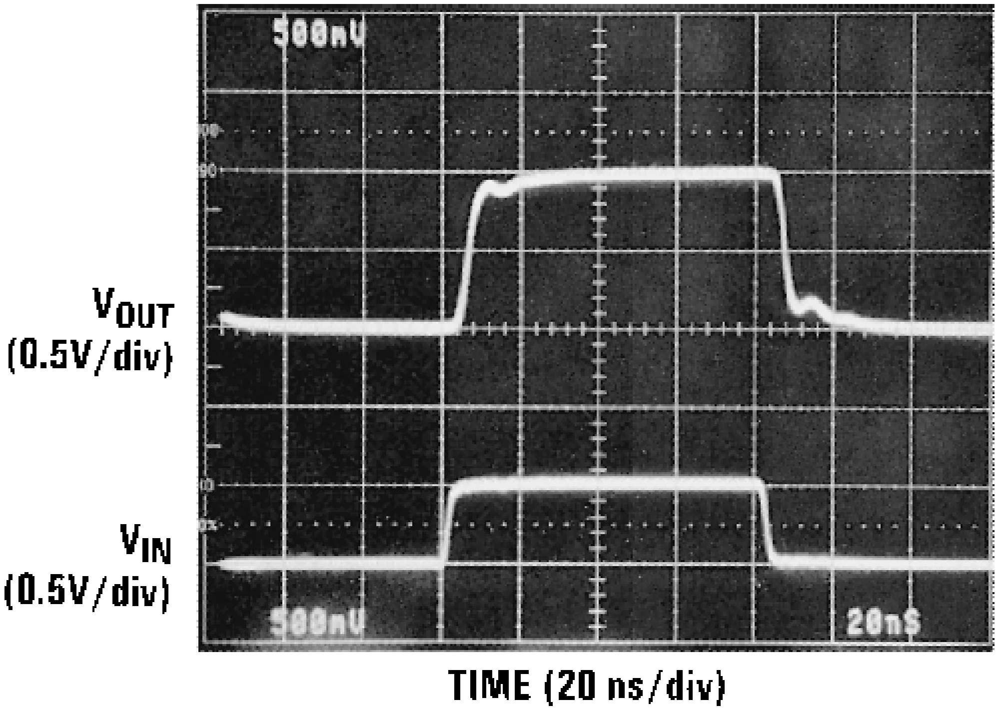


Figure 80. R_f = 820Ω



Increasing Compensation
with Increasing R_f

Figure 81. R_f = 1640Ω

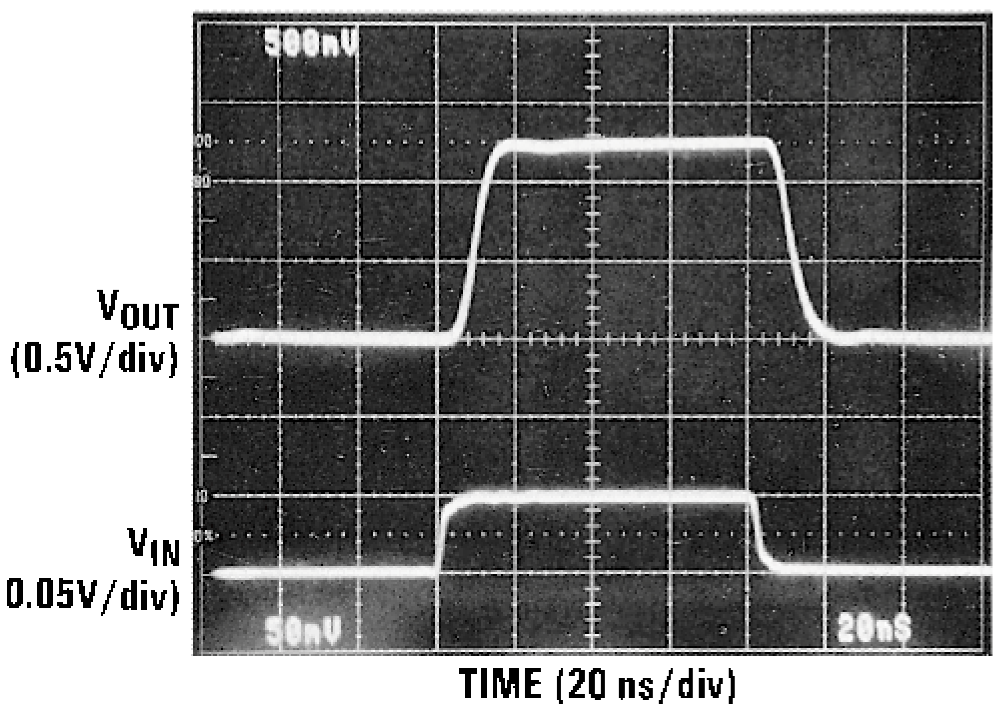


Figure 82. Reducing R_f for Large Closed Loop Gains, R_f = 500Ω

SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input determines slew rate for both inverting and non-inverting gains. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

The LM6181 can drive significantly larger capacitive loads than many current feedback amplifiers. Although the LM6181 can directly drive as much as 100 pF without oscillating, the resulting response will be a function of the feedback resistor value. Figure 84 illustrates the small-signal pulse response of the LM6181 while driving a 50 pF load. Ringing persists for approximately 70 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see typical curves Suggested R_f and R_s for C_L), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 86 illustrates the improvement obtained with using a 47Ω isolation resistor.

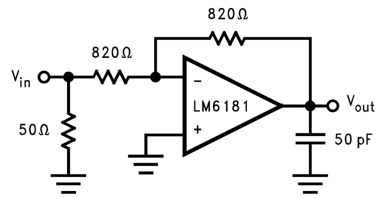


Figure 83.

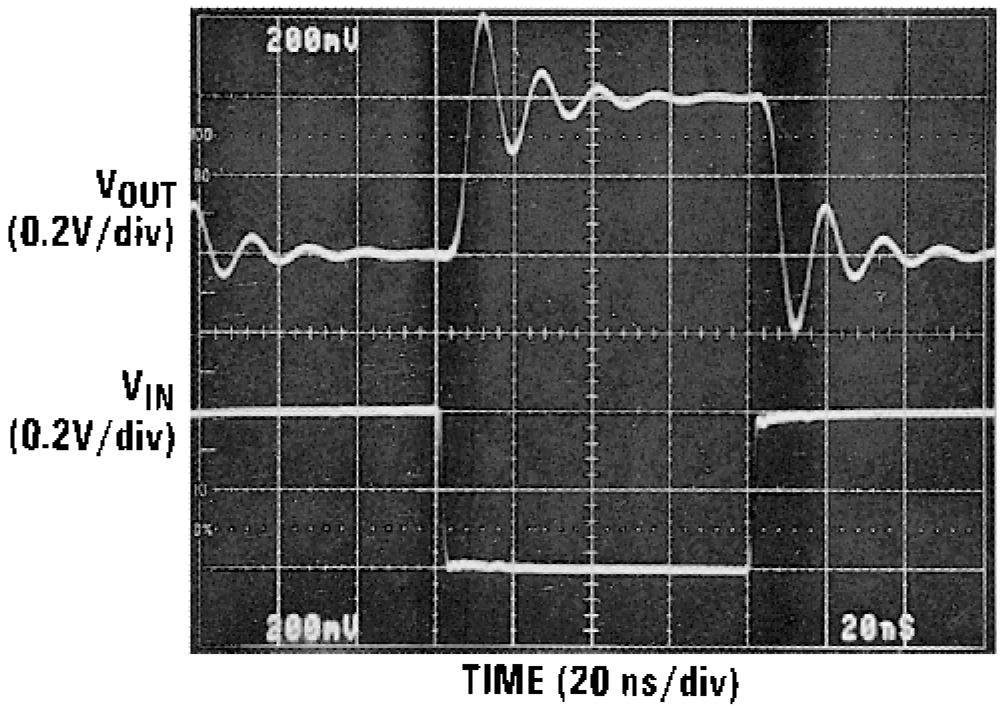


Figure 84. $A_V = -1$, LM6181 Can Directly Drive 50 pF of Load Capacitance with 70 ns of Ringing Resulting in Pulse Response

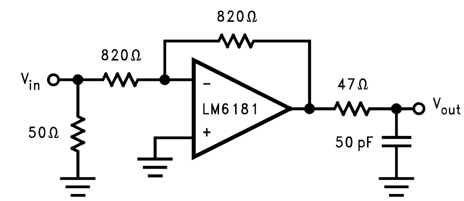
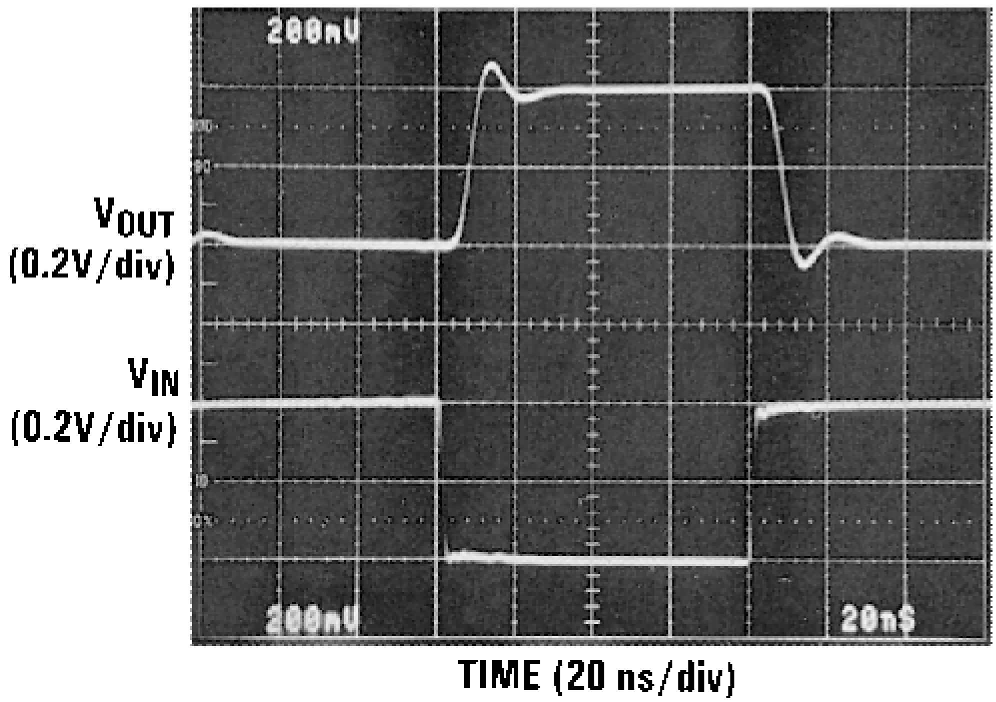


Figure 85.



R_f and R_S Could Be Increased to Maintain $A_V = -1$
and Improve Pulse Response Characteristics.

Figure 86. Resistive Isolation of C_L Provides Higher Fidelity Pulse Response.

CAPACITIVE FEEDBACK

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking in the frequency domain which equivalently tames the transient response. To limit the bandwidth of current feedback amplifiers, do not use a capacitor across R_f. The dynamic impedance of capacitors in the feedback loop reduces the amplifier's stability. Instead, reduced peaking in the frequency response, and bandwidth limiting can be accomplished by adding an RC circuit, as illustrated in Figure 88.

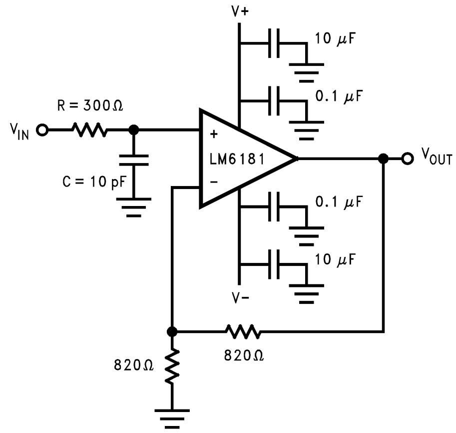


Figure 87.

$$f -3\ dB = \frac{1}{2\pi RC} \quad (1)$$

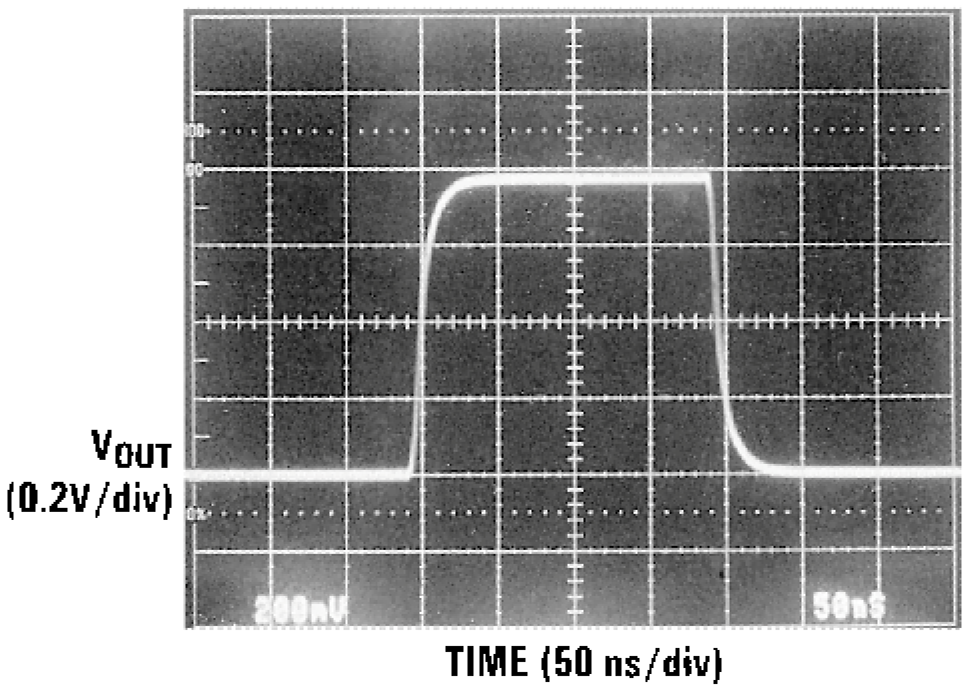


Figure 88. RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response

Typical Performance Characteristics

OVERDRIVE RECOVERY

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The typical recovery times for open-loop, closed-loop, and input common-mode voltage range overdrive conditions are illustrated in Figure 90, Figure 92, and Figure 93, respectively.

The open-loop circuit of Figure 89 generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times shown in Figure 90 are 5 ns and 25 ns, respectively.

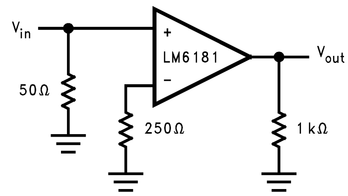


Figure 89.

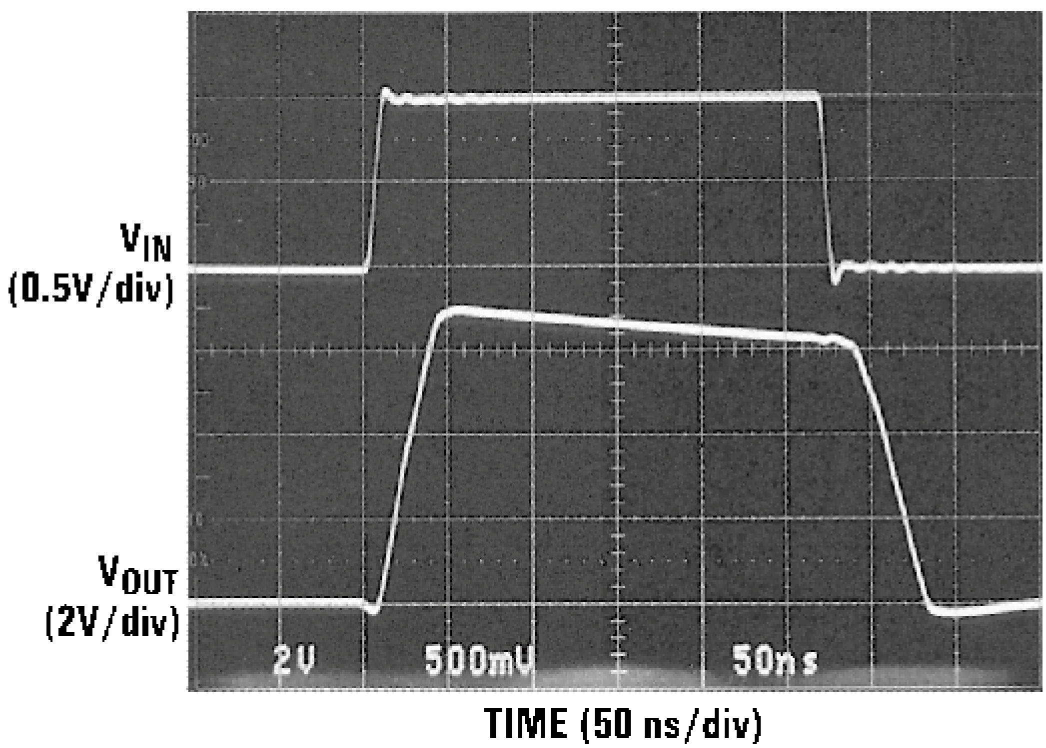


Figure 90. Open-Loop Overdrive Recovery Time of 5 ns, and 25 ns from Test Circuit in Figure 89

The large closed-loop gain configuration in Figure 91 forces the amplifier output into overdrive. Figure 92 displays the typical 30 ns recovery time to a linear output value.

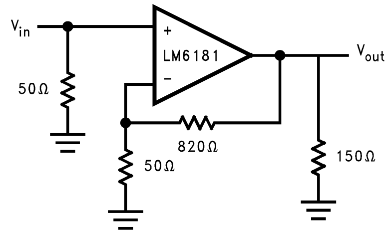


Figure 91.

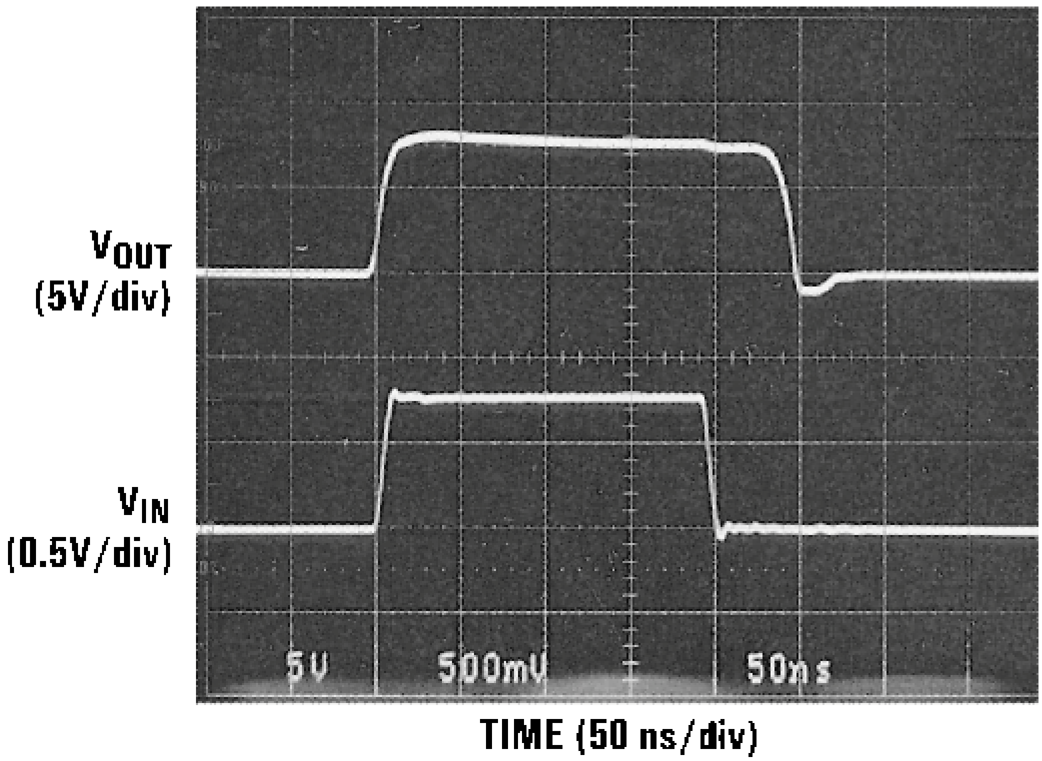


Figure 92. Closed-Loop Overdrive Recovery Time of 30 ns from Exceeding Output Voltage Range from Circuit in Figure 91

The common-mode input of the circuit in Figure 91 is exceeded by a 5V pulse resulting in a typical recovery time of 310 ns shown in Figure 93. The LM6181 supply voltage is ±5V.

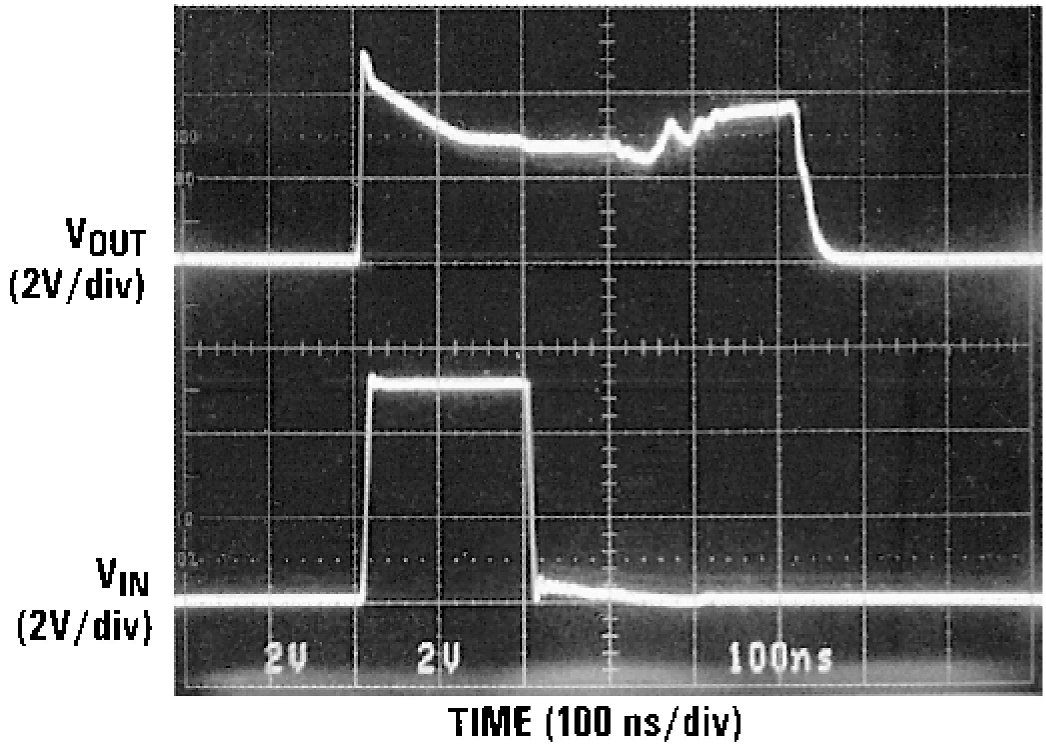


Figure 93. Exceptional Output Recovery from an Input that Exceeds the Common-Mode Range

Connection Diagrams

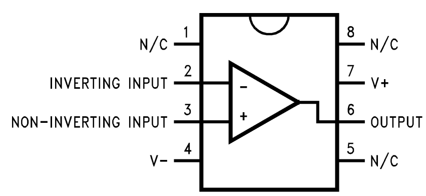
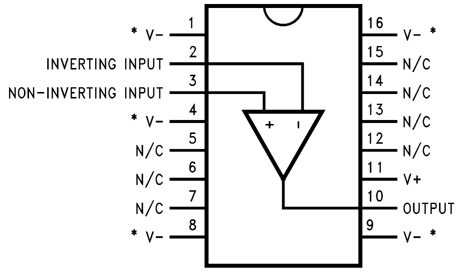


Figure 94. 8–Pin CDIP, PDIP (N), or SOIC (M-8) Package See Package Number NAB, P, or D



*Heat sinking pins(1)

Figure 95. 16-Pin SOIC Package (M)
See Package Number D

(1) The typical junction-to-ambient thermal resistance of the molded PDIP(N) package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the SOIC (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in^2 1 oz. copper trace. The 16-pin SOIC (M) package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V^- for proper operation. The typical junction-to-ambient thermal resistance of the SOIC (M-8) package soldered directly into a PC board is 153°C/W.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	32

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6181IM-8	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM618 1IM8	
LM6181IM-8/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM618 1IM8	Samples
LM6181IMX-8/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM618 1IM8	Samples
LM6181IN	NRND	PDIP	P	8	40	TBD	Call TI	Call TI	-40 to 85	LM6181IN	
LM6181IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM6181IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

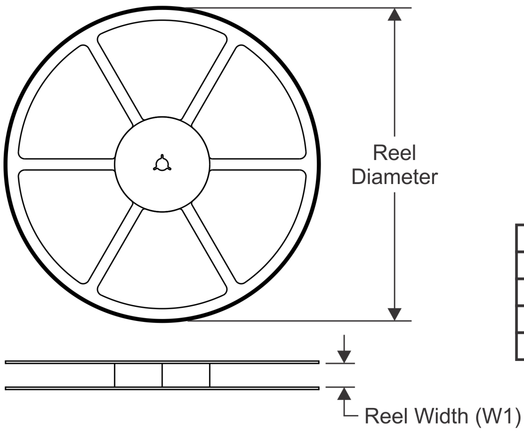
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

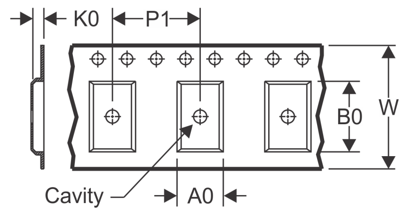
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

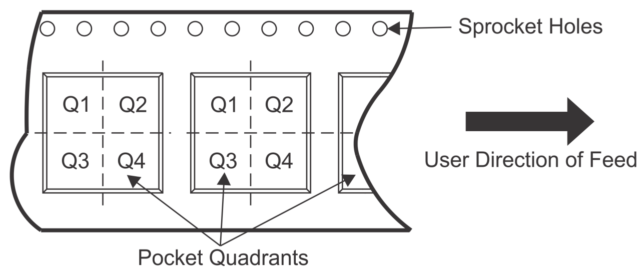


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

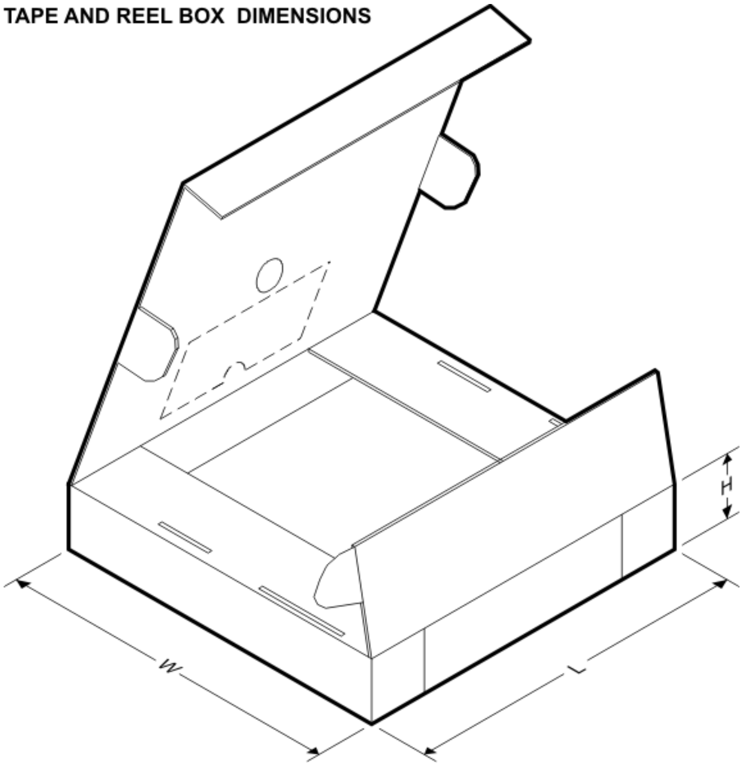
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6181IMX-8/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

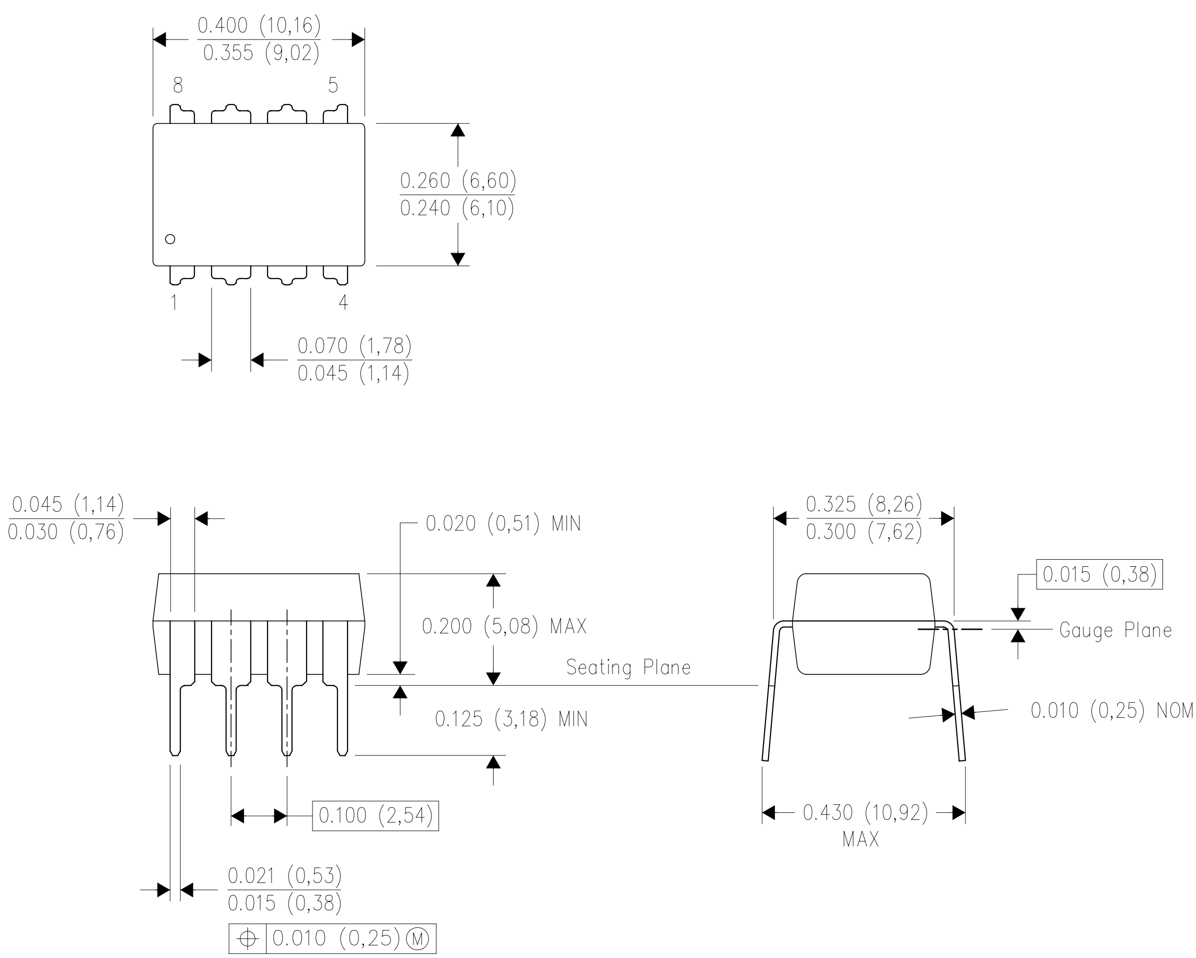
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6181IMX-8/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

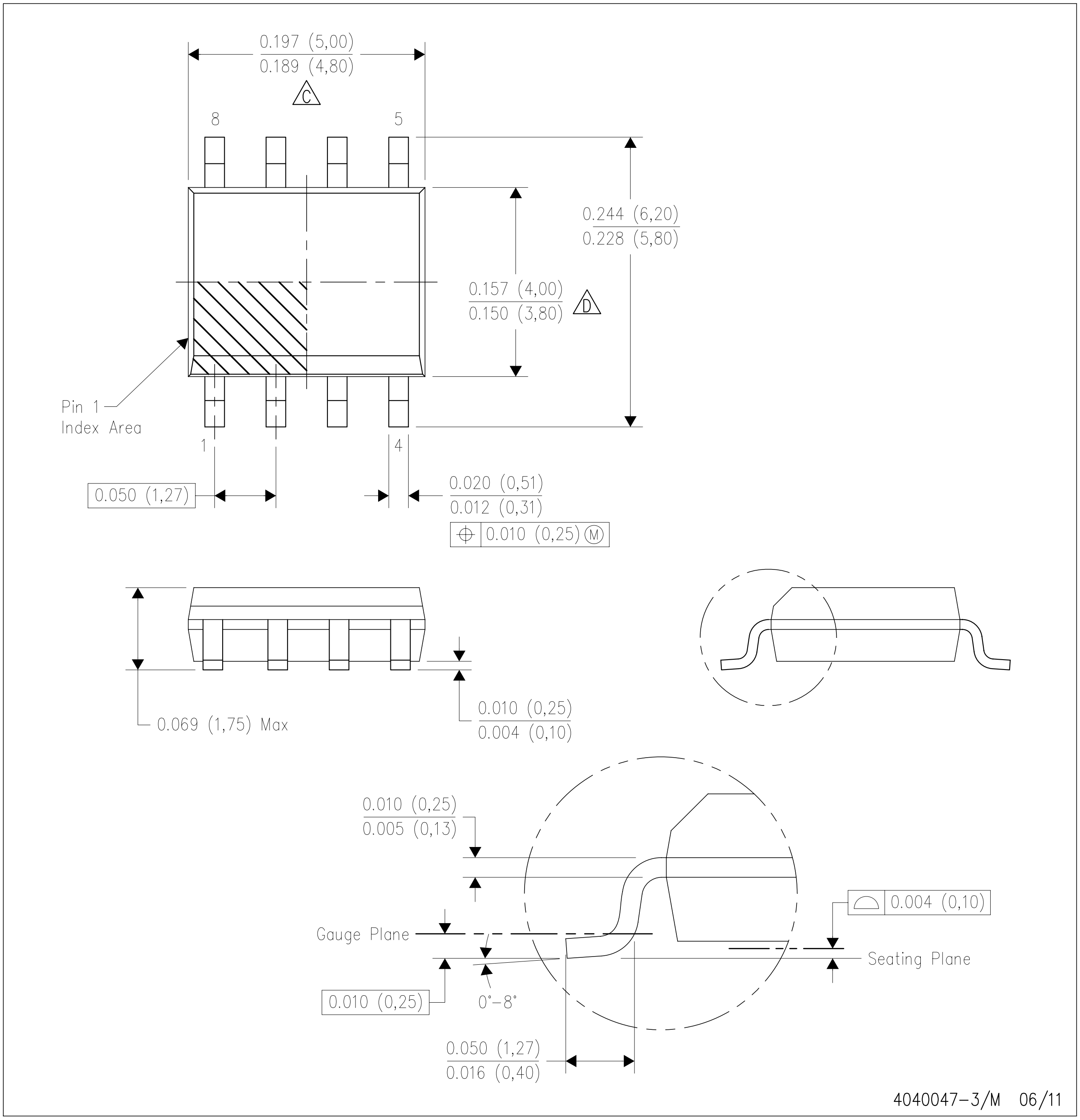
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265