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LM8262 Dual RRIO, High Output Current & Unlimited Cap Load Op Amp in VSSOP

Check for Samples: LM8262

FEATURES

 $(V_S = 5V, T_A = 25^{\circ}C, Typical Values Unless)$ Specified).

- **GBWP 21MHz**
- Wide Supply Voltage Range 2.5V to 22V
- Slew Rate 12V/us
- Supply Current/channel 1.15 mA
- Cap Load Limit Unlimited
- Output Short Circuit Current +53mA/-75mA
- +/-5% Settling Time 400ns (500pF, 100mV_{PP}
- Input Common Mode Voltage 0.3V Beyond
- Input Voltage Noise 15nV/√Hz
- Input Current Noise 1pA/√Hz
- THD+N < 0.05%

APPLICATIONS

- TFT-LCD Flat Panel V_{COM} driver
- A/D Converter Buffer
- High Side/low Side Sensing
- **Headphone Amplifier**

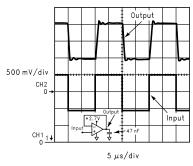


Figure 1. Output Response with Heavy Capacitive

DESCRIPTION

The LM8262 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability, and provides tested and guaranteed high speed and slew rate. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50dB of Common Mode Rejection, allows high side and low side sensing, among many applications, without having any concerns over exceeding the range and no compromise in accuracy. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage. The output stage has low distortion (0.05% THD+N) and can supply a respectable amount of current (15mA) with minimal headroom from either rail (300mV).

The LM8262 is offered in the space saving VSSOP package.

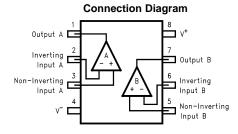


Figure 2. 8-Pin VSSOP (Top View)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)(2)

ESD Tolerance	ESD Tolerance				
V _{IN} Differential		+/-10V			
Output Short Circuit Duration	See (5) (6)				
Supply Voltage (V ⁺ - V ⁻)	24V				
Voltage at Input/Output pins		V+ +0.8V, V− −0.8V			
Storage Temperature Range		−65°C to +150°C			
Junction Temperature (7)		+150°C			
Soldering Information:	Infrared or Convection (20 sec.)	235°C			
	Wave Soldering (10 sec.)	260°C			

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5kΩ in series with 100pF.
- (4) Machine Model, 0Ω is series with 200pF.
- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (6) Output short circuit duration is infinite for $V_S \le 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.
- (7) The maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings

Supply Voltage (V ⁺ - V ⁻)		2.5V to 22V
Junction Temperature Range ⁽¹⁾		-40°C to +85°C
Package Thermal Resistance, θ _{JA} , ⁽¹⁾	8-Pin VSSOP	235°C/W

⁽¹⁾ The maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 0.5\text{V}$, $V_O = V^+/2$, and $R_L > 1M\Omega$ to V^- . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ	Max (1)	Units	
Vos	Input Offset Voltage	$V_{CM} = 0.5V \& V_{CM} = 2.2V$	-	+/-0.7	+/-5 +/-7	mV	
TC V _{OS}	Input Offset Average Drift	$V_{CM} = 0.5V \& V_{CM} = 2.2V$	_	+/-2	_	μV/C	
I _B	Input Bias Current	V _{CM} = 0.5V	_	-1.20	-2.00 -2.70		
		V _{CM} = 2.2V	_	+0.49	+1.00 +1.60	μΑ	
I _{OS}	Input Offset Current	$V_{CM} = 0.5V \& V_{CM} = 2.2V$	_	20	250 400	nA	
CMRR	Common Mode Rejection Ratio	V _{CM} stepped from 0V to 1.0V	76 60	100	_		
		V _{CM} stepped from 1.7V to 2.7V	_	100	-	dB	
		V _{CM} stepped from 0V to 2.7V	58 50	70	_		
+PSRR	Positive Power Supply Rejection Ratio	V ⁺ = 2.7V to 5V	78 74	104	_	dB	

- (1) All limits are guaranteed by testing or statistical analysis.
- (2) Typical Values represent the most likely parametric norm.
- (3) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

(4) Positive current corresponds to current flowing into the device.

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2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^{\circ}C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 0.5V$, $V_O = V^+/2$, and $R_L > 1M\Omega$ to V⁻. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ	Max (1)	Units
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	_	-0.3	-0.1 0.0	V
			2.8 2.7	3.0	_	V
A _{VOL}	Large Signal Voltage Gain	$V_{O} = 0.5 \text{ to } 2.2V,$ $R_{L} = 10 \text{k to } V^{-}$	70 67	78	_	dB
		$V_O = 0.5$ to 2.2V, $R_L = 2k$ to V^-	67 63	73	_	dB
Output Swing High		$R_L = 10k \text{ to } V^-$	2.49 2.46	2.59	-	V
		$R_L = 2k \text{ to } V^-$	2.45 2.41	2.53	_	V
	Output Swing Low	R _L = 10k to V ⁻	-	90	100 120	mV
I _{SC}	Output Short Circuit Current	Sourcing to V ⁻ V _{ID} = 200mV ⁽⁵⁾⁽⁶⁾	30 20	48	_	
		Sinking to V ⁺ $V_{ID} = -200 \text{mV}^{(5)(6)}$	50 30	65	_	mA
I _S	Supply Current (both amps)	No load, V _{CM} = 0.5V	-	2.0	2.5 3.0	mA
SR	Slew Rate (7)	$A_V = +1, V_I = 2V_{PP}$	_	9	_	V/µs
f _u	Unity Gain-Frequency	$V_I = 10 \text{mV}$, $R_L = 2 \text{k}\Omega$ to $V^+/2$	_	10	-	MHz
GBWP	Gain Bandwidth Product	f = 50KHz	15.5 14	21	-	MHz
Phi _m	Phase Margin	V _I = 10mV	_	50	_	Deg
en	Input-Referred Voltage Noise	$f = 2KHz$, $R_S = 50\Omega$	_	15	_	nV/ √ Hz
i _n	Input-Referred Current Noise	f = 2KHz	_	1	_	pA/ √ Hz
f _{max}	Full Power Bandwidth	$Z_{L} = (20pF 10k\Omega) \text{ to V}^{+}/2$	_	1	_	MHz

Product Folder Links: LM8262

Short circuit test is a momentary test. See Note 6. Output short circuit duration is infinite for $V_S \le 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms. Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.



5V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = $V^+/2$, and R_L > 1M Ω to V^- . Boldface limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ	Max (1)	Units	
V _{OS}	Input Offset Voltage	V _{CM} = 1V & V _{CM} = 4.5V	-	+/-0.7	+/-5 +/- 7	mV	
TC V _{OS}	Input Offset Average Drift	V _{CM} = 1V & V _{CM} = 4.5V	-	+/-2	_	μV/°C	
I _B	Input Bias Current	V _{CM} = 1V	-	-1.18	-2.00 - 2.70		
		V _{CM} = 4.5V	_	+0.49	+1.00 + 1.60	μΑ	
l _{OS}	Input Offset Current	V _{CM} = 1V & V _{CM} = 4.5V	_	20	250 400	nA	
CMRR Common Mode Rejection Ratio		V _{CM} stepped from 0V to 3.3V	84 72	110	_		
		V _{CM} stepped from 4V to 5V	_	100	_	dB	
		V _{CM} stepped from 0V to 5V	64 61	80	_		
+PSRR	Positive Power Supply Rejection Ratio	$V^{+} = 2.7V$ to 5V, $V_{CM} = 0.5V$	78 74	104	_	dB	
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB		-0.3	-0.1 0.0	V	
			5.1 5.0	5.3	_	V	
A _{VOL}	Large Signal Voltage Gain	$V_{O} = 0.5 \text{ to } 4.5V,$ $R_{L} = 10 \text{k to } V^{-}$	74 70	84	_	٩D	
		$V_{O} = 0.5 \text{ to } 4.5 \text{V},$ $R_{L} = 2 \text{k to V}^{-}$	70 66	80	_	dB	
Vo	Output Swing High	R _L = 10k to V ⁻	4.75 4.72	4.87	_	- V	
		$R_L = 2k \text{ to } V^-$	4.70 4.66	4.81	_	V	
	Output Swing Low	R _L = 10k to V ⁻	_	86	125 135	mV	
I _{SC}	Output Short Circuit Current	Sourcing to V ⁻ V _{ID} = 200mV ⁽⁵⁾⁽⁶⁾	35 20	53	_	4	
		Sinking to V ⁺ $V_{ID} = -200 \text{mV}^{(5)(6)}$	60 50	75	_	mA	
I _S	Supply Current (both amps)	No load, V _{CM} = 1V	_	2.3	2.8 3.5	mA	
SR	Slew Rate ⁽⁷⁾	$A_V = +1, V_I = 5V_{PP}$	10 7	12	_	V/µs	
fu	Unity Gain Frequency	$V_I = 10 \text{mV},$ $R_L = 2k\Omega \text{ to V}^+/2$	_	10.5	_	MHz	
GBWP	Gain-Bandwidth Product	f = 50KHz	16 15	21	_	MHz	
Phi _m	Phase Margin	V _I = 10mV	-	53	_	Deg	
e _n	Input-Referred Voltage Noise	$f = 2KHz, R_S = 50\Omega$	-	15	_	nV/ √Hz	
i _n	Input-Referred Current Noise	f = 2KHz	_	1	_	pA/ √ Hz	

⁽¹⁾ All limits are guaranteed by testing or statistical analysis.

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Typical Values represent the most likely parametric norm.

Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Positive current corresponds to current flowing into the device.

Short circuit test is a momentary test. See Note 6. (5)

Output short circuit duration is infinite for $V_S \le 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower. (7)



5V Electrical Characteristics (continued)

Unless otherwise specified, all limited guaranteed for $T_J = 25^{\circ}C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1V$, $V_O = V^+/2$, and $R_L > 1M\Omega$ to V^- . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Parameter Condition		Typ (2)	Max (1)	Units
f _{max}	Full Power Bandwidth	$Z_L = (20pF 10k\Omega) \text{ to } V^+/2$	_	900	_	KHz
t _S	Settling Time (+/-5%)	100mV _{PP} Step, 500pF load	_	400	_	ns
THD+N	Total Harmonic Distortion + Noise	$R_L = 1k\Omega$ to V ⁺ /2 f = 10KHz to $A_V = +2$, $4V_{PP}$ swing	_	0.05	_	%

+/-11V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for $T_J = 25^{\circ}C$, $V^+ = 11V$, $V^- = -11V$, $V_{CM} = 0V$, $V_O = 0V$, and $R_L > 1M\Omega$ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Тур (2)	Max (1)	Units	
V _{OS}	Input Offset Voltage	V _{CM} = −10.5V & V _{CM} = 10.5V	_	+/-0.7	+/-7 + /- 9	mV	
TC V _{OS}	Input Offset Average Drift	$V_{CM} = -10.5V \& V_{CM} = 10.5V$ (3)	_	+/-2		μV/°C	
В	Input Bias Current	V _{CM} = −10.5V	_	-1.05	-2.00 -2.80		
		V _{CM} = 10.5V	_	+0.49	+1.00 +1.50	μΑ	
los	Input Offset Current	$V_{CM} = -10.5V \& V_{CM} = 10.5V$		30	275 550	nA	
CMRR	Common Mode Rejection Ratio	V _{CM} stepped from -11V to 9V	84 80	100	_		
		V _{CM} stepped from 10V to 11V	_	100	_	dB	
		V _{CM} stepped from -11V to 11V	74 72	88			
+PSRR	Positive Power Supply Rejection Ratio	V ⁺ = 9V to 11V	70 66	100	_	dB	
-PSRR	Negative Power Supply Rejection Ratio	$V^- = -9V$ to $-11V$	70 66	100	_	dB	
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	_	-11.3	-11.1 - 11.0	V	
			11.1 11.0	11.3	-	V	
A _{VOL}	Large Signal Voltage Gain	$V_O = 0V \text{ to } +/-9V,$ $R_L = 10k\Omega$	78 74	85	_	40	
		$V_O = 0V$ to +/-9V, R _L = 2k Ω	72 66	79	_	dB	
Vo	Output Swing High	$R_L = 10k\Omega$	10.65 10.61	10.77	_		
1		$R_L = 2k\Omega$	10.6 10.55	10.69	_	V	
	Output Swing Low	$R_L = 10k\Omega$	_	-10.98	-10.75 - 10.65		
		$R_L = 2k\Omega$	-	-10.91	-10.65 -10.6	V	

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⁽¹⁾ All limits are guaranteed by testing or statistical analysis.

⁽²⁾ Typical Values represent the most likely parametric norm.

⁽³⁾ Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

⁽⁴⁾ Positive current corresponds to current flowing into the device.



+/-11V Electrical Characteristics (continued)

Unless otherwise specified, all limited guaranteed for $T_J = 25^{\circ}C$, $V^+ = 11V$, $V^- = -11V$, $V_{CM} = 0V$, $V_O = 0V$, and $R_L > 1M\Omega$ to 0V. Boldface limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units	
I _{SC}	Output Short Circuit Current	Sourcing to ground V _{ID} = 200mV ⁽⁵⁾⁽⁶⁾	40 25	60	-	0	
		Sinking to ground V _{ID} = 200mV ⁽⁵⁾⁽⁶⁾	65 55	100	-	mA mA	
I _S	Supply Current	No load, V _{CM} = 0V	-	2.5	4 5	mA	
SR	Slew Rate	$A_V = +1, V_I = 16V_{PP}$	10 8	15	-	V/µs	
f _U	Unity Gain Frequency	$V_I = 10 \text{mV}, R_L = 2 \text{k}\Omega$	_	13	_	MHz	
GBWP	Gain-Bandwidth Product	f = 50KHz	18 16	24	-	MHz	
Phi _m	Phase Margin	V _I = 10mV	_	58	_	Deg	
e _n	Input-Referred Voltage Noise	$f = 2KHz, R_S = 50\Omega$	_	15	_	nV/ √ Hz	
i _n	Input-Referred Current Noise	f = 2KHz	_	1	_	pA/ √ Hz	
t _S	Settling Time (+/ -1% , A _V = +1)	Positive Step, 5V _{PP}	_	320	_		
		Negative Step, 5V _{PP}	_	600	-	ns	
THD+N	Total Harmonic Distortion +Noise	$R_L = 1k\Omega$, $f = 10KHz$, $A_V = +2$, $15V_{PP}$ swing	-	0.01	-	%	
CT _{REJ}	Cross-Talk Rejection	f = 5MHz, Driver $R_1 = 10k\Omega$	_	68	-	dB	

Short circuit test is a momentary test. See Note 6.

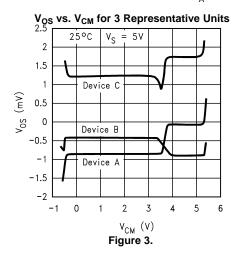
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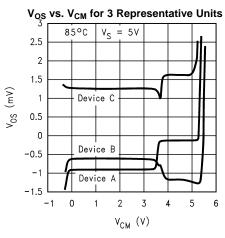
Output short circuit duration is infinite for $V_S \le 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms. Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.



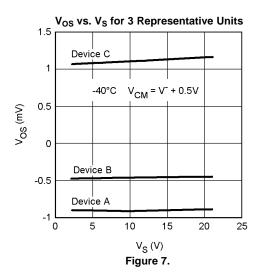
Typical Performance Characteristics

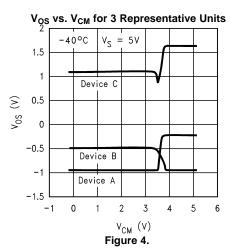
T_A = 25°C, Unless Otherwise Noted

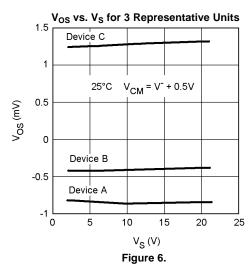


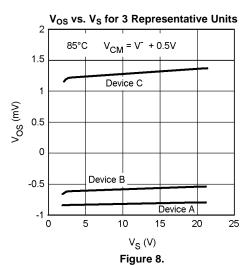














Typical Performance Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

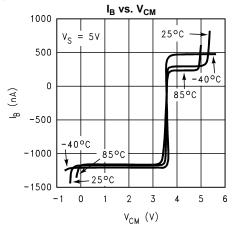
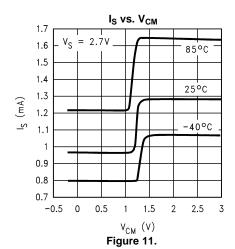
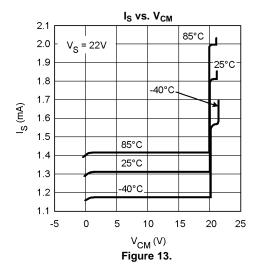


Figure 9.





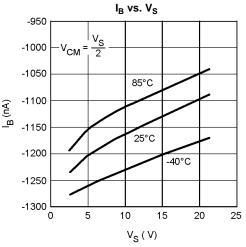
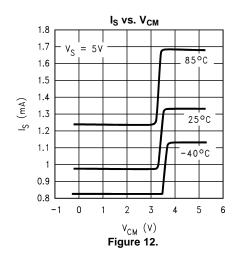


Figure 10.



I_S vs. V_S (PNP side) 1.5 $V_{CM} = V^{-} + 0.5V$ 1.4 1.3 85°C 1.2 1.1 25°C 0.9 -40°C 8.0 0.7 10 15 20 25 $V_{S}(V)$ Figure 14.

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Typical Performance Characteristics (continued)

 $T_A = 25$ °C, Unless Otherwise Noted

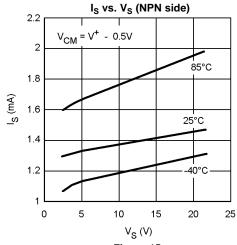


Figure 15.

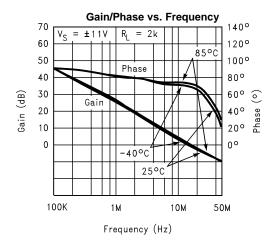


Figure 16.

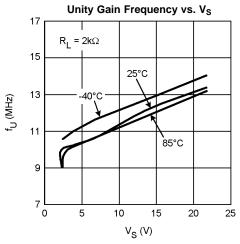


Figure 17.

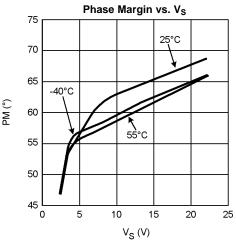


Figure 18.

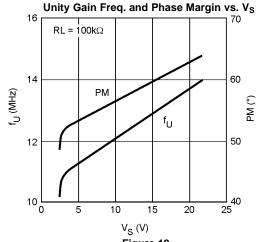


Figure 19.

SNOS975E-MAY 2001-REVISED APRIL 2013



REVISION HISTORY

Ch	nanges from Revision D (April 2013) to Revision E	Page
•	Changed layout of National Data Sheet to TI format	9



PACKAGE OPTION ADDENDUM

1-Nov-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
LM8262MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A46	
LM8262MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A46	Samples
LM8262MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A46	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



PACKAGE OPTION ADDENDUM

1-Nov-2013

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8262MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8262MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8262MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8262MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM8262MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM8262MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



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