LM9061 Power MOSFET Driver with Lossless Protection

Check for Samples: LM9061

FEATURES

- **Built-In Charge Pump for Gate Overdrive of High Side Drive Applications**
- **Lossless Protection of the Power MOSFET**
- **Programmable MOSFET Protection Voltage**
- **Programmable Delay of Protection Latch-OFF**
- **Fast Turn-ON (1.5 ms Max with Gate Capacitance of 25000 pF)**
- **Overvoltage Shut OFF with V_{CC} > 26V**
- **Withstands 60V Supply Transients**
- **CMOS Logic Compatible ON/OFF Control Input**
- **Available in 8-pin SOIC (SO-8) Package**

APPLICATIONS

- **Valve, Relay and Solenoid Drivers**
- **Lamp Drivers**
- **DC Motor PWM Drivers**
- **Logic Controlled Power Supply Distribution Switch**
- **Electronic Circuit Breaker**

DESCRIPTION

The LM9061 is a charge-pump device which provides the gate drive to any size external power MOSFET configured as a high side driver or switch. A CMOS logic compatible ON/OFF input controls the output gate drive voltage. In the ON state, the charge pump voltage, which is well above the available V_{CC} supply, is directly applied to the gate of the MOSFET. A built-in 15V zener clamps the maximum gate to source voltage of the MOSFET. When commanded OFF a 110 µA current sink discharges the gate capacitances of the MOSFET for a gradual turn-OFF characteristic to minimize the duration of inductive load transient voltages and further protect the power MOSFET.

Lossless protection of the power MOSFET is a key feature of the LM9061. The voltage drop (V_{DS}) across the power device is continually monitored and compared against an externally programmable threshold voltage. A small current sensing resistor in series with the load, which causes a loss of available energy, is not required for the protection circuitry. Should the V_{DS} voltage, due to excessive load current, exceed the threshold voltage, the output is latched OFF in a more gradual fashion (through a 10 µA output current sink) after programmable delay time interval.

The LM9061 has a wide operating temperature range of −40°C to +125°C, remains operational with V_{CC} up to 26V, and can withstand 60V power supply transients. The LM9061 is available in an 8-pin small outline surface mount package.

Typical Application

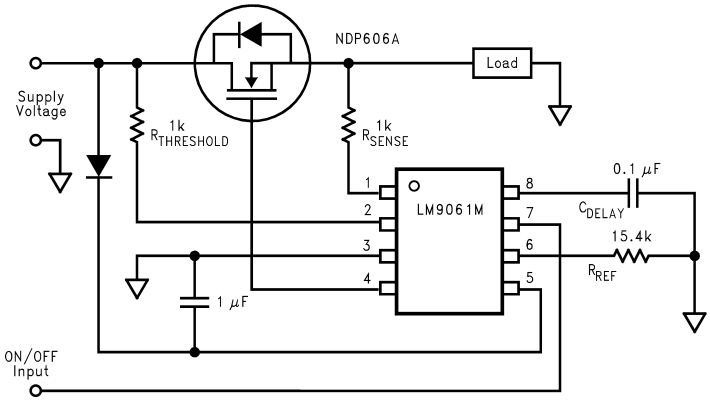

Figure 1.

Connection Diagram

Top View

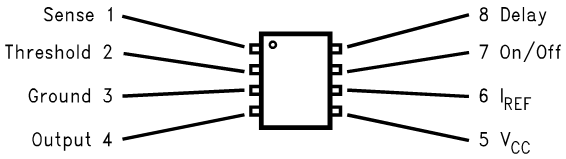

Figure 2. SOIC Package
See Package Number D0008A

PIN DESCRIPTIONS

Pin #	Pin Symbol	Pin Description
1	Sense	The inverting input to the protection comparator, connected to the external MOSFET source pin and the load.
2	Threshold	The non-inverting input to the protection comparator, and a current sink for the threshold resistor to set the allowed voltage drop across the external MOSFET.
3	Ground	Ground
4	Output	The gate drive connection. Charges, and discharges, the MOSFET gate.
5	V_{CC}	The voltage supply pin. The V_{CC} operating range has a minimum value of 7V, and a maximum value of 26V.
6	I_{REF}	A resistor on this pin to ground sets the current through the threshold resistor, which sets the allowed voltage drop across the external MOSFET.
7	On/Off	The control pin. A low voltage, $V_{IN}(0)$, will disable device operation, while a high voltage, $V_{IN}(1)$, will enable device operation.
8	Delay	A capacitor on this pin to ground will provide a delay time between when the protection comparator detects excessive V_{GS} across the MOSFET and when the gate drive circuitry is latched-OFF.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage	60V
Reverse Supply Current	20 mA
Output Voltage	V_{CC} +15V
Voltage at Sense and Threshold (through 1 kΩ)	−25V to +60V
ON/OFF Input Voltage	−0.3V to V_{CC} +0.3V
Junction Temperature	150°C
Storage Temperature	−55°C to +150°C
Lead Temperature Soldering, 10 seconds	260°C

(1) Absolute Maximum Ratings indicate the limits beyond which damage to the device may occur.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

OPERATING RATINGS(1)

Supply Voltage		7V to 26V
ON/OFF Input Voltage		−0.3V to V_{CC}
Ambient Temperature Range		−40°C to +125°C
Thermal Resistance (θ_{J-A})	LM9061M	150°C/W

(1) Operating Ratings indicate conditions for which the device is intended to be functional, but may not meet the ensured specific performance limits. For ensured specifications and test conditions see the TYPICAL ELECTRICAL CHARACTERISTICS.

DC ELECTRICAL CHARACTERISTICS

7V ≤ V_{CC} ≤20V, R_{REF} = 15.4 kΩ, −40°C ≤ T_J ≤ +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
POWER SUPPLY					
I_Q	Quiescent Supply Current	ON/OFF = “0”		5	mA
I_{CC}	Operating Supply Current	ON/OFF = “1”, C_{LOAD} = 0.025 µF, Includes Turn-ON Transient Output Current		40	mA
ON/OFF CONTROL INPUT					
$V_{IN}(0)$	ON/OFF Input Logic “0”	V_{OUT} = OFF		1.5	V
$V_{IN}(1)$	ON/OFF Input Logic “1”	V_{OUT} = ON	3.5		V
V_{HYST}	ON/OFF Input Hysteresis	Peak to Peak	0.8	2	V
I_{IN}	ON/OFF Input Pull-Down Current	VON/OFF = 5V	50	250	µA
GATE DRIVE OUTPUT					
V_{OH}	Charge Pump Output Voltage	ON/OFF = “1”	V_{CC} + 7	V_{CC} + 15	V
V_{OL}	OFF Output Voltage	ON/OFF = “0”, I_{SINK} = 110 µA		0.9	V
V_{CLAMP}	Sense to Output Clamp Voltage	ON/OFF = “1, V_{SENSE} = $V_{THRESHOLD}$	11	15	V
$I_{SINK(Normal-OFF)}$	Output Sink Current Normal Operation	ON/OFF = “0”, V_{DELAY} = 0V, V_{SENSE} = $V_{THRESHOLD}$	75	145	µA
$I_{SINK(Latch-OFF)}$	Output Sink Current with Protection Comparator Tripped	V_{DELAY} = 7V, V_{SENSE} < $V_{THRESHOLD}$	5	15	µA
PROTECTION CIRCUITRY					
I_{REF}	Threshold Pin Reference Current	V_{SENSE} = $V_{THRESHOLD}$	75	88	µA
V_{REF}	Reference Voltage		1.15	1.35	V
$I_{THR(LEAKAGE)}$	Threshold Pin Leakage Current	V_{CC} = Open, 7V ≤ $V_{THRESHOLD}$ ≤ 20V		10	µA
I_{SENSE}	Sense Pin Input Bias Current	V_{SENSE} = $V_{THRESHOLD}$		10	µA
DELAY TIMER					

DC ELECTRICAL CHARACTERISTICS (continued)

7V ≤ V_{CC} ≤20V, R_{REF} = 15.4 kΩ, −40°C ≤ T_J ≤ +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
I_{DELAY}	Delay Pin Source Current		6.74	15.44	µA
V_{TIMER}	Delay Timer Threshold Voltage		5	6.2	V
I_{DIS}	Delay Capacitor Discharge Current	V_{DELAY} = 5V	2	10	mA
V_{SAT}	Discharge Transistor Saturation Voltage	I_{DIS} = 1 mA		0.4	V

AC TIMING CHARACTERISTICS

7V ≤ V_{CC} ≤20V, R_{REF} = 15.4 kΩ, −40°C ≤ T_J ≤ +125°C, C_{LOAD} = 0.025 µF, C_{DELAY} = 0.022 µF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
T_{ON}	Output Turn-ON Time	C_{LOAD} = 0.025 µF 7V ≤ V_{CC} ≤ 10V, V_{OUT} ≥ V_{CC} + 7V 10V ≤ V_{CC} ≤ 20V, V_{OUT} ≥ V_{CC} + 11V		1.5 1.5	ms ms
$T_{OFF(NORMAL)}$	Output Turn-OFF Time, Normal Operation(1)	C_{LOAD} = 0.025 µF V_{CC} = 14V, V_{OUT} ≥ 25V V_{SENSE} = $V_{THRESHOLD}$	4	10	ms
$T_{OFF(Latch-OFF)}$	Output Turn-OFF Time, Protection Comparator Tripped(1)	C_{LOAD} = 0.025 µF V_{CC} = 14V, V_{OUT} ≥ 25V V_{SENSE} = $V_{THRESHOLD}$	45	140	ms
T_{DELAY}	Delay Timer Interval	C_{DELAY} = 0.022 µF	8	18	ms

(1) The AC Timing specifications for T_{OFF} are not production tested, and therefore are not specifically ensured. Limits are provided for reference purposes only. Smaller load capacitances will have proportionally faster turn-ON and turn-OFF times.

TYPICAL OPERATING WAVEFORMS

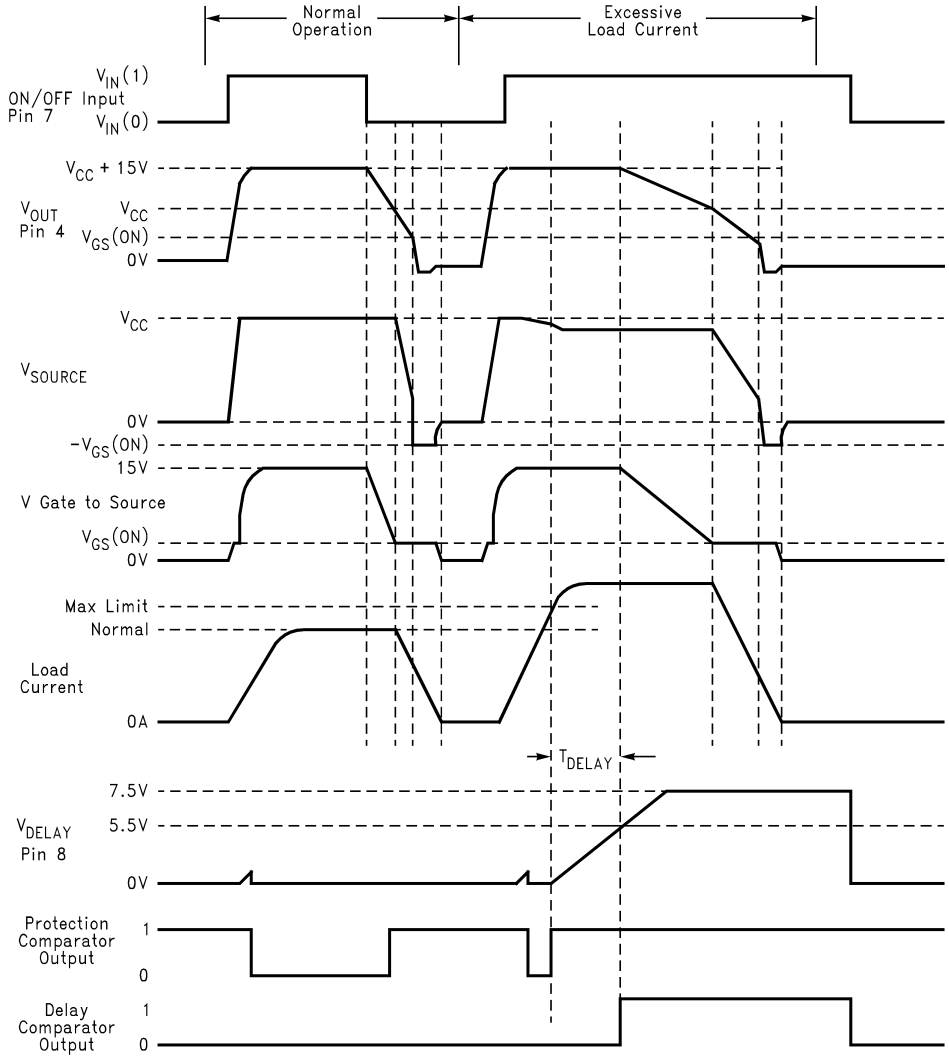

Figure 3.

TIMING DEFINITIONS

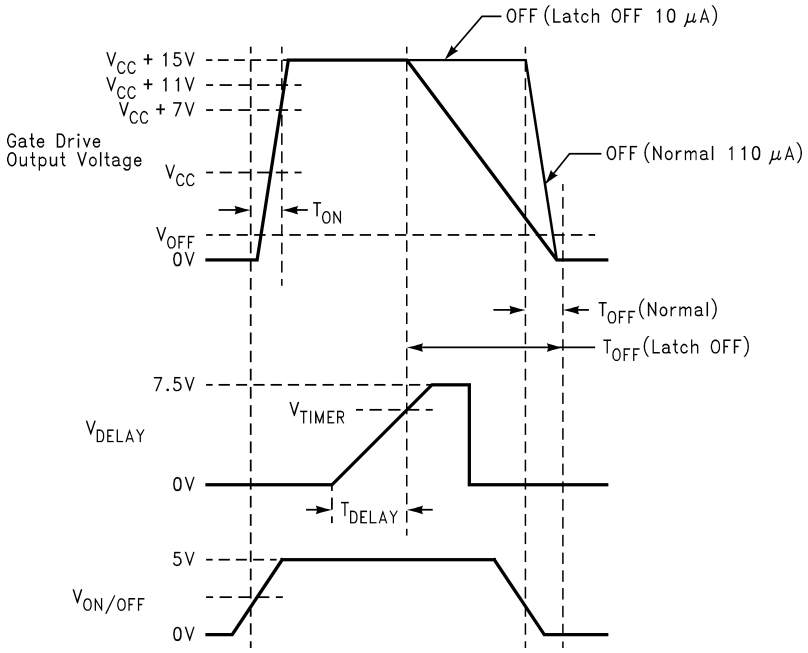

Figure 4.

TYPICAL ELECTRICAL CHARACTERISTICS

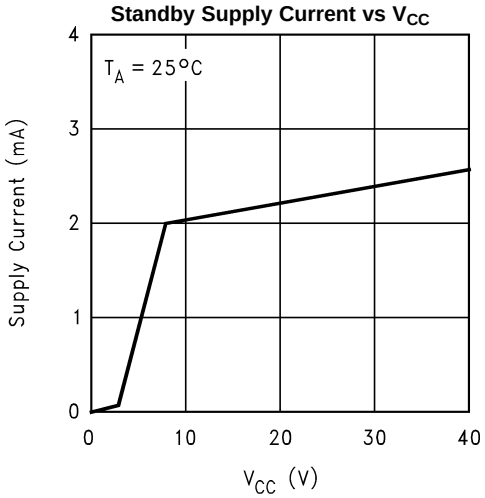

Figure 5.

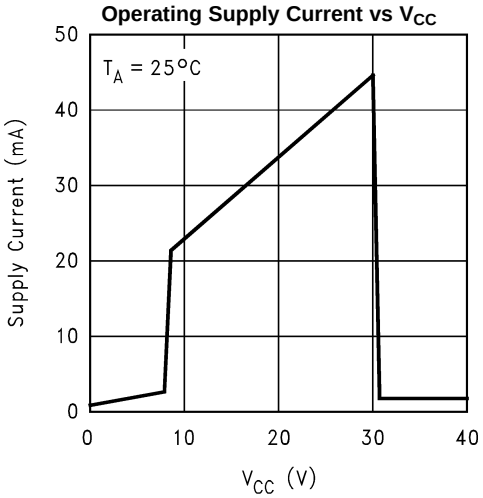

Figure 6.

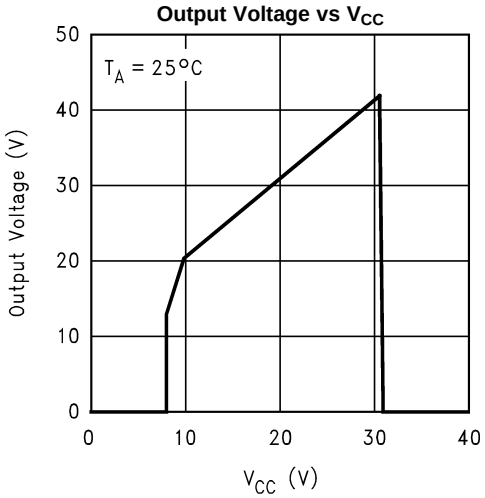

Figure 7.

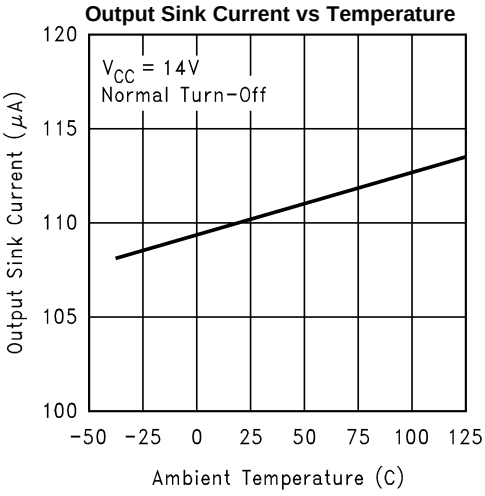

Figure 8.

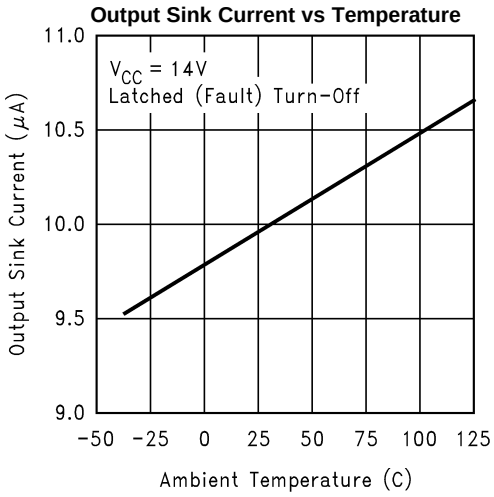

Figure 9.

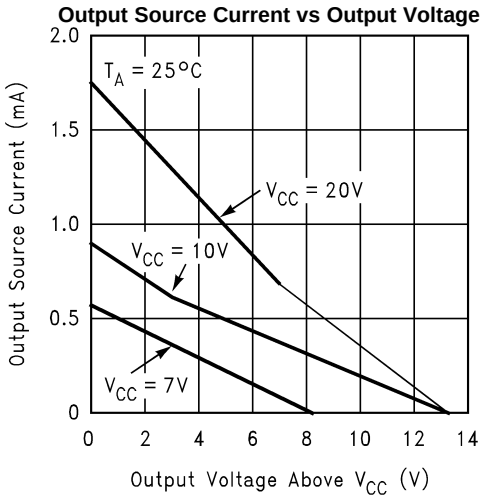

Figure 10.

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

Reference Voltage vs Temperature

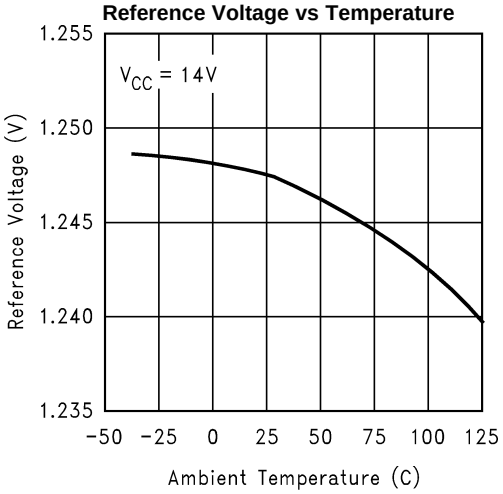

Figure 11.

Delay Threshold vs Temperature

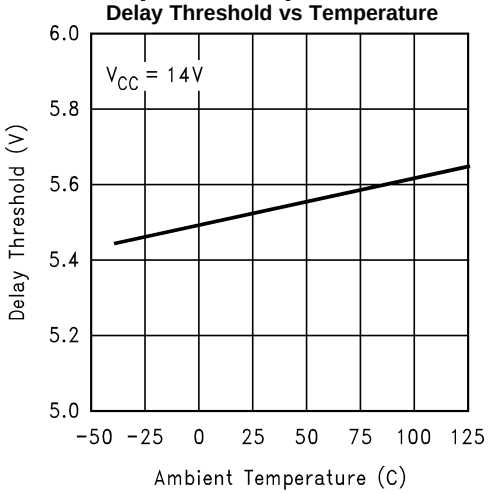

Figure 12.

Delay Charge Current vs Temperature

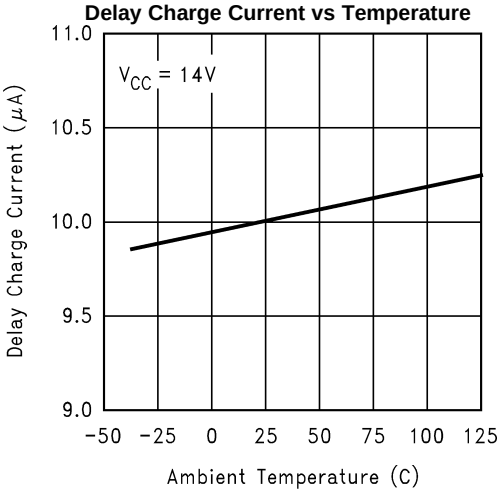

Figure 13.

BLOCK DIAGRAM

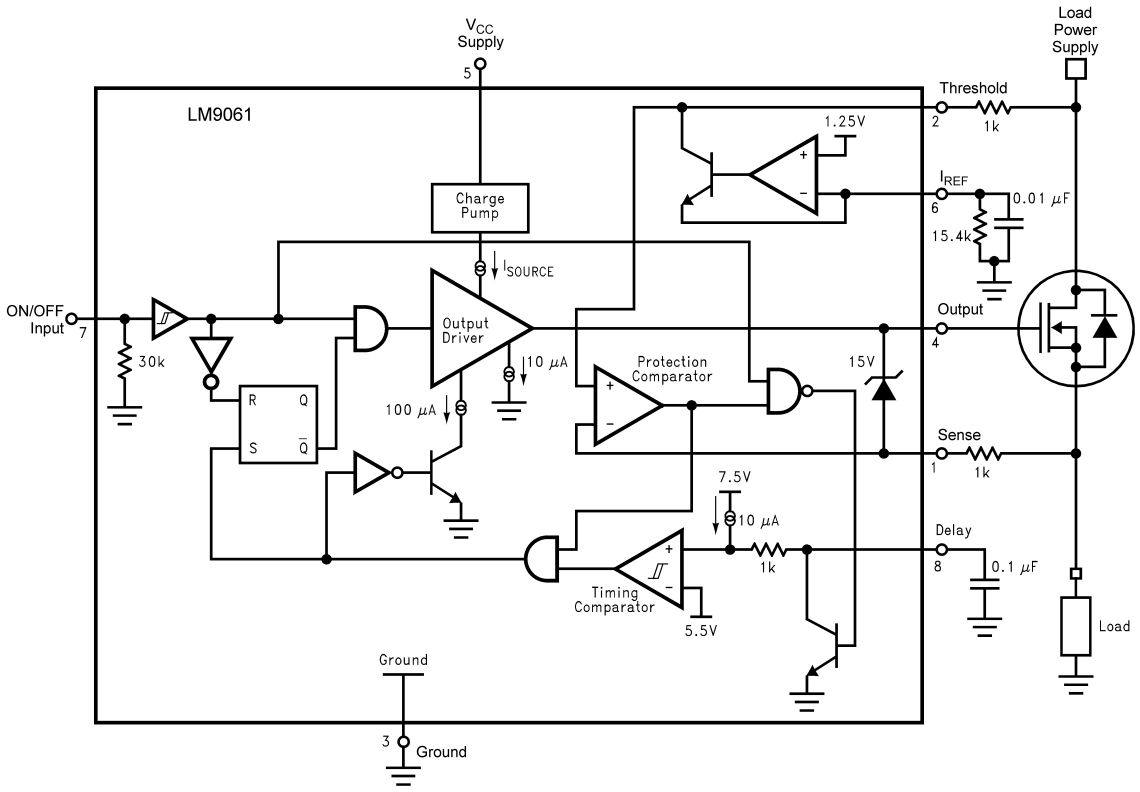

Figure 14.

APPLICATION INFORMATION

BASIC OPERATION

The LM9061 contains a charge pump circuit that generates a voltage in excess of the applied supply voltage to provide gate drive voltage to power MOSFET transistors. Any size of N-channel power MOSFET, including multiple parallel connected MOSFETs for very high current applications, can be used to apply power to a ground referenced load circuit in what is referred to as “high side drive” applications. Figure 15 shows the basic application of the LM9061.

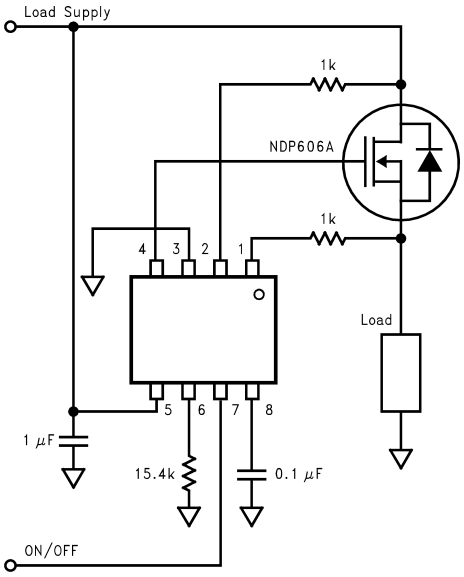

Figure 15. Basic Application Circuit

When commanded ON by a logic “1” input to pin 7 the gate drive output, pin 4, rises quickly to the V_{CC} supply potential at pin 5. Once the gate voltage exceeds the gate-source threshold voltage of the MOSFET, $V_{GS(ON)}$, (the source is connected to ground through the load) the MOSFET turns ON and connects the supply voltage to the load. With the source at near the supply potential, the charge pump continues to provide a gate voltage greater than the supply to keep the MOSFET turned ON. To protect the gate of the MOSFET, the output voltage of the LM9061 is clamped to limit the maximum V_{GS} to 15V.

It is important to remember that during the Turn-ON of the MOSFET the output current to the Gate is drawn from the V_{CC} supply pin. The V_{CC} pin should be bypassed with a capacitor with a value of at least ten times the Gate capacitance, and no less than 0.1 µF. The output current into the Gate will typically be 30 mA with V_{CC} at 14V and the Gate at 0V. As the Gate voltage rises to V_{CC}, the output current will decrease. When the Gate voltage reaches V_{CC}, the output current will typically be 1 mA with V_{CC} at 14V.

A logic “0” on pin 7 turns the MOSFET OFF. When commanded OFF a 110 µA current sink is connected to the output pin. This current discharges the gate capacitances of the MOSFET linearly. When the gate voltage equals the source voltage (which is near the supply voltage) plus the $V_{GS(ON)}$ threshold of the MOSFET, the source voltage starts following the gate voltage and ramps toward ground. Eventually the source voltage equals 0V and the gate continues to ramp to zero thus turning OFF the power device. This gradual Turn-OFF characteristic, instead of an abrupt removal of the gate drive, can, in some applications, minimize the power dissipation in the MOSFET or reduce the duration of negative transients, as is the case when driving inductive loads. In the event of an overstress condition on the power device, the turn OFF characteristic is even more gradual as the output sinking current is only 10 µA (see MOSFET PROTECTION CIRCUITRY section).

TURN ON AND TURN OFF CHARACTERISTICS

The actual rate of change of the voltage applied to the gate of the power device is directly dependent on the input capacitances of the MOSFET used. These times are important to know if the power to the load is to be applied repetitively as is the case with pulse width modulation drive. Of concern are the capacitances from gate to drain, C_{GD}, and from gate to source, C_{GS}. Figure 16 details the turn ON and turn OFF intervals in a typical application. An inductive load is assumed to illustrate the output transient voltage to be expected. At time t1, the ON/OFF input goes high. The output, which drives the gate of the MOSFET, immediately pulls the gate voltage towards the V_{CC} supply of the LM9061. The source current from pin 4 is typically 30 mA which quickly charges C_{GD} and C_{GS}. As soon as the gate reaches the $V_{GS(ON)}$ threshold of the MOSFET, the switch turns ON and the source voltage starts rising towards V_{CC}. V_{GS} remains equal to the threshold voltage until the source reaches V_{CC}. While V_{GS} is constant only C_{GD} is charging. When the source voltage reaches V_{CC}, at time t2, the charge pump takes over the drive of the gate to ensure that the MOSFET remains ON.

The charge pump is basically a small internal capacitor that acquires and transfers charge to the output pin. The clock rate is set internally at typically 300 kHz. In effect the charge pump acts as a switched capacitor resistor (approximately 67k) connected to a voltage that is clamped at 13V above the Sense input pin of the LM9061 which is equal to the V_{CC} supply in typical applications. The gate voltage rises above V_{CC} in an exponential fashion with a time constant dependent upon the sum of C_{GD} and C_{GS}. At this time however the load is fully energized. At time t3, the charge pump reaches its maximum potential and the switch remains ON.

At time t4, the ON/OFF input goes low to turn OFF the MOSFET and remove power from the load. At this time the charge pump is disconnected and an internal 110 µA current sink begins to discharge the gate input capacitances to ground. The discharge rate ($\Delta V/\Delta T$) is equal to 110 µA/ (C_{GD} + C_{GS}).

The load is still fully energized until time t5 when the gate voltage has reached a potential of the source voltage (V_{CC}) plus the $V_{GS(ON)}$ threshold voltage of the MOSFET. Between time t5 and t6, the V_{GS} voltage remains constant and the source voltage follows the gate voltage. With the voltage on C_{GD} held constant the discharge rate now becomes 110 µA/C_{GD}.

At time t6 the source voltage reaches 0V. As the gate moves below the $V_{GS(ON)}$ threshold the MOSFET tries to turn OFF. With an inductive load, if the current in the load has not collapsed to zero by time t6, the action of the MOSFET turning OFF will create a negative voltage transient (flyback) across the load. The negative transient will be clamped to $-V_{GS(ON)}$ because the MOSFET must turn itself back ON to continue conducting the load current until the energy in the inductance has been dissipated (at time t7).

MOSFET PROTECTION CIRCUITRY

A unique feature of the LM9061 is the ability to sense excessive power dissipation in the MOSFET and latch it OFF to prevent permanent failure. Instead of sensing the actual current flowing through the MOSFET to the load, which typically requires a small valued power resistor in series with the load, the LM9061 monitors the voltage drop from drain to source, V_{DS}, across the MOSFET. This “lossless” technique allows all of the energy available from the supply to be conducted to the load as required. The only power loss is that of the MOSFET itself and proper selection of a particular power device for an application will minimize this concern. Another benefit of this technique is that all applications use only standard inexpensive ¼W or less resistors.

To utilize this lossless protection technique requires knowledge of key characteristics of the power MOSFET used. In any application the emphasis for protection can be placed on either the power MOSFET or on the amount of current delivered to the load, with the assumption that the selected MOSFET can safely handle the maximum load current.

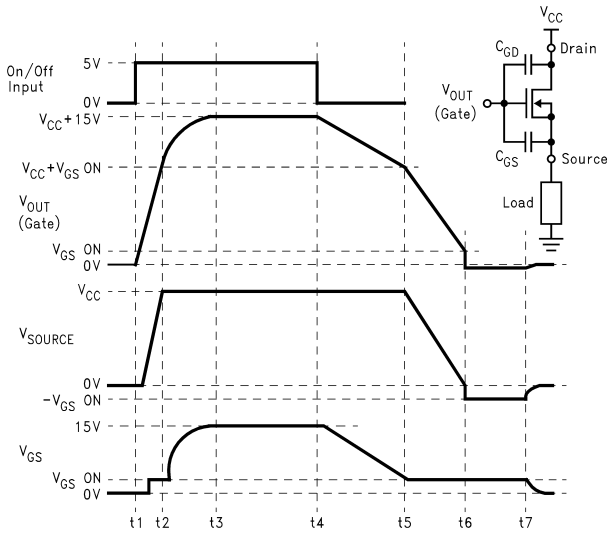

Figure 16. Turn ON and Turn OFF Waveforms

To protect the MOSFET from exceeding its maximum junction temperature rating, the power dissipation needs to be limited. The maximum power dissipation allowed (derated for temperature) and the maximum drain to source ON resistance, $R_{DS(ON)}$, with both at the maximum operating ambient temperature, needs to be determined. When switched ON the power dissipation in the MOSFET will be:

$$P_{DISS} = \frac{V_{DS}^2}{R_{DS(ON)}} \quad (1)$$

The V_{DS} voltage to limit the maximum power dissipation is therefore:

$$V_{DS\ (MAX)} = \sqrt{P_{D\ (MAX)}} \times R_{DS(ON)\ (MAX)} \quad (2)$$

With this restriction the actual load current and power dissipation obtained will be a direct function of the actual $R_{DS(ON)}$ of the MOSFET at any particular ambient temperature but the junction temperature of the power device will never exceed its rated maximum.

To limit the maximum load current requires an estimate of the minimum $R_{DS(ON)}$ of the MOSFET (the minimum $R_{DS(ON)}$ of discrete MOSFETs is rarely specified) over the required operating temperature range.

The maximum current to the load will be:

$$I_{LOAD\ (MAX)} = \frac{V_{DS}}{R_{DS(ON)\ (MIN)}} \quad (3)$$

The maximum junction temperature of the MOSFET and/or the maximum current to the load can be limited by monitoring and setting a maximum operational value for the drain to source voltage drop, V_{DS}. In addition, in the event that the load is inadvertently shorted to ground, the power device will automatically be turned-OFF.

In all cases, should the MOSFET be switched OFF by the built in protection comparator, the output sink current is switched to only 10 µA to gradually turn OFF the power device.

Figure 17 illustrates how the threshold voltage for the internal protection comparator is established.

Two resistors connect the drain and source of the MOSFET to the LM9061. The Sense input, pin 1, monitors the source voltage while the Threshold input, pin 2, is connected to the drain, which is also connected to the constant load power supply. Both of these inputs are the two inputs to the protection comparator. Should the voltage at the sense input ever drop below the voltage at the threshold input, the protection comparator output goes high and initiates an automatic latch-OFF function to protect the power device. Therefore the switching threshold voltage of the comparator directly controls the maximum V_{DS} allowed across the MOSFET while conducting load current.

The threshold voltage is set by the voltage drop across resistor $R_{THRESHOLD}$. A reference current is fixed by a resistor to ground at I_{REF}, pin 6. To precisely regulate the reference current over temperature, a stable band gap reference voltage is provided to bias a constant current sink. The reference current is set by:

$$I_{REF} = \frac{V_{REF}}{R_{REF}} \quad (4)$$

The reference current sink output is internally connected to the threshold pin. I_{REF} then flows from the load supply through $R_{THRESHOLD}$. The fixed voltage drop across $R_{THRESHOLD}$ is approximately equal to the maximum value of V_{DS} across the MOSFET before the protection comparator trips.

It is important to note that the programmed reference current serves a multiple purpose as it is used internally for biasing and also has a direct effect on the internal charge pump switching frequency. The design of the LM9061 is optimized for a reference current of approximately 80 µA, set with a 15.4 kΩ ±1% resistor for R_{REF}. To obtain the ensured performance characteristics it is recommended that a 15.4 kΩ resistor be used for R_{REF}.

The protection comparator is configured such that during normal operation, when the output of the comparator is low, the differential input stage of the comparator is switched in a manner that there is virtually no current flowing into the non-inverting input of the comparator. Therefore, only I_{REF} flows through resistor $R_{THRESHOLD}$. All of the input bias current, 20 µA maximum, for the comparator input stage (twice the I_{SENSE} specification of 10 µA maximum, defined for equal potentials on each of the comparator inputs) however flows into the inverting input through resistor R_{SENSE}. At the comparator threshold, the current through R_{SENSE} will be no more than the I_{SENSE} specification of 10 µA.

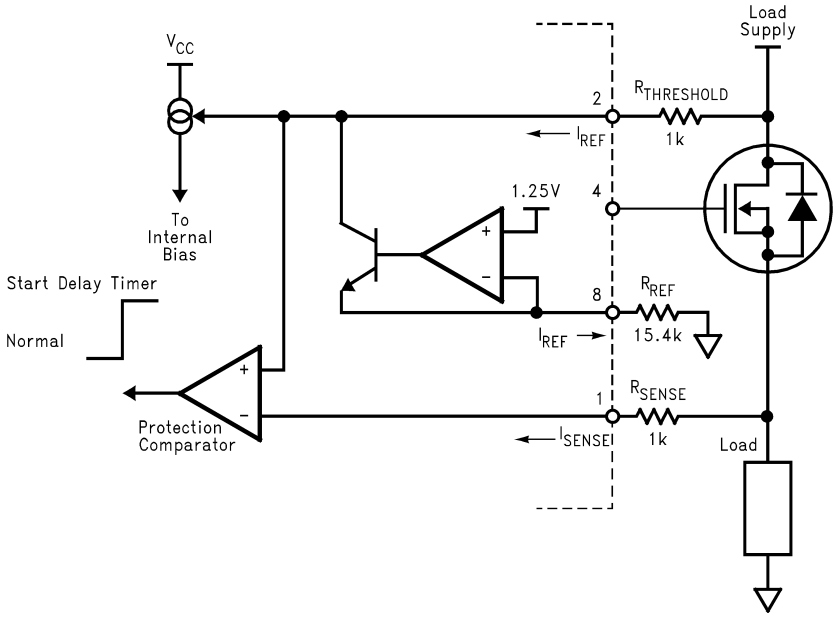

Figure 17. Protection Comparator Biasing

To tailor the $V_{DS\ (MAX)}$ threshold for any particular application, the resistor $R_{THRESHOLD}$ can be selected per the following formula:

$$V_{DS\ (MAX)} = \frac{V_{REF} \times R_{THR}}{R_{REF}} - (I_{SENSE} \times R_{SENSE}) + V_{OS} \quad (5)$$

where

- R_{REF} = 15.4 kΩ.
- I_{SENSE} is the input bias current to the protection comparator.
- R_{SENSE} is the resistor connected to pin 1.
- V_{OS} is the offset voltage of the protection comparator (typically in the range of ±10 mV).

The resistor R_{SENSE} is optional, but is strongly recommended to provide transient protection for the Sense pin, especially when driving inductive type loads. A minimum value of 1 kΩ will protect the pin from transients ranging from −25V to +60V. This resistor should be equal to, or less than, the resistor used for $R_{THRESHOLD}$. Never set R_{SENSE} to a value larger than $R_{THRESHOLD}$. When the protection comparator output goes high , the total bias current for the input stage transfers from the Sense pin to the Threshold pin, thereby changing the voltages present at the inputs to the comparator. For consistent switching of the comparator right at the desired threshold point, the voltage drop that occurs at the non-inverting input (Threshold) should equal, or exceed, the rise in voltage at the inverting input (Sense).

A bypass capacitor across R_{REF} is optional and is used to help keep the reference voltage constant in applications where the V_{CC} supply is subject to high levels of transient noise. This bypass capacitor should be no larger than 0.1 µF, and is not needed for most applications.

DELAY TIMER

To allow the MOSFET to conduct currents beyond the protection threshold for a brief period of time, a delay timer function is provided. This timer delays the actual latching OFF of the MOSFET for a programmable interval. This feature is important to drive loads which require a surge of current in excess of the normal ON current upon start up, or at any point in time, such as lamps and motors. Figure 18 details the delay timer circuitry. A capacitor connected from the Delay pin 8, to ground sets the delay time interval. With the MOSFET turned ON and all conditions normal, the output of the protection comparator is low and this keeps the discharge transistor ON. This transistor keeps the delay capacitor discharged. Should a surge of load current trip the protection comparator high, the discharge transistor turns OFF and an internal 10 µA current source begins linearly charging the delay capacitor.

If the surge current, with excessive V_{DS} voltage, lasts long enough for the capacitor to charge to the timing comparator threshold of typically 5.5V, the output of the comparator will go high to set a flip-flop and immediately latch the MOSFET OFF. It will not re-start until the ON/OFF Input is toggled low then high.

The delay time interval is set by the selection of C_{DELAY} and can be found from:

$$T_{DELAY} = \frac{(V_{TIMER} \times C_{DELAY})}{I_{DELAY}} \quad (6)$$

where

- Typically, V_{TIMER} = 5.5V.
- I_{DELAY} = 10 µA.

Charging of the delay capacitor is clamped at approximately 7.5V which is the internal bias voltage for the 10 µA current source.

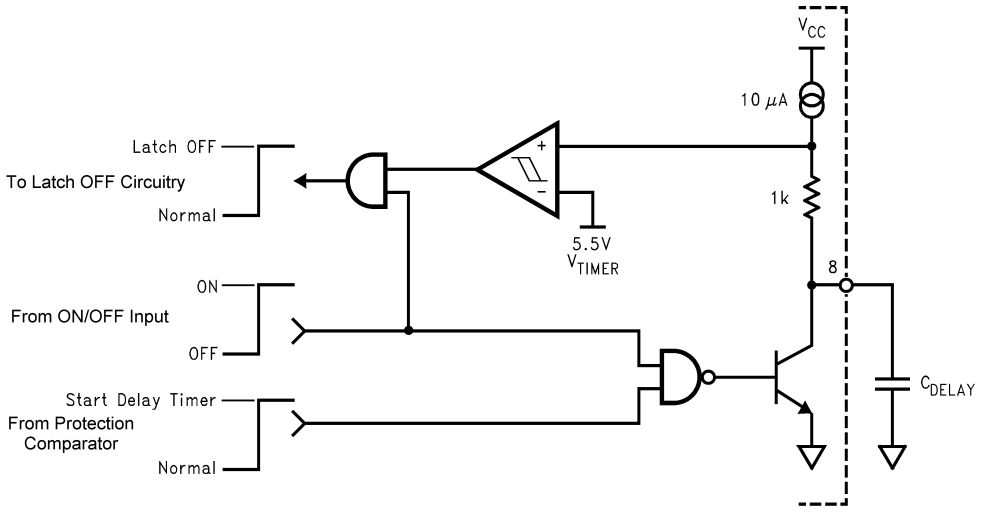

Figure 18. Delay Timer

MINIMUM DELAY TIME

A minimum delay time interval is required in all applications due to the nature of the protection circuitry. At the instant the MOSFET is commanded ON, the voltage across the MOSFET, V_{DS}, is equal to the full load supply voltage because the source is held at ground by the load. This condition will immediately trip the protection comparator. Without a minimum delay time set, the timing comparator will trip and force the MOSFET to latch-OFF thereby never allowing the load to be energized.

To prevent this situation a delay capacitor is required at pin 8. The selection of a minimum capacitor value to ensure proper start-up depends primarily on the load characteristics and how much time is required for the MOSFET to raise the load voltage to the point where the Sense input is more positive than the Threshold input ($T_{START-UP}$). Some experimentation is required if a specific minimum delay time characteristic is desired. Therefore:

$$C_{DELAY} = \frac{(I_{DELAY} \times T_{START-UP})}{V_{TIMER}} \quad (7)$$

In the absence of a specific delay time requirement, a value for C_{DELAY} of 0.1 µF is recommended.

OVER VOLTAGE PROTECTION

The LM9061 will remain operational with up to +26V on V_{CC}. If V_{CC} increases to more than typically +30V the LM9061 will turn off the MOSFET to protect the load from excessive voltage. When V_{CC} has returned to the normal operating range the device will return to normal operation without requiring toggling the ON/OFF input. This feature will allow MOSFET operation to continue in applications that are subject to periodic voltage transients, such as automotive applications.

For circuits where the load is sensitive to high voltages, the circuit shown in Figure 19 can be used. The addition of a zener on the Sense input (pin 1) will provide a maximum voltage reference for the Protection Comparator. The Sense resistor is required in this application to limit the zener current. When the device is ON, and the load supply attempts to rise higher than (V_{ZENER} + $V_{THRESHOLD}$), the Protection comparator will trip, and the Delay Timer will start. If the high supply voltage condition lasts long enough for the Delay Timer to time out, the MOSFET will be latched off. The ON/OFF input will need to be toggled to restart the MOSFET.

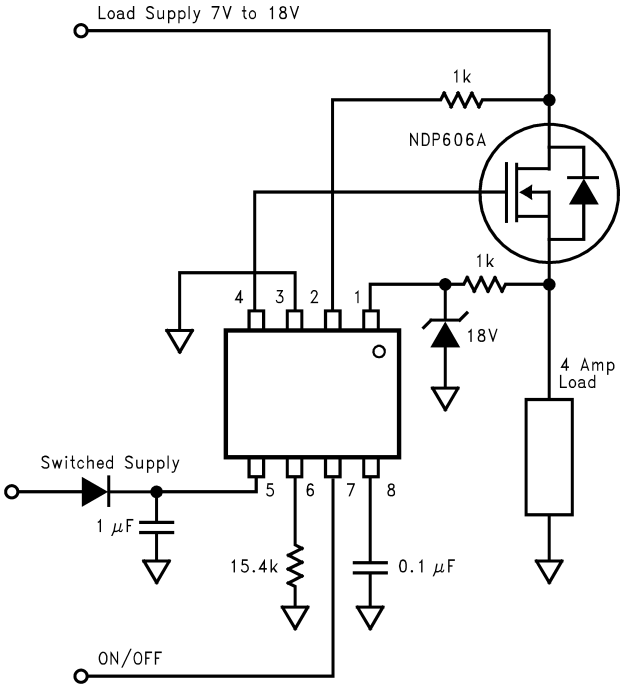

Figure 19. Adding Over-Voltage Protection

REVERSE BATTERY

The LM9061 is not protected against reverse polarity supply connections. If the V_{CC} supply should be taken negative with respect to ground, the current from the V_{CC} pin should be limited to 20 mA. The addition of a diode in series with the V_{CC} input is recommended. This diode drop does not subtract significantly from the charge pump gate overdrive output voltage.

LOW BATTERY

An additional feature the LM9061 is an Under-Voltage Shut-OFF function (UVSO). The typical UVSO threshold is 6.2V, and does not have hysteresis. When V_{CC} is between the ensured minimum operating voltage of 7.0V, and the UVSO threshold, the operation of the MOSFET gate drive, the delay timer, and the protection circuitry is not ensured. Operation in this region should be avoided. When V_{CC} falls below the UVSO threshold the charge pump will be disabled and the gate will be discharged at the Normal-OFF current sink rate, typically 110 µA.

Figure 20 shows the LM9061 used as an electronic circuit breaker. This circuit provides low voltage shutdown, over-voltage latch-OFF, and over-current latch-OFF.

The low voltage shutdown uses the 'On' and 'Off' voltage thresholds, and the typical 1.2V of hysteresis, to disable the LM9061 if V_{CC} falls near, or below, the 7.0V minimum operating voltage. The low voltage shutdown is accomplished with a voltage divider biased off V_{CC}. The voltage divider is formed by R1 (30 kΩ), R2 (82 kΩ), and the internal pull-down resistor of the ON/OFF pin (30 kΩ typical). In normal operation, V_{CC} will be above the minimum operating voltage of 7.0V, and the On/Off pin will be biased above the 'Off' threshold of 1.5V maximum (1.8V typical). When V_{CC} falls to 7.0V the On/Off pin voltage will fall below the 'Off' threshold voltage and the LM9061 will be turned off.

In the event of a latch-OFF shutdown, the circuit can be reset by shutting the main supply off, then back on. An optional, normally open, switch (Clear) from the ON/OFF pin to ground, will allow a “push button clear” of the circuit after latching OFF.

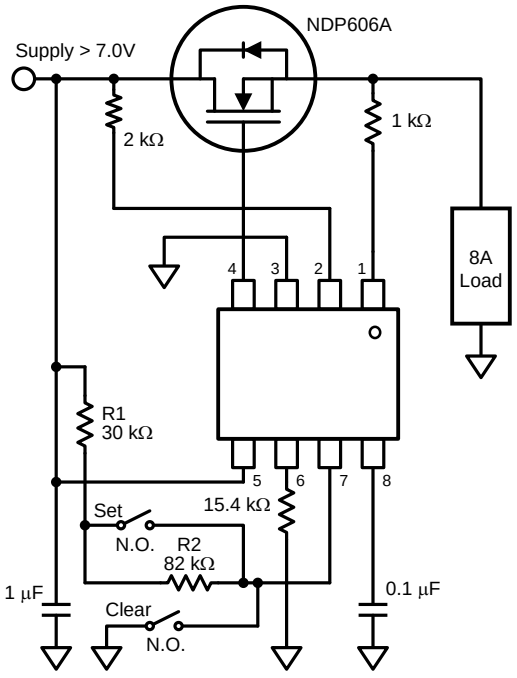

Figure 20. Electronic Circuit Breaker

This voltage divider arrangement requires a mechanism to raise the ON/OFF pin above the 'On' threshold of 3.5V minimum (3.1V typical) when V_{CC} is less than typically 16V. This can be accomplished with a second, normally open, switch from the ON/OFF pin across R2 (Set), so that closing the switch will short R2 and the voltage at the ON/OFF pin will be typically one-half of V_{CC}. When V_{CC} is at the minimum operating voltage of 7.0V this will bias the ON/OFF pin to about 3.5V causing the LM9061 to turn on. When V_{CC} is above typically 16.5V the resistor divider will have the ON/OFF pin biased above 3.5V and shorting of the resistor R2 will not be needed.

While the scaling of the external resistor values between V_{CC} and the ON/OFF input pin, against the internal 30 kΩ resistor, can be used to increase the startup voltage, it is important that the resistor ratio always has the ON/OFF pin biased below the 'Off' threshold (1.5V) when V_{CC} falls below the minimum operating voltage of 7.0V.

The accuracy of this voltage divider arrangement is affected by normal manufacturing variations of the 'On' and 'Off' voltage thresholds and the value of internal resistor at the ON/OFF pin. If any application needs to detect with greater precision when V_{CC} is near to 7.0V, an external voltage monitor should be used to drive the ON/OFF pin. The external voltage monitor would also eliminate both the need for the switch to short R2 to start the LM9061, as well as R2.

DRIVING MOSFET ARRAYS

The LM9061 is an ideal driver for any application that requires multiple parallel MOSFETs to provide the necessary load current. Only a few “common sense” precautions need to be observed. All MOSFETs in the array must have identical electrical and thermal characteristics. This can be solved by using the same part number from the same manufacturer for all of the MOSFETs in the array. Also, all MOSFETs should have the same style heat sink or, ideally, all mounted on the same heat sink. The electrical connection of the MOSFETs should get special attention. With typical $R_{DS(ON)}$ values in the range of tens of milli-Ohms, a poor electrical connection for one of the MOSFETs can render it useless in the circuit.

Also, the MOSFET dissipation during the Normal-OFF discharge of the gate capacitance, 70 µA minimum and 110 µA typical, needs consideration.

One particular caution is that, in the event of a fault condition, the Latch-OFF current sink, 10 µA typical, may not be able to discharge the total gate capacitance in a timely manner to prevent damage to the MOSFETs.

Figure 21 shows a circuit with four parallel NDP706A MOSFETs. This particular MOSFET has a typical $R_{DS(ON)}$ of 0.013Ω with a T_J of 25°C, and 0.020Ω with a T_J of +125°C.

With the V_{DS} threshold voltage being set to 500 mV, this circuit will provide a typical maximum load current of 150A at 25°C, and a typical maximum load current of 100A at 125°C. The maximum dissipation, per MOSFET, will be nearly 20W at 25°C, and 12.5W at 125°C. With up to 20W being dissipated by each of the four devices, an effective heat sink will be required to keep the T_J as low as possible when operating near the maximum load currents.

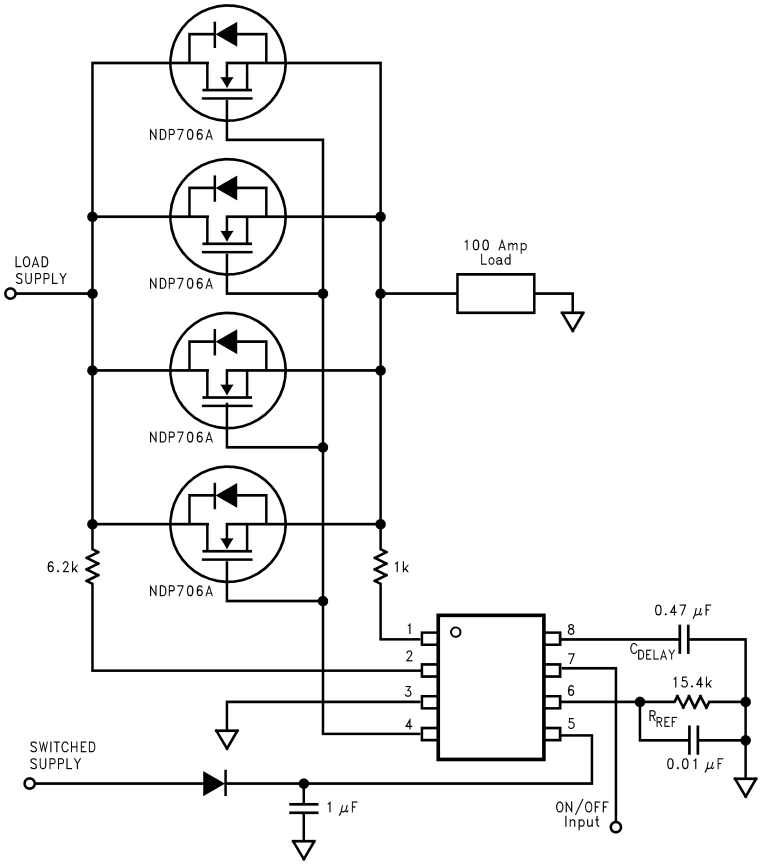

Figure 21. Driving Multiple MOSFETs

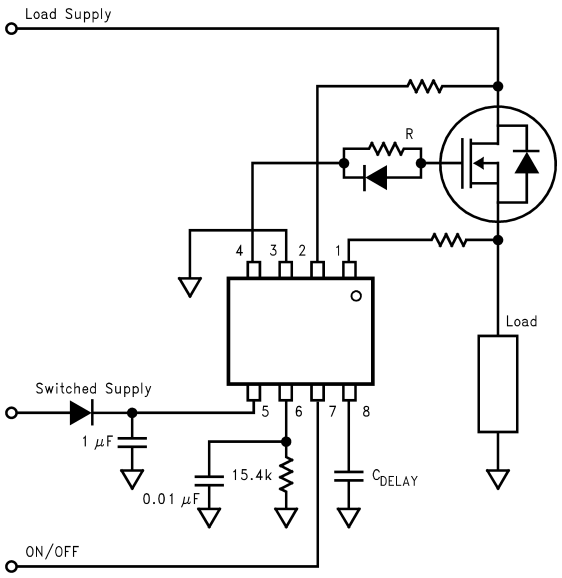

Figure 22. Increasing MOSFET Turn On Time

INCREASING MOSFET TURN ON TIME

The ability of the LM9061 to quickly turn on the MOSFET is an important factor in the management of the MOSFET power dissipation. Caution should be exercised when attempting to increase the MOSFET Turn On time by limiting the Gate drive current. The MOSFET average dissipation, and the LM9061 Delay time, must be recalculated with the extended switching transition time.

Figure 22 shows a method of increasing the MOSFET Turn On time, without affecting the Turn Off time. In this method the Gate is charged at an exponential rate set by the added external Gate resistor and the MOSFET Gate capacitances.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM9061M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LM90 61M	
LM9061M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-1-260C-UNLIM	-40 to 125	LM90 61M	Samples
LM9061MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM90 61M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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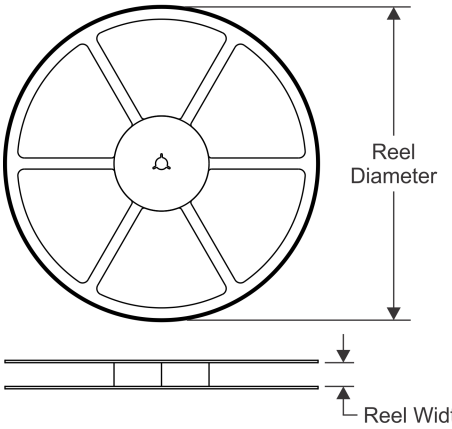
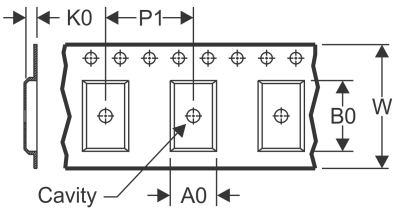
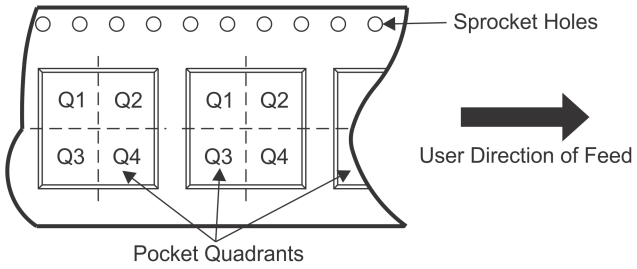


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

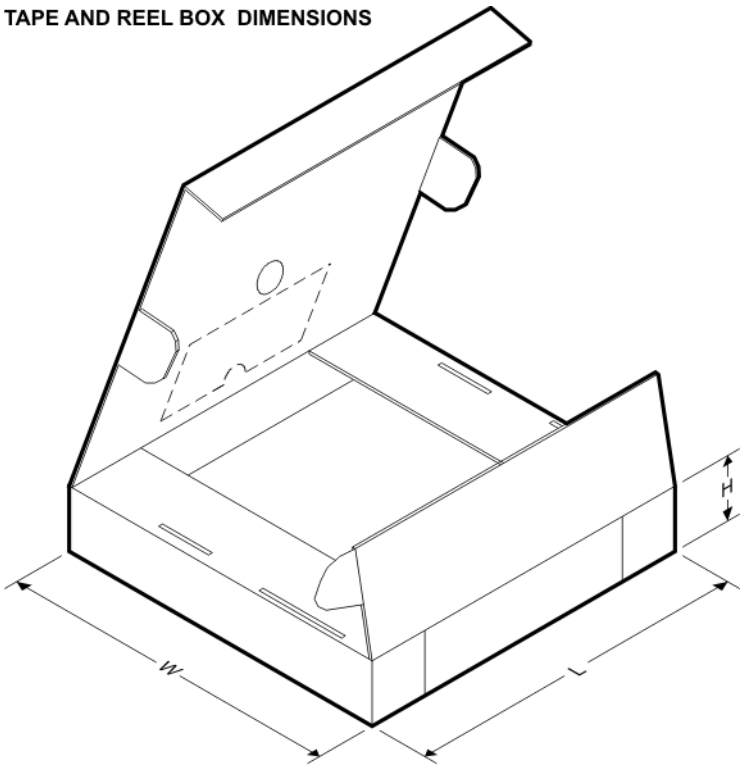
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9061MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

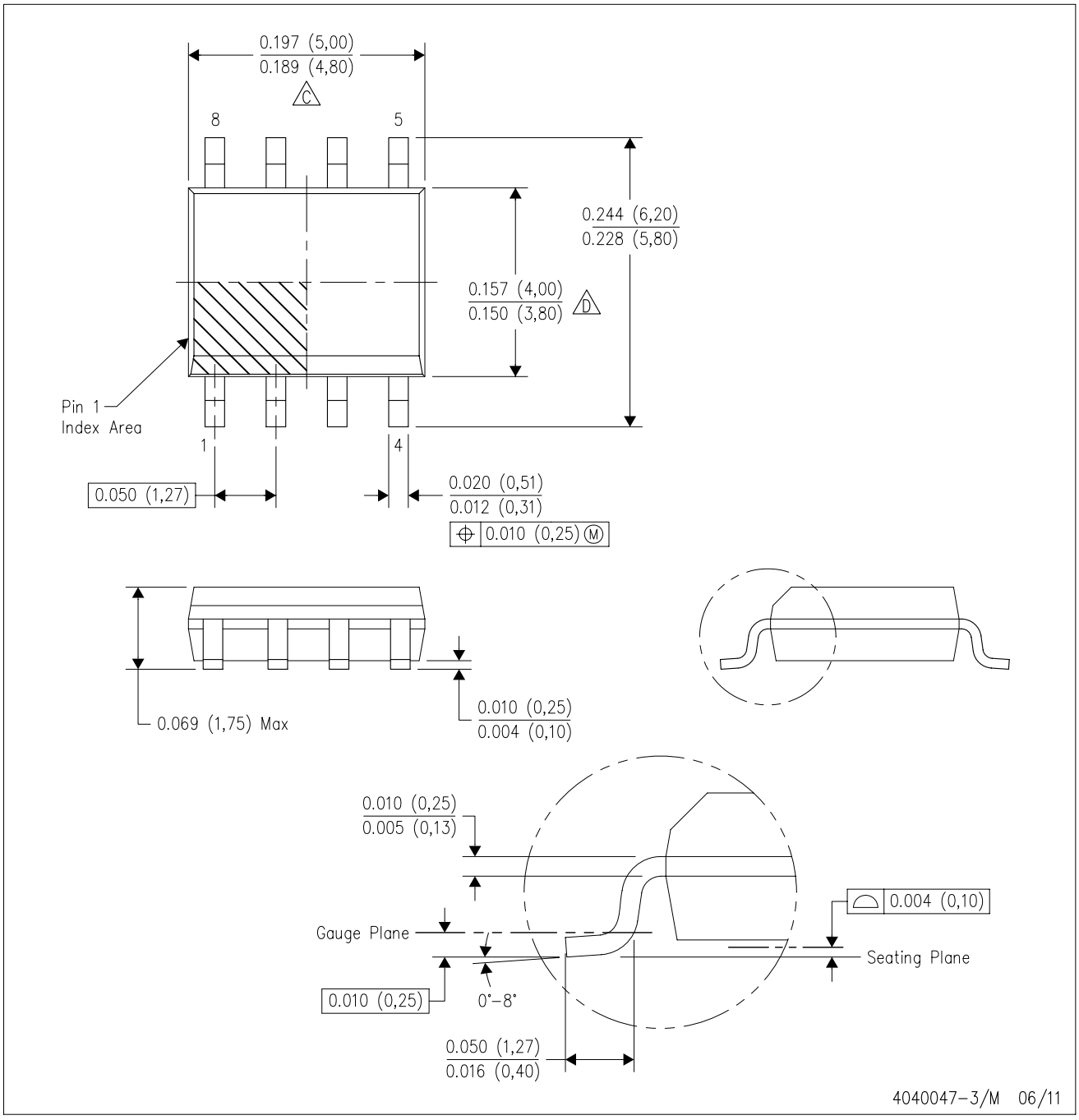
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9061MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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