LMC6953 PCI Local Bus Power Supervisor

Check for Samples: LMC6953

FEATURES

- **Compliant to PCI Specifications Revision 2.1.**
- **Under and Over Voltage Detectors for 5V and 3.3V**
- **Power Failure Detection (5V Falling Under 3.3V by 300 mV Max)**
- **Manual Reset Input Pin**
- **Specified $\overline{\text{RESET}}$ Assertion at V_{DD} = 1.5V**
- **Integrated Reset Delay Circuitry**
- **Open Drain Output**
- **Adjustable Reset Delay**
- **Response Time for Over and Under Voltage Detection: 490 ns Max**
- **Power Failure Response Time: 90 ns Max**
- **Requires Minimal External Components**

APPLICATIONS

- **Desktop PCs**
- **PCI-Based Systems**
- **Network servers**

DESCRIPTION

The LMC6953 is a voltage supervisory chip designed to meet PCI (Peripheral Component Interconnect) Specifications Revision 2.1. It monitors 5V and 3.3V power supplies. In cases of power-up, power-down, brown-out, power failure and manual reset interrupt, the LMC6953 provides an active low reset. $\overline{\text{RESET}}$ holds low for 100 ms after both 5V and 3.3V powers recover, or after manual reset signal returns to high state. The external capacitor on pin 8 adjusts the reset delay.

This part is ideal on PCI motherboards or add-in cards to ensure the integrity of the entire system when there is a fault condition. The active low reset sets the microprocessor or local device in a known state.

The LMC6953 has a built-in bandgap reference that accurately determines all the threshold voltages. The internal reset delay circuitry eliminates additional discrete components.

Typical Application Circuits

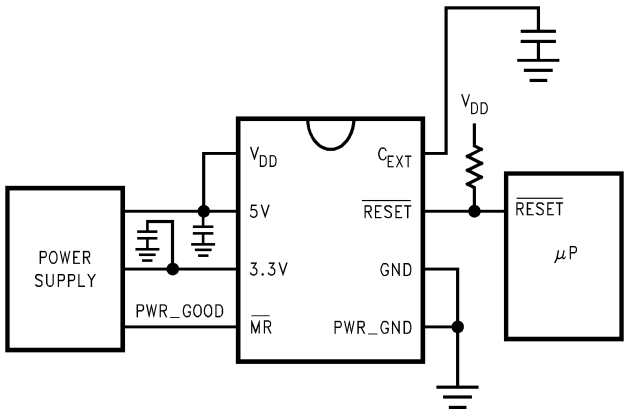


Figure 1. On Mother Board

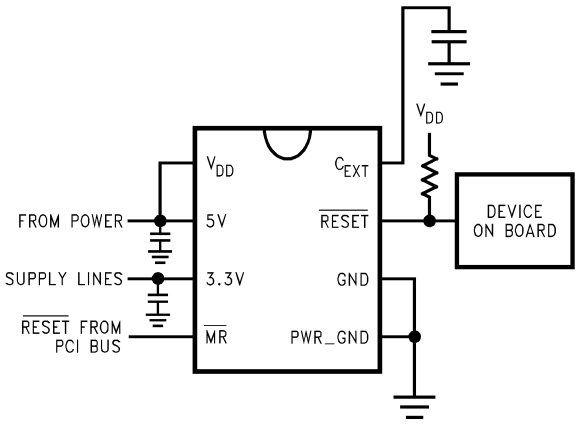


Figure 2. On Add-in Cards

Connection Diagram

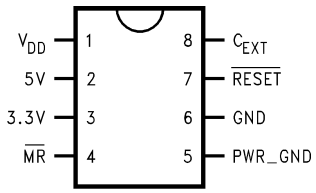


Figure 3. 8–Pin SOIC
Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

ESD Tolerance (3)	
Human Body Model	2 kV
Machine Model	200V
Voltage at Input Pin	7V
Supply Voltage	7V
Current at Output Pin	15 mA
Current at Power Supply Pin (4)	10 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see DC ELECTRICAL CHARACTERISTICS and AC ELECTRICAL CHARACTERISTICS.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF. Machine model. 200Ω in series with 100 pF.
(4) Supply current measured at pins 1, 2, and 3. The 4.7 kΩ pull-up resistor on pin 7 is not tied to V_{DD}in this measurement.

OPERATING RATINGS(1)

Supply Voltage	1.5V to 6V
Junction Temperature Range	
LMC6953C	−40°C to +85°C
Thermal Resistance (θ_{JA})	
D Package	165°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see DC ELECTRICAL CHARACTERISTICS and AC ELECTRICAL CHARACTERISTICS.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all **boldface** limits specified for T_J = −40°C to +85°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	T_J = 0°C to 70°C (1)	**5.45**	5.60	**5.75**	V
		T_J = −40°C to 85°C (1)	**5.30**	5.60	**5.90**	V
V_{L5}	V_{DD} Under-Voltage Threshold	T_J = 0°C to 70°C (1)	**4.25**	4.40	**4.55**	V
		T_J = −40°C to 85°C (1)	**4.10**	4.40	**4.70**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	T_J = 0°C to 70°C (2)	**3.80**	3.95	**4.10**	V
		T_J = −40°C to 85°C (2)	**3.60**	3.95	**4.30**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	T_J = 0°C to 70°C (2)	**2.50**	2.65	**2.80**	V
		T_J = −40°C to 85°C (2)	**2.30**	2.65	**3.00**	V
V_{MR}	Manual RESET Threshold			2.50	**2.80**	V
V_{PF}	Power Failure Differential Voltage (3.3V Pin–5V Pin)	(3)		150	**300**	mV
R_{IN}	Input Resistance at 5V and 3.3V Pins			35		kΩ
V_{OL}	$\overline{\text{RESET}}$ Output Low	T_J = 0°C to 70°C V_{DD} = 1.5V to 6V		0.05	**0.10**	V
		T_J = −40°C to 85°C V_{DD} = 1.55V to 6V				
I_S	Supply Current	(4)		0.8	**1.50**	mA

(1) PCI Specifications Revision 2.1, Section 4.2.1.1 and Section 4.3.2.
(2) PCI Specifications Revision 2.1, Section 4.2.2.1 and Section 4.3.2.
(3) PCI Specifications Revision 2.1 and Section 4.3.2.
(4) Supply current measured at pins 1, 2, and 3. The 4.7 kΩ pull-up resistor on pin 7 is not tied to V_{DD}in this measurement.

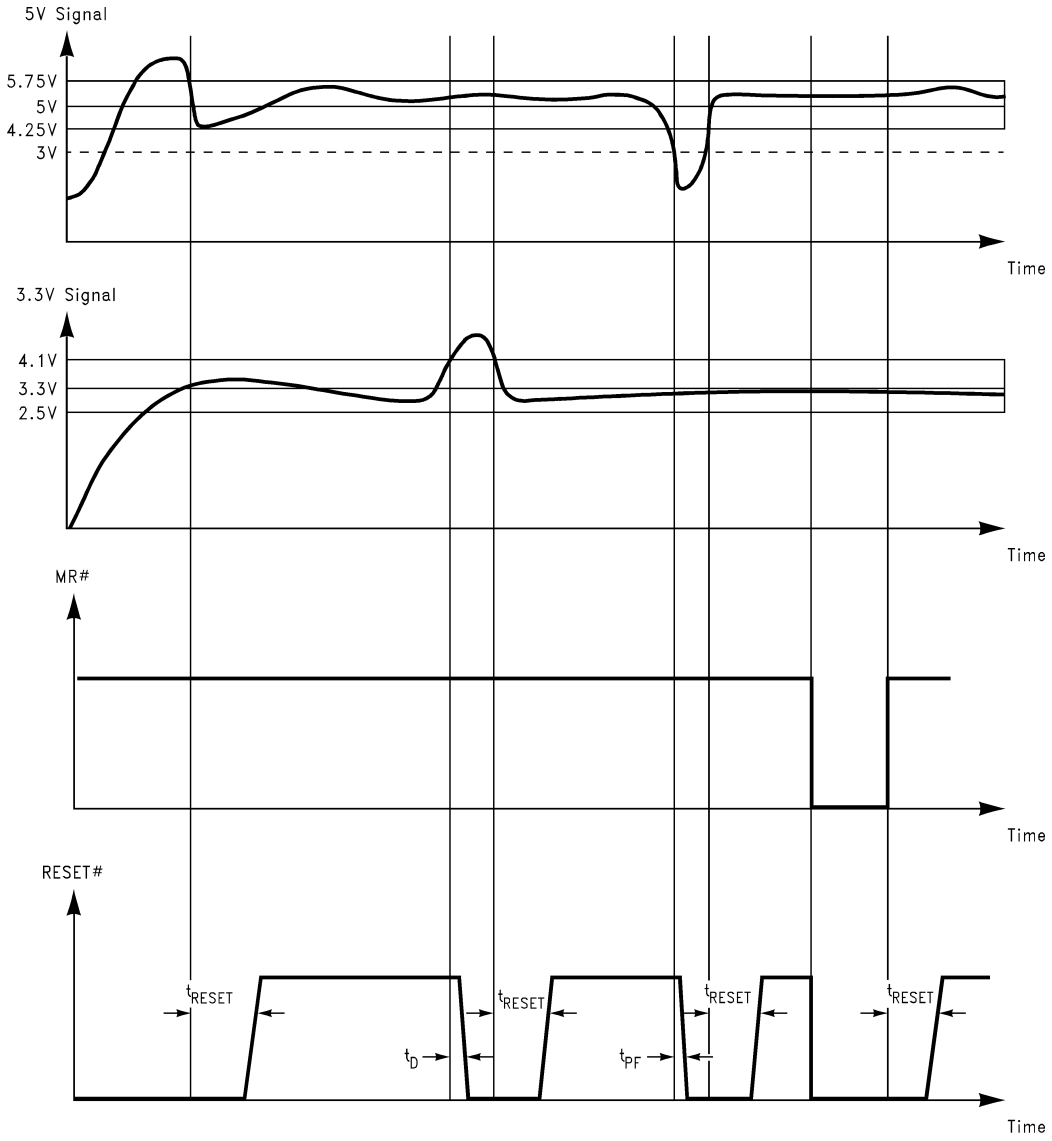
AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all **boldface** limits specified for T_J = −40°C to 85°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Typ	LMC6953 Limit	Units
t_D	Over or Under Voltage Response Time	(1)	150	**490**	ns max
t_{PF}	Power Failure Response Time	(2)	40	**90**	ns max
t_{RESET}	Reset Delay	C_{EXT} = 0.01 µF	100		ms

(1) PCI Specifications Revision 2.1, Section 4.3.2. The response time is measured individually with ±750 mV of overdrive applied to pin 2 then ±600 mV of overdrive applied to pin 3 and taking the worst number of the four measurements.
(2) PCI Specifications Revision 2.1, Section 4.3.2. The power failure response time is measured with a signal changing from 5V to 3V applied to pin 2 and a 3.3V DC applied to pin 3.

LMC6953 TIMING DIAGRAM



Note: t_{RESET}, t_D and t_{PF} are not to scale.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, T_A = 25°C

Supply Current vs Temperature

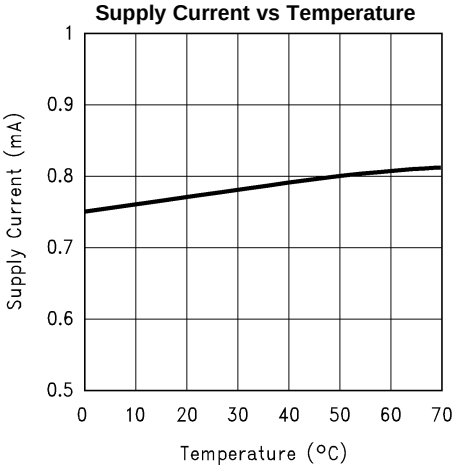


Figure 4.

Output Voltage vs Supply Voltage

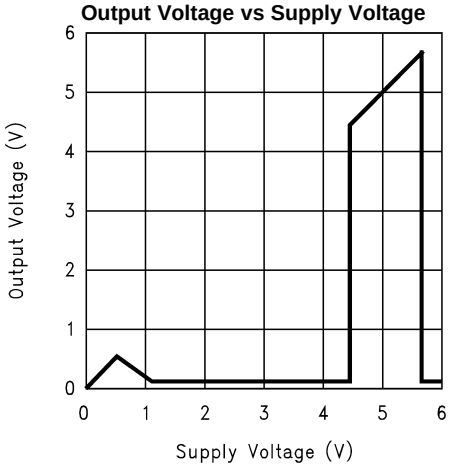


Figure 5.

Power-Up Supply Voltage vs Temperature

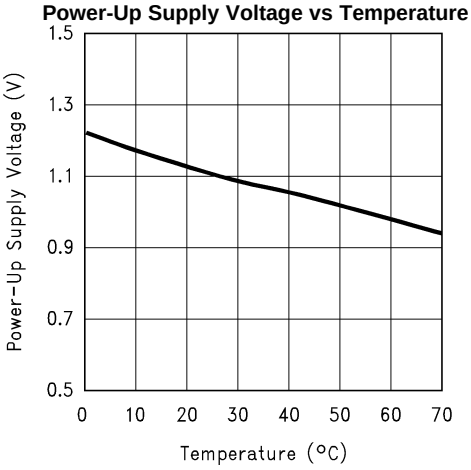


Figure 6.

V_{H5} vs Temperature

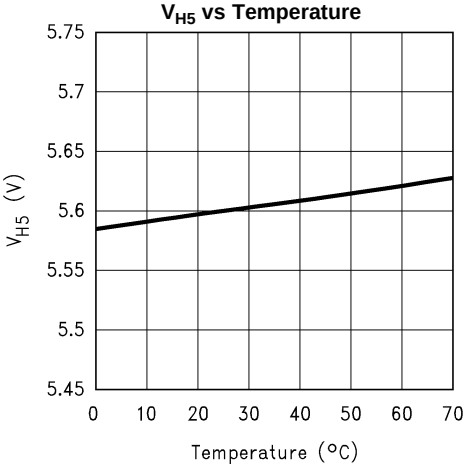


Figure 7.

V_{L5} vs Temperature

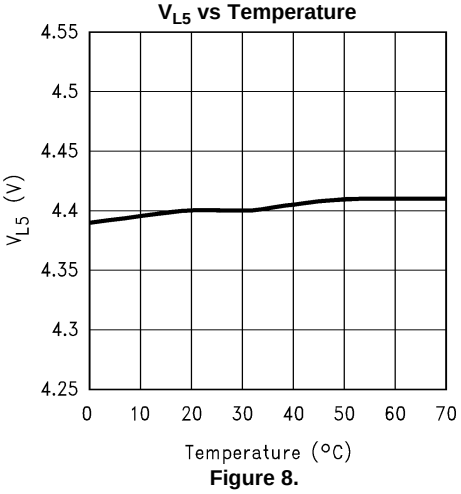


Figure 8.

$V_{H3.3}$ vs Temperature

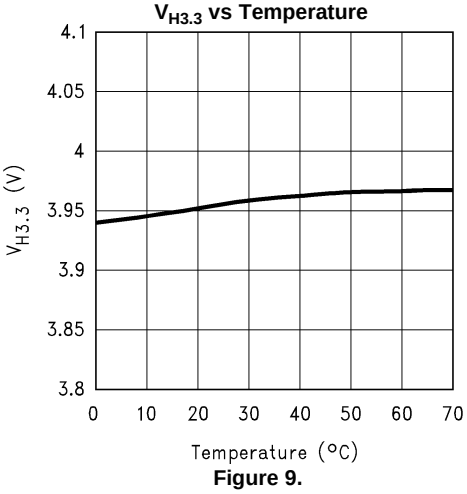


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C

$V_{L3.3}$ vs Temperature

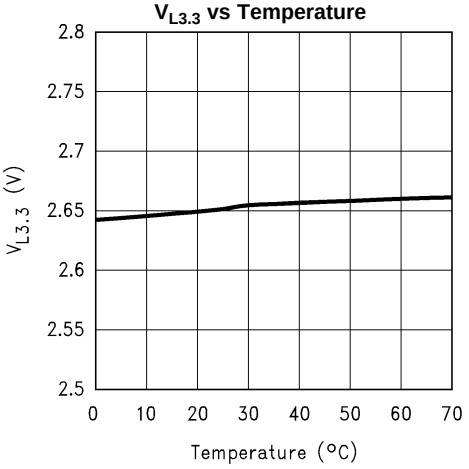


Figure 10.

Over-Voltage Response Time vs Temperature

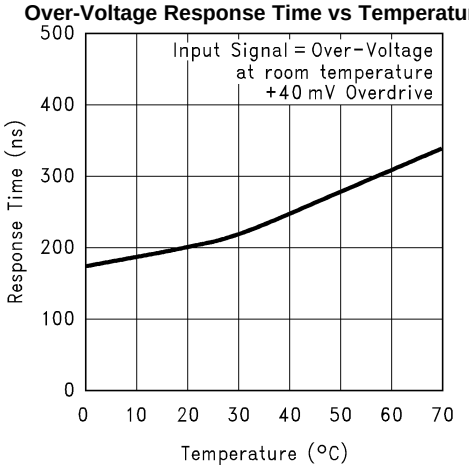


Figure 11.

3Under-Voltage Response Time vs Temperature

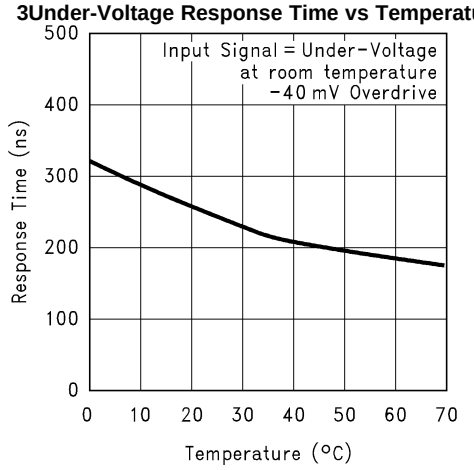


Figure 12.

Power Failure Response Time vs Temperature

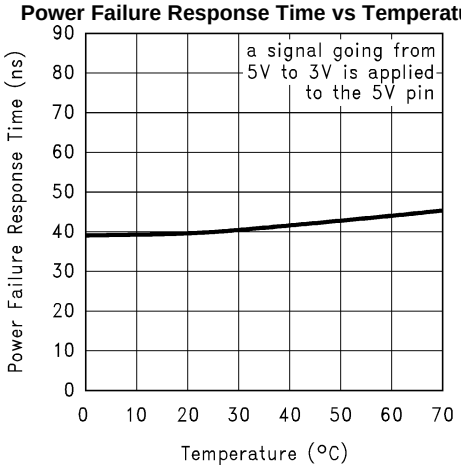


Figure 13.

V_{OL} vs $R_{PULL-UP}$

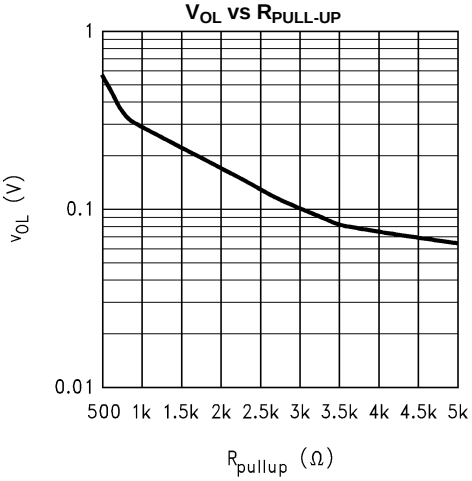


Figure 14.

I_{OL} vs $R_{PULL-UP}$

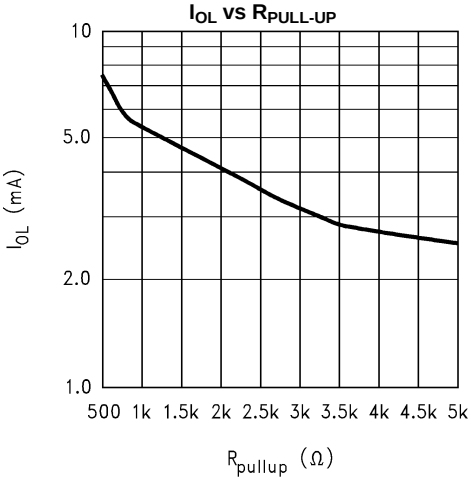


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C

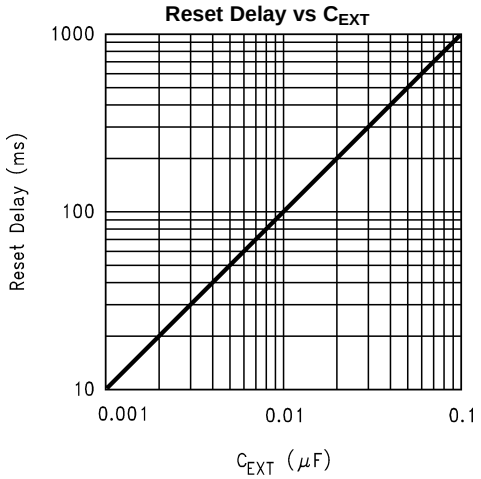


Figure 16.

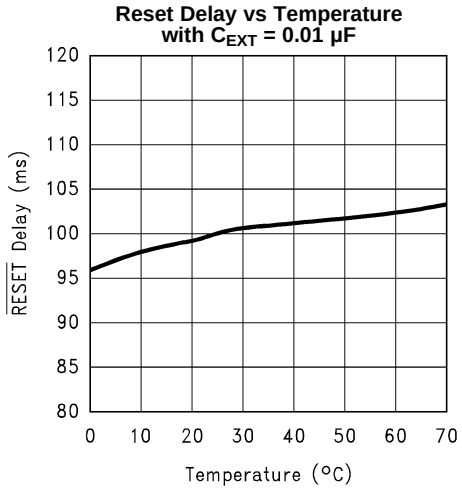
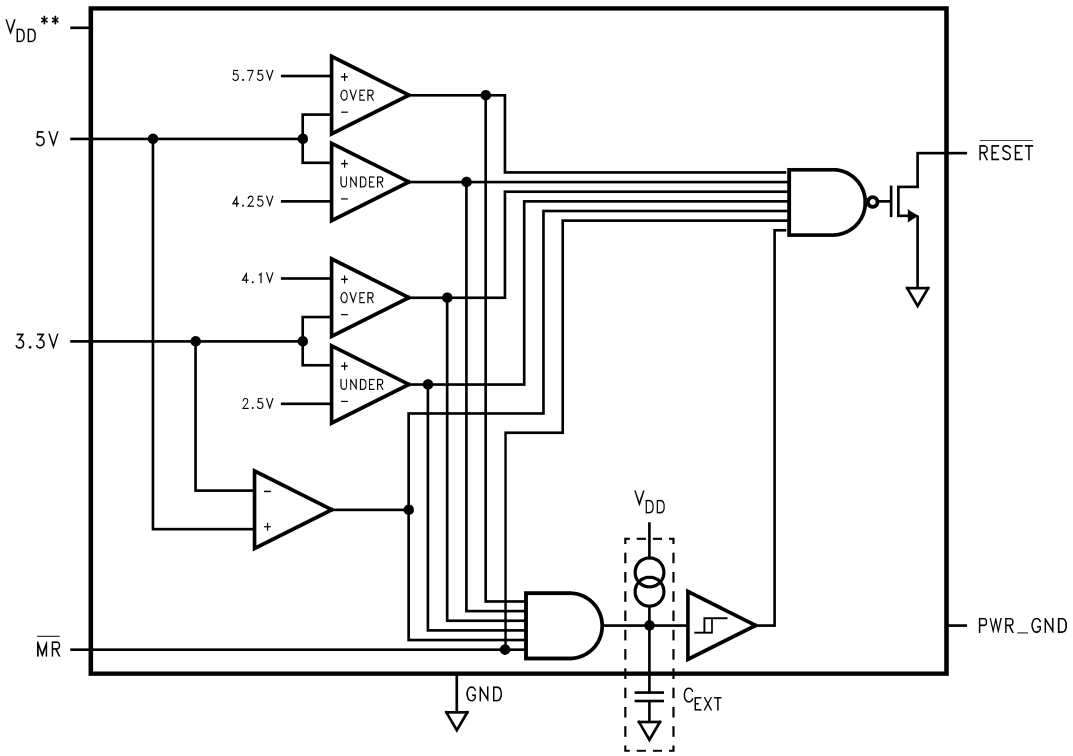


Figure 17.

BLOCK DIAGRAM OF THE LMC6953



** All five comparators' positive power supplies are connected to V_{DD}

TRUTH TABLE(1)

Power Failure	5V Over-Voltage	5V Under-Voltage	3.3V Over-Voltage	3.3V Under-Voltage	$\overline{MR}$	$\overline{RESET}$
Fail	X	X	X	X	High	Low
X	Fail	X	X	X	High	Low
X	X	Fail	X	X	High	Low
X	X	X	Fail	X	High	Low
X	X	X	X	Fail	High	Low
X	X	X	X	X	Low	Low
OK	OK	OK	OK	OK	High	High

(1) X = Don't Care

PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	5V input supply voltage. This pin supplies power to the internal comparators. It can be connected to a capacitor acting as a back-up battery. Otherwise, it should be shorted to the 5V pin.
2	5V	5V input supply voltage. This pin is not connected to the positive power supply of the internal comparators. It provides input signal to the 5V window comparators as well as the power failure comparator.
3	3.3V	3.3V input supply voltage. This pin provides input signal to the 3.3V window comparators and the power failure comparator.
4	$\overline{MR}$	Manual reset input pin. It takes 5V CMOS logic low and triggers $\overline{RESET}$. If not used, this pin should be connected to V_{DD}.
5	PWR—GND	Ground.
6	GND	This pin should be grounded at all times.
7	$\overline{RESET}$	Active low reset output. $\overline{RESET}$ holds low for 100 ms after both 5V and 3.3V powers recover, or after manual reset signal returns to high state.
8	C_{EXT}	External capacitor pin. The value of C_{EXT} sets the reset delay.

APPLICATION NOTE

HOW THE LMC6953 FUNCTIONS

The LMC6953 is a power supply supervisor with its performance specifications compliant to PCI Specifications Revision 2.1. The chip monitors power-up, power-down, brown-out, power failure and manual reset interrupt situations.

During power-up, the LMC6953 holds $\overline{\text{RESET}}$ low for 100 ms after both 5V and 3.3V are within specified windows. It asserts reset in 490 ns when a brown-out is detected. Brown-out occurs when 5V supply is above 5.75V over-voltage or below 4.25V under-voltage or when 3.3V supply is above 4.1V over-voltage or 2.5V under-voltage. In case of power failure where the 5V supply falls under 3.3V supply by 300 mV maximum, reset is asserted in 90 ns. $\overline{\text{RESET}}$ also can be asserted by sending a 5V CMOS logic low to the manual reset pin.

Each time $\overline{\text{RESET}}$ is asserted, it holds low for 100 ms after a fault condition is recovered. The 100 ms reset delay is generated by the 0.01 µF C_{EXT} capacitor, and can be adjusted by changing the value of C_{EXT}.

It is highly recommended to place lands on printed circuit boards for 120 pF capacitors between pin 2 and ground and also between pin 3 and ground. As power supplies may change abruptly, there can be very high frequency noise present and the capacitors can minimize the noise,

MINIMUM SUPPLY VOLTAGE FOR $\overline{\text{RESET}}$ ASSERTION

The LMC6953 specifies V_{DD} = 1.55V as the minimum supply voltage to achieve consistent $\overline{\text{RESET}}$ assertion. This ensures system stability in initialization state.

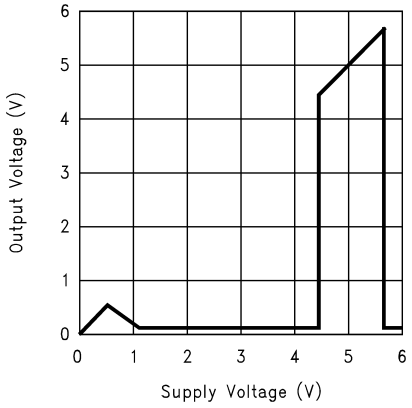


Figure 18. Output Voltage vs Supply Voltage

Figure 18 is measured by shorting pins 1, 2 and 3 together when supply voltage is from 0V to 3.3V. Then pin 3 is connected with a constant 3.3 V_{DC} and pins 1 and 2 are connected to a separate power supply that continues to vary from 3.3V to 6V.

5V AND V_{DD} PINS

By having the 5V and the V_{DD} pins separate, a capacitor can be used as a back-up power supply in event of a sudden power supply failure. This circuit is shown in Figure 22. Under normal condition, the diode is forward-biased and the capacitor is charged up to V_{DD} − 0.7V. If the power supply goes away, the diode becomes reverse-biased, isolating the 5V and the V_{DD} pins. The capacitor provides power to the internal comparators for a short duration for the LMC6953 to operate.

C_{EXT} SETS RESET DELAY IN LINEAR FASHION

The LMC6953 has internal delay circuitry to generate the reset delay. By choosing different values of capacitor C_{EXT}, reset delay can be programmed to the desired length for the system to stabilize after a fault condition occurs.

EVALUATING THE LMC6953

To Measure Over-Voltages And Under-Voltages

Connect a 3.3V DC to the 3.3V pin and a 5V DC to the V_{DD} and the 5V pins (V_{DD} and 5V pins are shorted). $\overline{\text{RESET}}$ output is high because voltages are within window. These voltages should be monitored. While keeping the 3.3V constant, increase the 5V DC signal until a $\overline{\text{RESET}}$ low is detected. The point on the 5V DC signal at which $\overline{\text{RESET}}$ changes from high to low is the 5V over-voltage. It is typically 5.6V. To detect 5V under-voltage, start the 5V DC signal from 5V and decrease it until a $\overline{\text{RESET}}$ low is detected. The point on the 5V DC signal at which $\overline{\text{RESET}}$ changes from high to low is the 5V under-voltage. It is typically 4.4V.

To find 3.3V over-voltage and under-voltage, keep the 5V DC at 5V and vary the 3.3V DC signal until a $\overline{\text{RESET}}$ low is detected.

To Measure Timing Specifications

For evaluation purposes only, the V_{DD} and the 5V pins should have separate signals. It is easier to measure response time in this manner. The V_{DD} pin is connected to a steady 5V DC and the 5V pin is connected to a pulse generator. To simulate the power supply voltages going out of window, a pulse generator with disable/enable feature and rise and fall time adjustment is recommended. To measure the $\overline{\text{RESET}}$ signal, a oscilloscope is recommended because of its ability to capture and store a signal.

To measure the 5V under-voltage response time on the LMC6953, set the pulse generator to trigger mode and program the amplitude to have a high value of 5V and a low value of the 5V under-voltage threshold measured previously with 50 mV overdrive. For example, if the measured 5V under-voltage is 4.4V, then a 50 mV overdrive on this signal is 4.35V. The disable feature on the pulse generator should be on. Program the fall time of the pulse to be 30 ns and program the scope to trigger on the falling edge, with trigger level of 4.5V. Set the scope to 200 ns/division. The probes should be connected to the 5V pin and the $\overline{\text{RESET}}$ pin. Now enable the 5V signal from the pulse generator and trigger the signal. Be aware that when the signal is enabled, there is high frequency noise present, and putting a 120 pF capacitor between the 5V pin and ground suppresses some of the noise. Response time is measured by taking the 5V under-voltage threshold on the 5V signal to the point where $\overline{\text{RESET}}$ goes low. Figure 19 shows a scope photo of 5V under-voltage waveforms. It is taken with a signal going from 5V to 4.25V at the 5V pin.

To measure the 100 ms $\overline{\text{RESET}}$ delay, change the scope to 50 ms/division and trigger the 5V signal again. $\overline{\text{RESET}}$ should stay low for 100 ms after the 5V is recovered and within window.

Other over-voltages and under-voltages can be measured by changing the pulse generator to different voltage steps. Putting a 120 pF capacitor between the 3.3V pin and ground is recommended in evaluating 3.3V signal.

To measure power-failure response time, set the pulse generator from 5V to 3V with fall time of the pulse 3 ns and connect it to the 5V pin. $\overline{\text{RESET}}$ should go low within 90 ns of power failure. Figure 20 shows a scope photo of power failure waveforms. It is taken with a signal going from 5V to 3V at the 5V pin.

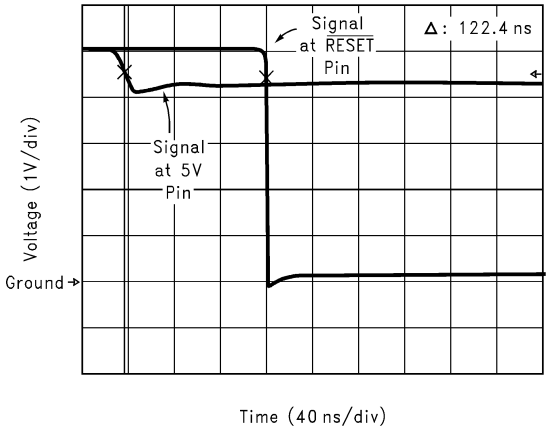


Figure 19. 5V Under-Voltage Waveforms

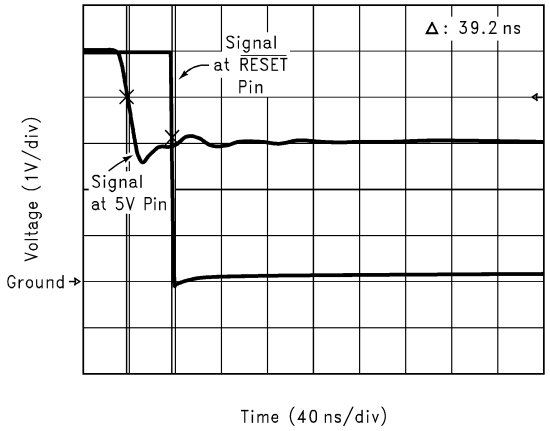


Figure 20. Power Failure Waveforms

Typical Application Circuits

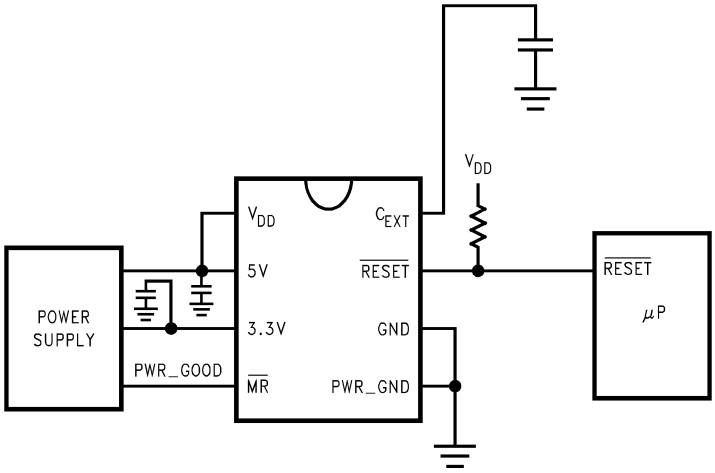


Figure 21. On Mother Board

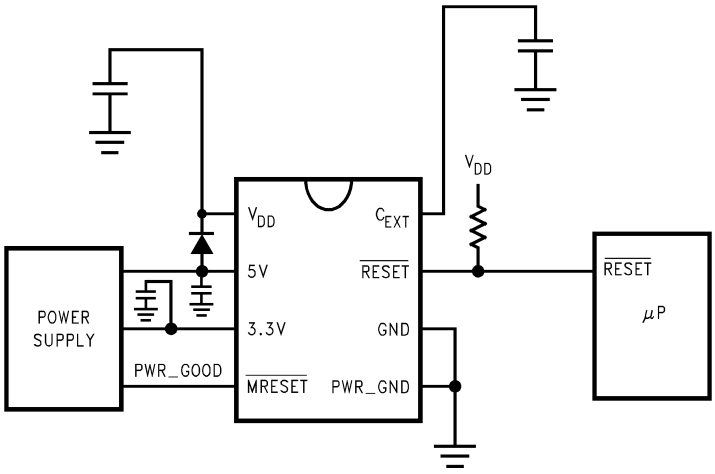


Figure 22. On Mother Board with Capacitor as a Back-up Power Supply

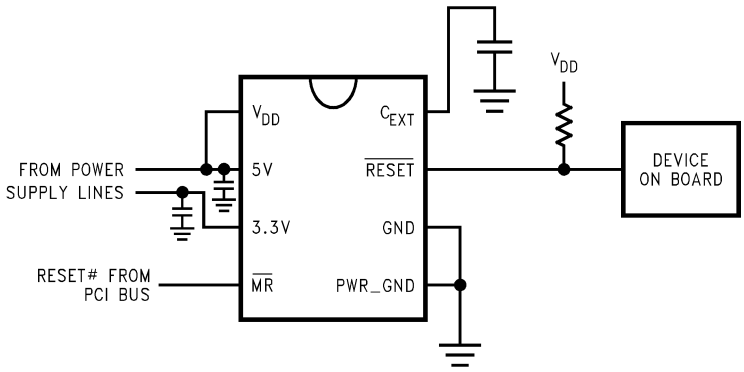


Figure 23. On Add-In Cards

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6953CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LMC69 53CM	Samples
LMC6953CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	0 to 70	LMC69 53CM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

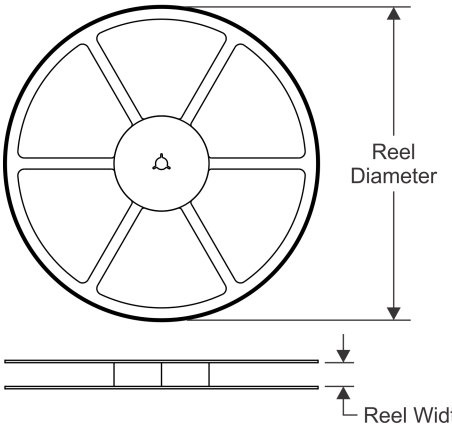
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

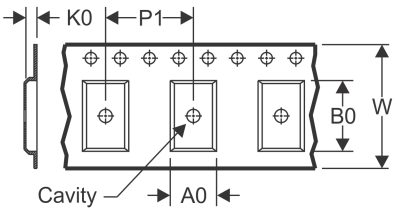
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

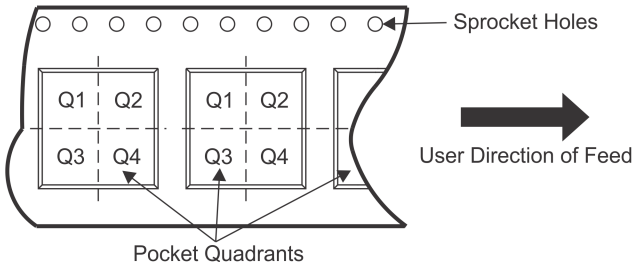


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

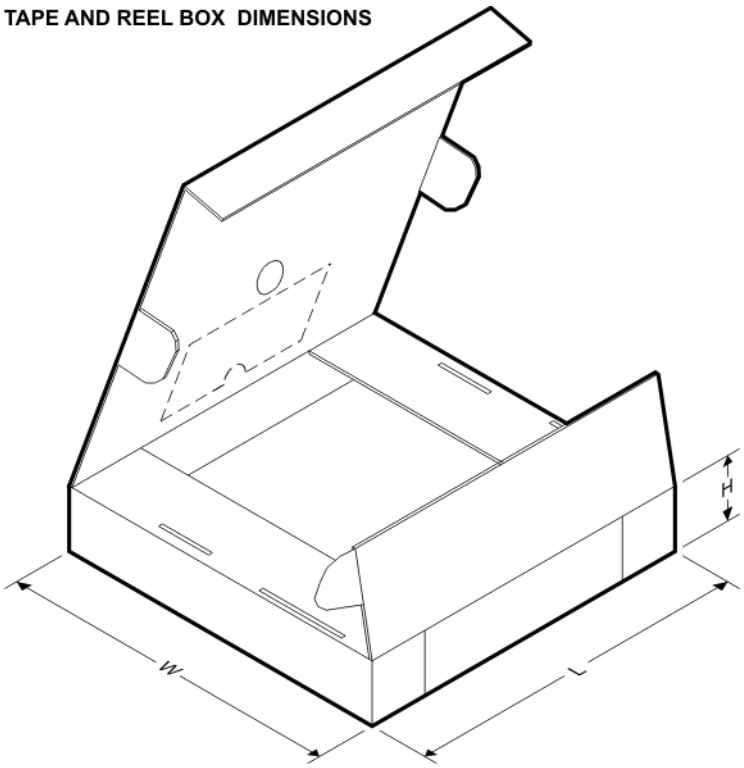
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6953CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

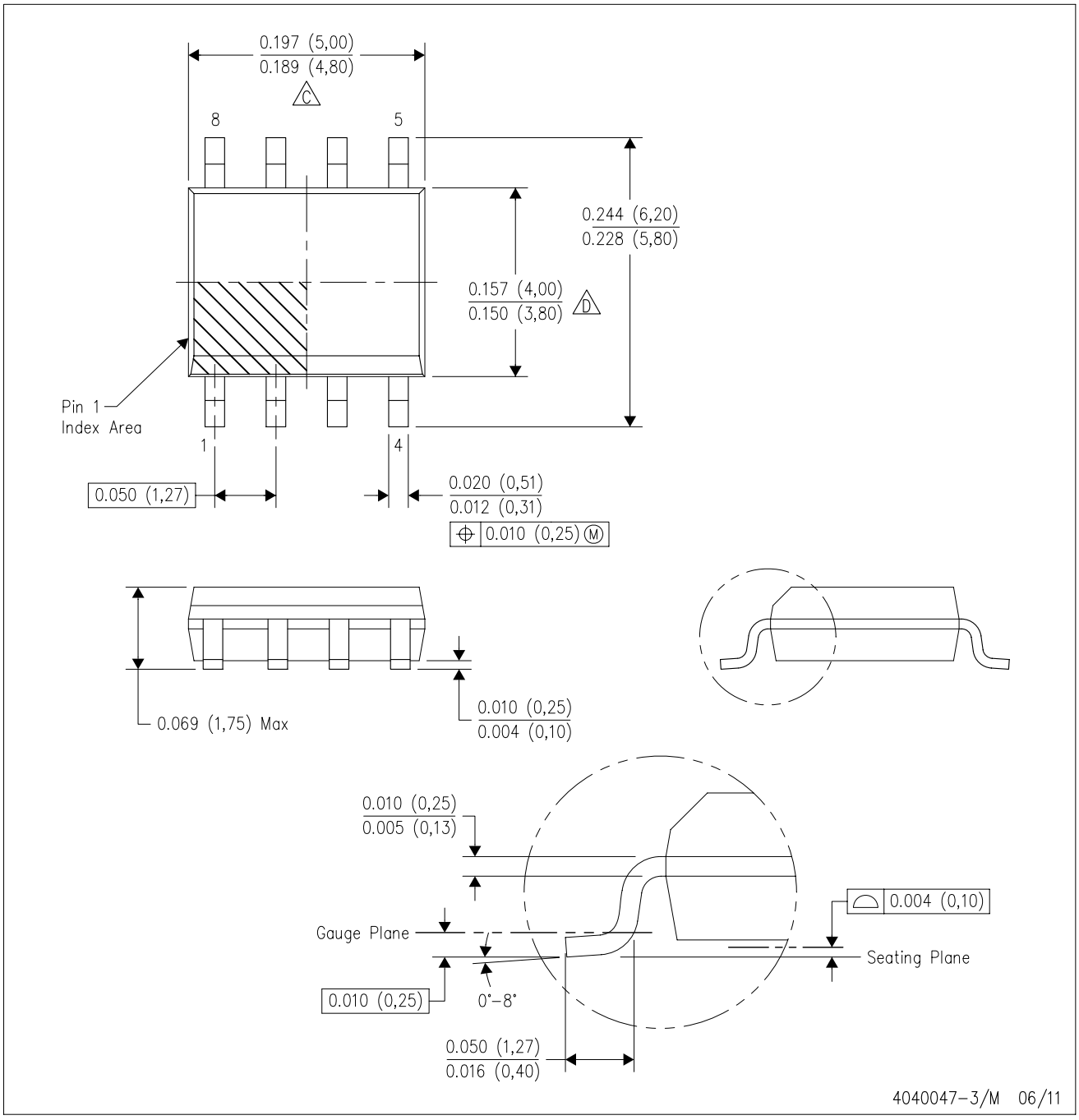
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6953CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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