LME49725 PowerWise® Dual High Performance, High Fidelity Audio Operational Amplifier

Check for Samples: LME49725

FEATURES

- **Optimized for Superior Audio Signal Fidelity**
- **Output Short Circuit Protection**
- **PSRR and CMRR Exceed 120dB (Typ)**

APPLICATIONS

- **Audio Amplification**
- **Preamplifiers**
- **Multimedia**
- **Phono Preamplifiers**
- **Professional Audio**
- **Equalization and Crossover Networks**
- **Line Drivers**
- **Line Receivers**
- **Active Filters**

KEY SPECIFICATIONS

- **Power Supply Voltage Range: ±4.5V to ±18 V**
- **THD+N (A_V = 1, V_{OUT} = 3V_{RMS}, f_{IN} = 1kHz)**
  - **R_L = 2kΩ: 0.00004% (Typ)**
  - **R_L = 600Ω: 0.00004% (Typ)**
- **Quiescent Current per Amplifier: 3.0 mA (Typ)**
- **Input Noise Density: 3.3 nV/√Hz (Typ)**
- **Slew Rate: ±15 V/μs (Typ)**
- **Gain Bandwidth Product: 40 MHz (Typ)**
- **Open Loop Gain (R_L = 600Ω): 135 dB (Typ)**
- **Input Bias Current: 15 nA (Typ)**
- **Input Offset Voltage: 0.5 mV (Typ)**
- **DC Gain Linearity Error: 0.000009 % (Typ)**

DESCRIPTION

The LME49725 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49725 audio operational amplifiers deliver superior audio signal amplification for outstanding audio performance. The LME49725 combines extremely low voltage noise density (3.3nV/√Hz) with vanishingly low THD+N (0.00004%) to easily satisfy the most demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49725 has a high slew rate of ±15V/μs and an output current capability of ±22mA. Further, dynamic range is maximized by an output stage that drives 2kΩ loads to within 1V of either power supply voltage and to within 1.4V when driving 600Ω loads.

Part of the PowerWise® family of energy efficient solutions, the LME49725 consumes only 3.0mA of supply current per amplifier while providing superior performance to high performance, high fidelity applications.

The LME49725's outstanding CMRR (120dB), PSRR (120dB), and V_{OS} (0.5mV) give the amplifier excellent operational amplifier DC performance.

The LME49725 has a wide supply range of ±4.5V to ±18V. Over this supply range the LME49725's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49725 is unity gain stable. This audio operational amplifier achieves outstanding AC performance while driving complex loads with values as high as 100pF.

The LME49725 is available in 8–lead narrow body SOIC.

Connection Diagram

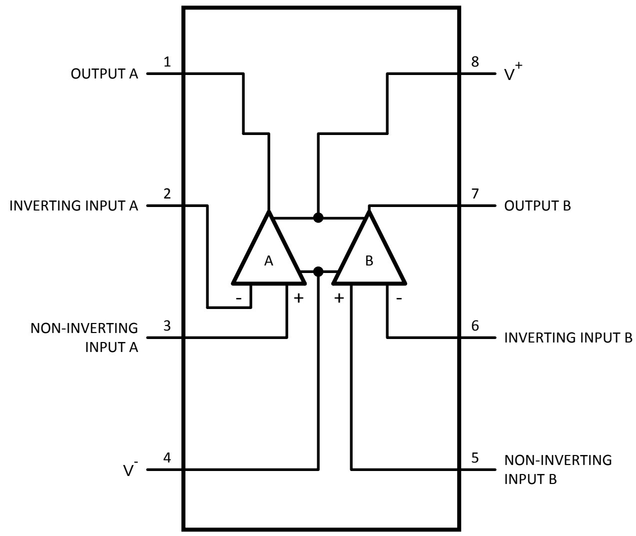


Figure 1. SOIC Package
See Package Number D0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Power Supply Voltage ($V_S = V^+ - V^-$)		38V
Storage Temperature		−65°C to 150°C
Input Voltage		(V-)-0.7V to (V+)+0.7V
Differential Input Voltage		±0.7V
Output Short Circuit(3)		Continuous
Power Dissipation		Internally Limited
ESD Rating(4)		2000V
ESD Rating(5)	Pins 1, 4, 7 and 8	200V
	Pins 2, 3, 5 and 6	100V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (SOIC)	145°C/W
Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)		$-40°C \le T_A \le 85°C$
Supply Voltage Range		$\pm4.5V \le V_S \le \pm18V$

(1) "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
(4) Human body model, applicable std. JESD22-A114C.
(5) Machine model, applicable std. JESD22-A115-A.

Electrical Characteristics for the LME49725[1]

The specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, T_A = 25°C, unless otherwise specified.

Parameter		Test Conditions	LME49725		Units (Limits)
			Typ[2]	Limit[3]	
THD+N	Total Harmonic Distortion + Noise	A_V = 1, V_{OUT} = $3V_{rms}$ R_L = 2kΩ R_L = 600Ω	0.00004 0.00004	0.0002	% %
IMD	Intermodulation Distortion	A_V = 1, V_{OUT} = $3V_{RMS}$ Two-tone, 60Hz & 7kHz 4:1	0.00005		%
GBWP	Gain Bandwidth Product		40	30	MHz (min)
SR	Slew Rate		±15	±10	V/μs (min)
FPBW	Full Power Bandwidth	V_{OUT} = $1V_{P-P}$, –3dB referenced to output magnitude at f = 1kHz	7		MHz
t_s	Settling time	A_V = –1, 10V step, C_L = 100pF 0.1% error range	1.6		μs
e_n	Equivalent Input Noise Voltage	f_{BW} = 20Hz to 20kHz	0.4	0.8	$μV_{RMS}$ (max)
	Equivalent Input Noise Density	f = 1kHz f = 10Hz	3.3 20	5.2	nV/√Hz (max)
i_n	Current Noise Density	f = 1kHz f = 10Hz	1.4 3.5		pA/√Hz pA/√Hz
V_{OS}	Offset Voltage		±0.5	±1.0	mV (max)
$ΔV_{OS}$/ΔTemp	Average Input Offset Voltage Drift vs Temperature	–40°C ≤ T_A ≤ 85°C	0.2		μV/°C
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	$ΔV_S$ = 20V[4]	120	100	dB (min)
ISO_{CH-CH}	Channel-to-Channel Isolation	f_{IN} = 1kHz f_{IN} = 20kHz	118 112		dB dB
I_B	Input Bias Current	V_{CM} = 0V	±15	±90	nA (max)
$ΔI_{OS}$/ΔTemp	Input Bias Current Drift vs Temperature	–40°C ≤ T_A ≤ 85°C	0.1		nA/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	11	65	nA (max)
V_{IN-CM}	Common-Mode Input Voltage Range		±13.9	(V+)-2.0 (V-)+2.0	V (min) V (min)
CMRR	Common-Mode Rejection	–10V<Vcm<10V	120	100	dB (min)
Z_{IN}	Differential Input Impedance		30		kΩ
	Common Mode Input Impedance	–10V<Vcm<10V	1000		MΩ
A_{VOL}	Open Loop Voltage Gain	–10V<Vout<10V, R_L = 600Ω	135	110	dB (min)
		–10V<Vout<10V, R_L = 2kΩ	135		dB
		–10V<Vout<10V, R_L = 10kΩ	135		dB
V_{OUTMAX}	Maximum Output Voltage Swing	R_L = 600Ω	±13.6	±11.5	V (min)
		R_L = 2kΩ	±13.9		V
		R_L = 10kΩ	±14.0		V
I_{OUT}	Output Current	R_L = 600Ω, V_S = ±17V	±22		mA (min)
I_{OUT-CC}	Instantaneous Short Circuit Current		+45 –35		mA mA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(3) Datasheet min/max specification limits are ensured by test or statistical analysis.
(4) PSRR is measured as follows: V_{OS} is measured at two supply voltages, ±5V and ±15V, PSRR = $|20\log(ΔV_{OS}/ΔV_S)|$.

Electrical Characteristics for the LME49725[1] (continued)

The specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, T_A = 25°C, unless otherwise specified.

Parameter		Test Conditions	LME49725		Units (Limits)
			Typ[2]	Limit[3]	
R_{OUT}	Output Impedance	f_{IN} = 10kHz Closed-Loop Open-Loop	 0.01 18		 Ω Ω
C_{LOAD}	Capacitive Load Drive Overshoot	100pF	16		%
I_S	Quiescent Current per Amplifier	I_{OUT} = 0mA	3.0	4.5	mA (max)
f_C	1/f Corner Frequency		120		Hz

Typical Performance Characteristics

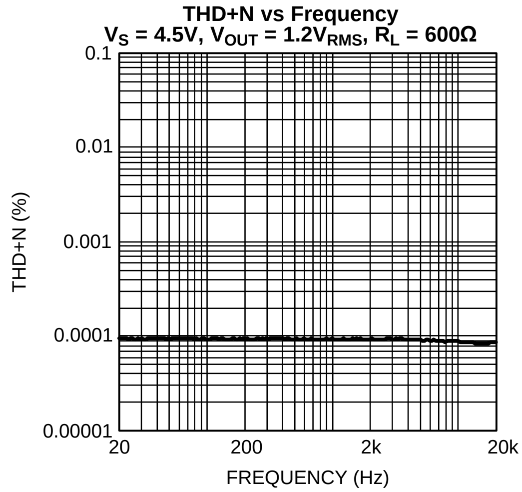


Figure 2.

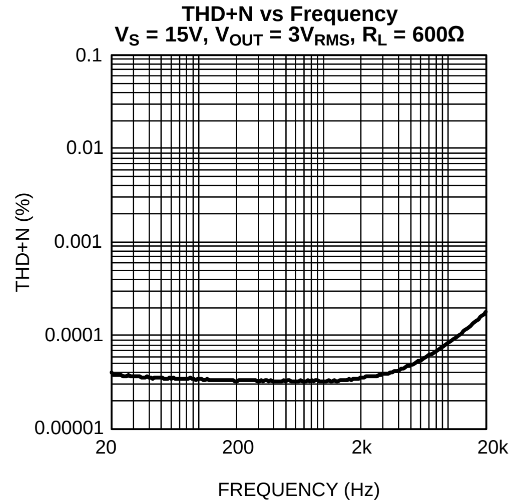


Figure 3.

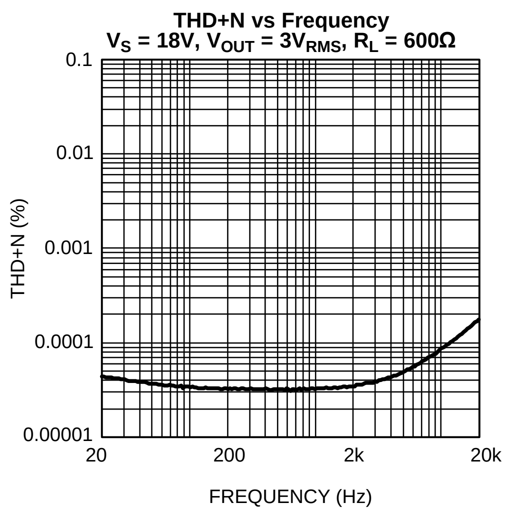


Figure 4.

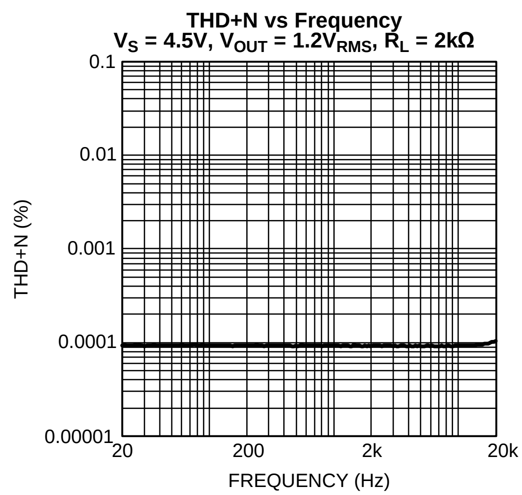


Figure 5.

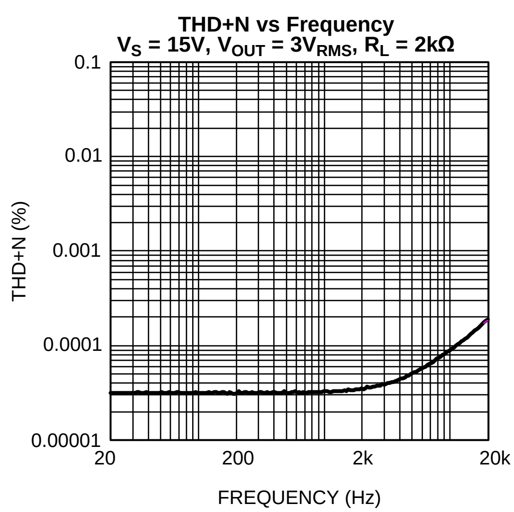


Figure 6.

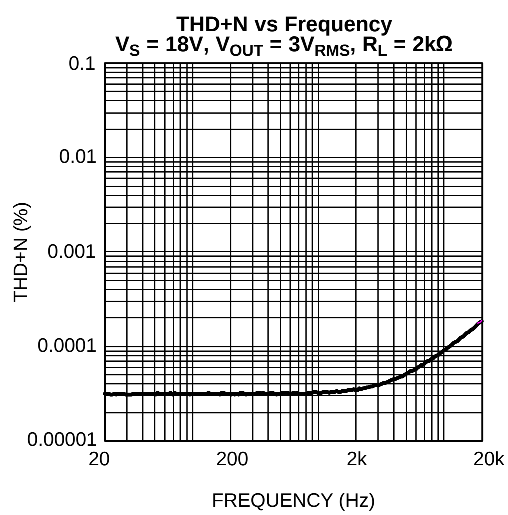
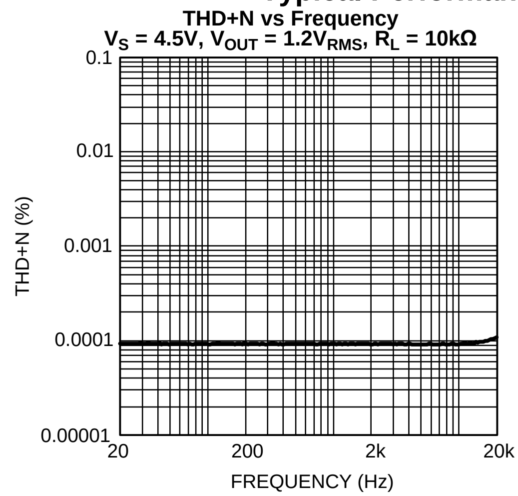


Figure 7.

Typical Performance Characteristics (continued)



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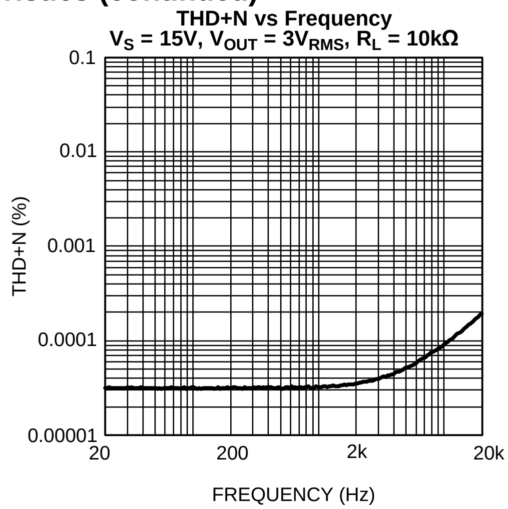

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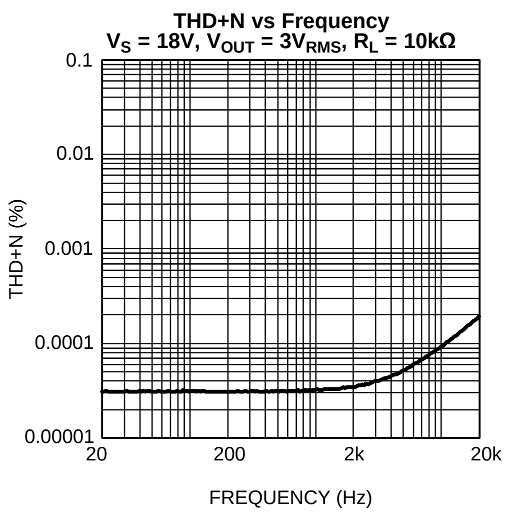


Figure 10.

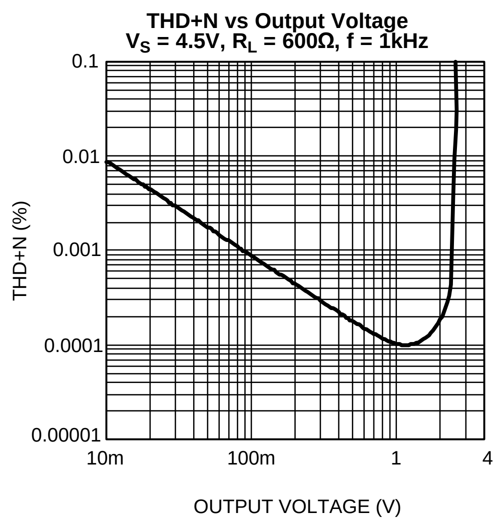


Figure 11.

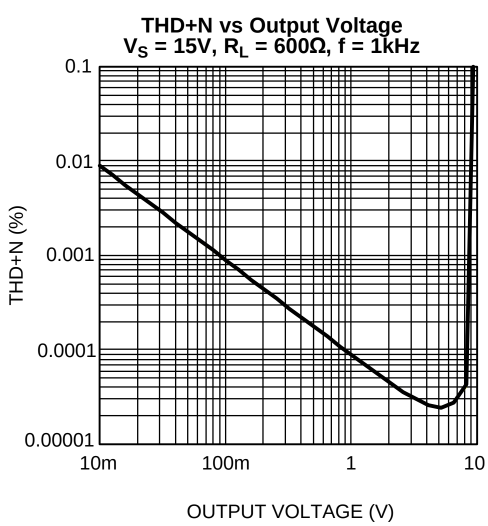


Figure 12.

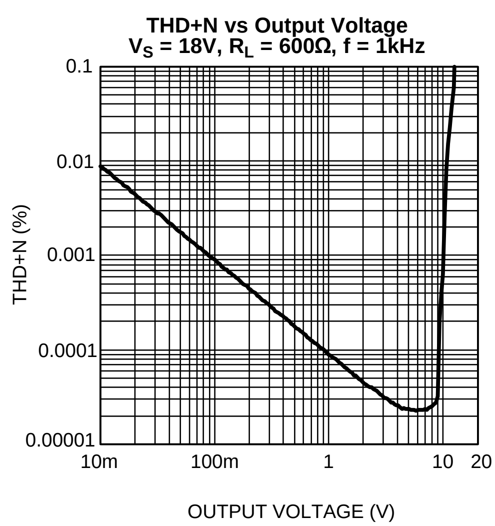


Figure 13.

Typical Performance Characteristics (continued)

THD+N vs Output Voltage
V_S = 4.5V, R_L = 2kΩ, f = 1kHz

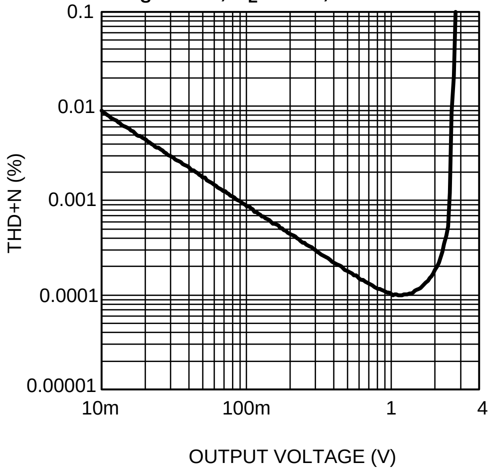


Figure 14.

THD+N vs Output Voltage
V_S = 15V, R_L = 2kΩ, f = 1kHz

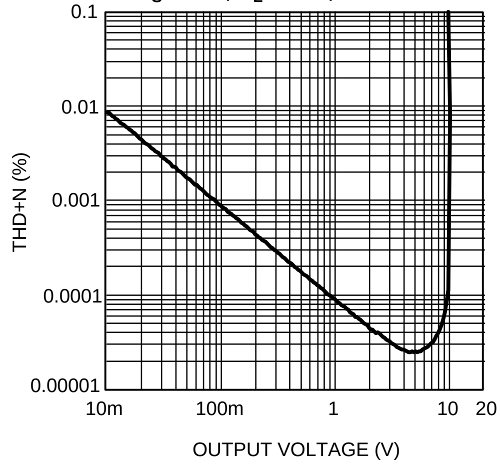


Figure 15.

THD+N vs Output Voltage
V_S = 18V, R_L = 2kΩ, f = 1kHz

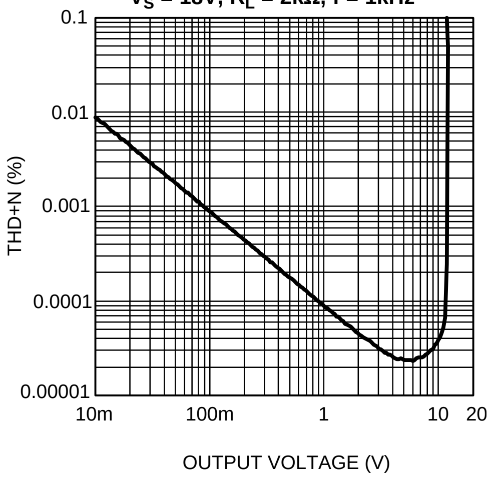


Figure 16.

THD+N vs Output Voltage
V_S = 4.5V, R_L = 10kΩ, f = 1kHz

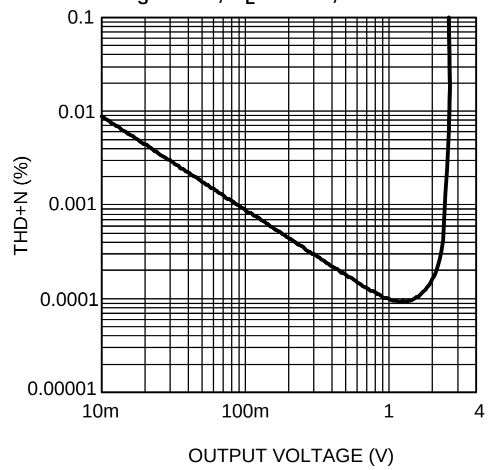


Figure 17.

THD+N vs Output Voltage
V_S = 15V, R_L = 10kΩ, f = 1kHz

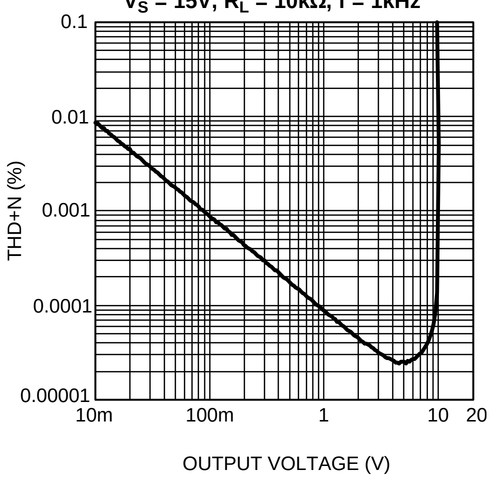


Figure 18.

THD+N vs Output Voltage
V_S = 18V, R_L = 10kΩ, f = 1kHz

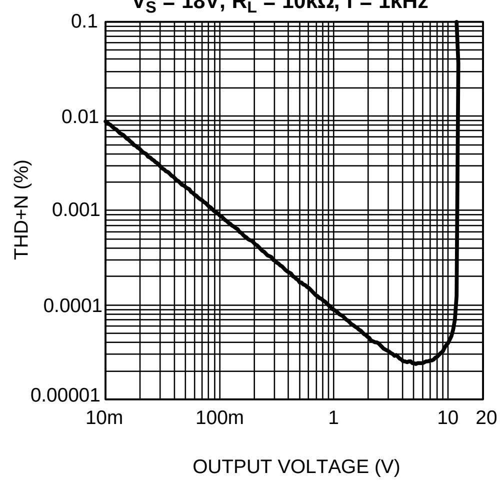


Figure 19.

Typical Performance Characteristics (continued)

CMRR vs Frequency
V_S = 4.5V, R_L = 600Ω

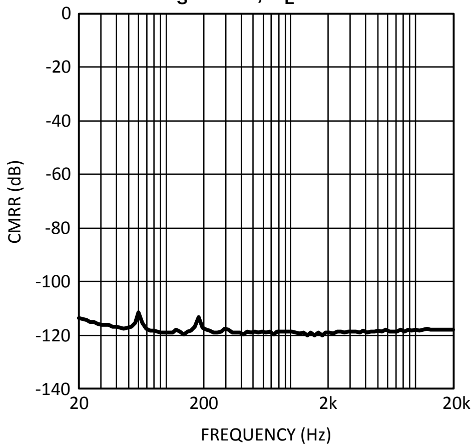


Figure 20.

CMRR vs Frequency
V_S = 15V, R_L = 600Ω

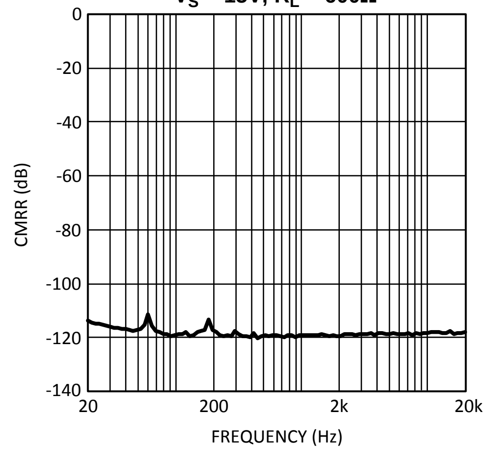


Figure 21.

CMRR vs Frequency
V_S = 15V, R_L = 600Ω

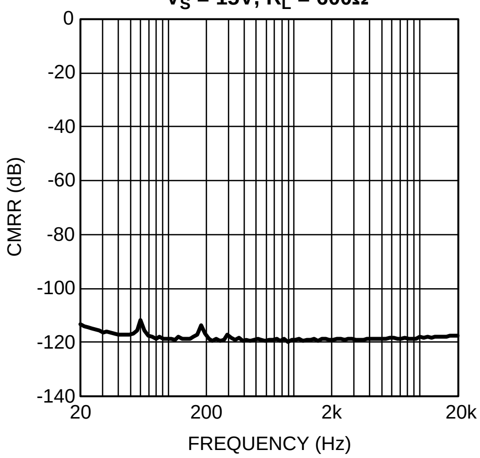


Figure 22.

CMRR vs Frequency
V_S = 4.5V, R_L = 2kΩ

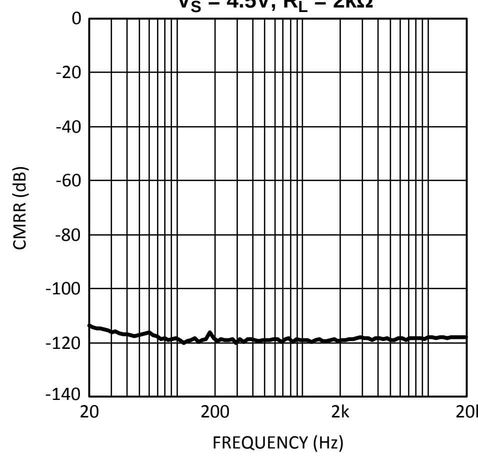


Figure 23.

CMRR vs Frequency
V_S = 15V, R_L = 2kΩ

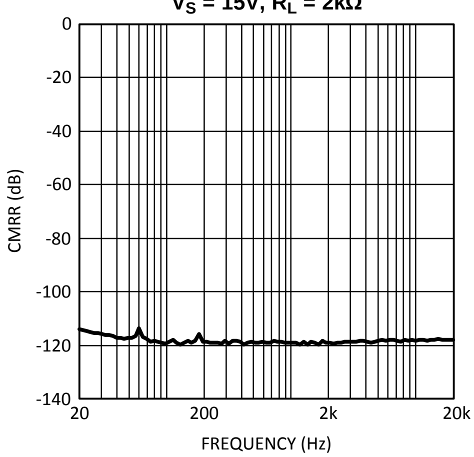


Figure 24.

CMRR vs Frequency
V_S = 18V, R_L = 2kΩ

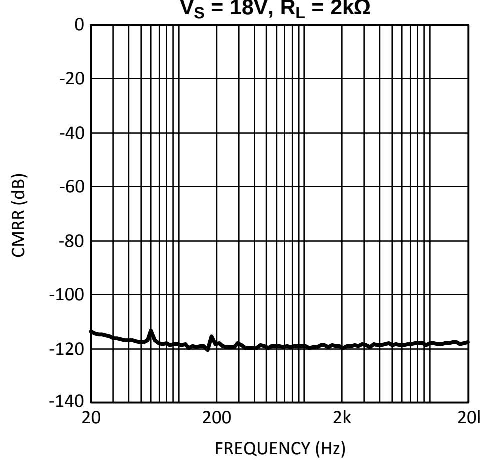


Figure 25.

Typical Performance Characteristics (continued)

CMRR vs Frequency
V_S = 4.5V, R_L = 10kΩ

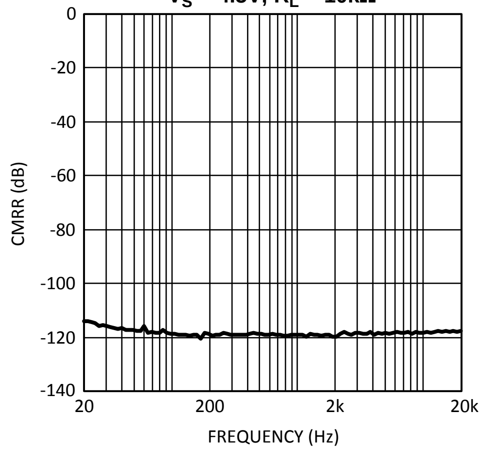


Figure 26.

CMRR vs Frequency
V_S = 15V, R_L = 10kΩ

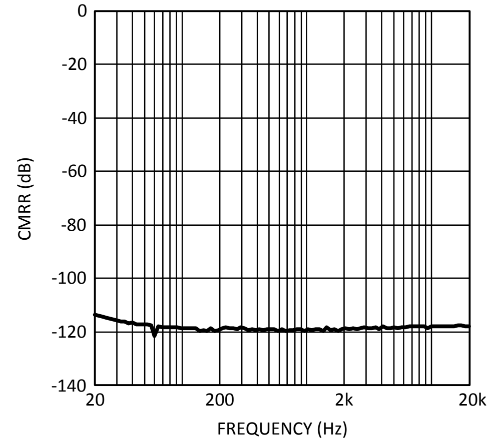


Figure 27.

CMRR vs Frequency
V_S = 18V, R_L = 10kΩ

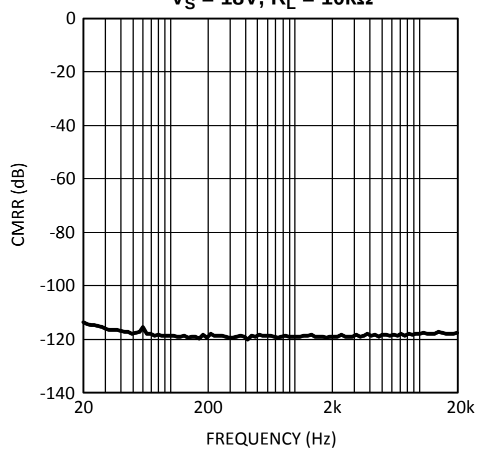


Figure 28.

+PSRR vs Frequency
V_S = 4.5V, R_L = 2kΩ, V_{RIPPLE} = 200mV_{P-P}

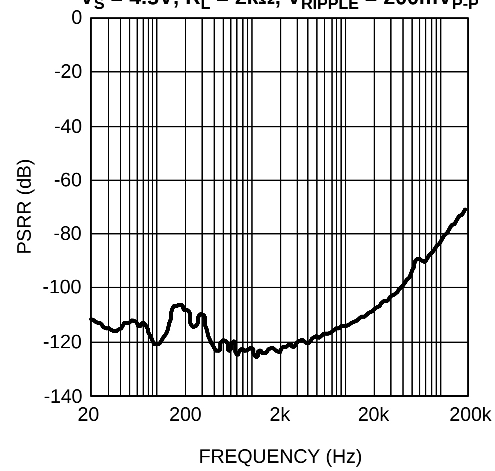


Figure 29.

+PSRR vs Frequency
V_S = 4.5V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{P-P}

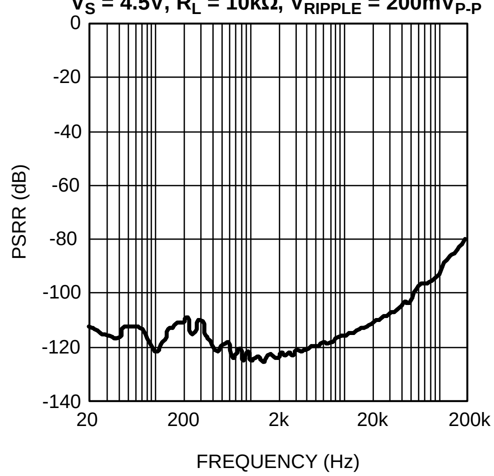


Figure 30.

+PSRR vs Frequency
V_S = 4.5V, R_L = 600Ω, V_{RIPPLE} = 200mV_{P-P}

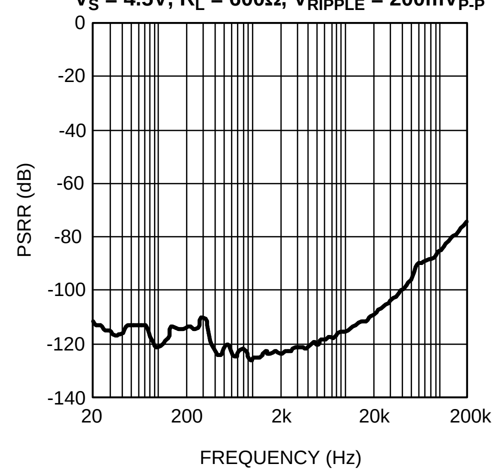


Figure 31.

Typical Performance Characteristics (continued)

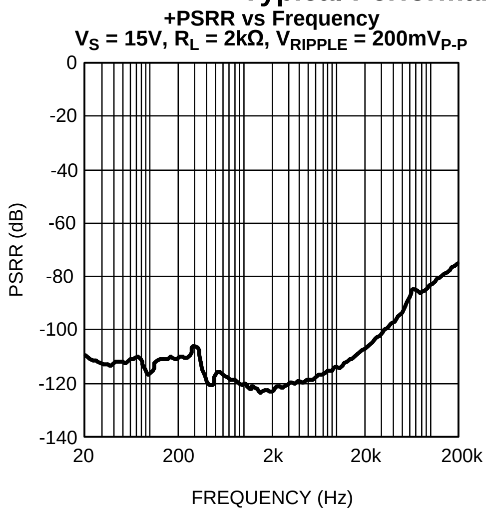


Figure 32.

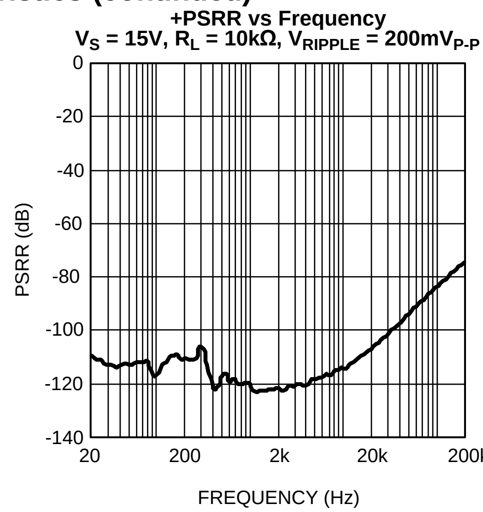
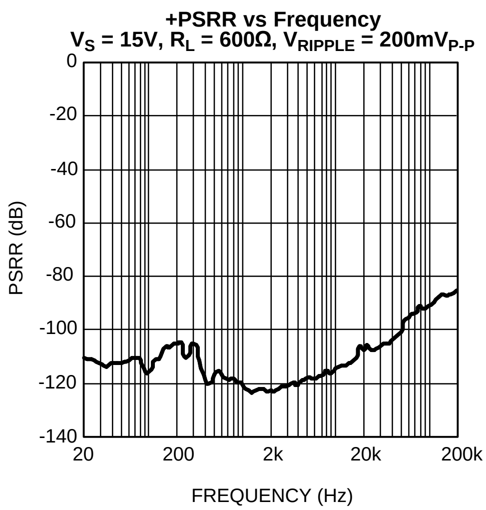


Figure 33.



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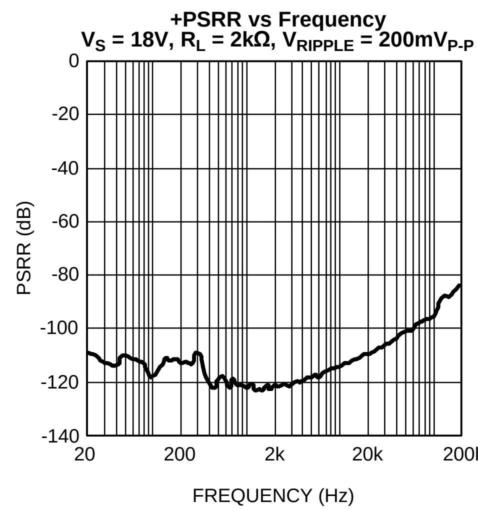


Figure 35.

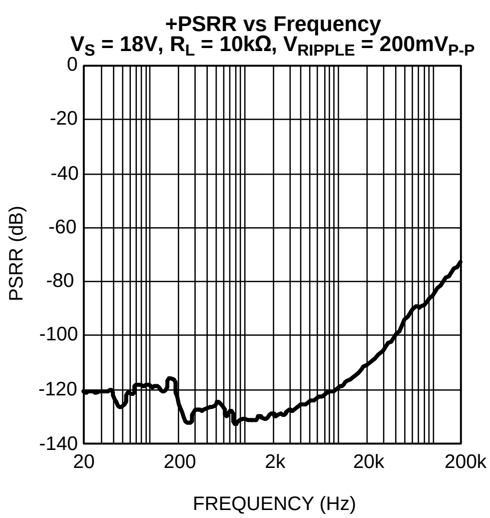


Figure 36.

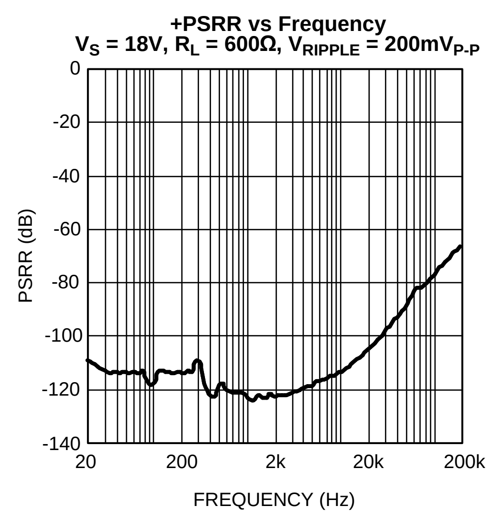


Figure 37.

Typical Performance Characteristics (continued)

-PSRR vs Frequency
V_S = 4.5V, R_L = 2kΩ, V_{RIPPLE} = 200mV_{P-P}

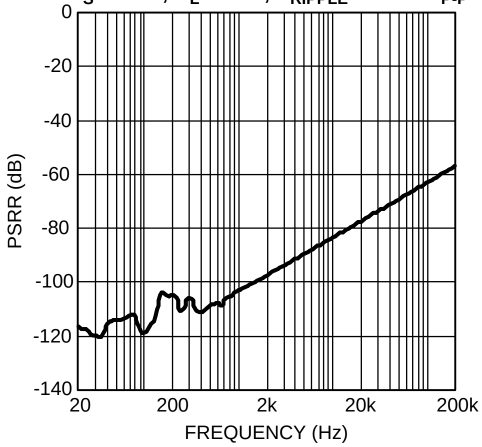


Figure 38.

-PSRR vs Frequency
V_S = 4.5V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{P-P}

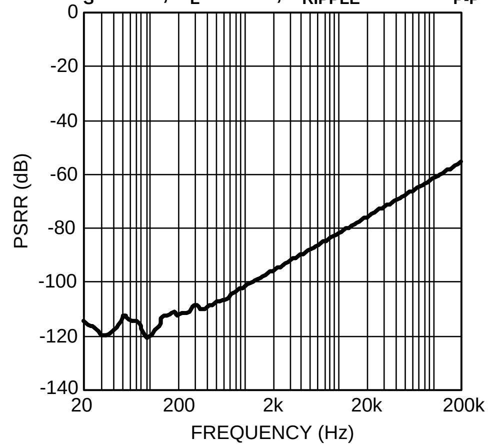


Figure 39.

-PSRR vs Frequency
V_S = 4.5V, R_L = 600Ω, V_{RIPPLE} = 200mV_{P-P}

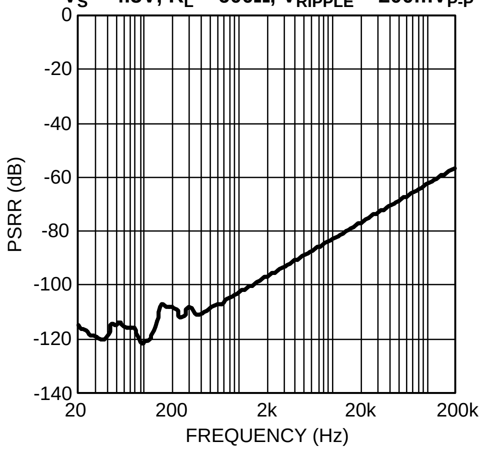


Figure 40.

-PSRR vs Frequency
V_S = 15V, R_L = 2kΩ, V_{RIPPLE} = 200mV_{P-P}

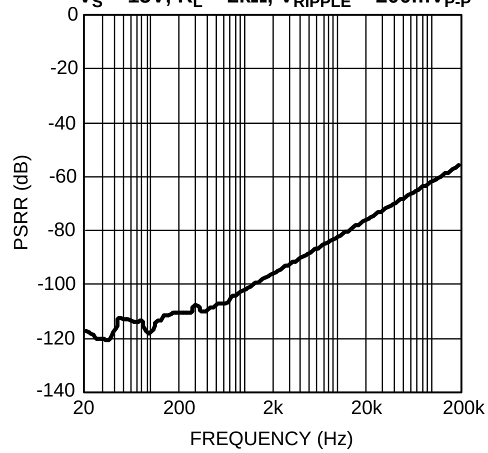


Figure 41.

-PSRR vs Frequency
V_S = 15V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{P-P}

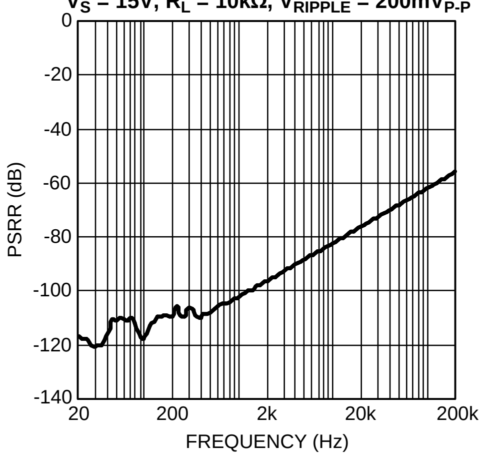


Figure 42.

-PSRR vs Frequency
V_S = 15V, R_L = 600Ω, V_{RIPPLE} = 200mV_{P-P}

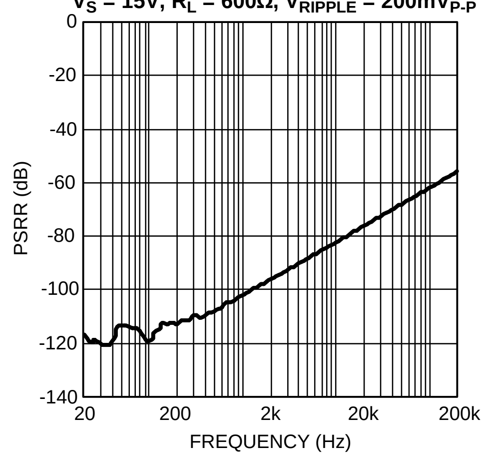


Figure 43.

Typical Performance Characteristics (continued)

-PSRR vs Frequency
V_S = 18V, R_L = 2kΩ, V_{RIPPLE} = 200mV_{P-P}

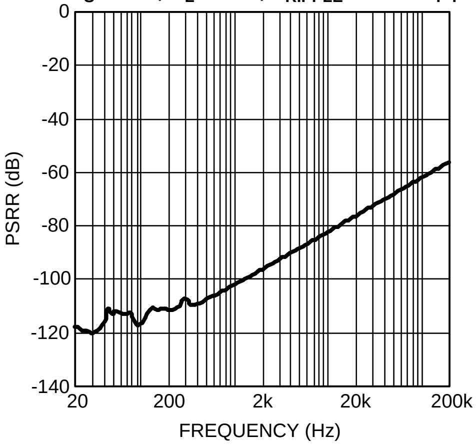


Figure 44.

-PSRR vs Frequency
V_S = 18V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{P-P}

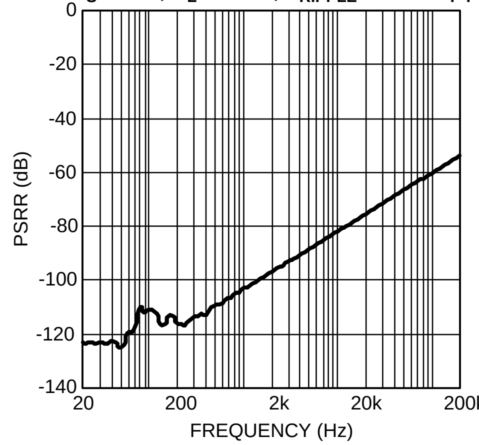


Figure 45.

-PSRR vs Frequency
V_S = 18V, R_L = 600Ω, V_{RIPPLE} = 200mV_{P-P}

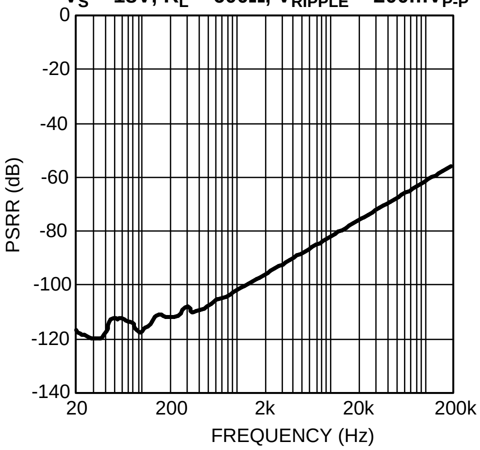


Figure 46.

Crosstalk vs Frequency
V_S = 4.5V, V_{OUT} = 1.2V_{RMS}, R_L = 600Ω

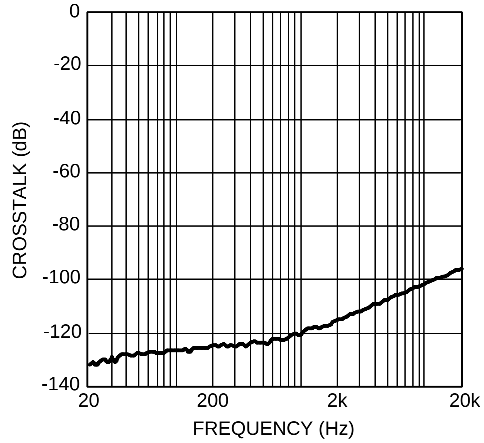


Figure 47.

Crosstalk vs Frequency
V_S = 15V, V_{OUT} = 3V_{RMS}, R_L = 600Ω

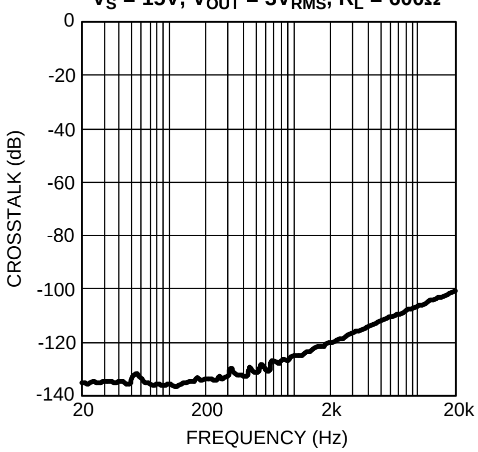


Figure 48.

Crosstalk vs Frequency
V_S = 18V, V_{OUT} = 3V_{RMS}, R_L = 600Ω

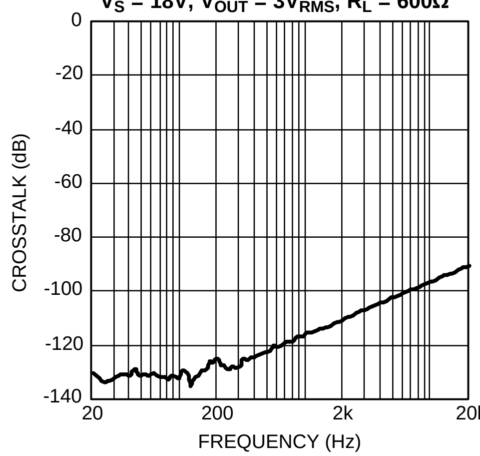


Figure 49.

Typical Performance Characteristics (continued)

Crosstalk vs Frequency
V_S = 4.5V, V_{OUT} = 1.2V_{RMS}, R_L = 2kΩ

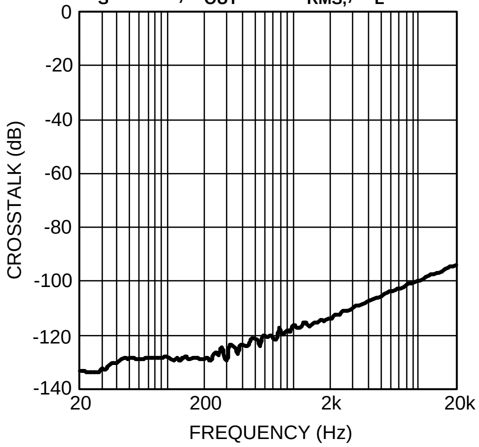


Figure 50.

Crosstalk vs Frequency
V_S = 15V, V_{OUT} = 3V_{RMS}, R_L = 2kΩ

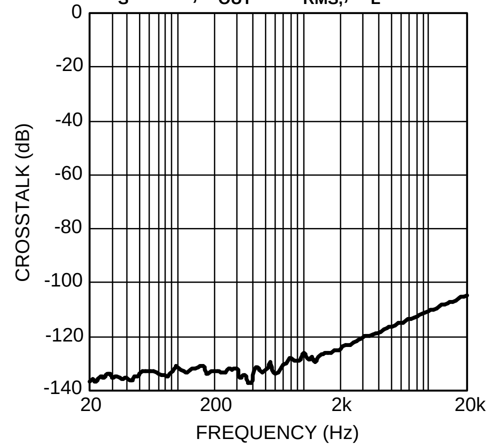


Figure 51.

Crosstalk vs Frequency
V_S = 18V, V_{OUT} = 3V_{RMS}, R_L = 2kΩ

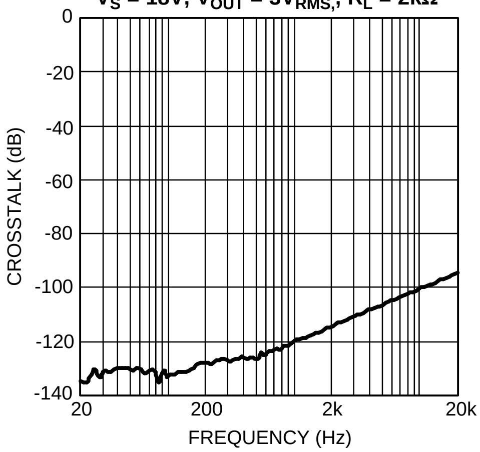


Figure 52.

Crosstalk vs Frequency
V_S = 4.5V, V_{OUT} = 1.2V_{RMS}, R_L = 10kΩ

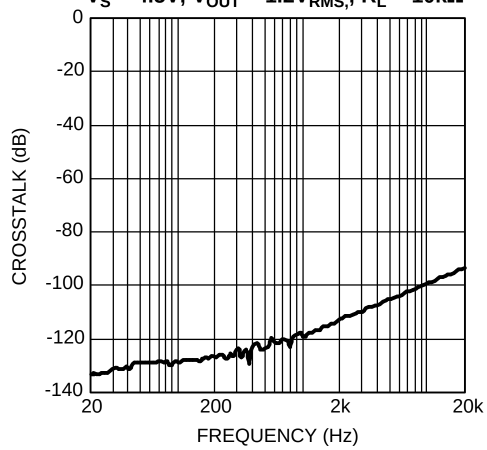


Figure 53.

Crosstalk vs Frequency
V_S = 4.5V, V_{OUT} = 1.2V_{RMS}, R_L = 600Ω

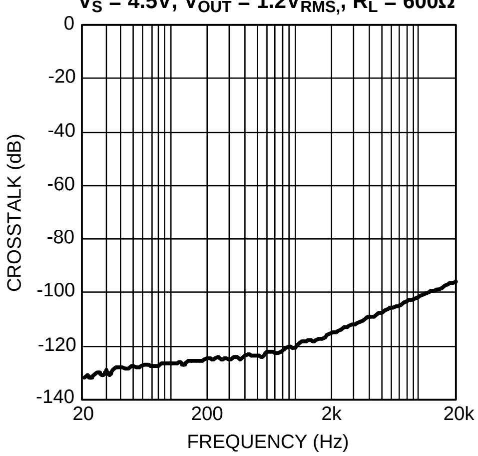


Figure 54.

Crosstalk vs Frequency
V_S = 15V, V_{OUT} = 3V_{RMS}, R_L = 10kΩ

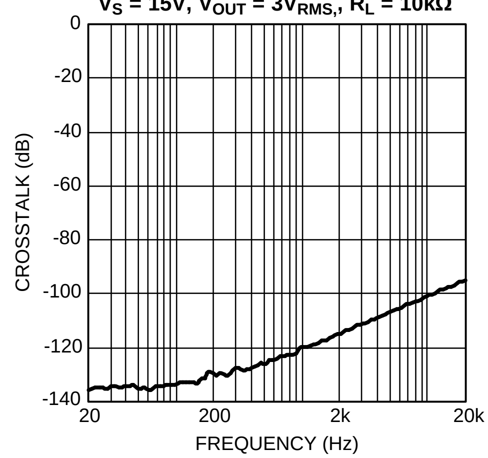


Figure 55.

Typical Performance Characteristics (continued)

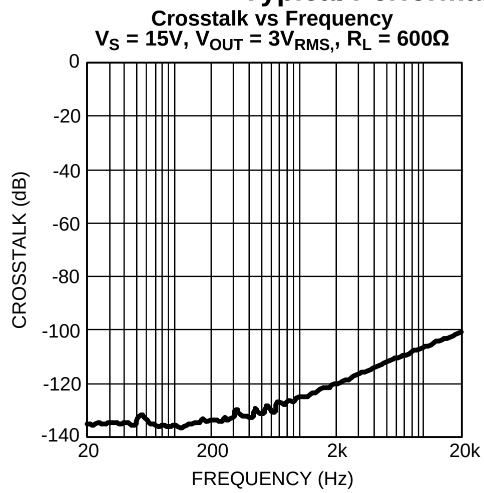


Figure 56.

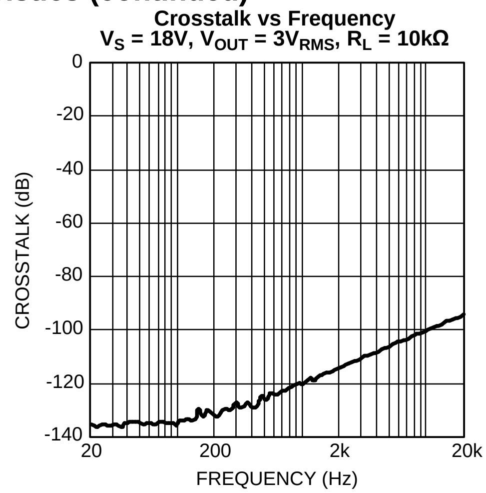


Figure 57.

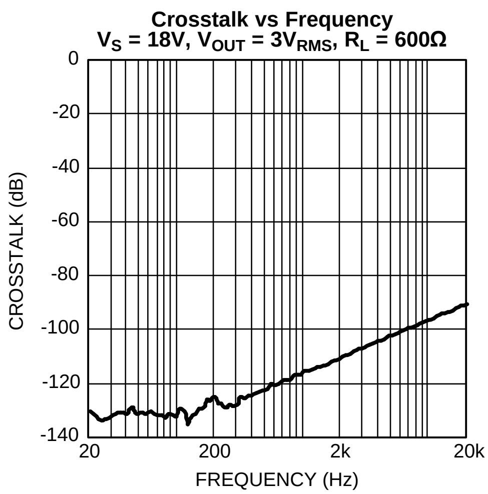


Figure 58.

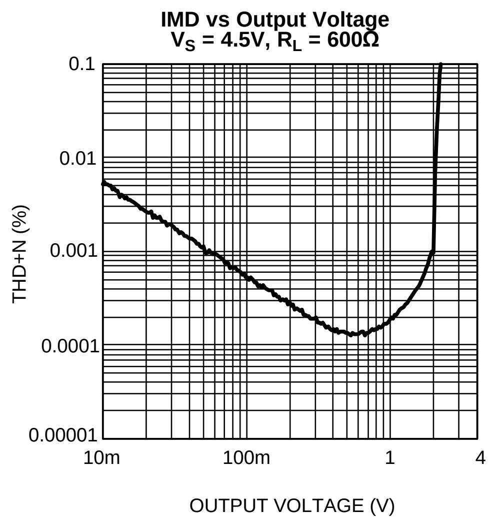


Figure 59.

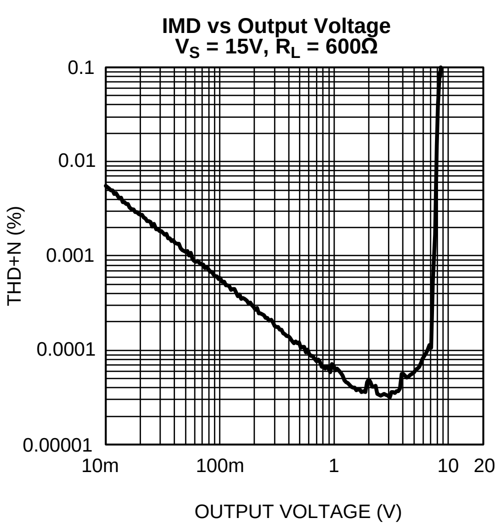


Figure 60.

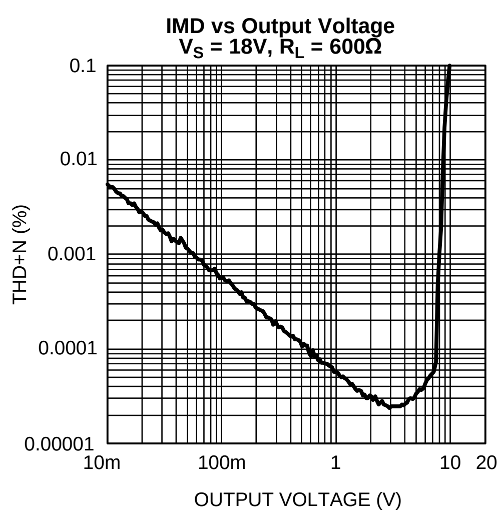


Figure 61.

Typical Performance Characteristics (continued)

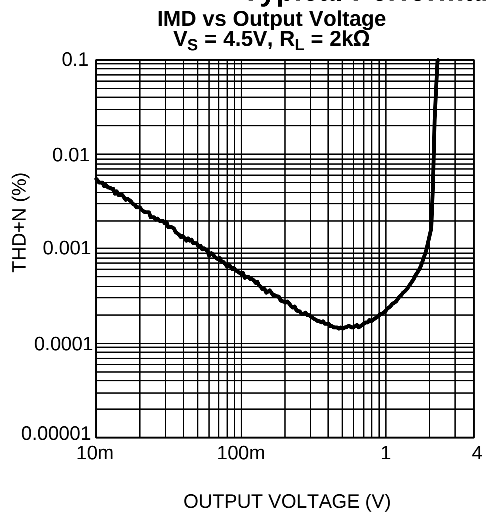


Figure 62.

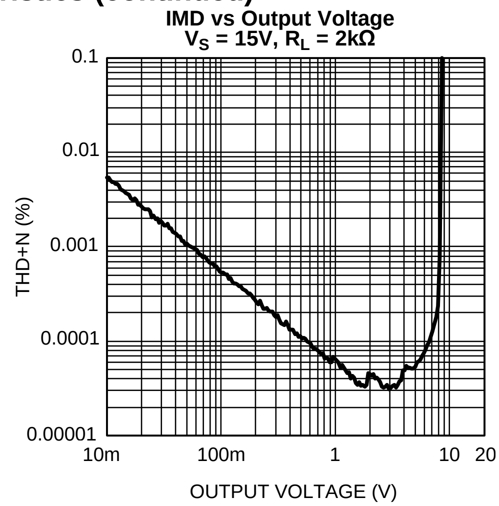


Figure 63.

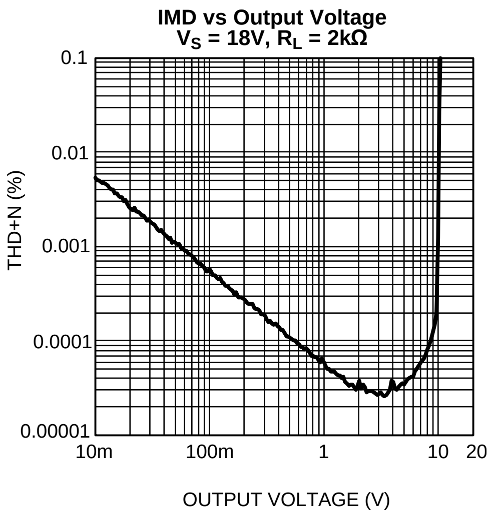


Figure 64.

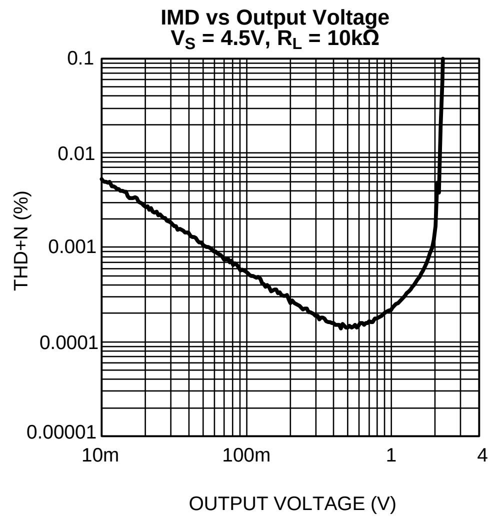


Figure 65.

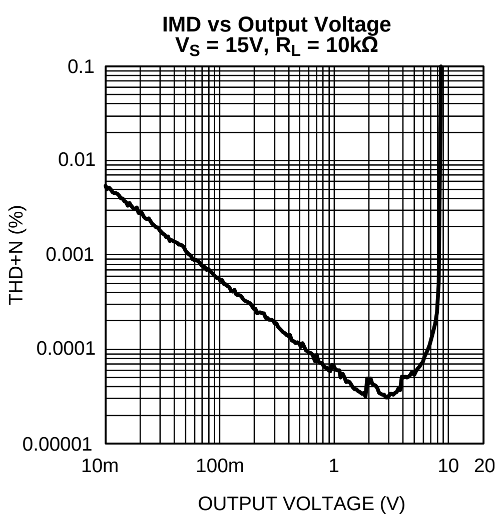


Figure 66.

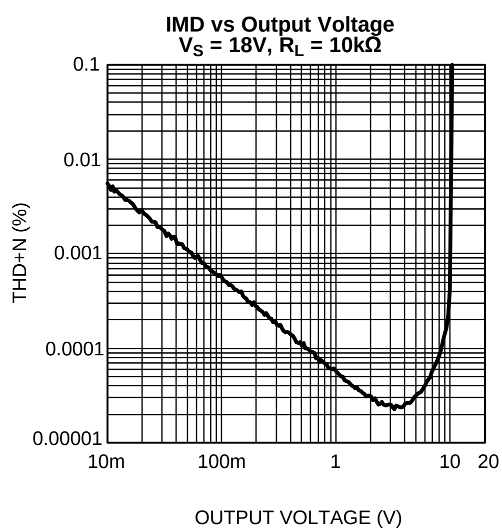


Figure 67.

Typical Performance Characteristics (continued)

Total Quiescent Current vs Power Supply

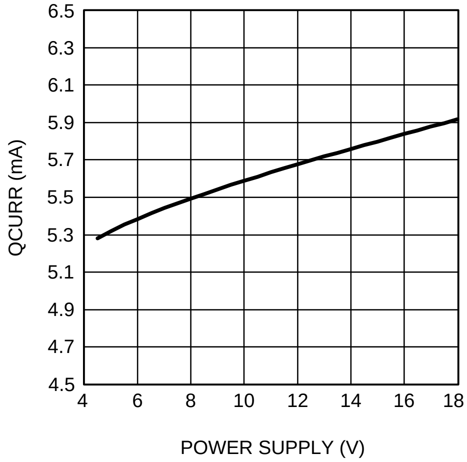


Figure 68.

Voltage Noise Density vs Frequency
V_{CC} = 15V, V_{EE} = –15V, No Load

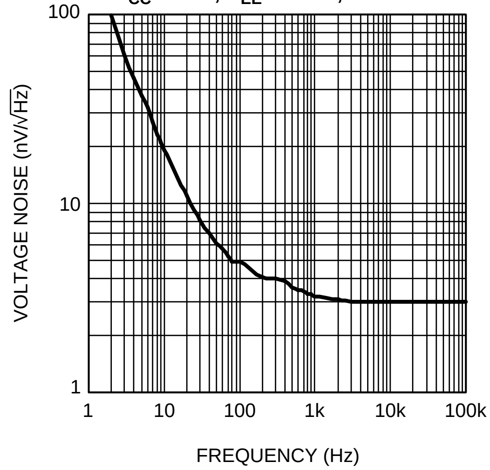


Figure 69.

Current Noise vs Frequency
V_{CC} = 15V, V_{EE} = –15V, No Load

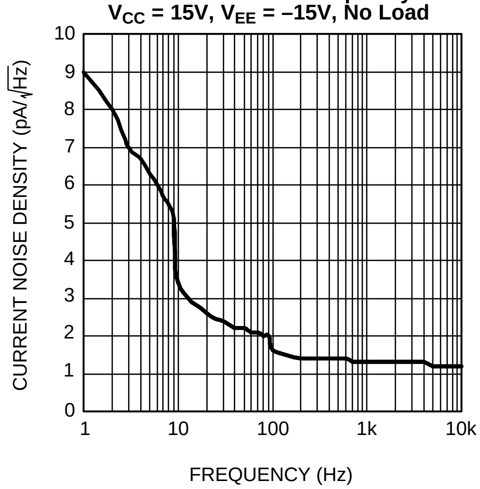


Figure 70.

APPLICATION INFORMATION

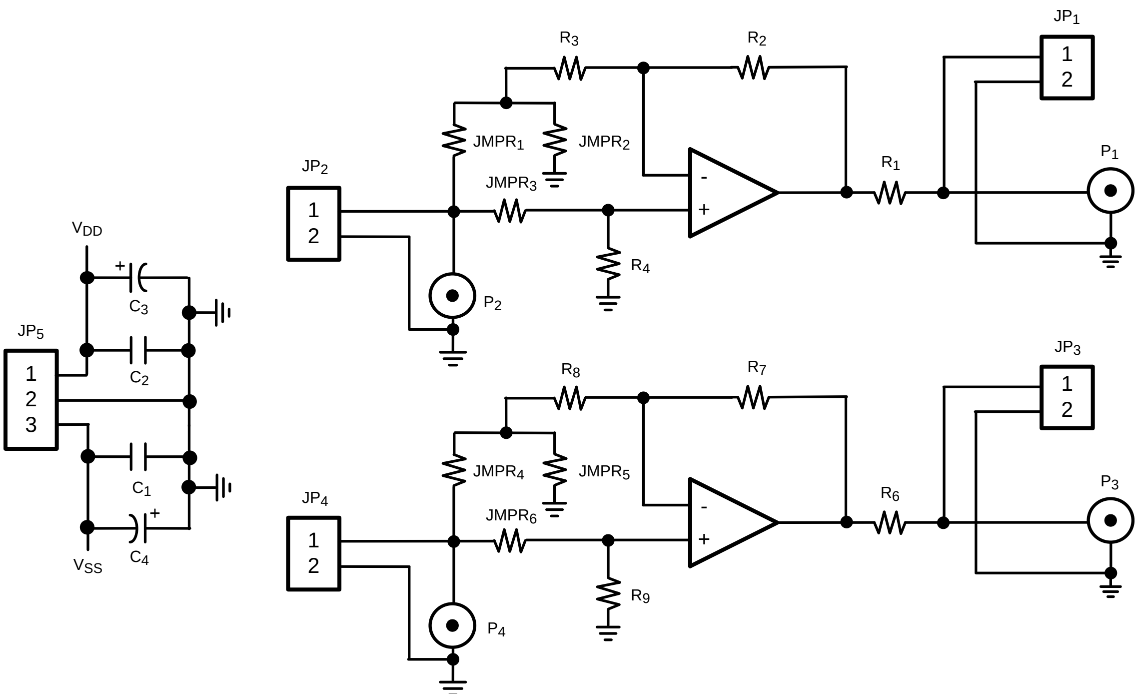
OPERATING RATINGS AND BASIC DESIGN GUIDELINES

The LME49725 has a supply voltage range from +9V to +36V single supply or ±4.5V to ±18V dual supply.

Bypass capacitors for the supplies should be placed as close to the amplifier as possible. This will help minimize any inductance between the power supply and the supply pins. In addition to a 10μF capacitor, a 0.1μF capacitor is also recommended.

The amplifier's inputs lead lengths should also be as short as possible. If the op amp does not have a bypass capacitor, it may oscillate.

Demonstration Board Schematic



Bill Of Materials For Demonstration Board (Inverting Configuration)

Description	Designator(1)	Part Number	Mfg
Ceramic Capacitor 0.1µF, 10% 50V 0805 SMD	C1, C2	C0805C104K3RAC7533	Kemet
Tantalum Capacitor 10µF, 10% 20V, B-size	C3, C4	T491B106K025AT	Kemet
Resistor 0Ω, 1/8W, 1% 0805 SMD	JMPR1, JMPR4, R1, R4, R6, R9	CRCW0805000020EA	Vishay
Resistor 10kΩ, 1/8W, 1% 0805 SMD	R2, R3, R8, R7	CRCW080510K0FKEA	Vishay
Header, 2-Pin	JP1, JP2, JP3, JP4		
Header, 3-Pin	JP5		
SMA stand-up connectors	P1-P4 (Optional)	132134	Amphenol COnnex

(1) Do not stuff JMPR2, JMPR3, JMPR5, and JMPR6.

Demonstration Board Layout

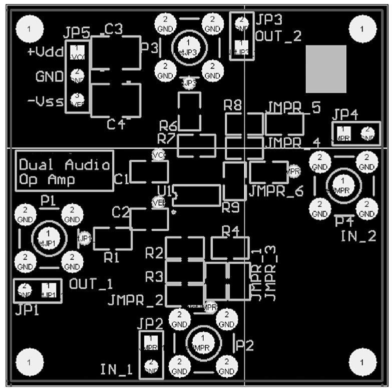


Figure 71. Silkscreen Layer

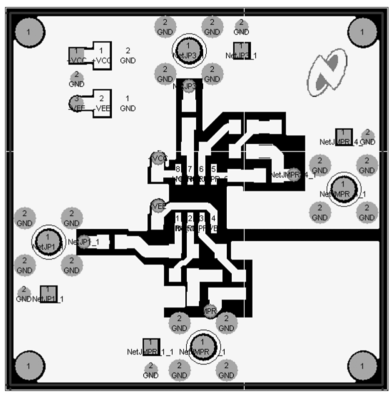


Figure 72. Top Layer

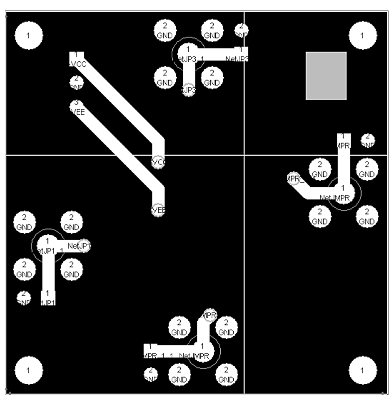


Figure 73. Bottom Layer

REVISION HISTORY

Rev	Date	Description
1.0	04/03/08	Initial release.
A	04/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49725MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	L49725 MA	Samples
LME49725MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49725 MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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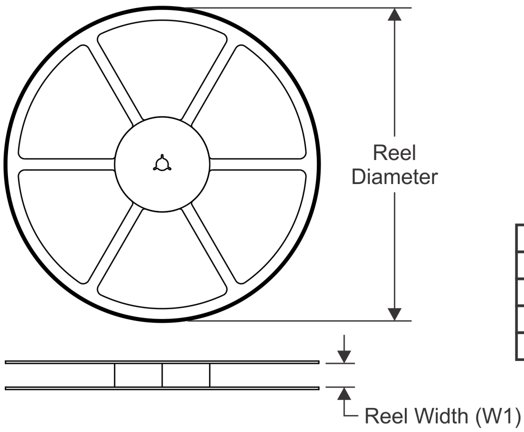
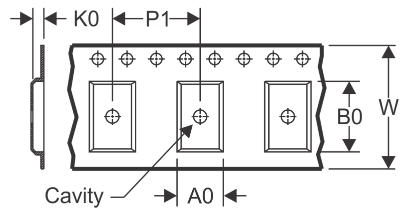
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

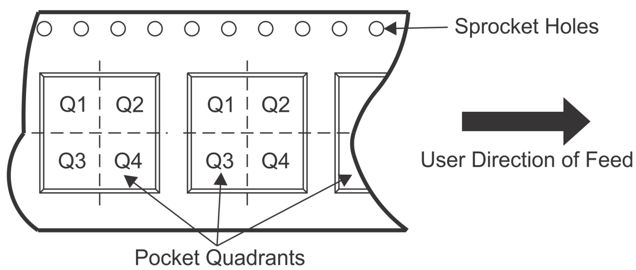


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

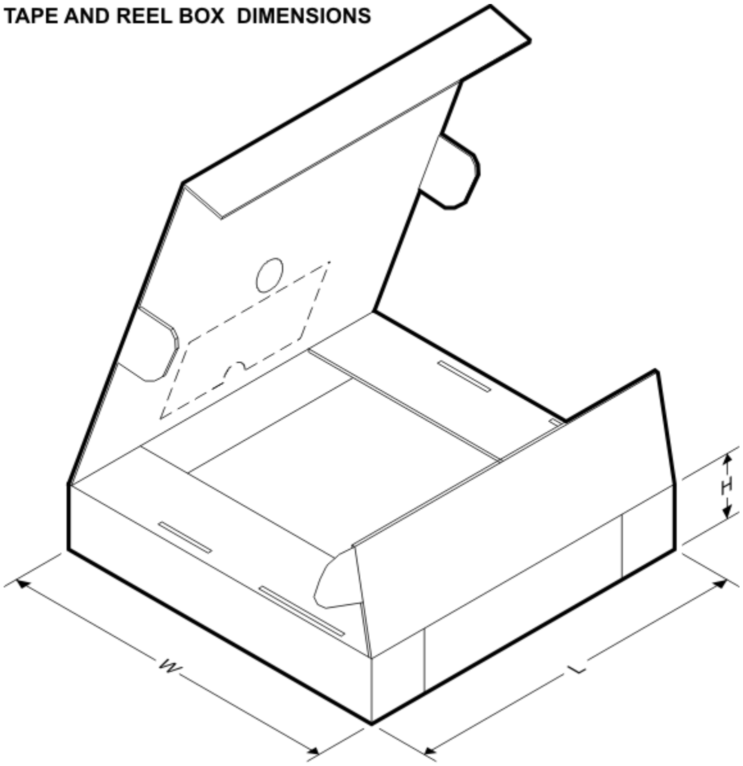
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49725MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

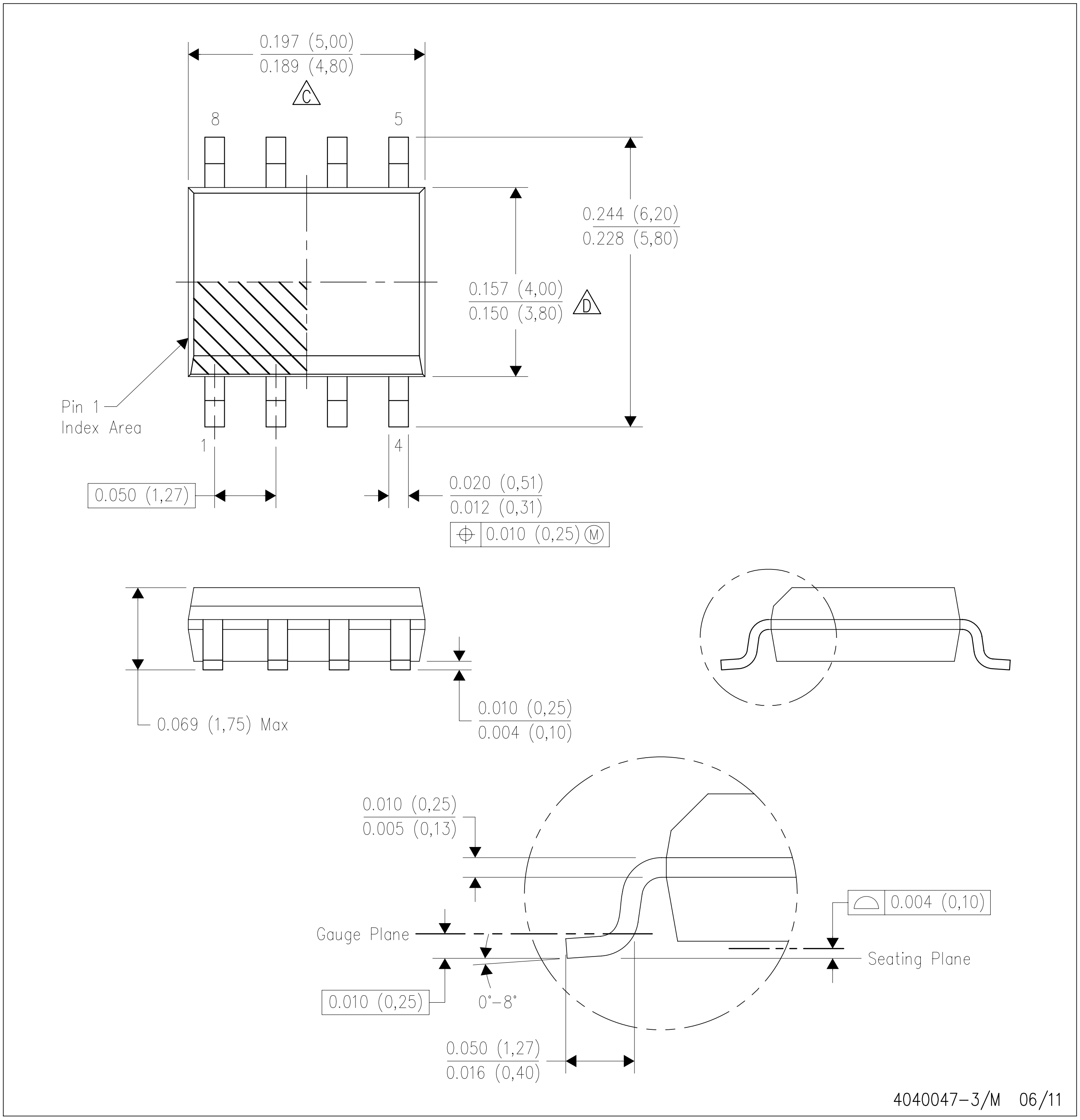
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49725MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.