LMH6622 Dual Wideband, Low Noise, 160MHz, Operational Amplifiers

Check for Samples: LMH6622

FEATURES

- **V_S = ±6V, T_A = 25°C, Typical Values Unless Specified**
- **Bandwidth (A_V = +2) 160MHz**
- **Supply Voltage Range ±2.5V to ±6V+5V to +12**
- **Slew Rate 85V/µs**
- **Supply Current 4.3mA/amp**
- **Input Common Mode Voltage −4.75V to +5.7V**
- **Output Voltage Swing (R_L = 100Ω) ±4.6V**
- **Input Voltage Nise 1.6nV/$\sqrt{Hz}$**
- **Input Current Noise 1.5pA/$\sqrt{Hz}$**
- **Linear Output Current 90mA**
- **Excellent Harmonic Distortion 90dBc**

APPLICATIONS

- **xDSL Receiver**
- **Low Noise Instrumentation Front End**
- **Ultrasound Preamp**
- **Active Filters**
- **Cellphone Basestation**

DESCRIPTION

The LMH6622 is a dual high speed voltage feedback operational amplifier specifically optimized for low noise. A voltage noise specification of 1.6nV/$\sqrt{Hz}$, a current noise specification 1.5pA/$\sqrt{Hz}$, a bandwidth of 160MHz, and a harmonic distortion specification that exceeds 90dBc combine to make the LMH6622 an ideal choice for the receive channel amplifier in ADSL, VDSL, or other xDSL designs. The LMH6622 operates from ±2.5V to ±6V in dual supply mode and from +5V to +12V in single supply configuration. The LMH6622 is stable for A_V ≥ 2 or A_V ≤ −1. The fabrication of the LMH6622 on TI's advanced VIP10 process enables excellent (160MHz) bandwidth at a current consumption of only 4.3mA/amplifier. Packages for this dual amplifier are the 8-lead SOIC and the 8-lead VSSOP.

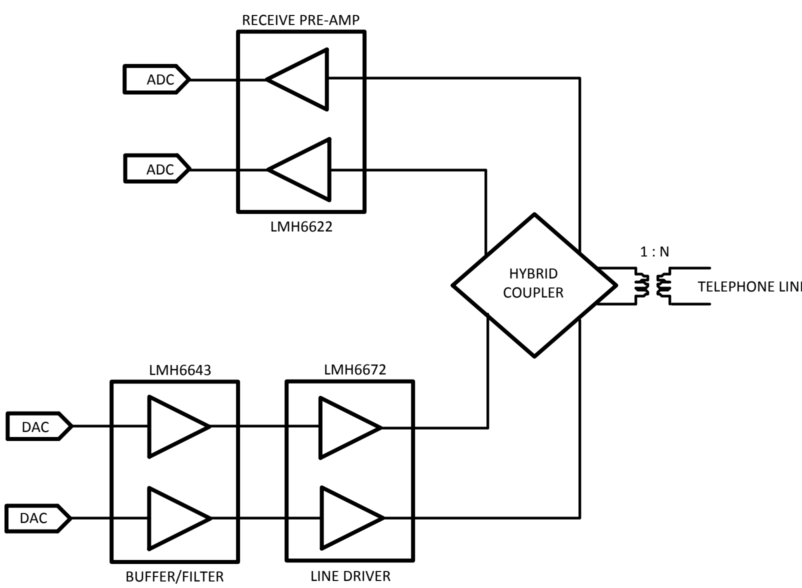


Figure 1. xDSL Analog Front End

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance	
Human Body Model	2kV (3)
Machine Model	200V (3)
V_{IN} Differential	±1.2V
Supply Voltage ($V^+ – V^−$)	13.2V
Voltage at Input Pins	V^+ +0.5V, $V^−$ −0.5V
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (4)	+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 200pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Supply Voltage ($V^+– V^−$)	±2.25V to ±6V
Junction Temperature Range (2), (3)	−40°C to +85°C
Package Thermal Resistance (3) ($θ_{JA}$)	
8-pin SOIC	166°C/W
8-pin VSSOP	211°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

±6V Electrical Characteristics

Unless otherwise specified, T_J = 25°C, V^+ = 6V, $V^−$ = −6V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Dynamic Performance						
f_{CL}	−3dB BW	V_O = 200mV_{PP}		160		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	V_O = 200mV_{PP}		30		MHz
SR	Slew Rate (3)	V_O = 2V_{PP}		85		V/μs
TS	Settling Time	V_O = 2V_{PP} to ±0.1%		40		ns
		V_O = 2V_{PP} to ±1.0%		35		
Tr	Rise Time	V_O = 0.2V Step, 10% to 90%		2.3		ns
Tf	Fall Time	V_O = 0.2V Step, 10% to 90%		2.3		ns

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the slowest of the rising and falling slew rates.

±6V Electrical Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 100kHz		1.6		nV/√Hz
i_n	Input Referred Current Noise	f = 100kHz		1.5		pA/√Hz
DG	Differential Gain	R_L = 150Ω, R_F = 470Ω, NTSC		0.03		%
DP	Differential Phase	R_L = 150Ω, R_F = 470Ω, NTSC		0.03		deg
HD2	2^{nd} Harmonic Distortion	f_c = 1MHz, V_O = $2V_{PP}$, R_L = 100Ω		−90		dBc
		f_c = 1MHz, V_O = $2V_{PP}$, R_L = 500Ω		−100		
HD3	3^{rd} Harmonic Distortion	f_c = 1MHz, V_O = $2V_{PP}$, R_L = 100Ω		−94		dBc
		f_c = 1MHz, V_O = $2V_{PP}$, R_L = 500Ω		−100		
MTPR	Upstream	V_O = 0.6 V_{RMS}, 26kHz to 132kHz (see Figure 35)		−78		dBc
	Downstream	V_O = 0.6 V_{RMS}, 144kHz to 1.1MHz (see Figure 35)		−70		
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−1.2 **−2**	+0.2	+1.2 **+2**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0V (4)		−2.5		μV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	−1 **−1.5**	−0.04	1 **1.5**	μA
I_B	Input Bias Current	V_{CM} = 0V		4.7	10 **15**	μA
R_{IN}	Input Resistance	Common Mode		17		MΩ
		Differential Mode		12		kΩ
C_{IN}	Input Capacitance	Common Mode		0.9		pF
		Differential Mode		1.0		pF
CMVR	Input Common Mode Voltage Range	CMRR ≥ 60dB		−4.75	−4.5	V
			5.5	+5.7		
CMRR	Common-Mode Rejection Ratio	Input Referred, V_{CM} = −4.2 to +5.2V	80 **75**	100		dB
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	V_O = $4V_{PP}$	74 **70**	83		dB
X_t	Crosstalk	f = 1MHz		−75		dB
Output Characteristics						
V_O	Output Swing	No Load, Positive Swing	4.8 **4.6**	5.2		V
		No Load, Negative Swing		−5.0	−4.6 **−4.4**	
		R_L = 100Ω, Positive Swing	4.0 **3.8**	4.6		
		R_L = 100Ω, Negative Swing		−4.6	−4 **−3.8**	
R_O	Output Impedance	f = 1MHz		0.08		Ω

(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±6V Electrical Characteristics (continued)

Unless otherwise specified, T_J = 25°C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing to Ground ΔV_{IN} = 200mV (5), (6)	100	135		mA
		Sinking to Ground ΔV_{IN} = −200mV (5), (6)	100	130		
I_{OUT}	Output Current	Sourcing, V_O = +4.3V Sinking, V_O = −4.3V		90		mA
Power Supply						
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, V_S = +5V to +6V	80 **74**	95		dB
−PSRR	Negative Power Supply Rejection Ratio	Input Referred, V_S = −5V to −6V	75 **69**	90		
I_S	Supply Current (per amplifier)	No Load		4.3	6 **6.5**	mA

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ ±2.5V, at room temperature and below. For V_S > ±2.5V, allowable short circuit duration is 1.5ms.

±2.5V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.5V, V^- = −2.5V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Dynamic Performance						
f_{CL}	−3dB BW	V_O = 200mV$_{PP}$		150		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	V_O = 200mV$_{PP}$		20		MHz
SR	Slew Rate (3)	V_O = 2V$_{PP}$		80		V/μs
T_S	Settling Time	V_O = 2V$_{PP}$ to ±0.1%		45		ns
		V_O = 2V$_{PP}$ to ±1.0%		40		
T_r	Rise Time	V_O = 0.2V Step, 10% to 90%		2.5		ns
T_f	Fall Time	V_O = 0.2V Step, 10% to 90%		2.5		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 100kHz		1.7		nV/√Hz
i_n	Input Referred Current Noise	f = 100kHz		1.5		pA/√Hz
HD2	2nd Harmonic Distortion	fc = 1MHz, V_O = 2V$_{PP}$, R_L = 100Ω		−88		dBc
		fc = 1MHz, V_O = 2V$_{PP}$, R_L = 500Ω		−98		
HD3	3rd Harmonic Distortion	fc = 1MHz, V_O = 2V$_{PP}$, R_L = 100Ω		−92		dBc
		fc = 1MHz, V_O = 2V$_{PP}$, R_L = 500Ω		−100		
MTPR	Upstream	V_O = 0.4V$_{RMS}$,26kHz to 132kHz (see Figure 35)		−76		dBc
	Downstream	V_O = 0.4V$_{RMS}$,144kHz to 1.1MHz (see Figure 35)		−68		
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−1.5 **−2.3**	+0.3	+1.5 **+2.3**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0V (4)		−2.5		μV/°C

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the slowest of the rising and falling slew rates.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.5V, V^- = −2.5V, V_{CM} = 0V, A_V = +2, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{OS}	Input Offset Current	V_{CM} = 0V	−1.5 **−2.5**	+0.01	1.5 **2.5**	μA
I_B	Input Bias Current	V_{CM} = 0V		4.6	10 **15**	μA
R_{IN}	Input Resistance	Common Mode		17		MΩ
		Differential Mode		12		kΩ
C_{IN}	Input Capacitance	Common Mode		0.9		pF
		Differential Mode		1.0		pF
CMVR	Input Common Mode Voltage Range	CMRR ≥ 60dB		−1.25	−1	V
			2	+2.2		
CMRR	Common Mode Rejection Ratio	Input Referred, V_{CM} = −0.7 to +1.7V	80 **75**	100		dB
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	V_O = $1V_{PP}$	74	82		dB
X_t	Crosstalk	f = 1MHz		−75		dB
Output Characteristics						
V_O	Output Swing	No Load, Positive Swing	1.4 **1.2**	1.7		V
		No Load, Negative Swing		−1.5	−1.2 **−1**	
		R_L = 100Ω, Positive Swing	1.2 **1**	1.5		
		R_L = 100Ω, Negative Swing		−1.4	−1.1 **−0.9**	
R_O	Output Impedance	f = 1MHz		0.1		Ω
I_{SC}	Output Short Circuit Current	Sourcing to Ground ΔV_{IN} = 200mV (5), (6)	100	137		mA
		Sinking to Ground ΔV_{IN} = −200mV (5), (6)	100	134		
I_{OUT}	Output Current	Sourcing, V_O = +0.8V Sinking, V_O = −0.8V		90		mA
Power Supply						
+PSRR	Positive Power Supply Rejection Ratio	Input Referred, V_S = +2.5V to +3V	78 **72**	93		dB
−PSRR	Negative Power Supply Rejection Ratio	Input Referred, V_S = −2.5V to −3V	75 **70**	88		dB
I_S	Supply Current (per amplifier)	No Load		4.1	5.8 **6.4**	mA

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ ±2.5V, at room temperature and below. For V_S > ±2.5V, allowable short circuit duration is 1.5ms.

Typical Performance Characteristics

Current and Voltage Noise vs. Frequency

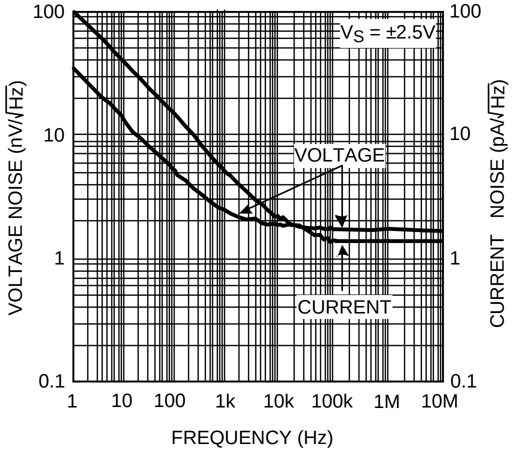


Figure 2.

Current and Voltage Noise vs. Frequency

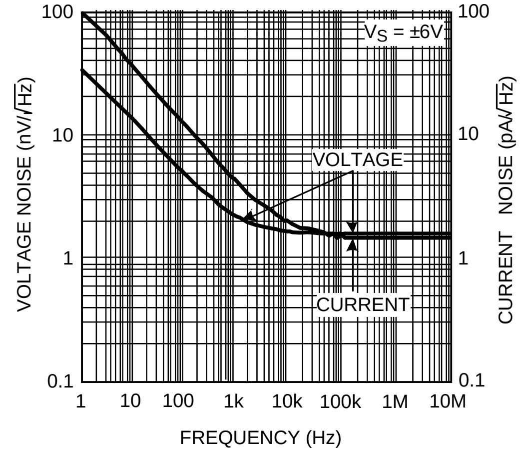


Figure 3.

Frequency Response vs. Input Signal Level

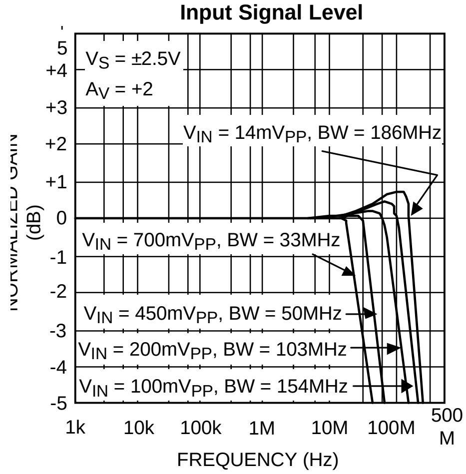


Figure 4.

Frequency Response vs. Input Signal Level

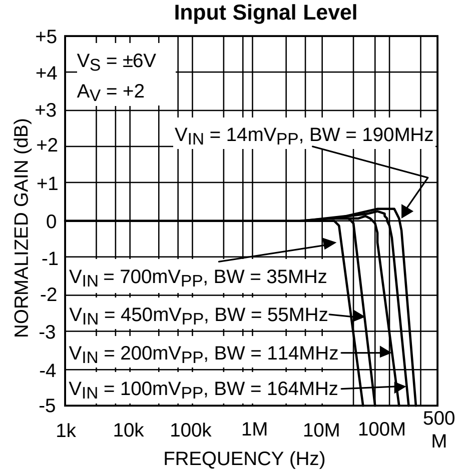


Figure 5.

Inverting Amplifier Frequency Response

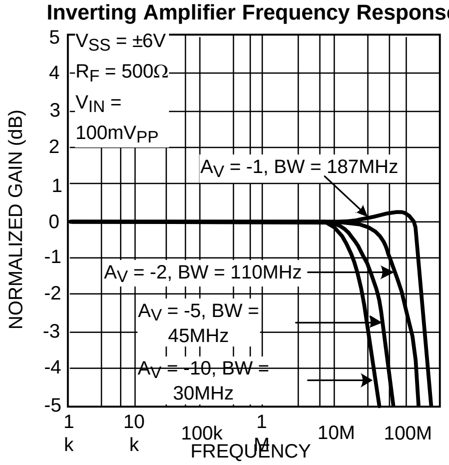


Figure 6.

Non-Inverting Amplifier Frequency Response

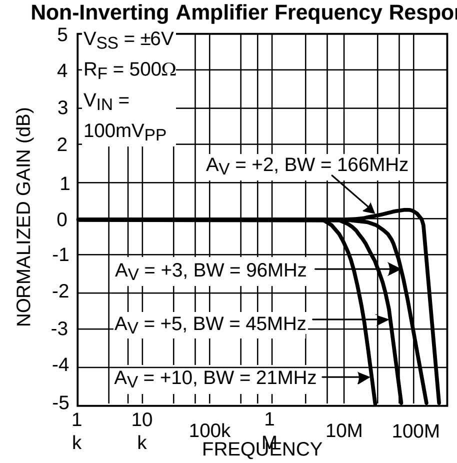


Figure 7.

Typical Performance Characteristics (continued)

Open Loop Gain and Phase Response

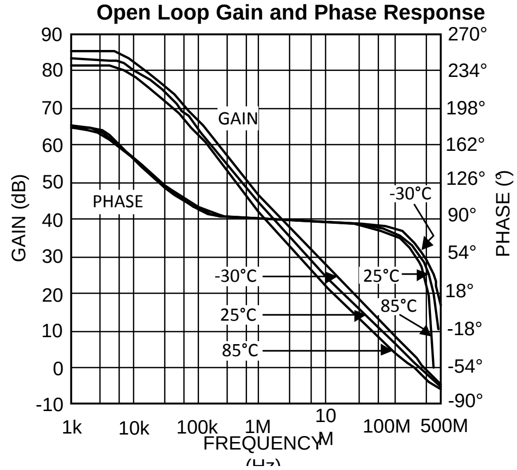


Figure 8.

Crosstalk vs. Frequency

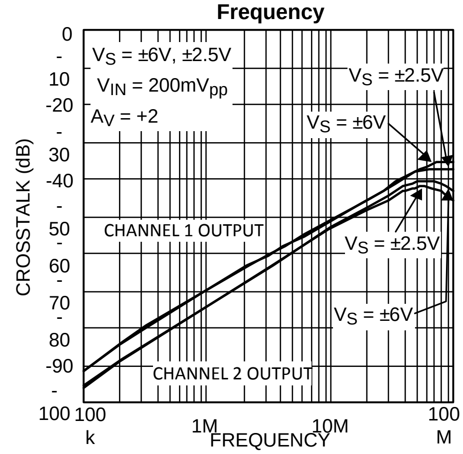


Figure 9.

PSRR vs. Frequency

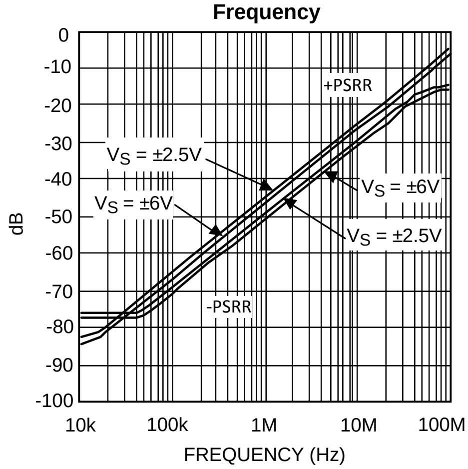


Figure 10.

CMRR vs. Frequency

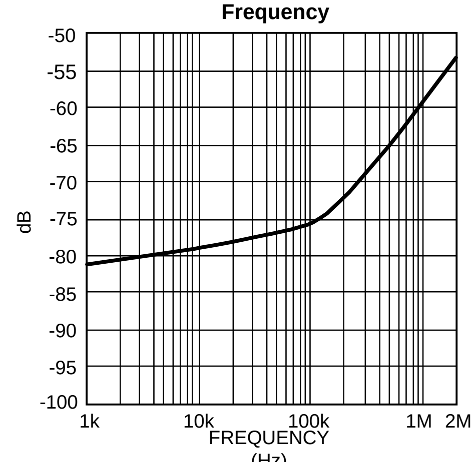


Figure 11.

Positive Output Swing vs. Source Current

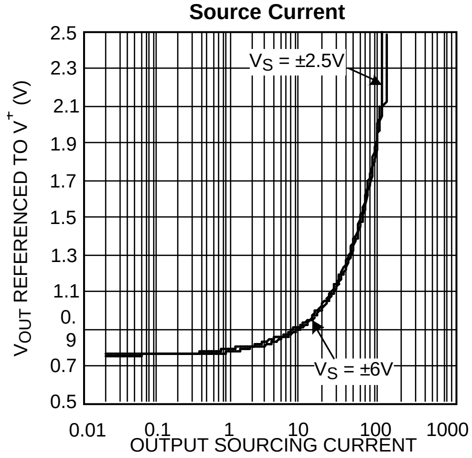


Figure 12.

Negative Output Swing vs. Sink Current

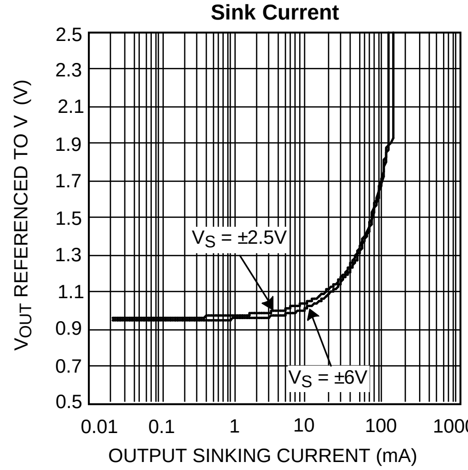


Figure 13.

Typical Performance Characteristics (continued)

Non-Inverting Small Signal Pulse Response $V_S = \pm2.5V$, $R_L = 100\Omega$, $A_V = +2$, $R_F = 500\Omega$

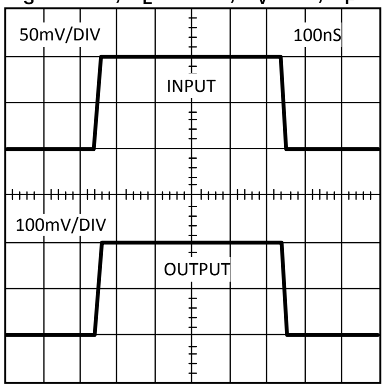


Figure 14.

Non-Inverting Small Signal Pulse Response $V_S = \pm6V$, $R_L = 100\Omega$, $A_V = +2$, $R_F = 500\Omega$

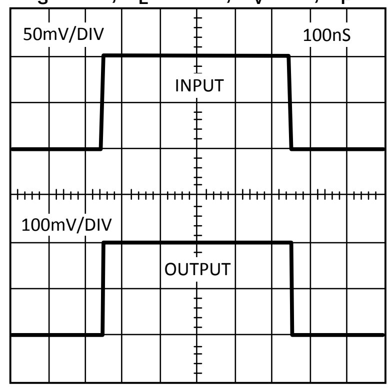


Figure 15.

Non-Inverting Large Signal Pulse Response $V_S = \pm2.5V$, $R_L = 100\Omega$, $A_V = +2$, $R_F = 500\Omega$

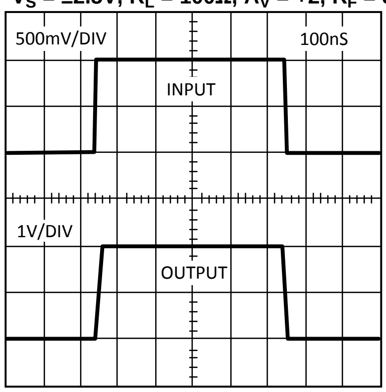


Figure 16.

Non-Inverting Large Signal Pulse Response $V_S = \pm6V$, $R_L = 100\Omega$, $A_V = +2$, $R_F = 500\Omega$

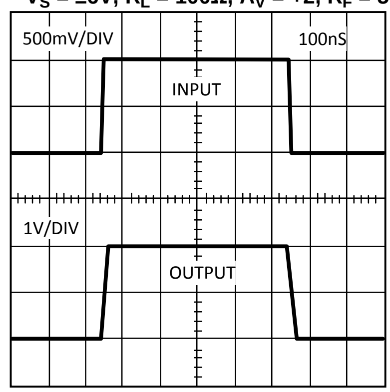


Figure 17.

Harmonic Distortion vs. Input Signal Level

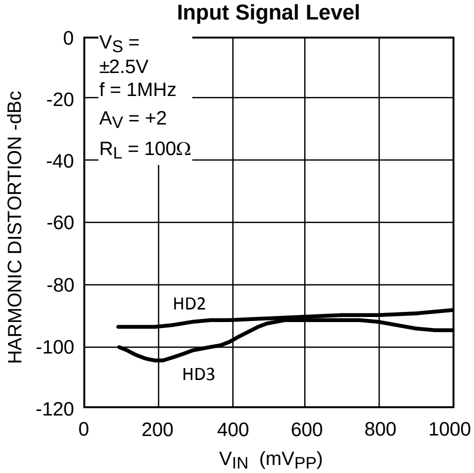


Figure 18.

Harmonic Distortion vs. Input Signal Level

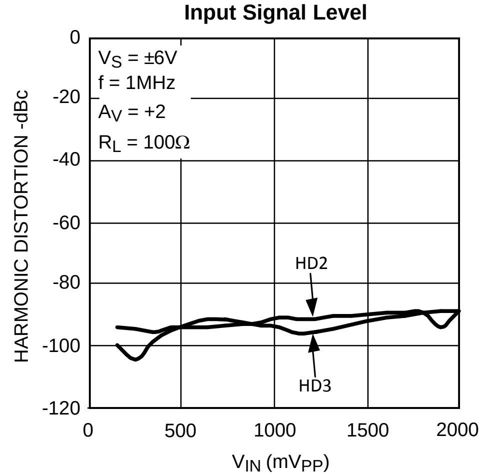


Figure 19.

Typical Performance Characteristics (continued)

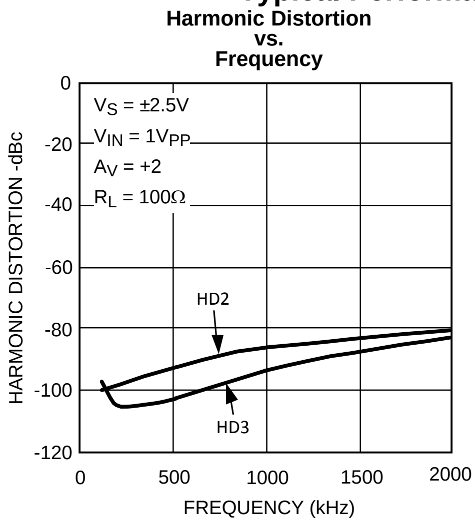


Figure 20.

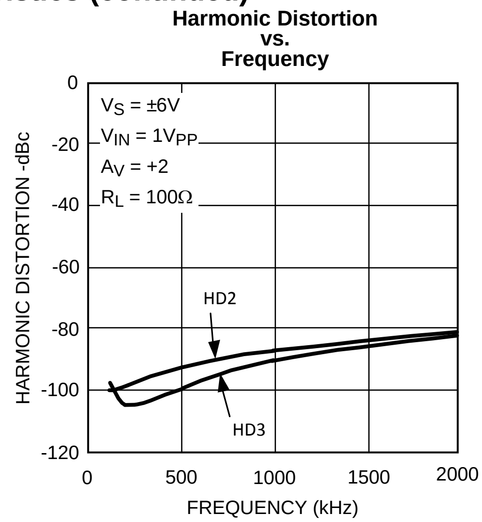


Figure 21.

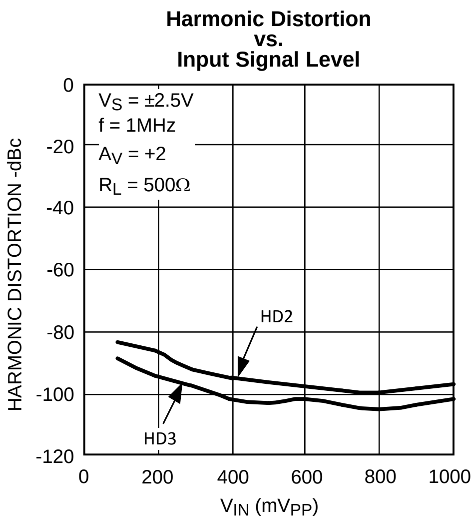


Figure 22.

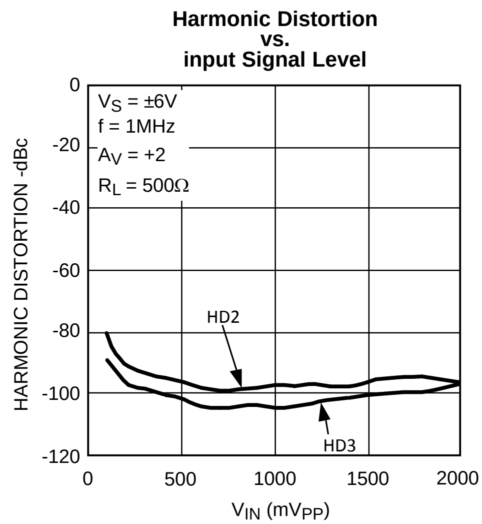


Figure 23.

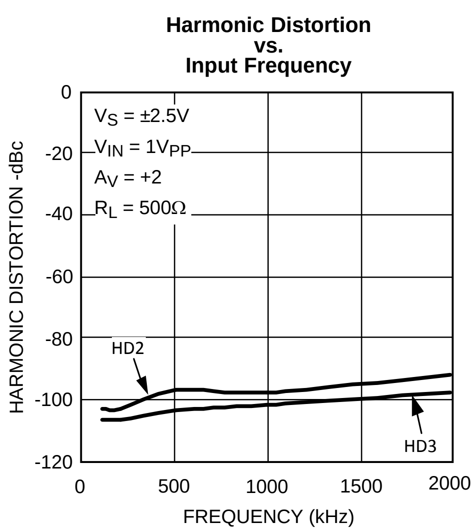


Figure 24.

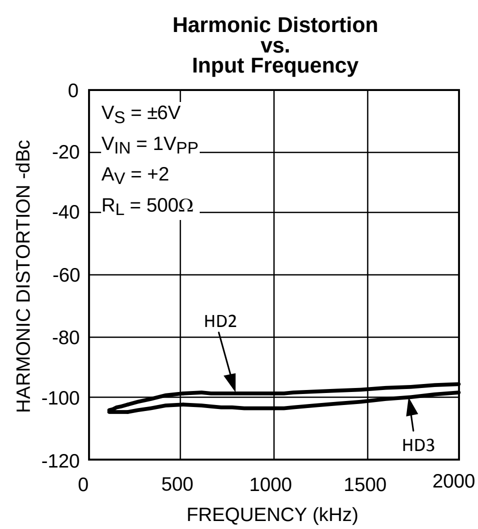


Figure 25.

Typical Performance Characteristics (continued)

Full Rate ADSL (DMT) Upstream MTPR @ V_S = ±2.5V

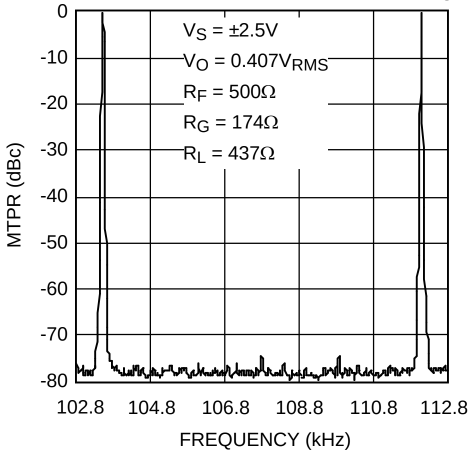


Figure 26.

Full Rate ADSL (DMT) Downstream MTPR @ V_S = ±2.5V

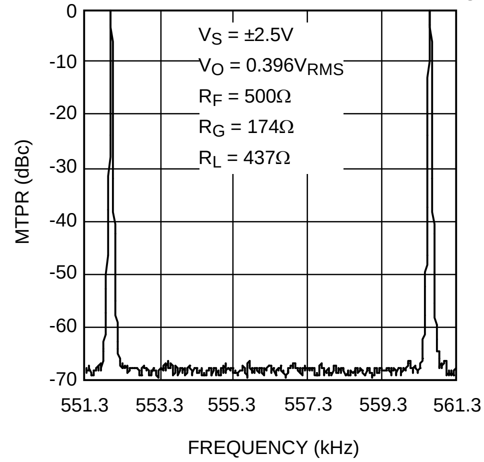


Figure 27.

Full Rate ADSL (DMT) Upstream MTPR @ V_S = ±6V

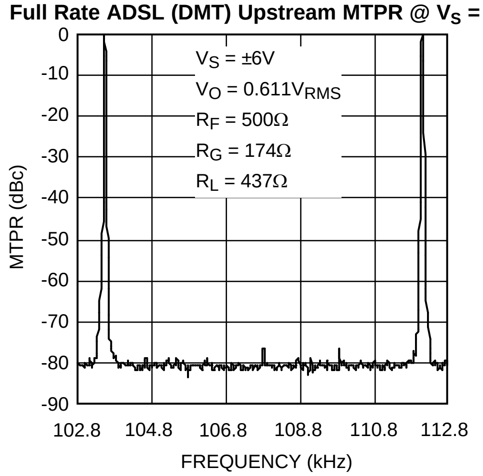


Figure 28.

Full Rate ADSL (DMT) Downstream MTPR @ V_S = ±6V

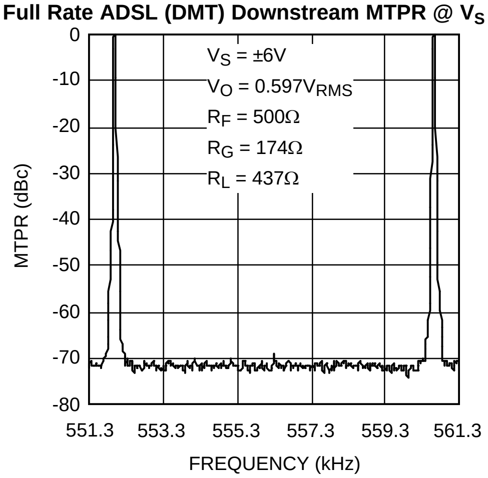


Figure 29.

Connection Diagram

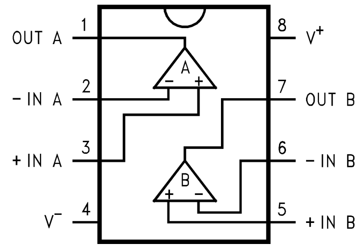


Figure 30. 8-Pin SOIC/VSSOP (Top View)

Test Circuits

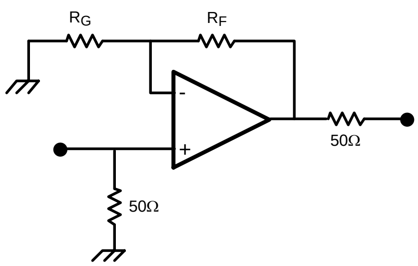


Figure 31. Non-Inverting Amplifier

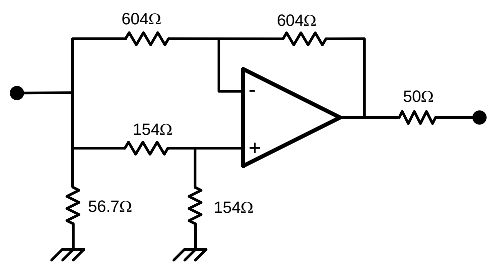


Figure 32. CMRR

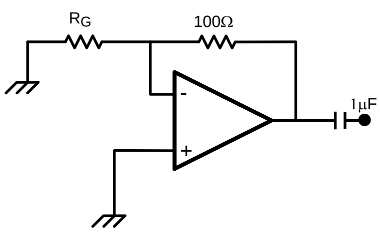


Figure 33. Voltage Noise
R_G = 1Ω for f ≤ 100kHz, R_G = 20Ω for f > 100kHz

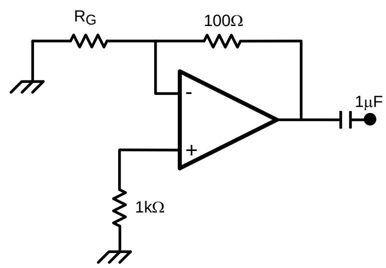


Figure 34. Current Noise
R_G = 1Ω for f ≤ 100kHz, R_G = 20Ω for f > 100kHz

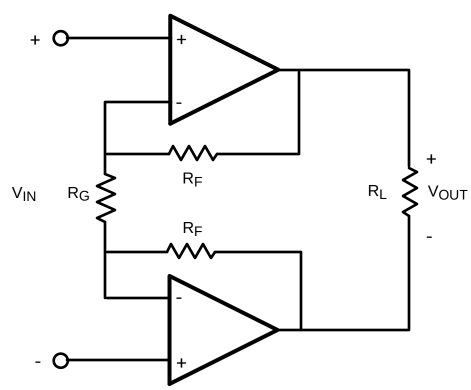


Figure 35. Multitone Power Ratio, R_F = 500Ω, R_G = 174Ω, R_L = 437Ω

DSL RECEIVE CHANNEL APPLICATIONS

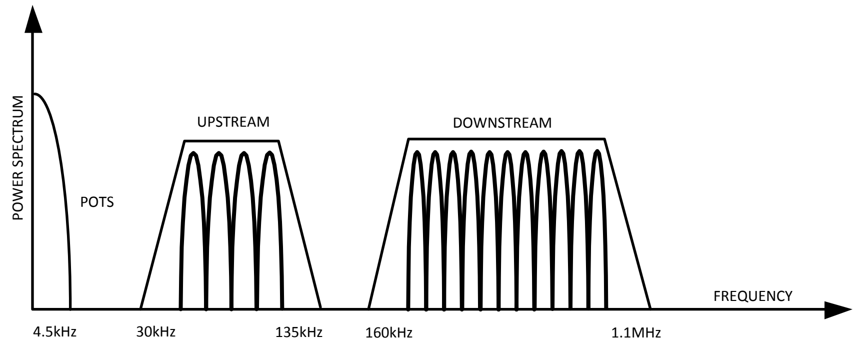


Figure 36. ADSL Signal Description

The LMH6622 is a dual, wideband operational amplifier designed for use as a DSL line receiver. In the receive band of a Customer Premises Equipment (CPE) ADSL modem it is possible that as many as 255 Discrete Multi-Tone (DMT) QAM signals will be present, each with its own carrier frequency, modulation, and signal level. The ADSL standard requires a line referred noise power density of -140dBm/Hz within the CPE receive band of 100KHz to 1.1MHz. The CPE driver output signal will leak into the receive path because of full duplex operation and the imperfections of the hybrid coupler circuit. The DSL analog front end must incorporate a receiver pre-amp which is both low noise and highly linear for ADSL-standard operation. The LMH6622 is designed for the twin performance parameters of low noise and high linearity.

Applications ranging from +5V to +12V or ±2.5V to ±6V are fully supported by the LMH6622. In Figure 37, the LMH6622 is used as an inverting summing amplifier to provide both received pre-amp channel gain and driver output signal cancellation, i.e., the function of a hybrid coupler.

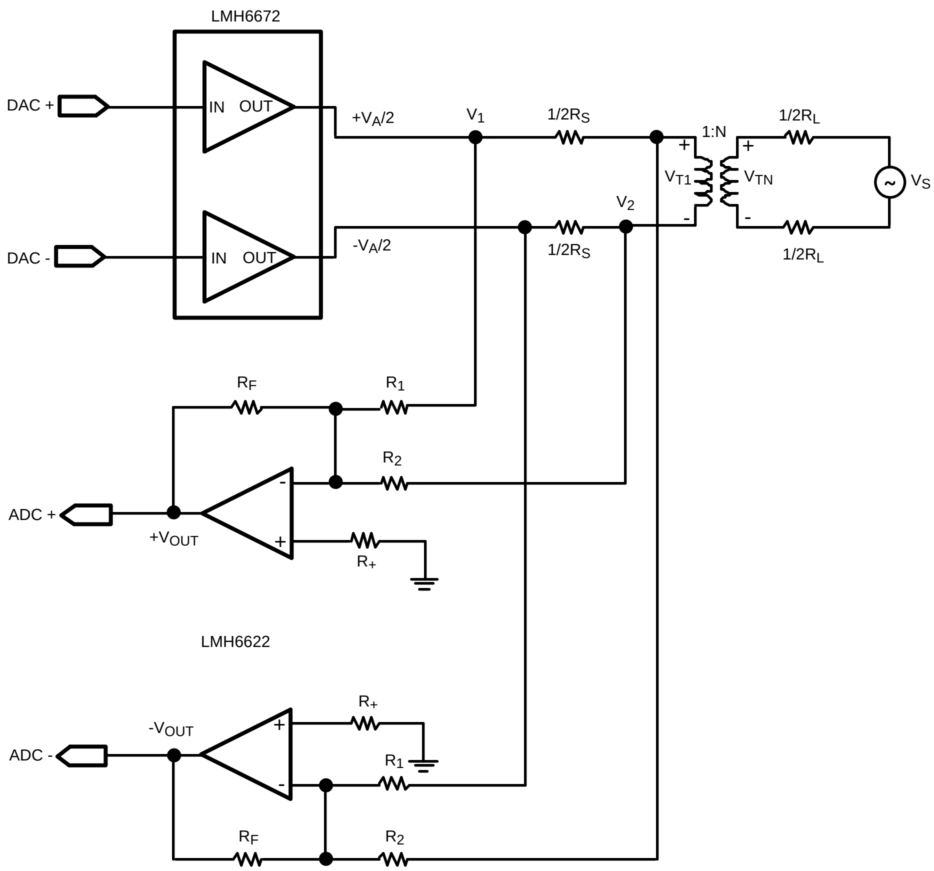


Figure 37. ADSL Receive Applications Circuit

The two R_S resistors are used to provide impedance matching through the 1:N transformer.

$$R_S = \frac{R_L}{N^2} \tag{1}$$

Where R_L is the impedance of the twisted pair line.

N is the turns ratio of the transformer.

The resistors R_2 and R_F are used to set the receive gain of the pre-amp. The receive gain is selected to meet the ADC full-scale requirement of a DSL chipset.

Resistor R_1 and R_2 along with R_F are used to achieve cancellation of the output driver signal at the output of the receiver.

Since the LMH6622 is configured as an inverting summing amplifier, V_{OUT} is found to be,

$$V_{OUT} = -R_F\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] \tag{2}$$

The expression for V_1 and V_2 can be found by using superposition principle.

When $V_S = 0$,

$$V_1 = \frac{1}{2}V_A \quad \text{and} \quad V_2 = -\frac{1}{4}V_A \tag{3}$$

When $V_A = 0$,

$$V_1 = 0 \text{ and } V_2 = -\frac{1}{2}V_{T1} \quad (4)$$

Therefore,

$$V_1 = \frac{1}{2}V_A \quad \text{and} \quad V_2 = -\frac{1}{4}V_A - \frac{1}{2}V_{T1} \quad (5)$$

And then,

$$V_{OUT} = -R_F\left[\frac{V_A}{2R_1} - \frac{V_A}{4R_2} - \frac{V_{T1}}{2R_2}\right] \quad (6)$$

Setting $R_1 = 2*R_2$ to cancel unwanted driver signal in the receive path, then we have

$$V_{OUT} = \frac{R_F}{2R_2}V_{T1} \quad (7)$$

We can also find that,

$$V_{TN} = \frac{1}{2}V_S \text{ and } V_{T1} = \frac{1}{N}V_{TN} = \frac{1}{2N}V_S \quad (8)$$

And then

$$V_{OUT} = \frac{R_F}{4NR_2}V_S \quad (9)$$

In conclusion, the peak-to-peak voltage to the ADC would be,

$$2\ V_{OUT} = \frac{R_F}{2NR_2}V_S \quad (10)$$

RECEIVE CHANNEL NOISE CALCULATION

The circuit of Figure 37 also has the characteristic that it cancels noise power from the drive channel.

The noise gain of the receive pre-amp is found to be:

$$A_N = 1 + \frac{R_F}{R_1//R_2} \quad (11)$$

Noise power at each of the output of LMH6622:

$$e^2_o = A^2_n\,[V^2_n + i^2_{non\text{-}inv}\,R_+^2 + 4kT\,R_+] + i^2_{inv}\,R^2_F + 4kT\,R_F\,A_n \quad (12)$$

where

V_n	Input referred voltage noise
i_n	Input referred current noise
$i_{non\text{-}inv}$	Input referred non-inverting current noise
i_{inv}	Input referred inverting current noise
k	Boltzmann’s constant, K = 1.38 x 10^{-23}
T	Resistor temperature in k
R_+	Source resistance at the non-inverting input to balance offset voltage, typically very small for this inverting summing applications

For a voltage feedback amplifier,

$$i_{inv} = i_{non\text{-}inv} = i_n \quad (13)$$

Therefore, total output noise from the differential pre-amp is:

$$e^2_{TotalOutput} = 2\,e^2_o \quad (14)$$

The factor '2 ' appears here because of differential output.

DIFFERENTIAL ANALOG-TO-DIGITAL DRIVER

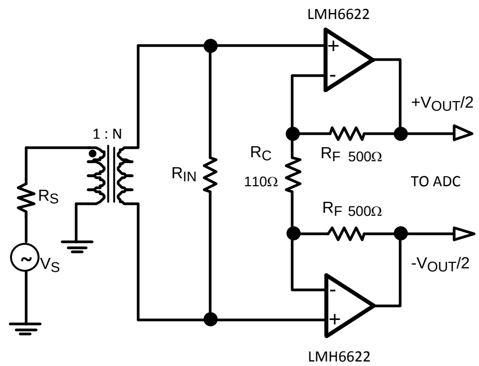


Figure 38. Circuit for Differential A/D Driver

The LMH6622 is a low noise, low distortion high speed operational amplifier. The LMH6622 comes in either SOIC-8 or VSSOP-8 packages. Because two channels are available in each package the LMH6622 can be used as a high dynamic range differential amplifier for the purpose of driving a high speed analog-to-digital converter. Driving a 1kΩ load, the differential amplifier of Figure 38 provides 20dB gain, a flat frequency response up to 6MHz, and harmonic distortion that is lower than 80dBc. This circuit makes use of a transformer to convert a single-ended signal to a differential signal. The input resistor R_{IN} is chosen by the following equation,

$$R_{IN} = \frac{1}{N^2} R_S \tag{15}$$

The gain of this differential amplifier can be adjusted by R_C and R_F,

$$A_V = 2 \frac{R_F}{R_C} \tag{16}$$

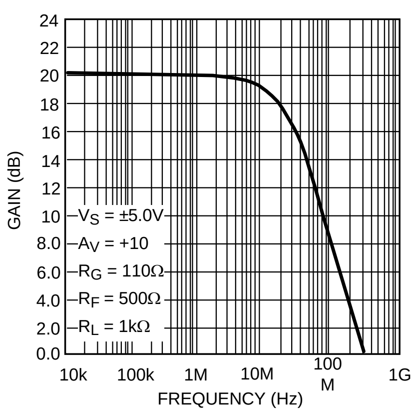


Figure 39. Frequency Response

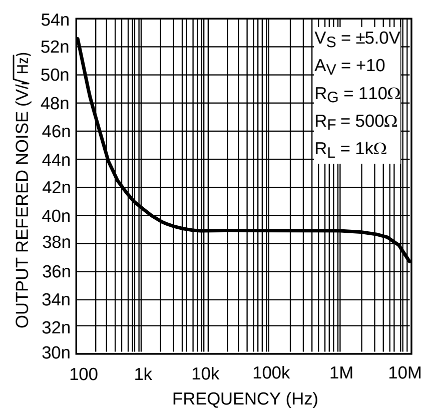


Figure 40. Total Output Referred Noise Density

CIRCUIT LAYOUT CONSIDERATIONS

Texas Instruments suggests the copper patterns on the evaluation boards listed below as a guide for high frequency layout. These boards are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice R_F design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). High quality chip capacitors with values in the range of 1000pF to 0.1µF should be used for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, a tantalum capacitor with a value between 4.7µF and 10µF should be connected in parallel with the chip capacitor. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Input and output termination resistors should be placed as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained so as to minimize the imbalance of amplitude and phase of the differential signal.

Device	Package	Evaluation Board P/N
LMH6622MA	SOIC-8	CLC730036
LMH6622MM	VSSOP-8	CLC730123

Component value selection is another important parameter in working with high speed/high performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and worse distortion.

DRIVING CAPACITIVE LOAD

Capacitive Loads decrease the phase margin of all op amps. The output impedance of a feedback amplifier becomes inductive at high frequencies, creating a resonant circuit when the load is capacitive. This can lead to overshoot, ringing and oscillation. To eliminate oscillation or reduce ringing, an isolation resistor can be placed between the load and the output. In general, the bigger the isolation resistor, the more damped the pulse response becomes. For initial evaluation, a 50Ω isolation resistor is recommended.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6622MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH66 22MA	
LMH6622MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 22MA	Samples
LMH6622MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 22MA	Samples
LMH6622MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A80A	
LMH6622MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A80A	Samples
LMH6622MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A80A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

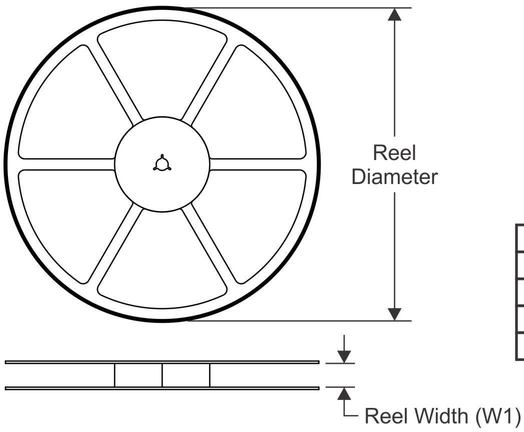
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

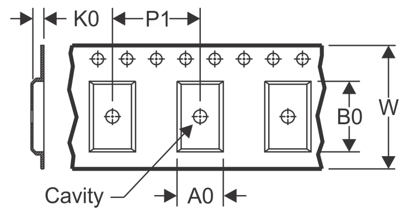
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

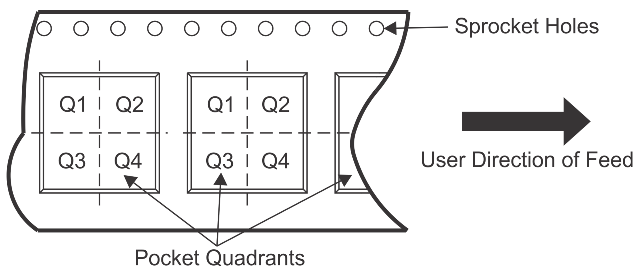


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

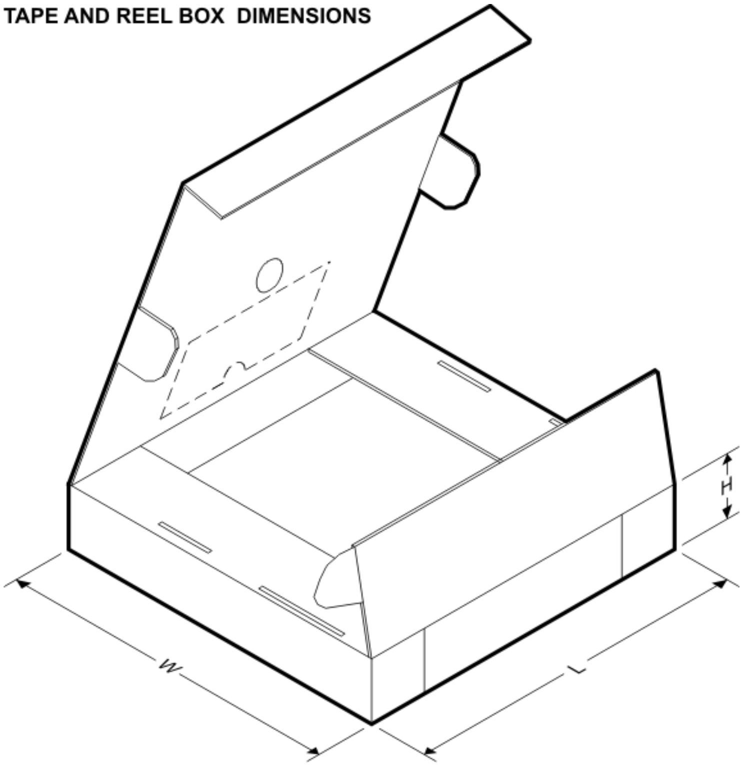
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6622MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

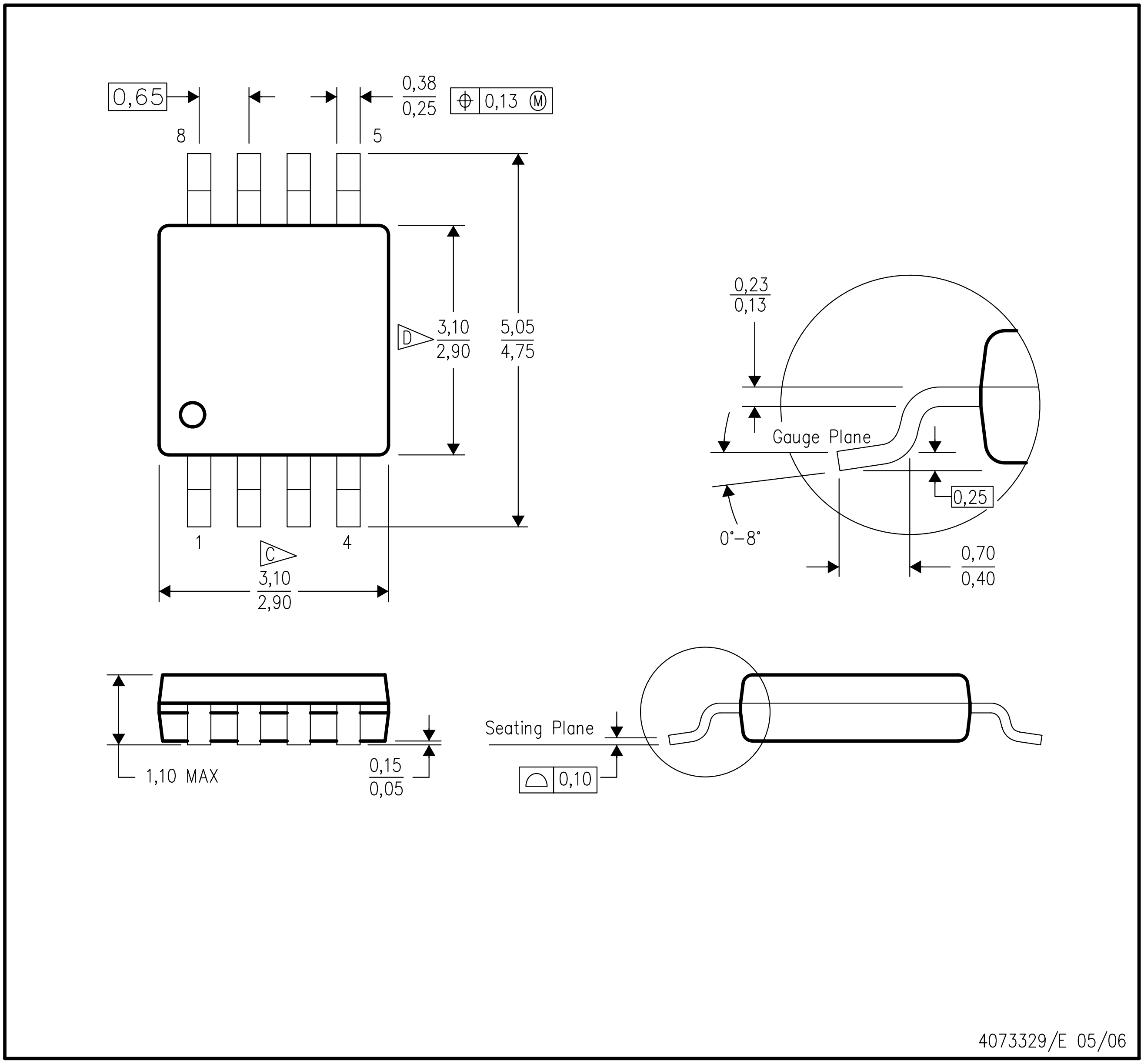
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

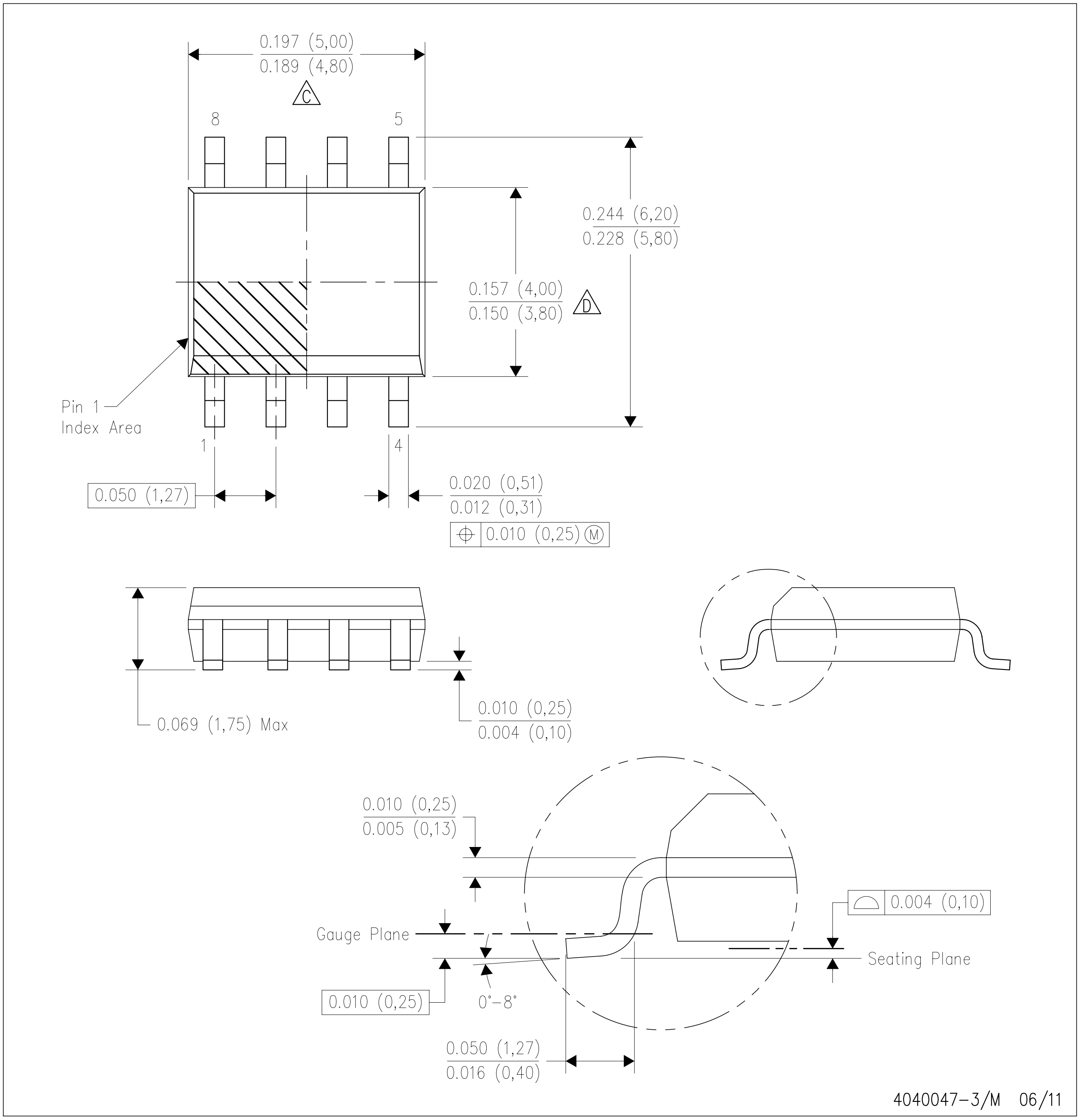
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6622MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265