LMH6702 1.7 GHz, Ultra Low Distortion, Wideband Op Amp

Check for Samples: LMH6702

FEATURES

V_S = ±5V, T_A = 25°C, A_V = +2V/V, R_L = 100Ω, V_{OUT} = 2V_{PP}, Typical Unless Noted:

- **2nd/3rd Harmonics (5MHz, SOT-23) −100/−96dBc**
- **−3dB Bandwidth (V_{OUT} = 0.5 V_{PP}) 1.7 GHz**
- **Low Noise 1.83nV/√Hz**
- **Fast Settling to 0.1% 13.4ns**
- **Fast Slew Rate 3100V/µs**
- **Supply Current 12.5mA**
- **Output Current 80mA**
- **Low Intermodulation Distortion (75MHz) −67dBc**
- **Improved Replacement for CLC409 and CLC449**

APPLICATIONS

- **Flash A/D Driver**
- **D/A Transimpedance Buffer**
- **Wide Dynamic Range IF amp**
- **Radar/Communication Receivers**
- **Line Driver**
- **High Resolution Video**

DESCRIPTION

The LMH6702 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefiting from current feedback architecture, the LMH6702 offers unity gain stability at exceptional speed without need for external compensation.

With its 720MHz bandwidth (A_V = 2V/V, V_O = 2V_{PP}), 10-bit distortion levels through 60MHz (R_L = 100Ω), 1.83nV/√Hz input referred noise and 12.5mA supply current, the LMH6702 is the ideal driver or buffer for high-speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers, requiring a wideband amplifier offering exceptional signal purity, will find the LMH6702's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

The LMH6702 is constructed using VIP10™ complimentary bipolar process and proven current feedback architecture. The LMH6702 is available in SOIC and SOT-23 packages.

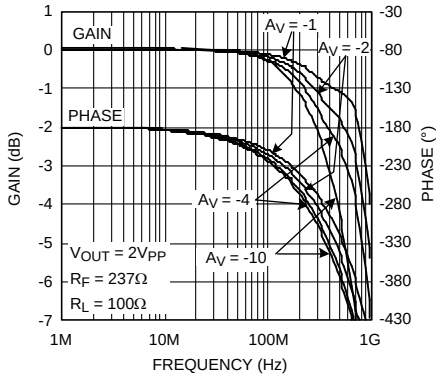

Figure 1. Inverting Frequency Response

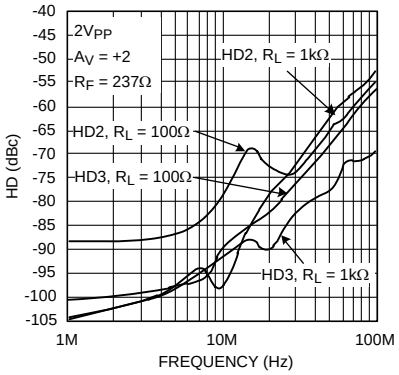

Figure 2. Harmonic Distortion vs. Load and Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Absolute Maximum Ratings[1][2]

V_S		±6.75V
I_{OUT}		See[3]
Common Mode Input Voltage		V^- to V^+
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C
ESD Tolerance[4]	Human Body Model	2000V
	Machine Model	200V
Storage Temperature Range		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.
(4) Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.

Operating Ratings[1]

Thermal Resistance	**Package**	**(θ_{JC})**	**(θ_{JA})**
	8-Pin SOIC	75°C/W	160°C/W
	5-Pin SOT-23	120°C/W	187°C/W
Operating Temperature			−40°C to +85°C
Nominal Supply Voltage			±5V to ±6V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Electrical Characteristics[1]

A_V = +2, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; unless specified

Symbol	Parameter	Conditions	Min[2]	Typ[2]	Max[2]	Units
Frequency Domain Performance						
$SSBW_{SM}$	-3dB Bandwidth	V_{OUT} = 0.5V_{PP}		1700		MHz
$SSBW_{LG}$		V_{OUT} = 2V_{PP}		720		
$LSBW_{LG}$		V_{OUT} = 4V_{PP}		480		
$SSBW_{HG}$		V_{OUT} = 2V_{PP}, A_V = +10		140		
$GF_{0.1dB}$	0.1dB Gain Flatness	V_{OUT} = 2V_{PP}		120		MHz
LPD	Linear Phase Deviation	DC to 100MHz		0.09		deg
DG	Differential Gain	R_L =150Ω, 3.58MHz/4.43MHz		0.024/0.021		%
DP	Differential Phase	R_L = 150Ω, 3.58MHz/4.43MHz		0.004/0.007		deg
Time Domain Response						
TRS/TRL	Rise and Fall Time	2V Step		0.87/0.77		ns
		6V Step		1.70/1.70		ns
OS	Overshoot	2V Step		0		%
SR	Slew Rate	6V_{PP}, 40% to 60%[3]		3100		V/µs
T_s	Settling Time to 0.1%	2V Step		13.4		ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Min/Max ratings are based on production testing unless otherwise specified.
(2) Typical numbers are the most likely parametric norm. Bold numbers refer to over temperature limits.
(3) Slew Rate is the average of the rising and falling edges.

Electrical Characteristics[1] (continued)

A_V = +2, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; unless specified

Symbol	Parameter	Conditions	Min[2]	Typ[2]	Max[2]	Units
Distortion And Noise Response						
HD2L	2nd Harmonic Distortion	$2V_{PP}$, 5MHz[4] (SOT-23/SOIC)		−100/ −87		dBc
HD2		$2V_{PP}$, 20MHz[4] (SOT-23/SOIC)		−79/ −72		dBc
HD2H		$2V_{PP}$, 60MHz[4] (SOT-23/SOIC)		−63/ −64		dBc
HD3L	3rd Harmonic Distortion	$2V_{PP}$, 5MHz[4] (SOT-23/SOIC)		−96/ −98		dBc
HD3		$2V_{PP}$, 20MHz[4] (SOT-23/SOIC)		−88/ −82		dBc
HD3H		$2V_{PP}$, 60MHz[4] (SOT-23/SOIC)		−70/ −65		dBc
OIM3	IMD	75MHz, P_O = 10dBm/ tone		−67		dBc
V_N	Input Referred Voltage Noise	>1MHz		1.83		nV/√Hz
I_N	Input Referred Inverting Noise Current	>1MHz		18.5		pA/√Hz
I_{NN}	Input Referred Non-Inverting Noise Current	>1MHz		3.0		pA/√Hz
SNF	Total Input Noise Floor	>1MHz		−158		dBm_{1Hz}
INV	Total Integrated Input Noise	1MHz to 150MHz		35		µV
Static, DC Performance						
V_{IO}	Input Offset Voltage			±1.0	±4.5 **±6.0**	mV
DV_{IO}	Input Offset Voltage Average Drift	See[5]		−13		µV/°C
I_{BN}	Input Bias Current	Non-Inverting[6]		−6	±15 **±21**	µA
DI_{BN}	Input Bias Current Average Drift	Non-Inverting[5]		+40		nA/°C
I_{BI}	Input Bias Current	Inverting[6]		−8	±30 **±34**	µA
DI_{BI}	Input Bias Current Average Drift	Inverting[5]		−10		nA/°C
PSRR	Power Supply Rejection Ratio	DC	47 **45**	52		dB
CMRR	Common Mode Rejection Ration	DC	45 **44**	48		dB
I_{CC}	Supply Current	R_L = ∞	11.0 **10.0**	12.5	16.1 **17.5**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		1.4		MΩ
C_{IN}	Input Capacitance	Non-Inverting		1.6		pF
R_{OUT}	Output Resistance	Closed Loop		30		mΩ
V_{OL}	Output Voltage Range	R_L = 100Ω	±3.3 **±3.2**	±3.5		V
CMIR	Input Voltage Range	Common Mode	±1.9	±2.2		V
I_O	Output Current		50	80		mA

(4) Harmonic distortion is strongly influenced by package type (SOT-23 or SOIC). See Application Note section under "Harmonic Distortion" for more information.
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Negative input current implies current flowing out of the device.

Connection Diagrams

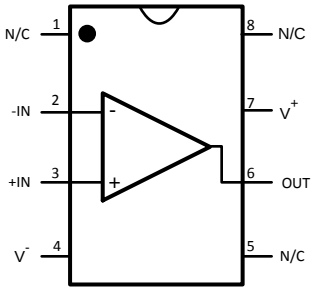


Figure 3. 8-Pin SOIC
Top View

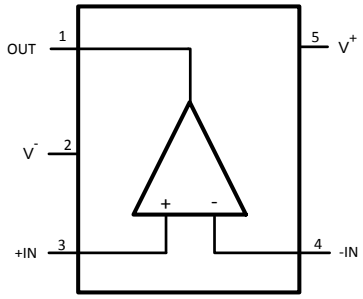


Figure 4. 5-Pin SOT-23
Top View

Typical Performance Characteristics

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified).

Non-Inverting Frequency Response

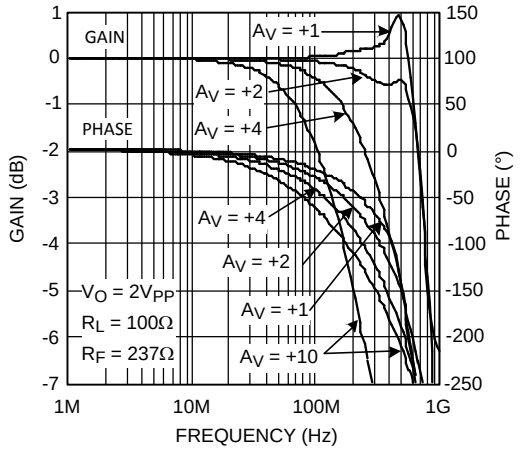


Figure 5.

Inverting Frequency Response

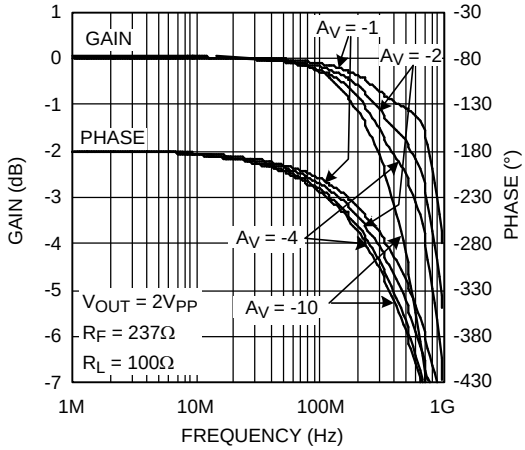


Figure 6.

Small Signal Bandwidth

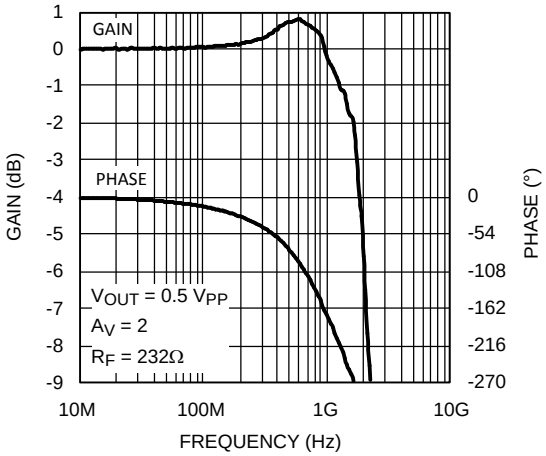


Figure 7.

Frequency Response for Various R_L's, A_V = +2

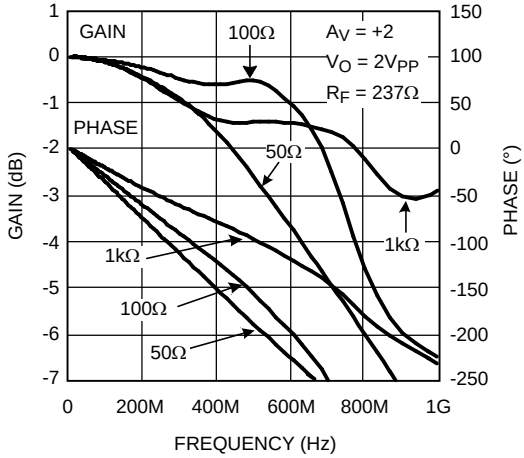


Figure 8.

Frequency Response for Various R_L's, A_V = +4

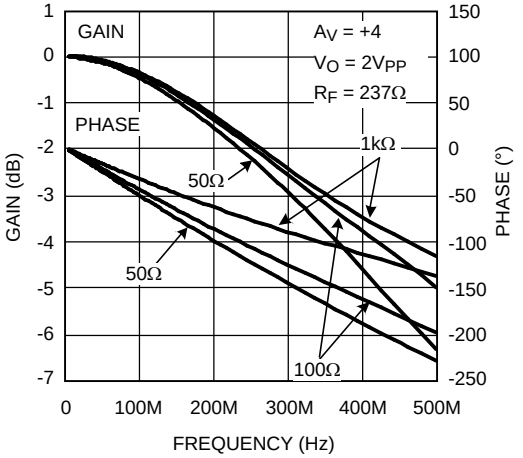


Figure 9.

Step Response, $2V_{PP}$

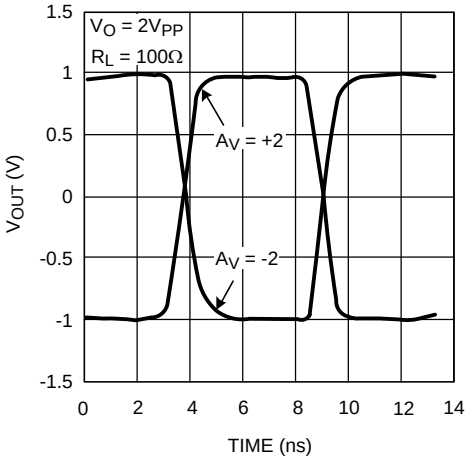


Figure 10.

Typical Performance Characteristics (continued)

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified).

Step Response, $6V_{PP}$

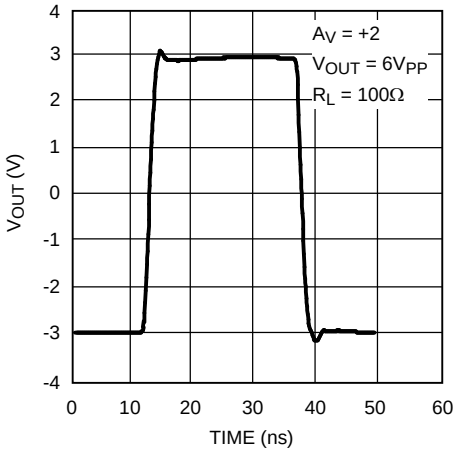


Figure 11.

Percent Settling vs Time

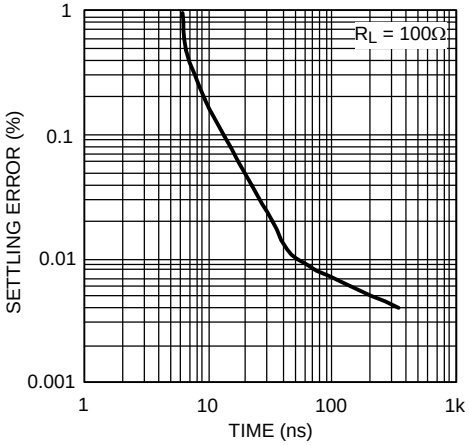


Figure 12.

Harmonic Distortion vs. Load and Frequency (SOIC package)

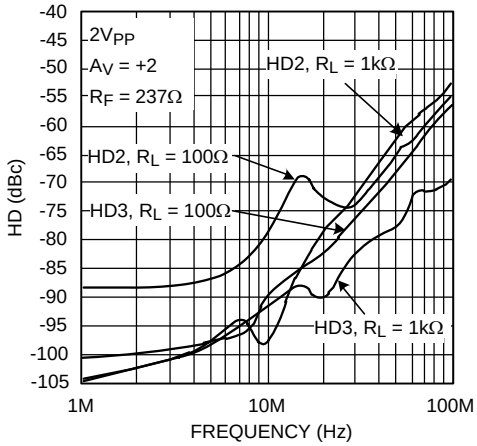


Figure 13.

2 Tone 3rd Order Spurious Level (SOIC package)

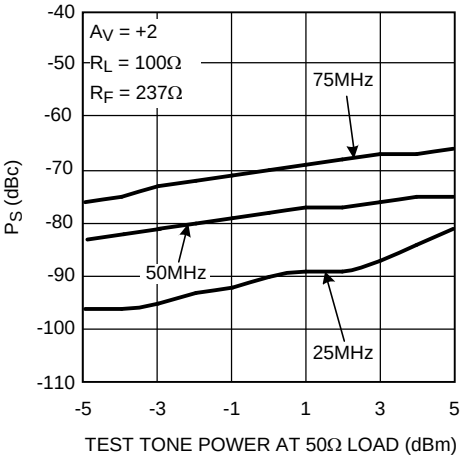


Figure 14.

R_S and Settling Time vs. C_L

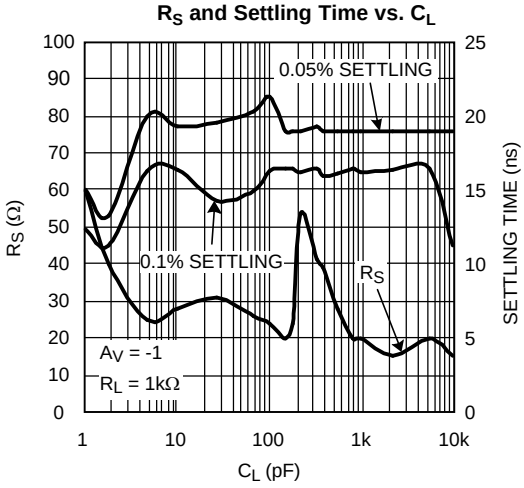


Figure 15.

HD2 vs. Output Power (across 100Ω) (SOIC package)

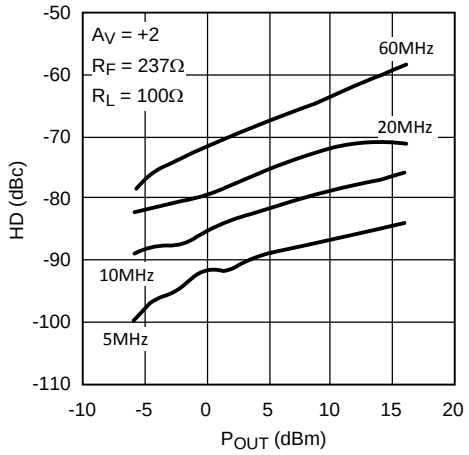


Figure 16.

Typical Performance Characteristics (continued)

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified).

HD3 vs. Output Power (across 100Ω) (SOIC package)

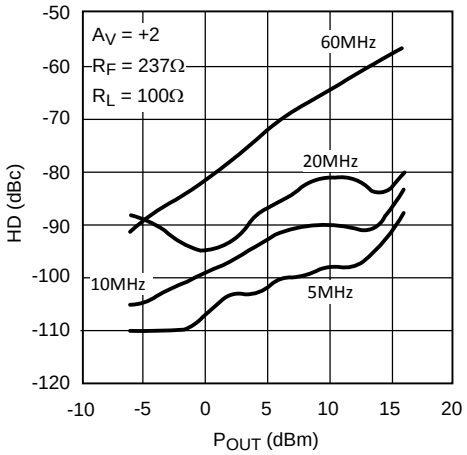


Figure 17.

Input Offset for 3 Representative Units

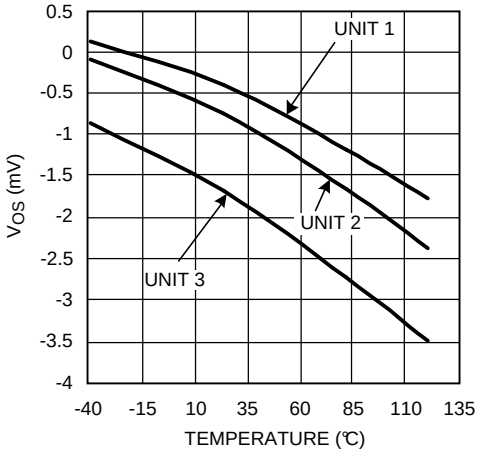


Figure 18.

Inverting Input Bias for 3 Representative Units

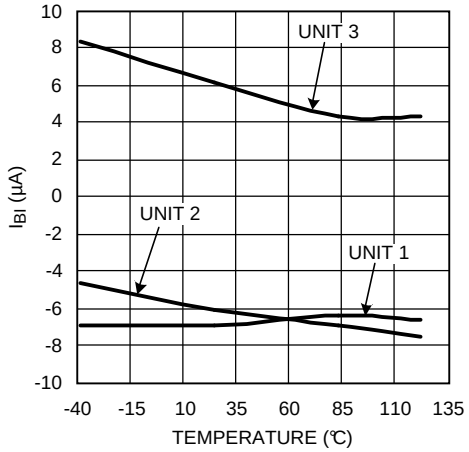


Figure 19.

Non-Inverting Input Bias for 3 Representative Units

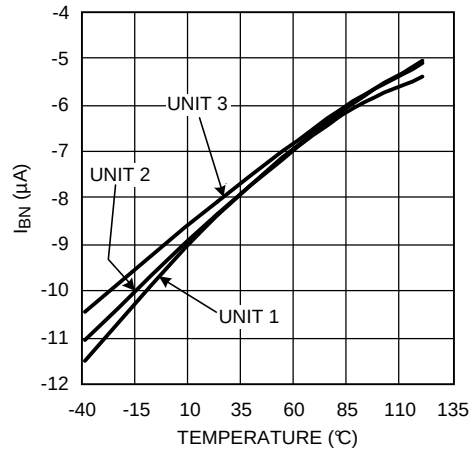


Figure 20.

Noise

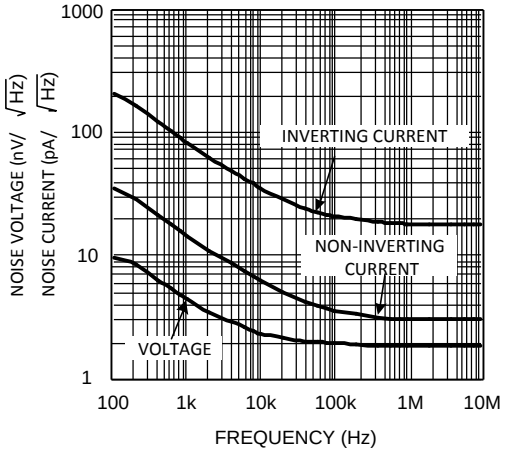


Figure 21.

CMRR, PSRR, R_{OUT}

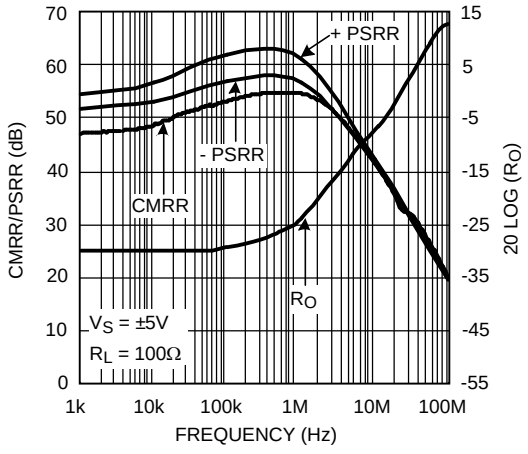


Figure 22.

Typical Performance Characteristics (continued)

(T_A = 25°C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified).

Transimpedance

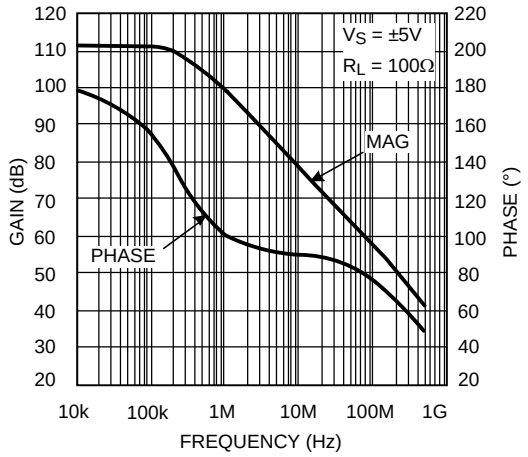


Figure 23.

DG/DP (NTSC)

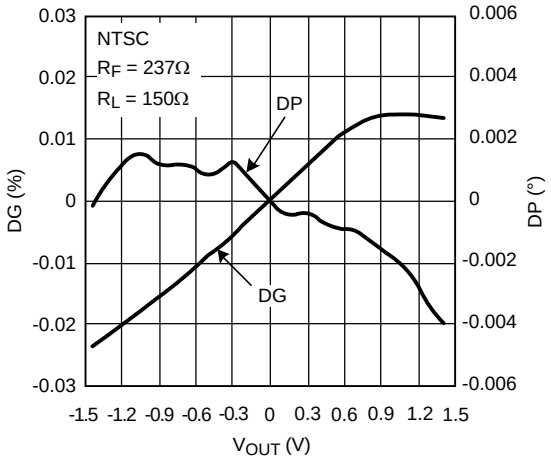


Figure 24.

DG/DP (PAL)

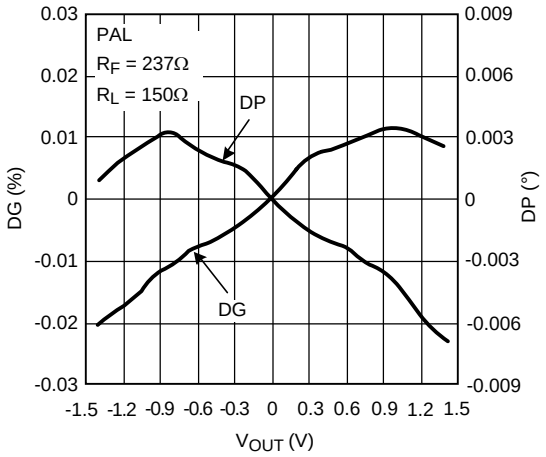


Figure 25.

APPLICATION SECTION

FEEDBACK RESISTOR

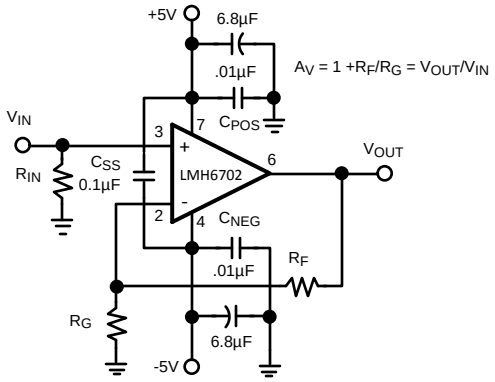


Figure 26. Recommended Non-Inverting Gain Circuit

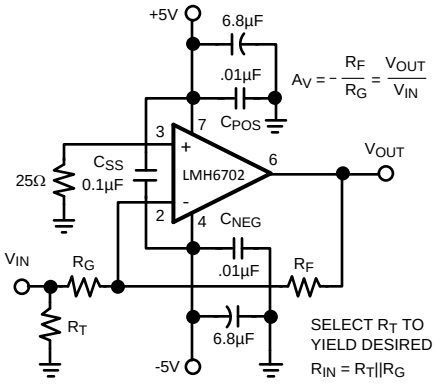


Figure 27. Recommended Inverting Gain Circuit

The LMH6702 achieves its excellent pulse and distortion performance by using the current feedback topology. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6702 is optimized for use with a 237Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with the occasions where a different R_F might be advantageous.

HARMONIC DISTORTION

The LMH6702 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low LMH6702 distortions shown in the Typical Performance Characteristics section. The capacitor C_{SS}, shown across the supplies in Figure 26 and Figure 27, is critical to achieving the lowest 2nd harmonic distortion. For absolute minimum distortion levels, it is also advisable to keep the supply decoupling currents (ground connections to C_{POS}, and C_{NEG} in Figure 26 and Figure 27) separate from the ground connections to sensitive input circuitry (such as R_G, R_T, and R_{IN} ground connections). Splitting the ground plane in this fashion and separately routing the high frequency current spikes on the decoupling caps back to the power supply (similar to "Star Connection" layout technique) ensures minimum coupling back to the input circuitry and results in best harmonic distortion response (especially 2nd order distortion).

If this lay out technique has not been observed on a particular application board, designer may actually find that supply decoupling caps could adversely affect HD2 performance by increasing the coupling phenomenon already mentioned. Figure 28 below shows actual HD2 data on a board where the ground plane is "shared" between the supply decoupling capacitors and the rest of the circuit. Once these capacitors are removed, the HD2 distortion levels reduce significantly, especially between 10MHz-20MHz, as shown in Figure 28 below:

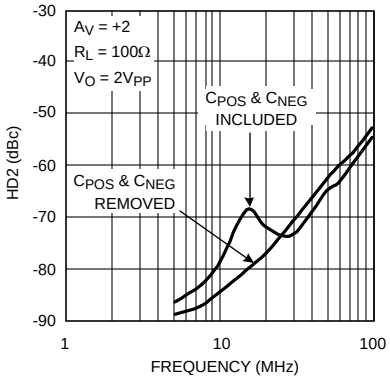


Figure 28. Decoupling Current Adverse Effect on a Board with Shared Ground Plane

At these extremely low distortion levels, the high frequency behavior of decoupling capacitors themselves could be significant. In general, lower value decoupling caps tend to have higher resonance frequencies making them more effective for higher frequency regions. A particular application board which has been laid out correctly with ground returns "split" to minimize coupling, would benefit the most by having low value and higher value capacitors paralleled to take advantage of the effective bandwidth of each and extend low distortion frequency range.

Another important variable in getting the highest fidelity signal from the LMH6702 is the package itself. As already noted, coupling between high frequency current transients on supply lines and the device input can lead to excess harmonic distortion. An important source of this coupling is in fact through the device bonding wires. A smaller package, in general, will have shorter bonding wires and therefore lower coupling. This is true in the case of the SOT-23 compared to the SOIC package where a marked improvement in HD can be measured in the SOT-23 package. Figure 29 below shows the HD comparing SOT-23 to SOIC package:

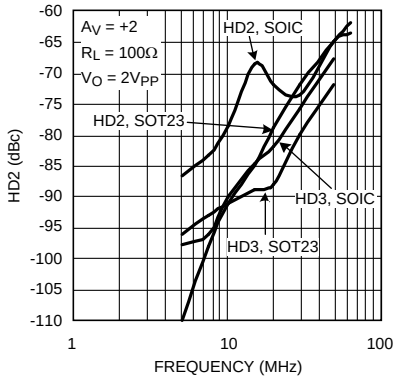


Figure 29. SOIC and SOT-23 Packages Distortion Terms Compared

The LMH6702 data sheet shows both SOT-23 and SOIC data in the Electrical Characteristic section to aid in selecting the right package. The Typical Performance Characteristics section shows SOIC package plots only.

2-TONE 3rd ORDER INTERMODULATION

The 2-tone, 3rd order spurious plot shows a relatively constant difference between the test power level and the spurious level with the difference depending on frequency. The LMH6702 does not show an intercept type performance, (where the relative spurious levels change at a 2X rate vs. the test tone powers), due to an internal full power bandwidth enhancement circuit that boosts the performance as the output swing increases while dissipating negligible quiescent power under low output power conditions. This feature enhances the distortion performance and full power bandwidth to match that of much higher quiescent supply current parts.

CAPACITIVE LOAD DRIVE

Figure 30 shows a typical application using the LMH6702 to drive an ADC.

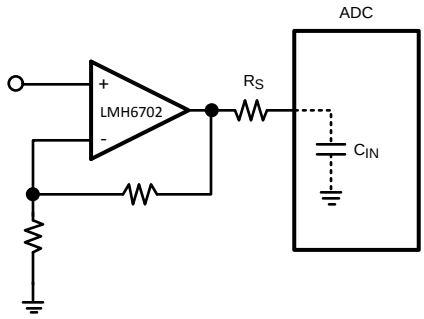


Figure 30. Input Amplifier to ADC

The series resistor, R_S, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of "R_S and Settling Time vs. C_L" in the Typical Performance Characteristics section is an excellent starting point for selecting R_S. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load with the output driving a very light resistive load (1kΩ). Sensitivity to capacitive loading is greatly reduced once the output is loaded more heavily. Therefore, for cases where the output is heavily loaded, R_S value may be reduced. The exact value may best be determined experimentally for these cases.

In applications where the LMH6702 is replacing the CLC409, care must be taken when the device is lightly loaded and some capacitance is present at the output. Due to the much higher frequency response of the LMH6702 compared to the CLC409, there could be increased susceptibility to low value output capacitance (parasitic or inherent to the board layout or otherwise being part of the output load). As already mentioned, this susceptibility is most noticeable when the LMH6702's resistive load is light. Parasitic capacitance can be minimized by careful lay out. Addition of an output snubber R-C network will also help by increasing the high frequency resistive loading.

Referring back to Figure 30, it must be noted that several additional constraints should be considered in driving the capacitive input of an ADC. There is an option to increase R_S, band-limiting at the ADC input for either noise or Nyquist band-limiting purposes. Increasing R_S too much, however, can induce an unacceptably large input glitch due to switching transients coupling through from the "convert" signal. Also, C_{IN} is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as R_S is increased. Only slight adjustments up or down from the recommended R_S value should therefore be attempted in optimizing system performance.

DC ACCURACY AND NOISE

Example below shows the output offset computation equation for the non-inverting configuration using the typical bias current and offset specifications for A_V = + 2:

Output Offset :

$$V_O = (\pm I_{BN} \cdot R_{IN} \pm V_{IO}) (1 + R_F/R_G) \pm I_{BI} \cdot R_F \quad (1)$$

Where R_{IN} is the equivalent input impedance on the non-inverting input.

Example computation for A_V = +2, R_F = 237Ω, R_{IN} = 25Ω:

$$V_O = (\pm 6\mu A \cdot 25\Omega \pm 1mV) (1 + 237/237) \pm 8\mu A \cdot 237 = \pm 4.20mV \quad (2)$$

A good design, however, should include a worst case calculation using Min/Max numbers in the data sheet tables, in order to ensure "worst case" operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7. The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

PRINTED CIRCUIT LAYOUT

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6702MF	SOT-23	CLC730216
LMH6702MA	SOIC	CLC730227

These free evaluation boards are shipped when a device sample request is placed with Texas Instruments.

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6702MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH67 02MA	
LMH6702MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH67 02MA	Samples
LMH6702MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH67 02MA	Samples
LMH6702MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A83A	Samples
LMH6702MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A83A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

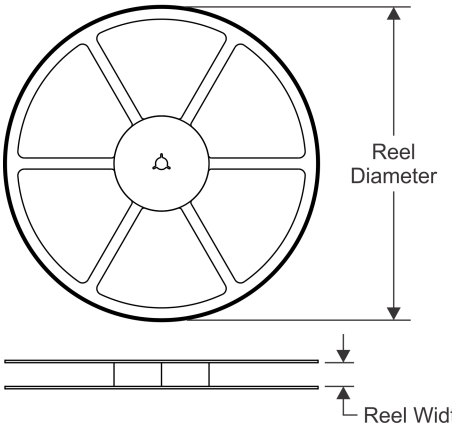
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

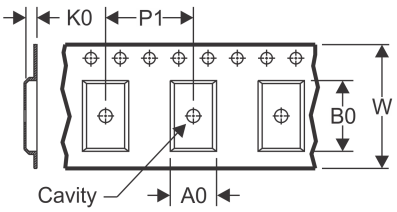
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

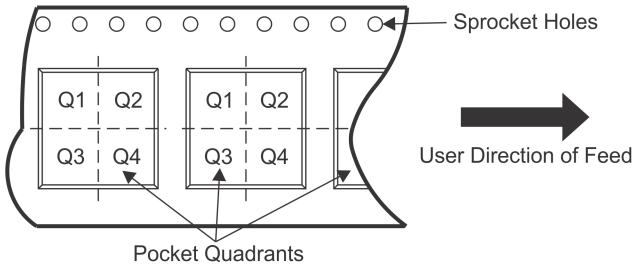


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

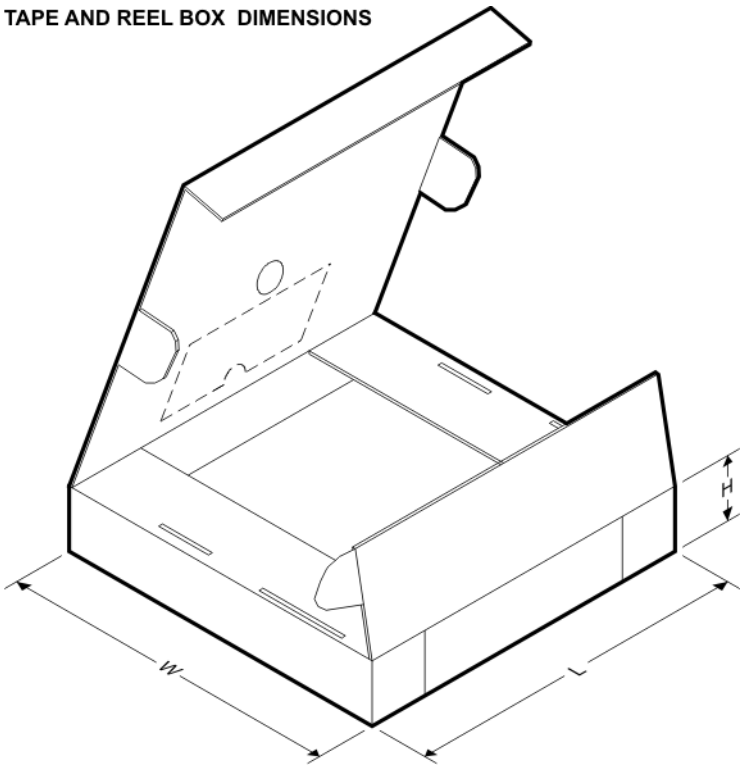
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6702MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6702MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6702MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

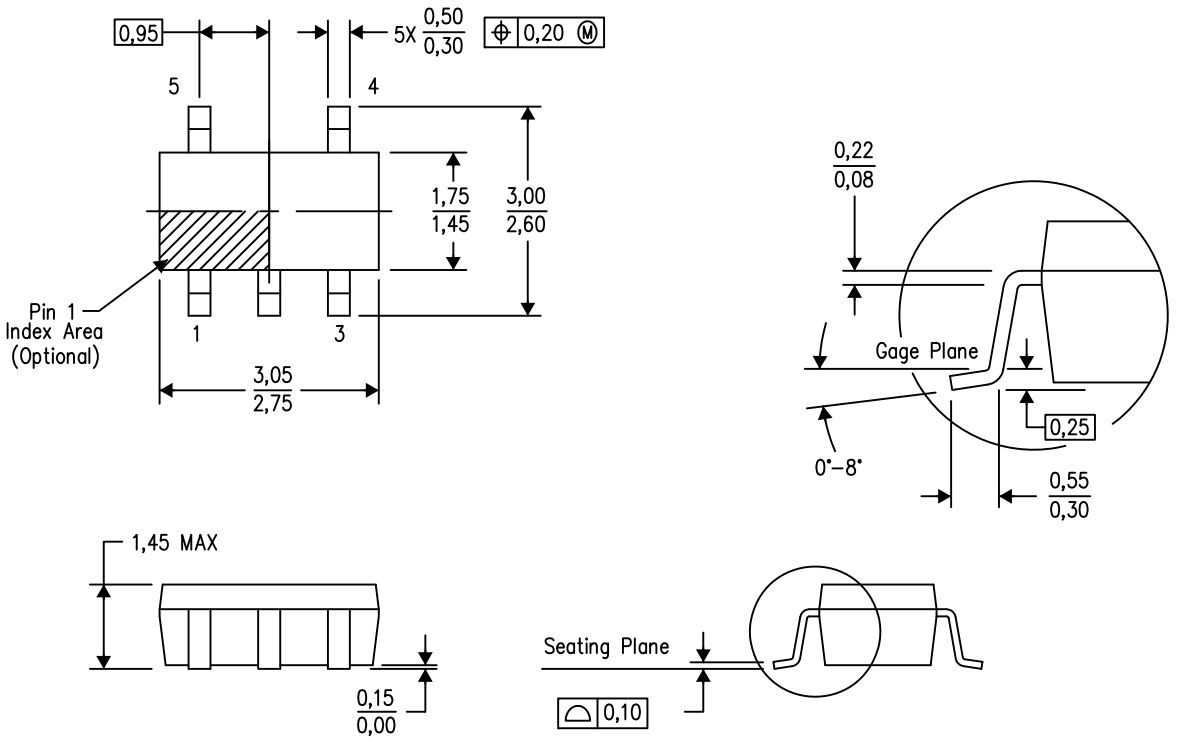
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6702MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6702MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6702MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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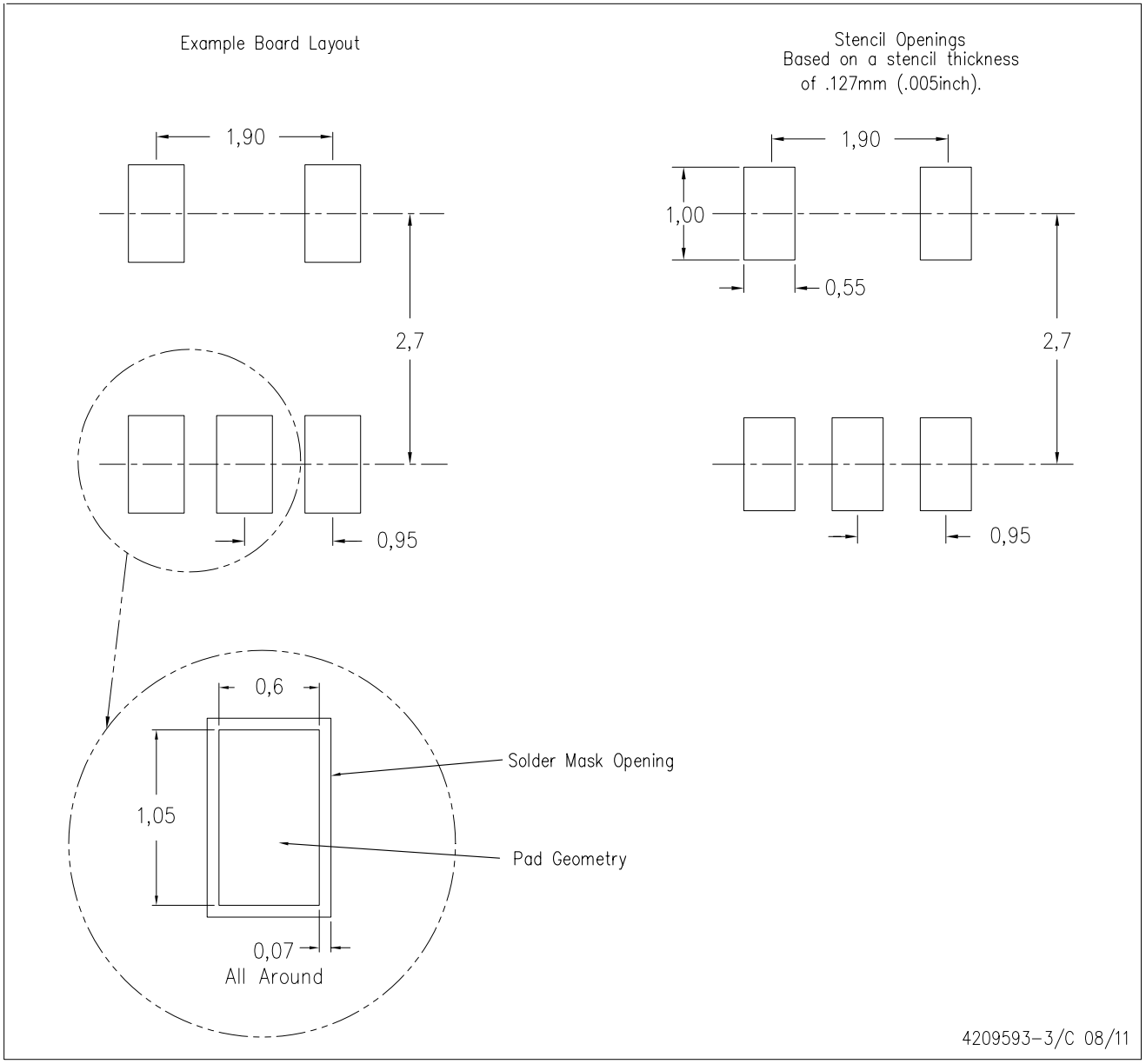
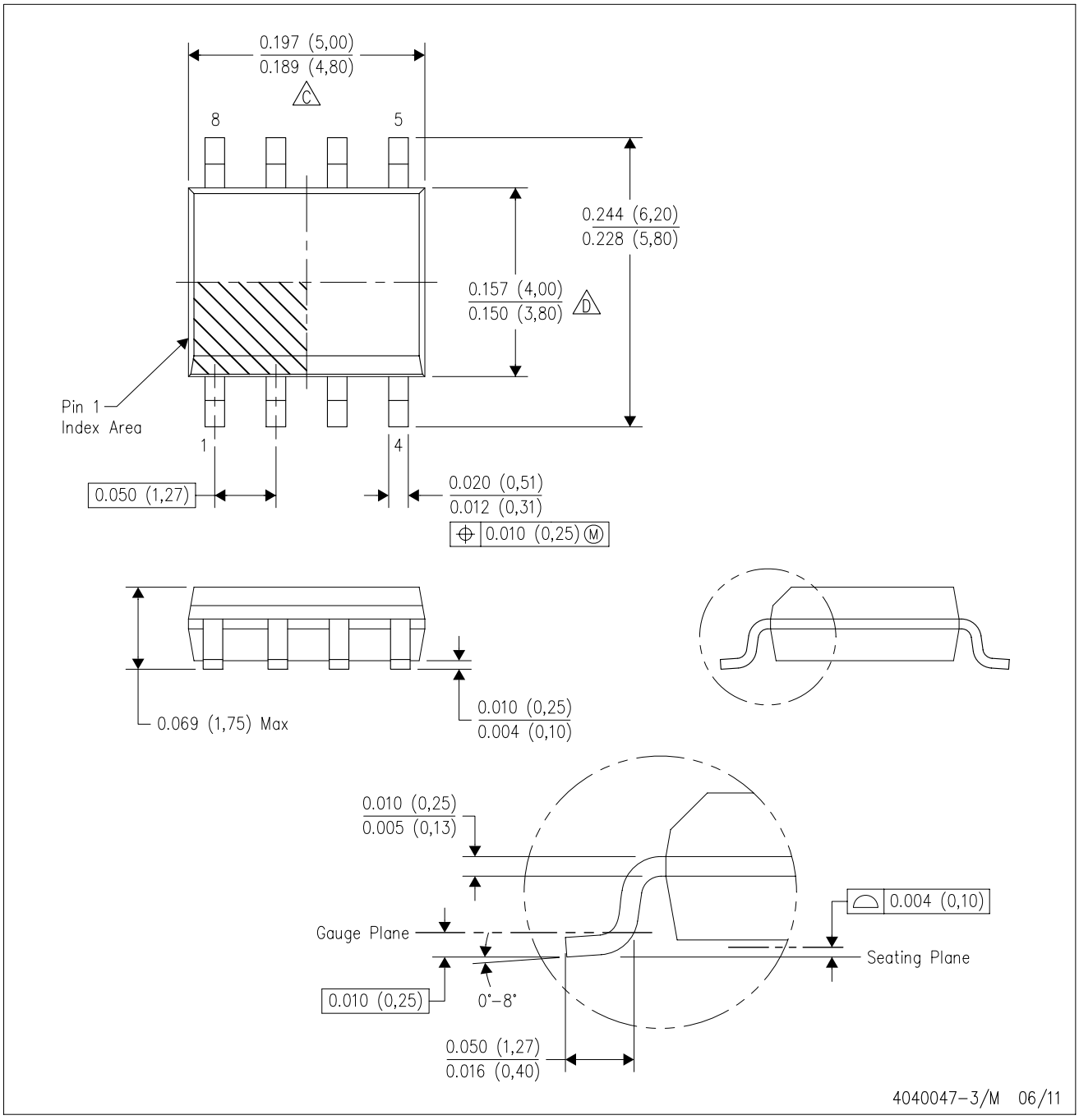
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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