LMH6881 DC to 2.4GHz, High Linearity, Programmable Differential Amplifier

Check for Samples: LMH6881

FEATURES

- **Small Signal Bandwidth: 2400 MHz**
- **OIP3 @ 100 MHz: 44 dBm**
- **HD3 @ 100 MHz: −100 dBc**
- **Noise Figure: 9.7 dB**
- **Voltage Gain Range: 26 dB to 6 dB**
- **Voltage Gain Step Size 0.25 dB**
- **Input Impedance 100 Ω**
- **Parallel and Serial Gain Control**
- **Power Down Capability**

APPLICATIONS

- **Oscilloscope Front End**
- **Spectrum Analyzer Gain Block**
- **Differential ADC Driver**
- **Differential Cable Driver**
- **IF / RF and Baseband Gain Blocks**
- **Medical Imaging**

DESCRIPTION

The LMH6881 is a high-speed, high-performance, programmable differential amplifier. With a bandwidth of 2.4 GHz and high linearity of 44 dBm OIP3, the LMH6881 is suitable for a wide variety of signal conditioning applications.

The LMH6881 programmable differential amplifier combines the best of both fully differential amplifiers and variable gain amplifiers. It offers superior noise and distortion performance over the entire gain range without external resistors, enabling the use of just one device and one design for multiple applications requiring different gain settings.

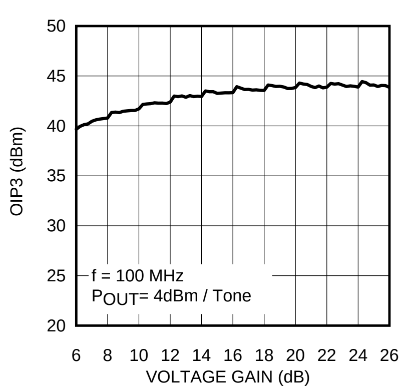
The LMH6881 is an easy-to-use amplifier that can replace both fully differential, fixed gain amplifiers as well as variable gain amplifiers. The LMH6881 requires no external gain-setting components and supports gain settings from 6 dB to 26 dB with small, accurate 0.25-dB gain steps. With an input impedance of 100 Ω the LMH6881 is easy to drive from a variety of sources such as mixers or filters. The LMH6881 also supports 50 Ω single-ended signal sources and supports both DC- and AC-coupled applications.

Parallel gain control allows the LMH6881 to be soldered down in a fixed gain so that no control circuit is required. If dynamic-gain control is desired, the LMH6881 can be changed with SPI™ serial commands or with the parallel pins.

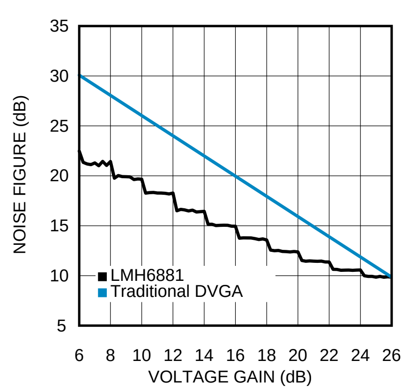
The LMH6881 is fabricated in TI's CBiCMOS8 proprietary complementary silicon germanium process and is available in a space saving, thermally enhanced 24-pin Lead Quad WQFN package. The same amplifier is offered in a dual package as the LMH6882.

Performance Curves

OIP3 over Voltage Gain Range



Noise Figure Over Voltage Gain Range
DVGA Response Shown for Comparison



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	1 kV
	Charged Device Model	250V
Positive Supply Voltage (VCC)		−0.6V to 5.5V
Differential Voltage between Any Two Grounds		<200 mV
Analog Input Voltage Range		−0.6V to 5.5V
Digital Input Voltage Range		−0.6V to 5.5V
Output Short Circuit Duration (one pin to ground)		Infinite
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Soldering Information	Infrared or Convection (30 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For verified specifications, see the Electrical Characteristics table.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Operating Ratings(1)

Supply Voltage (VCC)			4.75V to 5.25V
Differential Voltage Between Any Two Grounds			<10 mV
Analog Input Voltage Range, AC Coupled			0V to VCC
Temperature Range(2)			−40°C to +85°C
Package Thermal Resistance(3)	24–pin WQFN	(θ_{JA})	53°C/W
		(θ_{JC})	6°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For verified specifications, see the Electrical Characteristics table.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(3) Junction to ambient (θ_{JA}) thermal resistance measured on JEDEC 4-layer board. Junction-to-case (θ_{JC}) thermal resistance measured at exposed thermal pad; package is not mounted to any PCB.

5V Electrical Characteristics (1)(2)(3)

The following specifications apply for single supply with VCC = 5 V, Maximum Gain (26 dB), R_L = 200 Ω, fin = 100 MHz. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (4)	Typ (5)	Max (4)	Units
Dynamic Performance						
3 dBBW	−3 dB Bandwidth	V_{OUT}= 2 V_{PPD}		2.4		GHz
NF	Noise Figure	Source Resistance (Rs) = 100 Ω		9.7		dB
OIP3	Output Third Order Intercept Point (6)	f = 100 MHz, P_{OUT} = 4 dBm per tone, tone spacing = 1 MHz		44		dBm
		f = 200 MHz, P_{OUT} = 4 dBm per tone, tone spacing = 2 MHz		42		
OIP2	Output Second Order Intercept Point	P_{OUT}= 4 dBm per Tone, f1 =112.5 MHz, f2 = 187.5 MHz		76		dBm
IMD3	Third Order Intermodulation Products	f = 100 MHz, P_{OUT} = 4 dBm per tone, tone spacing = 1 MHz		−80		dBc
		f = 200 MHz, P_{OUT} = 4 dBm per tone, tone spacing =2 MHz		−76		
P1dB	1dB Compression Point	Output Power		17		dBm
HD2	Second Order Harmonic Distortion	f = 200 MHz, P_{OUT} = 4 dBm		−65		dBc
HD3	Third Order Harmonic Distortion	f = 200 MHz, P_{OUT} = 4 dBm		−74		dBc
CMRR	Common Mode Rejection Ratio (7)	Pin = −15 dBm, f = 100 MHz		−40		dBc
SR	Slew Rate			6000		V/us
	Output Voltage Noise	Maximum Gain f > 1 MHz		47		nV/√Hz
	Input Referred Voltage Noise	Maximum Gain f > 1 MHz		2.3		nV/√Hz
Analog I/O						
R_{IN}	Input Resistance	Differential, INPD to INMD		100		Ω
R_{IN}	Input Resistance	Single Ended, INPS or INPD, 50-Ω termination on unused input		50		Ω
V_{ICM}	Input Common Mode Voltage	Self Biased		2.5		V
	Maximum Input Voltage Swing	Volts peak to peak, differential		2.85		V_{PPD}
	Maximum Differential Output Voltage Swing	Differential, f < 10MHz		6		V_{PPD}
R_{OUT}	Output Resistance	Differential, f = 100MHz		0.4		Ω
Gain Parameters						
	Maximum Voltage Gain	Parallel Inputs (INPD and INMD), Rs = 100 Ω		26		dB
		Single ended input (INMS or INPS), 50-Ω Rs and 50-Ω termination on unused input.		26.6		
	Minimum Gain	Parallel Inputs, Rs = 100 Ω		6		dB
	Gain Steps	Available using SPI interface		80		
		Available using parallel interface		10		
	Gain Step Size	Available using SPI interface		0.25		dB
		Available using parallel interface		2		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No verification of parametric performance is indicated in the electrical tables under conditions different than those tested
(2) Negative input current implies current flowing out of the device.
(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(6) OIP3 is the third order intermodulation intercept point. In this datasheet OIP3 numbers are single power measurements where OIP3 = IMD3 / 2 + POUT (per tone). OIP2 is the second order intercept point where OIP2 = IMD2 + POUT (per tone). HD2 is the second order harmonic distortion and is a single tone measurement. HD3 is the third order harmonic distortion and is a single tone measurement. Power measurements are made at the amplifier output pins.
(7) CMRR is defined as the differential response at the output in response to a common mode signal at the input.

5V Electrical Characteristics[(1)(2)(3)] (continued)

The following specifications apply for single supply with VCC = 5 V, Maximum Gain (26 dB), R_L = 200 Ω, fin = 100 MHz. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min[(4)]	Typ[(5)]	Max[(4)]	Units
	Gain Step Error	Any two adjacent steps over entire range		±0.125		dB
	Gain Step Phase Shift	Any two adjacent steps over entire range		±3		Degrees
	Gain Step Switching Time			20		ns
	Enable/ Disable Time	Settled to 90% level		15		ns
Power Requirements						
ICC	Supply Current			100	135	mA
P	Power			0.5		W
ICCD	Disabled Supply Current			15		mA
All Digital Inputs						
	Logic Compatibility	TTL, 2.5V CMOS, 3.3V CMOS, 5V CMOS				
VIL	Logic Input Low Voltage			0.4		V
VIH	Logic Input High Voltage			2.0-5.0		V
IIH	Logic Input High Input Current			−9		μA
IIL	Logic Input Low Input Current			−47		μA
Parallel Mode Timing						
t_{GS}	Setup Time			3		ns
t_{GH}	Hold Time			3		ns
Serial Mode						
f_{CLK}	SPI Clock Frequency	50% duty cycle	10	50		MHz

CONNECTION DIAGRAM

24-Pin WQFN

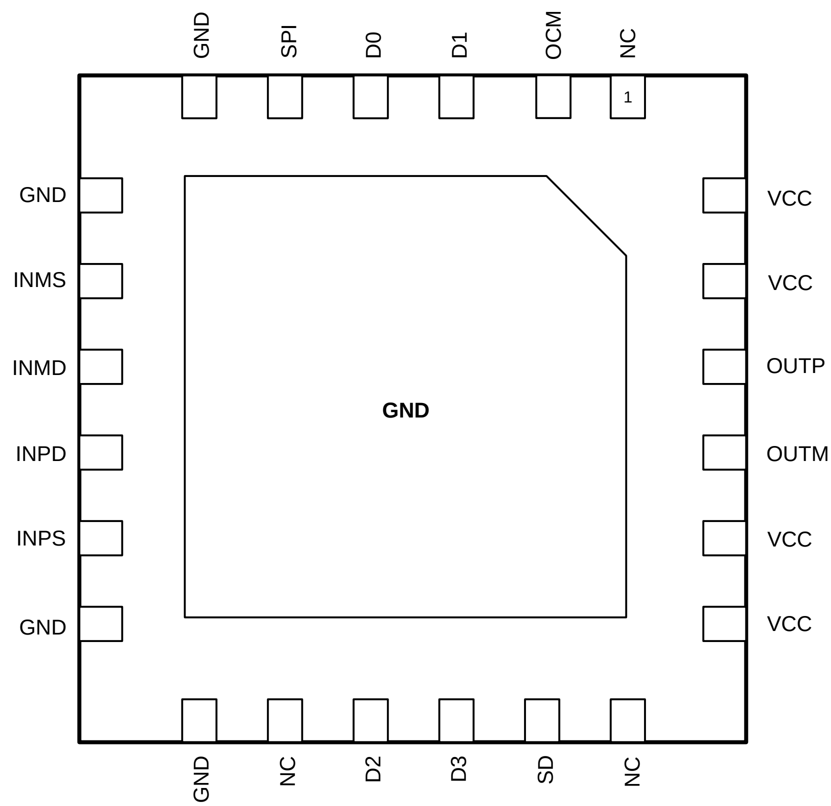


Figure 1. Top View

PIN DESCRIPTIONS

Pin Number	Symbol	Pin Category	Description
Analog I/O			
9,10	INPD, INMD	Analog Input	Differential inputs 100 Ω
8, 11	INPS, INMS	Analog Input	Single-ended inputs 50 Ω
21, 22	OUTP, OUTM	Analog Output	Differential outputs, low impedance
Power			
6, 7, 12, 13	GND	Ground	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
19, 20, 23, 24	VCC	Power	Power supply pins. Valid power supply range is 4.75 V to 5.25 V.
Exposed Center Pad		Thermal/ Ground	Thermal management/ Ground
Digital Inputs			
5	SPI	Digital Input	0 = Parallel Mode, 1 = Serial Mode
Parallel Mode Digital Pins, SPI = Logic Low			
3, 4, 15, 16	D0, D1, D2, D3	Digital Input	Attenuator control
17	SD	Digital Input	Shutdown 0 = amp on, 1 = amp off
Serial Mode Digital Pins, SPI= Logic High, SPI compatible			
4	SDO	Digital Output - Open Emitter	Serial Data Output (Requires external bias.)
3	SDI	Digital Input	Serial Data In
16	CS	Digital Input	Chip Select (active low)
15	CLK	Digital Input	Clock

PIN LIST

Pin Number	Description	Pin
1	NC	
2	OCM	Output Common Mode, gain of 2
3	D1, SDI	Parallel mode = Logic control signal, position 1 or weight 2^1 SPI mode = serial data in (SDI)
4	D0, SDO	Parallel mode = Logic control signal, position 0 or weight 2^0 SPI mode = serial data out (SDO)
5	SPI	Serial mode control
6	GND	Ground
7	GND	Ground
8	INMS	Amplifier single ended input minus swing (negative)
9	INMD	Amplifier differential input minus swing (negative)
10	INPD	Amplifier differential input plus swing (positive)
11	INPS	Amplifier single ended input plus swing (positive)
12	GND	Ground
13	GND	Ground
14	NC	

PIN LIST (continued)

Pin Number	Description	Pin
15	D2	Parallel mode = Logic control signal, position 2 or weight 2^2 SPI mode = serial clock (CLK)
16	D3	Parallel mode = Logic control signal, position 3 or weight 2^3 SPI mode = chip select (CS)
17	SD	Device Shutdown
18	NC	
19	VCC	Power supply nominal value of 5V
20	VCC	Power supply nominal value of 5V
21	OUTM	Amplifier output minus (negative)
22	OUTP	Amplifier output plus (positive)
23	VCC	Power supply nominal value of 5V
24	VCC	Power supply nominal value of 5V

Typical Performance Characteristics

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

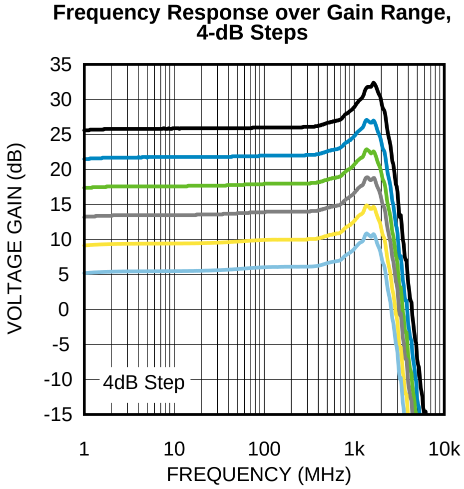


Figure 2.

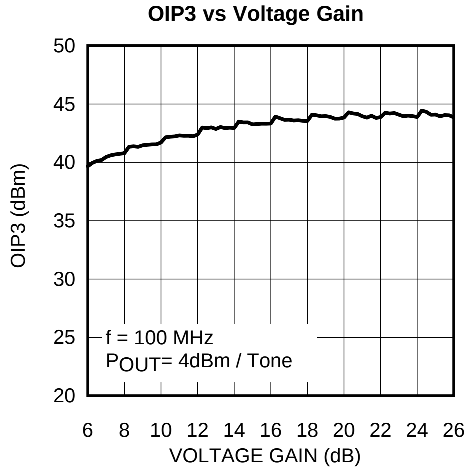


Figure 3.

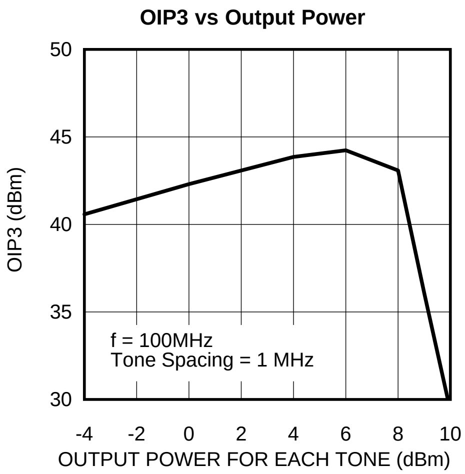
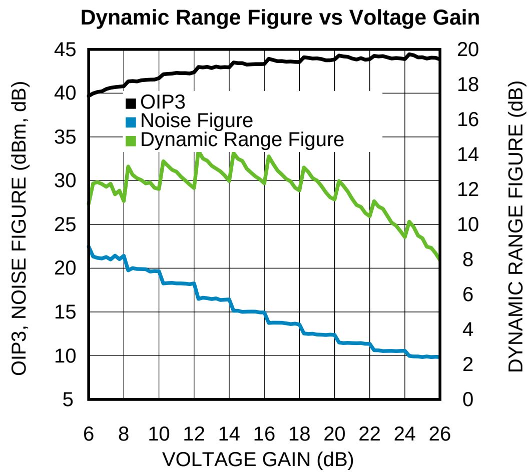


Figure 4.



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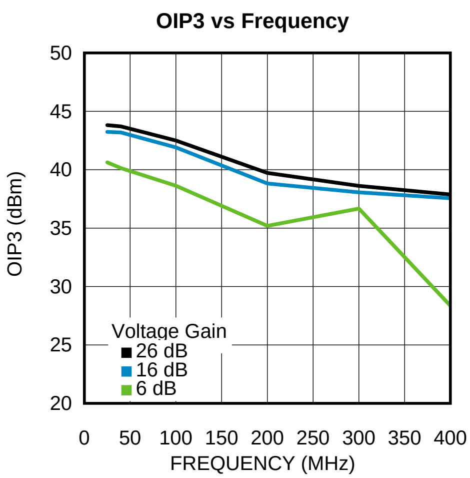


Figure 6.

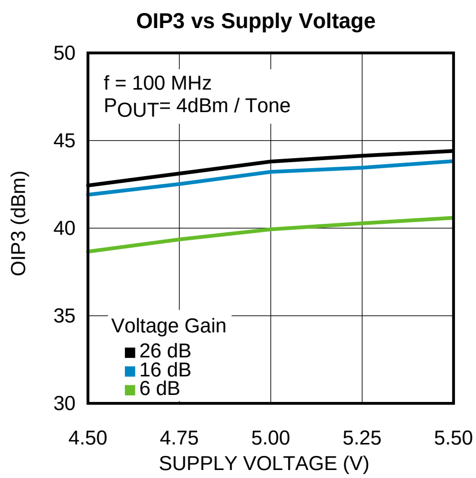


Figure 7.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

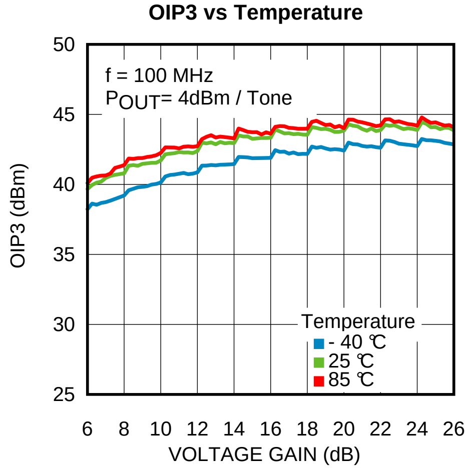


Figure 8.

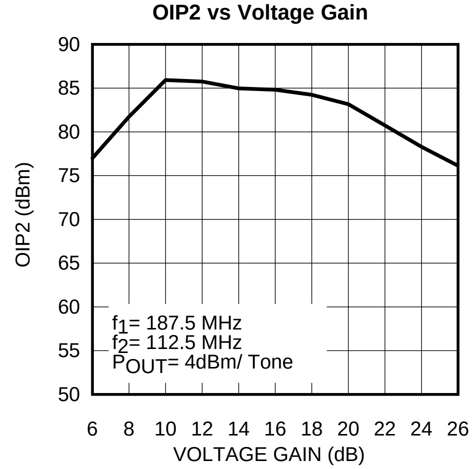


Figure 9.

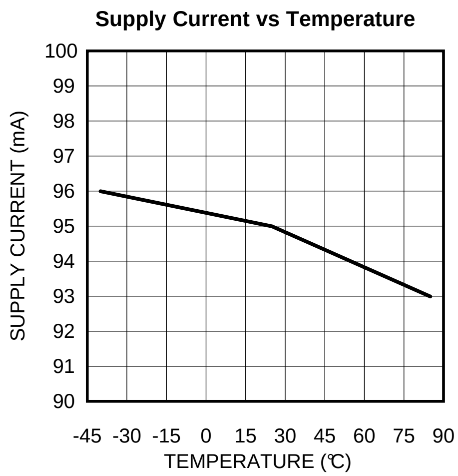
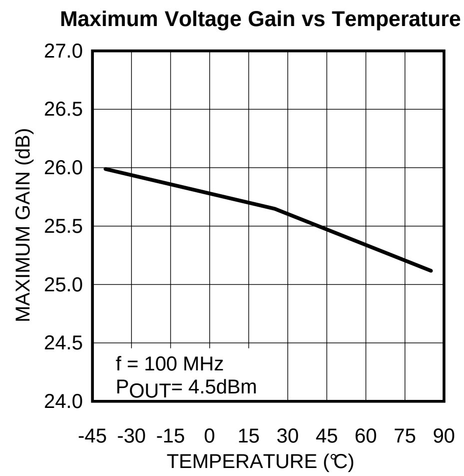


Figure 10.



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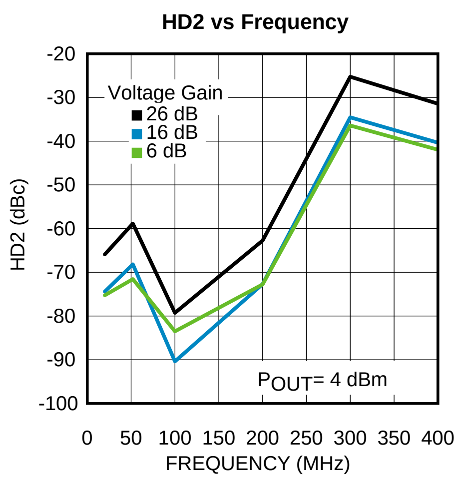

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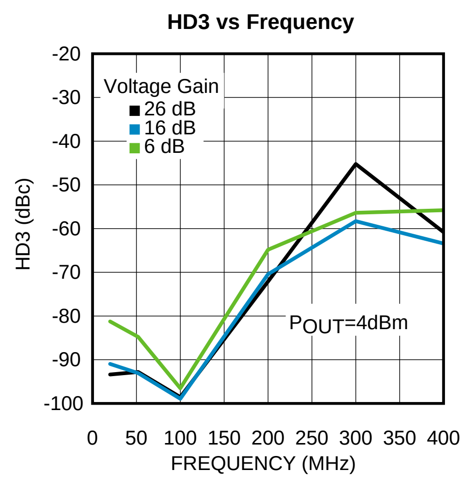

Figure 13.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

HD2 & HD3 vs Voltage Gain

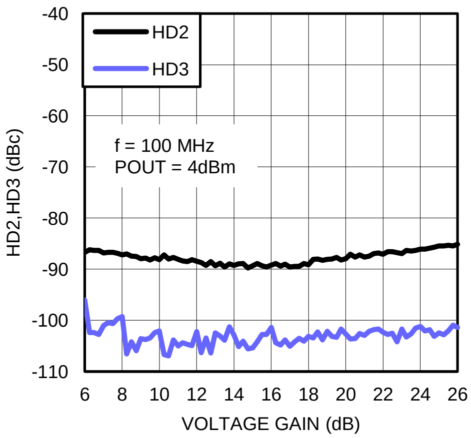

Figure 14.

HD2 vs Output Power

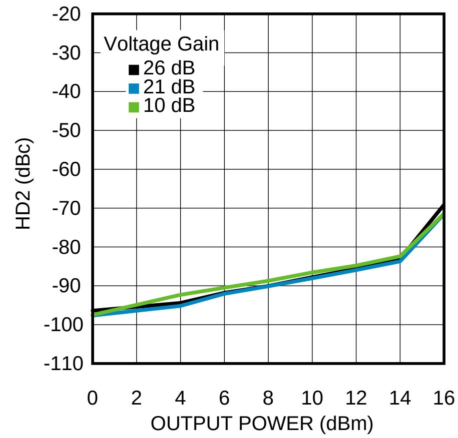

Figure 15.

HD3 vs Output Power

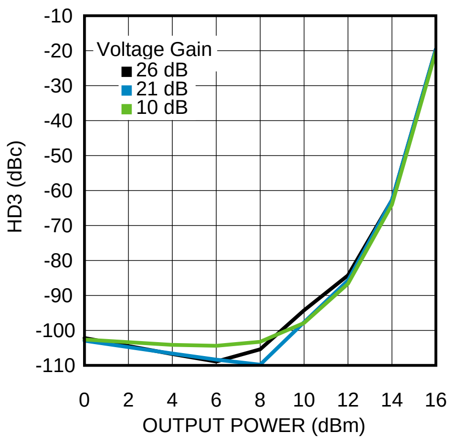

Figure 16.

Output Power vs Input Power

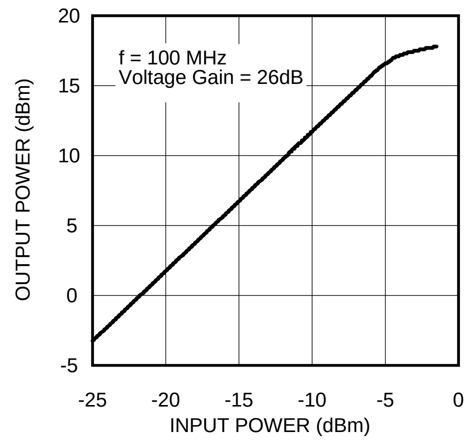

Figure 17.

Gain Step Amplitude Error

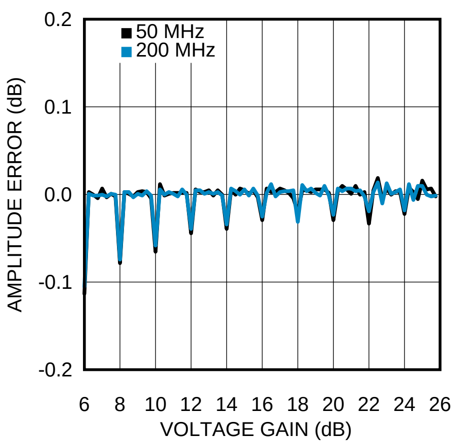

Figure 18.

Gain Step Phase Error

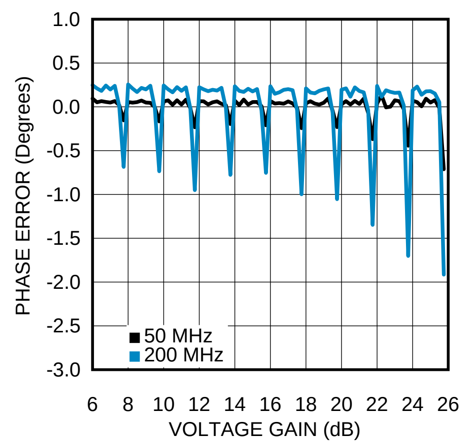

Figure 19.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

Cumulative Amplitude Error

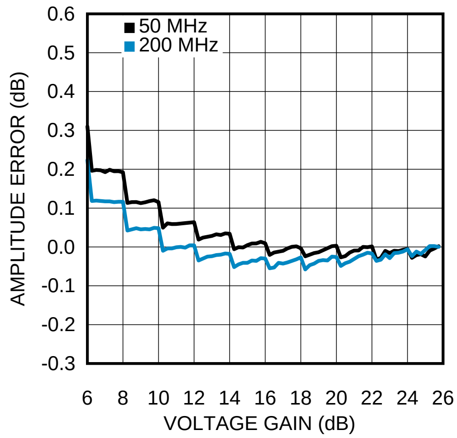

Figure 20.

Cumulative Phase Error

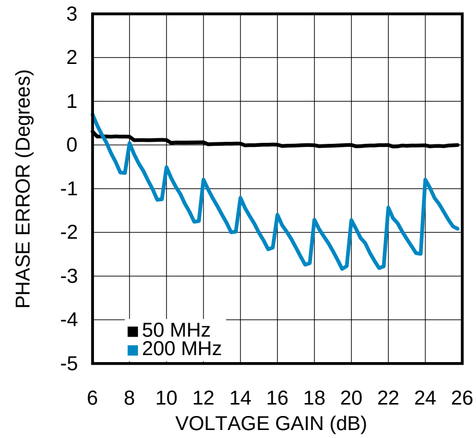

Figure 21.

Noise Figure vs Voltage Gain

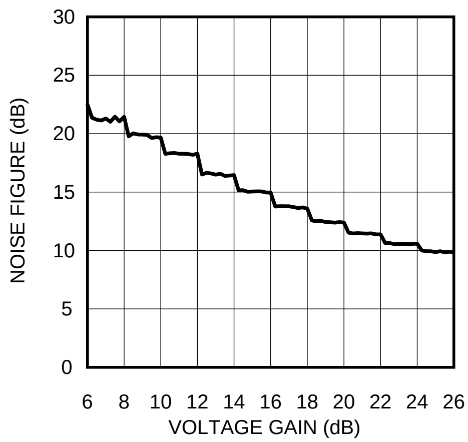

Figure 22.

Noise Figure vs Frequency

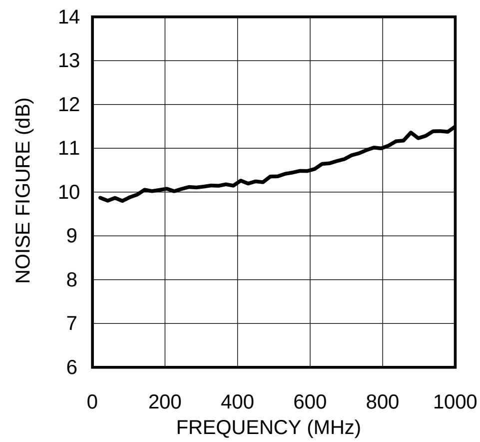

Figure 23.

Channel Enable Control Timing Behavior

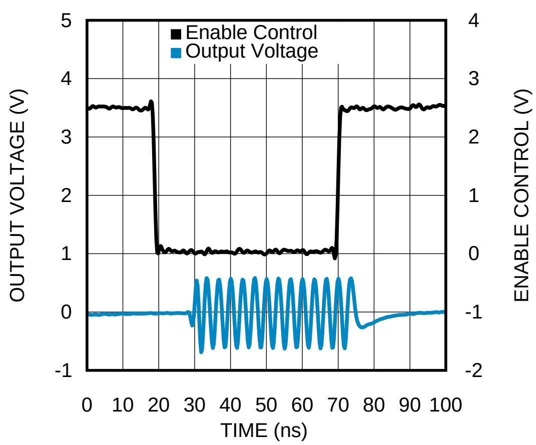

Figure 24.

16dB Gain Control Timing Behavior

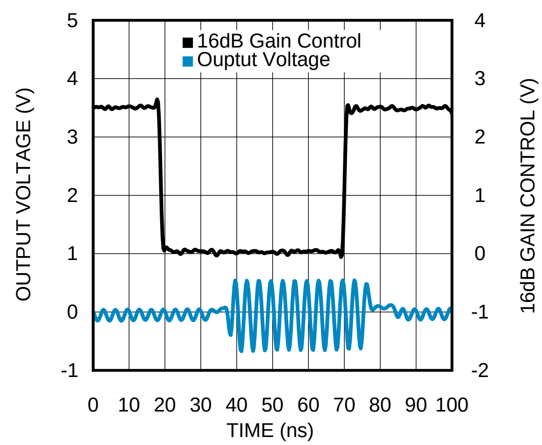

Figure 25.

Typical Performance Characteristics (continued)

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

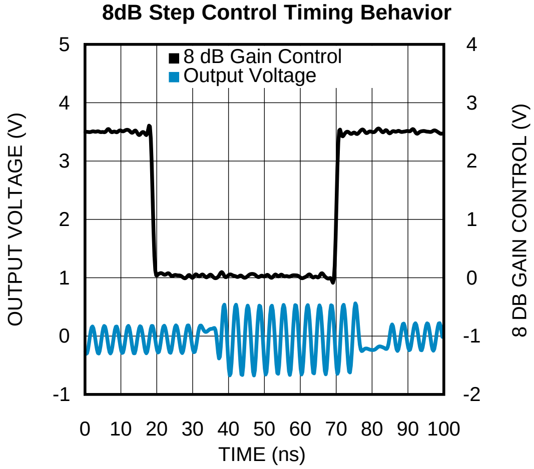

Figure 26.

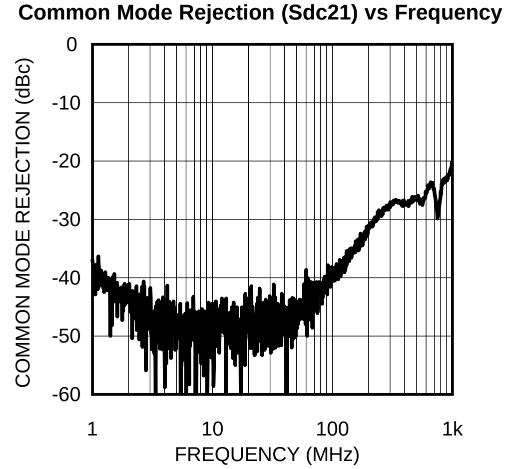

Figure 27.

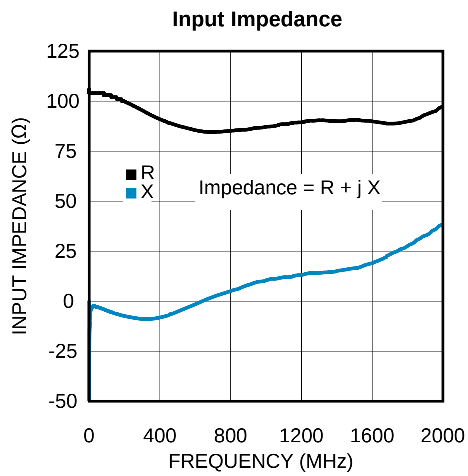

Figure 28.

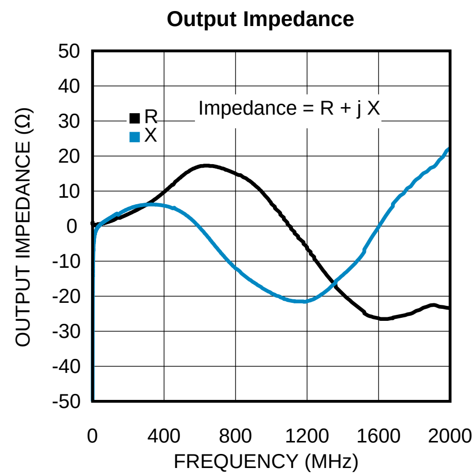

Figure 29.

Typical Performance Characteristics, Single-Ended Input

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain.)

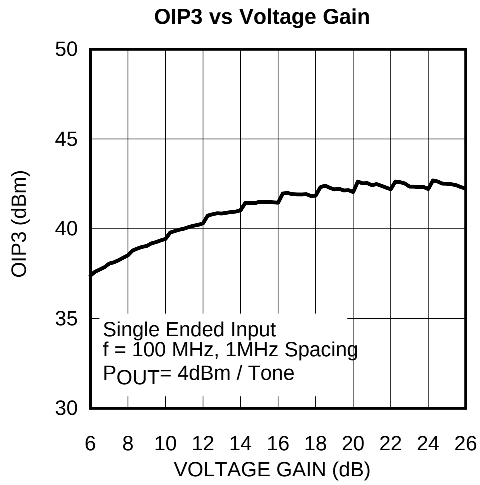

Figure 30.

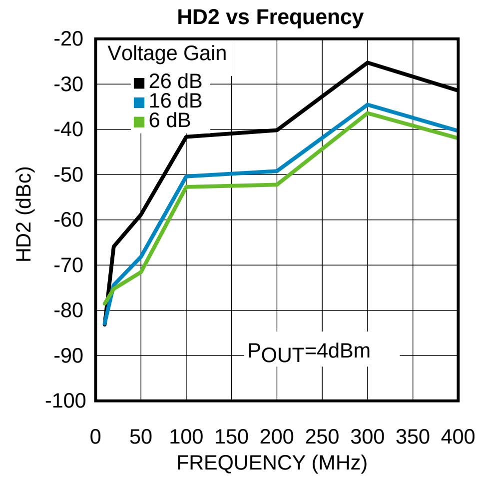

Figure 31.

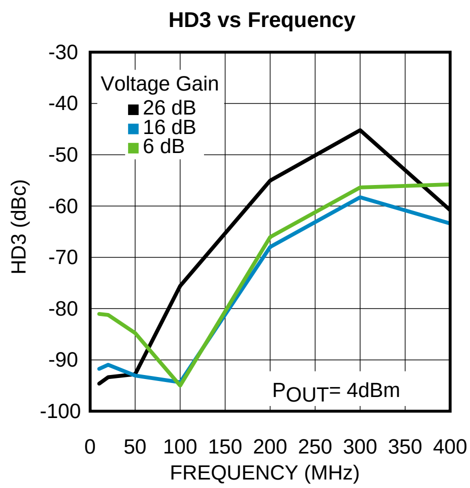

Figure 32.

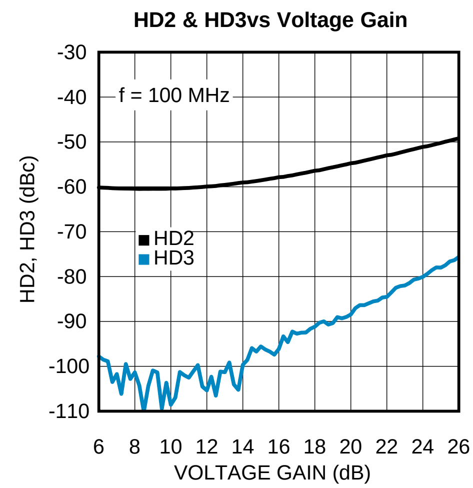

Figure 33.

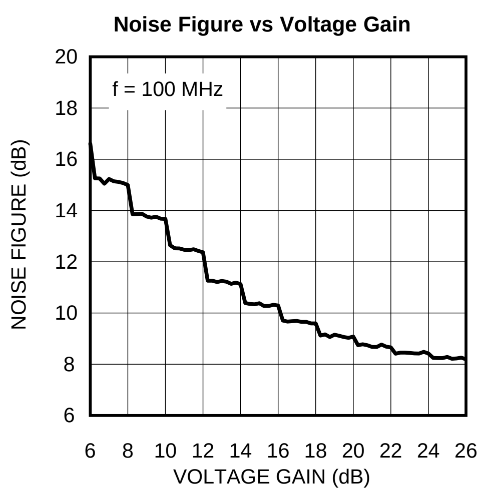

Figure 34.

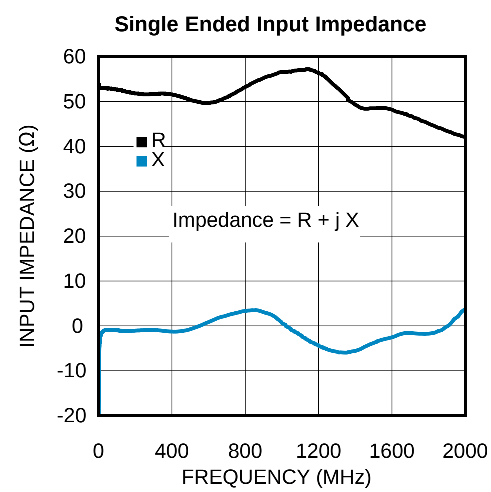

Figure 35.

APPLICATION INFORMATION

INTRODUCTION

The LMH6881 has been designed to replace traditional, fixed-gain amplifiers, as well as variable-gain amplifiers, with an easy-to-use device which can be flexibly configured to many different gain settings while maintaining excellent performance over the entire gain range. Many systems can benefit from this programmable-gain, DC-capable, differential amplifier. Last-minute design changes can be implemented immediately, and external resistors are not required to set the gain.

Gain control is enabled with a parallel or a serial-control interface, and as a result, the amplifier can also serve as a digitally controlled variable-gain amplifier (DVGA) for automatic gain-control applications. Figure 36 and Figure 37 show typical implementations of the amplifier.

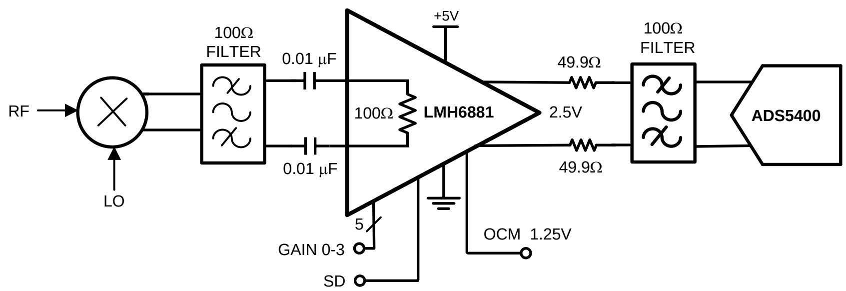

Figure 36. LMH6881 Typical Application

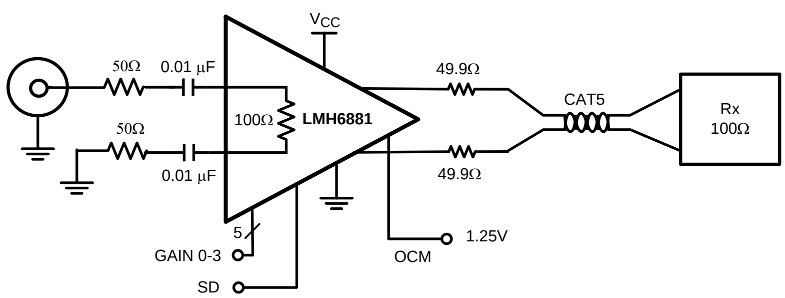

Figure 37. LMH6881 Used as Twisted Pair Cable Driver

This application section will cover the use and function of the amplifier, common applications, detailed instructions on digital control and power supply as well as thermal and board layout recommendations.

BASIC CIRCUIT DESCRIPTION

The LMH6881 has three functional stages, a low-noise amplifier, followed by a digital attenuator, and a low-distortion, low-impedance output amplifier. The amplifier has four signal-input pins, to accommodate both differential signals and single-ended signals. The amplifier has an OCM pin used to set the output common mode voltage. There is a gain of 2 on this pin so that 1.25 V applied on that pin will place the output common mode at 2.5 V.

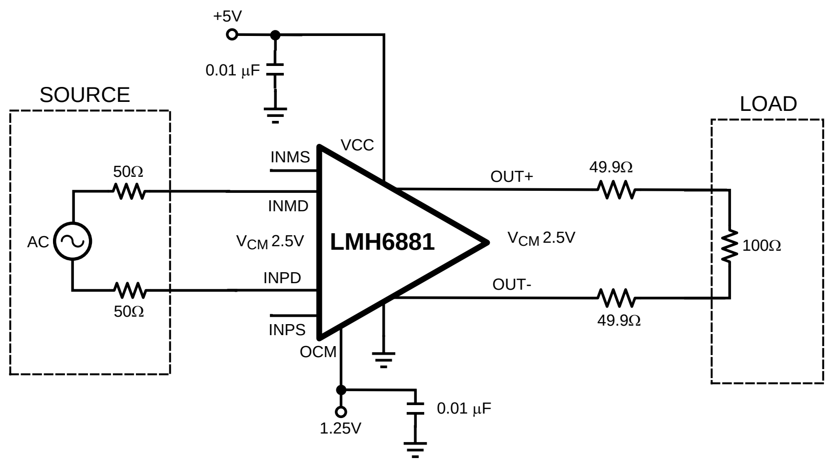

Figure 38. Typical Implementation with a Differential Input Signal

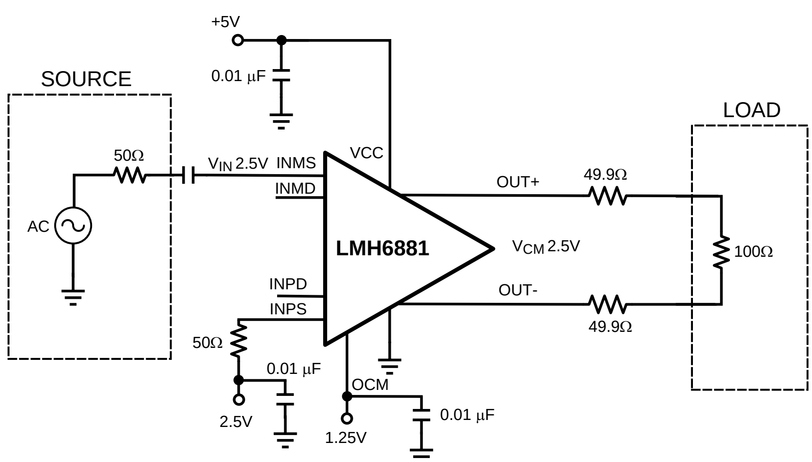

Figure 39. Typical Implementation with a Single-Ended Input Signal

INPUT CHARACTERISTICS

The LMH6881 has internally terminated inputs. The INMD and INPD pins are intended to be the differential input pins and have an internal 100-Ω resistive termination. An example differential circuit is shown in Figure 38. When using the differential inputs, the single-ended inputs should be left disconnected.

The INMS and INPS pins are intended to be used for single ended inputs and have been designed to support single ended termination of 50 Ω working as an active termination. For single-ended signals an external 50-Ω resistor is required as shown in Figure 39. When using the single-ended inputs, the differential inputs should be left disconnected.

All of the input pins are self biased to 2.5 V. When using the LMH6881 for DC-coupled applications it is possible to externally bias the input pins to voltages from 1.5 V to 3.5 V. Performance is best at the 2.5-V level specified. Performance will degrade slightly as the common mode shifts away from 2.5 V.

The first stage of the LMH6881 is a low-noise amplifier that can accommodate a maximum input signal of 2 V_{ppd} on the differential input pins and 1 V_{pp} on either of the single-ended pins. Signals larger than this will cause severe distortion. Although the inputs are protected against ESD, sustained electrical overstress will damage the part. Signal power over 13 dBm should not be applied to the amplifier differential inputs continuously. On the single-ended pins the power limit is 10 dBm for each pin.

OUTPUT CHARACTERISTICS

The LMH6881 has a low-impedance output very similar to a traditional Op-amp output. This means that a wide range of loads can be driven with good performance. Matching load impedance for proper termination of filters is as easy as inserting the proper value of resistor between the filter and the amplifier (See Figure 36 for example.) This flexibility makes system design and gain calculations very easy. By using a differential output stage the LMH6881 can achieve large voltage swings on a single 5-V supply. This is illustrated in Figure 40. This figure shows how a voltage swing of 4 V_{PPD} is realized while only swinging 2 V_{PP} on each output. A 1-V_P signal on one branch corresponds to 2 V_{PP} on that branch and 4 V_{PPD} when looking at both branches (positive and negative).

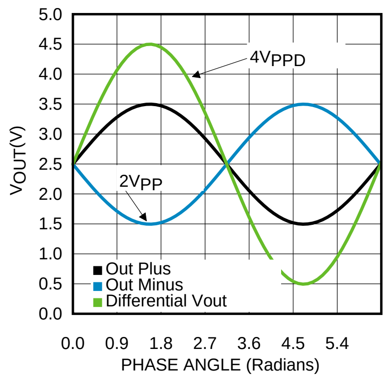

Figure 40. Differential Output Voltage

The LMH6881 has been designed for both AC-coupled and DC-coupled applications. To give more flexibility in DC-coupled applications, the common mode voltage of the output pins is set by the OCM pin. The OCM pin needs to be driven from an external low-noise source. If the OCM pin is left floating, the output common mode is undefined, and the amplifier will not operate properly.

There is a DC gain of 2 between the OCM pin and the output pins so that the OCM voltage should be between 1 V and 1.5 V. This will set the output common mode voltage between 2 V and 3 V. Output common mode voltages outside the recommended range will exhibit poor voltage swing and distortion performance. The amplifier will give optimum performance when the output common mode is set to half of the supply voltage (2.5 V or 1.25 V at the OCM pin).

The ability of the LMH6881 to drive low-impedance loads while maintaining excellent OIP3 performance creates an opportunity to greatly increase power gain and drive low-impedance filters. This gives the system designer much needed flexibility in filter design. In many cases using a lower impedance filter will provide better component values for the filter. Another benefit of low-impedance filters is that they are less likely to be influenced by circuit board parasitic reactances such as pad capacitance or trace inductance. The output stage is a low-impedance voltage amplifier, so voltage gain is constant over different load conditions. Power gain will change based on load conditions. See Figure 41 for details on power gain with respect to different load conditions. The graph was prepared for the 26-dB voltage gain. Other gain settings will behave similarly.

All measurements in this data sheet, unless specified otherwise, refer to voltage or power at the device output pins. For instance, in an OIP3 measurement the power out will be equal to the output voltage at the device pins squared, divided by the total load voltage. In back terminated applications, power to the load would be 3 dB less. Common back terminated applications include driving a matched filter or driving a transmission line.

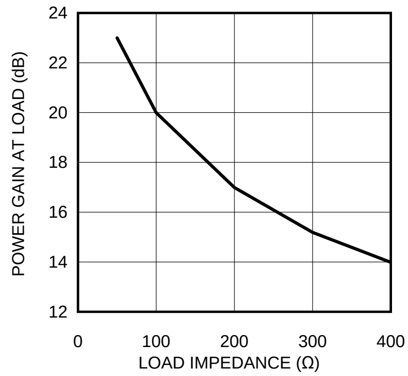

Figure 41. Power Gain as a Function of the Load

Printed circuit board (PCB) design is critical to high-frequency performance. In order to ensure output stability the load-matching resistors should be placed as close to the amplifier output pins as possible. This allows the matching resistors to mask the board parasitics from the amplifier output circuit. An example of this is shown in Figure 36. Also note that the low-pass filters in Figure 43 and Figure 44 use center-tapped capacitors. Having capacitors to ground provides a path for high-frequency, common-mode energy to dissipate. This is equally valuable for the ADC, so there are also capacitors to ground on the ADC side of the filter. The LMH6881EVAL evaluation board is available to serve as a guide for system board layout. See also application note AN-2235 for more details.

INTERFACING TO AN ADC

The LMH6881 is an excellent choice for driving high-speed ADCs such as the ADC12D1800RF, ADC12D1600RF or the ADS5400. The following sections will detail several elements of ADC system design, including noise filters, AC-, and DC-coupling options.

ADC NOISE FILTER

When connecting a broadband amplifier to an analog-to-digital converter, it is nearly always necessary to filter the signal before sampling it with the ADC. Figure 42 shows a schematic of a second order Butterworth filter, and Table 1 shows component values for some common IF frequencies. These filters offer a good compromise between bandwidth, noise rejection and cost. This filter topology is the same as is used on the ADC14V155KDRB High IF Receiver reference design board. This filter topology is adequate for reducing aliasing of broadband noise and will also provide rejection of harmonic distortion and many of the images that are commonly created by mixers.

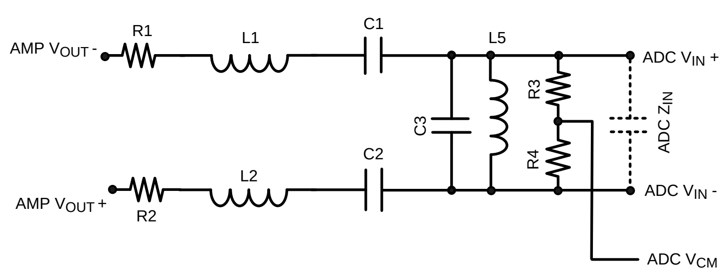

Figure 42. ADC Noise Filter Schematic

Table 1. Filter Component Values(1)

Center Frequency	75 MHz	150 MHz	180 MHz	250 MHz
Bandwidth	40 MHz	60 MHz	75 MHz	100 MHz
R1, R2	90 Ω	90 Ω	90 Ω	90 Ω
L1, L2	390 nH	370 nH	300 nH	225 nH
C1, C2	10 pF	3 pF	2.7 pF	1.9 pF
C3	22 pF	19 pF	15 pF	11 pF
L5	220 nH	62 nH	54 nH	36 nH
R3, R4	100 Ω	100 Ω	100 Ω	100 Ω

(1) Resistor values are approximate, but have been reduced due to the internal 10 Ω of output resistance per pin.

AC COUPLING TO ADC

AC coupling is an effective method for interfacing to an ADC for many communications systems. In many applications this will be the best choice. The LMH6881 evaluation board is configured for AC coupling as shipped from the factory. Coupling with capacitors is usually the most cost effective method. Transformers can provide both AC coupling and impedance transformation as well as single ended to differential conversion. One of the key benefits to AC coupling is that each stage of the system can be biased to the ideal DC operating point. Many systems operate with lower overall power dissipation when DC bias currents are eliminated between stages.

DC COUPLING TO ADC

The LMH6881 supports DC-coupled signals. In order to successfully implement a DC-coupled signal chain the common-mode voltage requirements of every stage need to be met. This will require careful planning, and in some cases there will be signal level, gain or termination compromises required to meet the requirements of every part. Shown in Figure 43 and Figure 44 is a method using resistors to change the 2.5-V common mode of the amplifier output to a common mode compatible for the input of a low-input-voltage ADC such as the ADC12D1800RF. This DC level shift is achieved while maintaining an AC impedance match with the filter in Figure 43, while in Figure 44 there is a small mismatch between the amplifier termination resistors and the ADC input. Since there is no universal ADC input common mode and some ADC's have impedance controlled input, each design will require a different resistor ratio. For high-speed data conversion systems it is very important to keep the physical distance between the amplifier and the ADC electrically short. When connections between the amplifier and the ADC are electrically short, termination mismatches are not critical.

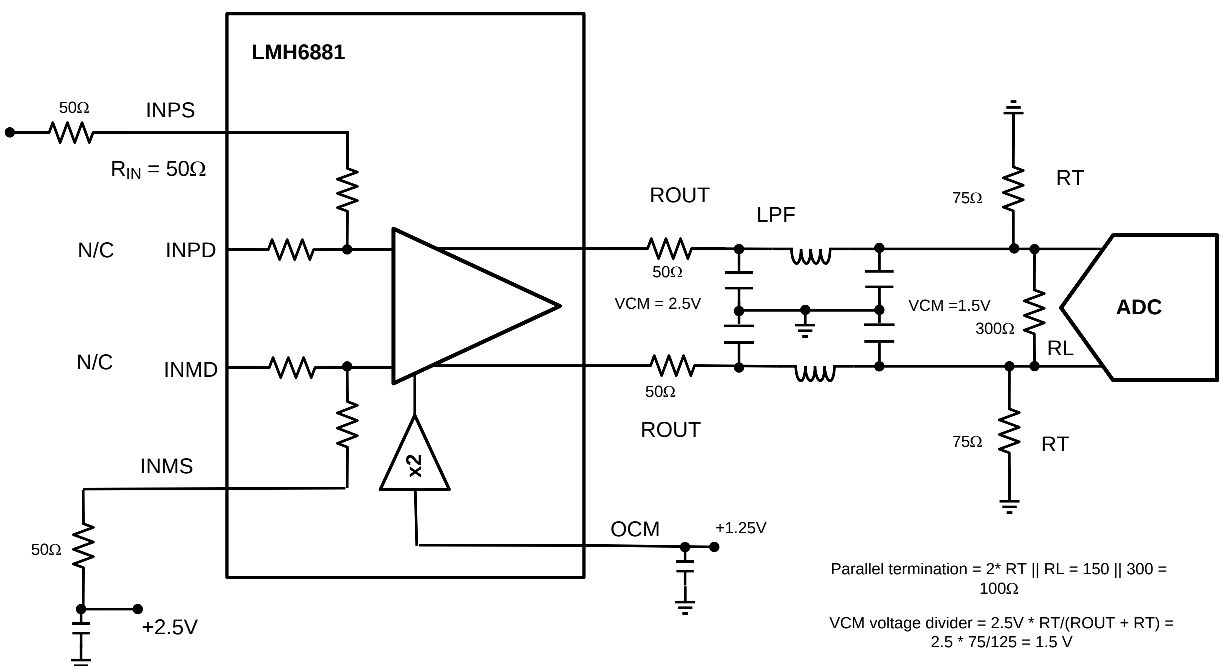

Figure 43. DC-Coupled ADC Driver Example 1, High Input Impedance ADC

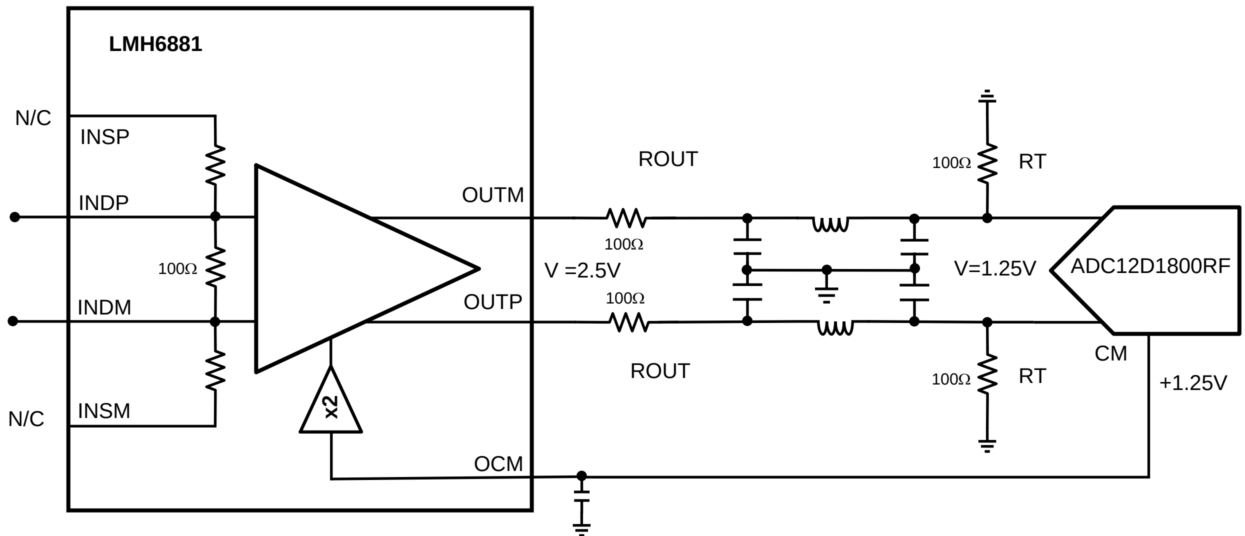

Figure 44. DC-Coupled ADC Driver Example 2, Terminated Input ADC

DIGITAL CONTROL OF THE GAIN AND POWER-DOWN PINS

The LMH6881 will support two modes of control for its gain: a parallel mode and a serial mode (SPI compatible). Parallel mode is fastest and requires the most board space for logic line routing. Serial mode is compatible with existing SPI-compatible systems. The device has gain settings covering a range of 20 dB. In parallel mode, only 2-dB steps are available. The serial interface should be used for finer gain control of 0.25 dB for a gain between 6 dB and 26 dB of voltage gain. If fixed gain is desired the pins can be strapped to ground or VCC, as required. The device has a shutdown pin to enable power savings when the amplifier is not being used.

The LMH6881 was designed to interface with 2.5-V to 5-V CMOS logic circuits. If operation with 5-V logic is required care should be taken to avoid signal transients exceeding the amplifier supply voltage. Long, unterminated digital signal traces should be avoided. Signal voltages on the logic pins that exceed the device power supply voltage may trigger ESD protection circuits and cause unreliable operation. Some digital input-output pins have different functions depending on the digital control mode. Table 2 shows the mapping of the digital pins. These functions for each pin will be described in the sections PARALLEL INTERFACE and SPI-COMPATIBLE SERIAL INTERFACE.

Table 2. Pins with Dual Functions

Pin	SPI = 0	SPI = 1
3	D1	SDI
4	D0	SDO(1)
15	D2	CLK
16	D3	CS (active low)

(1) Pin 4 requires external bias. See SPI-COMPATIBLE SERIAL INTERFACE section for Details.

PARALLEL INTERFACE

Parallel mode offers the fastest gain update capability with the drawback of requiring the most board space dedicated to control lines. To place the LMH6881 into parallel mode the SPI pin (pin 5) is set to the logical zero state. Alternately the SPI pin can be connected directly to ground. The SPI pin has a weak internal resistor to ground. If left unconnected, the amplifier will operate in parallel mode.

In parallel mode the gain can be changed in 2-dB steps with a 4-bit gain control bus. The attenuator control pins are internally biased to logic high state with weak pull-up resistors, with the exception of D0 which is biased low due to the shared SDO function. If the control bus is left unconnected, the amplifier gain will be set to 6 dB. Table 3 shows the gain of the amplifier when controlled in parallel mode.

Table 3. Amplifier Gain for All Control Pin Combinations

Control pins logical level in parallel mode					
D3	**D2**	**D1**	**D0**	**Decimal value**	**Amplifier voltage gain [dB]**
1	X	1	X	10 - 15	6
1	0	0	1	9	8
1	0	0	0	8	10
0	1	1	1	7	12
0	1	1	0	6	14
0	1	0	1	5	16
0	1	0	0	4	18
0	0	1	1	3	20
0	0	1	0	2	22
0	0	0	1	1	24
0	0	0	0	0	26

For fixed-gain applications the attenuator-control pins should be connected to the desired logic state instead of relying on the weak internal bias. Data from the gain-control pins directly drive the amplifier gain circuits. To minimize gain change glitches all gain pins should be driven with minimal skew. If gain-pin timing is uncertain, undesirable transients can be avoided by using the shutdown pin to disable the amplifier while the gain is changed. Gain glitches are most likely to occur when multiple bits change value for a small gain change, such as the gain change from 10 dB to 12 dB which requires changing all 4 gain-control pins.

A shutdown pin (SD == 0, amplifier on, SD == 1, amplifier off) is provided to reduce power consumption by disabling the highest power portions of the amplifier. The digital control circuit is not shut down and will preserve the last active gain setting during the disabled state. See the Typical Performance Characteristics section for disable and enable timing information. The SD pin is functional in parallel mode only and disabled in serial mode.

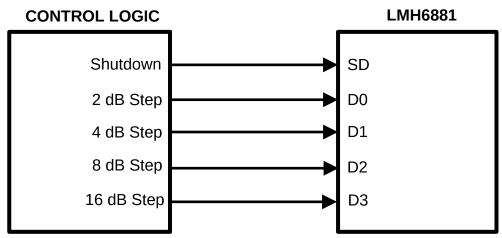

Figure 45. Parallel Mode Connection

SPI-COMPATIBLE SERIAL INTERFACE

The serial interface allows a great deal of flexibility in gain programming and reduced board complexity. The LMH6881 serial interface is a generic 4-wire synchronous interface that is compatible with SPI-type interfaces that are used on many microcontrollers and DSP controllers. Using only 4 wires, the SPI mode offers access to the 0.25-dB gain steps of the amplifier.

For systems where gain is changed only infrequently, or where only slower gain changes are required, serial mode is the best choice. To place the LMH6881 into serial mode the SPI pin (Pin 5) should be put into the logic high state. Alternatively the SPI pin can be connected directly to the 5-V supply bus. In this configuration the pins function as shown in Table 2. The SPI interface uses the following signals: clock input (CLK), serial data in (SDI), serial data out (SDO), and serial chip select (CS). The chip select pin is active low meaning the device is selected when the pin is low.

The SD pin is inactive in the serial mode. This pin can be left disconnected for serial mode. The SPI interface has the ability to shut down the amplifier without using the SD pin.

The CLK pin is the serial clock pin. It is used to register the input data that is presented on the SDI pin on the rising edge and to source the output data on the SDO pin on the falling edge. The user may disable clock and hold it in the low state, as long as the clock pulse-width minimum specification is not violated when the clock is enabled or disabled. The clock pulse-width minimum is equal to one setup plus one hold time, or 6 ns.

The CS pin is the chip select pin. This pin is active low; the chip is selected in the logic low state. Each assertion starts a new register access - i.e., the SDATA field protocol is required. The user is required to de-assert this signal after the 16th clock. If the CS pin is de-asserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the de-asserted pulse - which is specified in the Electrical Specifications section.

The SDI pin is the input pin for the serial data. Each write cycle is 16-bits long.

The SDO pin is the data output pin. This output is normally at a high impedance state, and is driven only when CS is asserted. Upon CS assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. The SDO pin is a current output and requires external bias resistor to develop the correct logic voltage. See Figure 47 for details on sizing the external bias resistor. Resistor values of 180 Ω to 400 Ω are recommended. The SDO pin can source 10 mA in the logic high state. With a bias resistor of 250 Ω the logic 1 voltage would be 2.5 V. In the logic 0 state, the SDO output is off and no current flows, so the bias resistor will pull the voltage to 0 V.

Each serial interface write access cycle is exactly 16 bits long as shown in Figure 46.

The external bias resistor means that in the high-impedance state the SDO pin impedance is equal to the external bias resistor value. If bussing multiple SPI devices make sure that the SDO pins of the other devices can drive the bias resistor.

The serial interface has 4 registers with address [0] to address [3]. Table 4 shows the content of each SPI register. Registers 0 and 1 are read only. Registers 2 and three are read/write and control the gain and power of the amplifier. Table 5 shows the data format of register 2 and Table 6 shows the data format of register 3.

Table 4. SPI Registers

Address	Read/Write	Name	Description	Default value [Hex]
0	R	Revision ID	Revision of the product	1 (first revision)
1	R	Product ID	Identification of the product	20
2	R/W	Power down	Power up/down of the amplifier	0
3	R/W	Attenuation	Attenuation control	50

Table 5. Register 2 Definition

7	6	5	4	3	2	1	0
Reserved					OFF = 1,1: ON = 0,0		Reserved

Table 6. Register 3 Definition

7	6	5	4	3	2	1	0
Reserved	16dB	8dB	4dB	2dB	1dB	0.5dB	0.25dB
	Gain [dB] = 26- (Register3 * 0.25); valid range is 0 to 80 in decimal.						

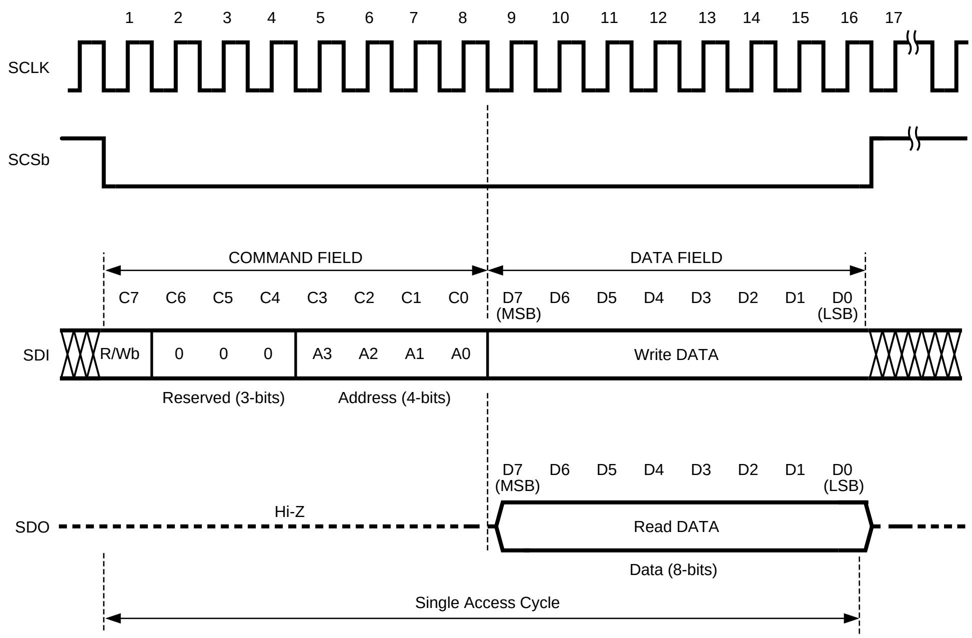

Figure 46. Serial Interface Protocol (SPI Compatible)

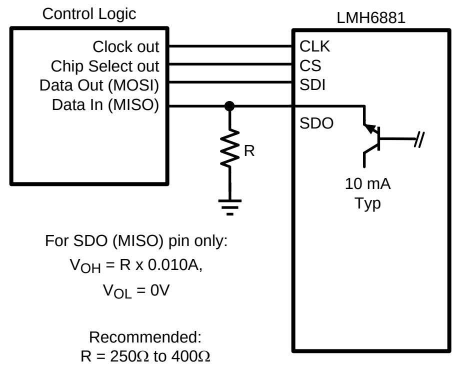

Figure 47. Internal Operation of the SDO pin

FIGURE OF MERIT: DYNAMIC RANGE FIGURE

The dynamic range figure (DRF) as illustrated in Figure 5, is defined as the input third order intercept point (IIP3) minus the noise figure (NF). The combination of noise figure and linearity gives a good proxy for the total dynamic range of an amplifier. In some ways this figure is similar to the SFDR of an analog-to-digital converter. In contrast to an ADC, though, an amplifier will not have a full-scale input to use as a reference point. With amplifiers, there is no one point where signal amplitude hits “full scale”. Yet, there are real limitations to how large of a signal the amplifier can handle. Normally, the distortion products produced by the amplifier will determine the upper limit to signal amplitude. The intermodulation intercept point is an imaginary point that gives a well understood figure of merit for the maximum signal an amplifier can handle. For low-amplitude signals the noise figure gives a threshold of the lowest signal that the amplifier can reproduce. By combining the third-order input intercepts point and the noise figure the DRF gives a very good indication of the available dynamic range offered.

POWER SUPPLY CONSIDERATIONS

The LMH6881 was designed to be operated on 5-V power supplies. The voltage range for VCC is 4.75 V to 5.25 V. Power-supply accuracy of 5% or better is advised. When operated on a board with high-speed digital signals it is important to provide isolation between digital signal noise and the analog input pins. The SP16160CH1RB reference board provides an example of good board layout.

The power supply pins are 19, 20, 23 and 24. Each supply pin should be decoupled with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF as close to the device as possible. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems two capacitors per supply pin are advised.

To avoid undesirable signal transients the LMH6881 should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

THERMAL CONSIDERATION

The LMH6881 is packaged in a thermally enhanced package. The exposed pad on the bottom of the package is the primary means of removing heat from the package. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. In any case, the thermal dissipation of the device is largely dependent on the attachment of the exposed pad to the system PCB. The exposed pad should be attached to as much copper on the PCB as possible, preferably external layers of copper. It is also very important to maintain good high-speed layout practices when designing a system board. Please refer to the LMH6881 evaluation board for suggested layout techniques. The LMH6881EVAL evaluation board was designed for both signal integrity and thermal dissipation. The LMH6881EVAL evaluation board uses higher performance dielectric (Rogers) on the top layer for high frequency signal fidelity.

CONCLUSION

The LMH6881 is a fully differential amplifier optimized for signal-path applications up to 1000 MHz. The LMH6881 has a 100-Ω input impedance and a low (less than 0.5 Ω) impedance output. The gain is digitally controlled over a 20-dB range from 26 dB to 6 dB. The LMH6881 is designed to replace fixed-gain differential amplifiers with a single, flexible-gain device. It has been designed to provide good noise figure and OIP3 over the entire gain range. This design feature is highlighted by the DRF of merit. Traditional variable gain amplifiers generally have the best OIP3 and NF performance at maximum gain only.

Table 7. COMPATIBLE HIGH SPEED ANALOG-TO-DIGITAL CONVERTERS

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC12D1800RF	1800	12	DUAL
ADC12D1600RF	1600	12	DUAL
12D1000 RF	1000	12	DUAL
ADC12D800RF	800	12	DUAL
ADS5400	1000	12	SINGLE
ADC12C105	105	12	SINGLE
ADC10D1500	1500	10	DUAL
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC16V130	130	16	SINGLE
ADC16DV160	160	16	DUAL
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6881SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples
LMH6881SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples
LMH6881SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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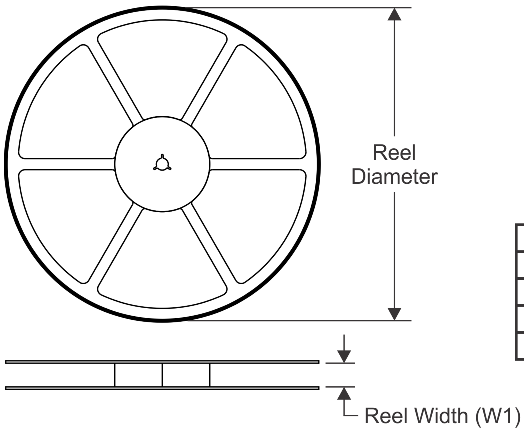
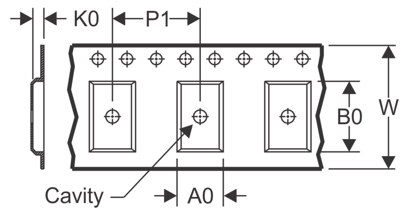
TAPE AND REEL INFORMATION

REEL DIMENSIONS

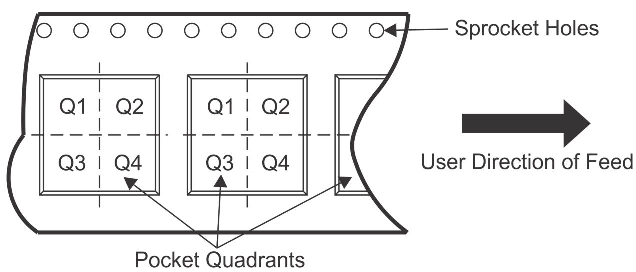


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

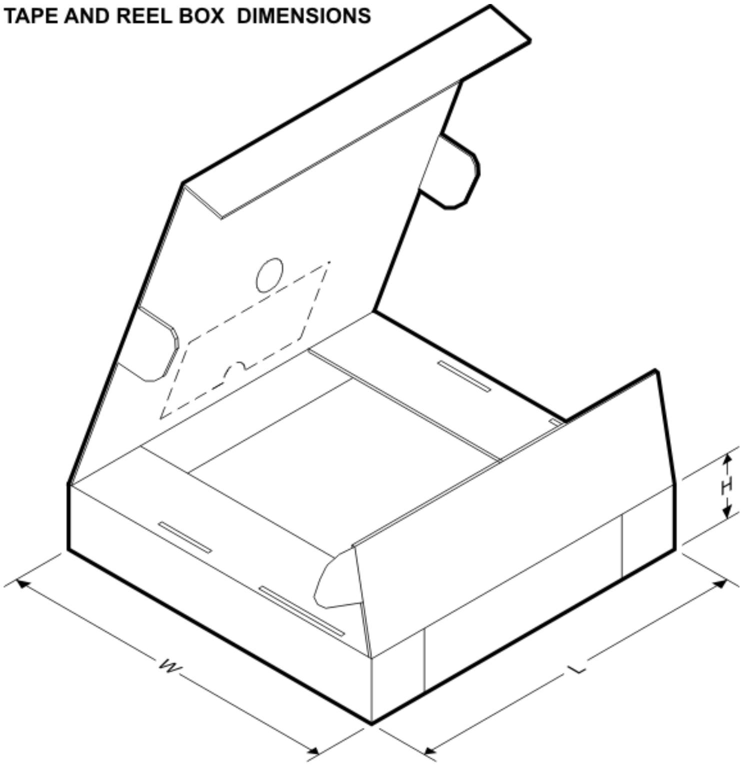
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6881SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6881SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6881SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

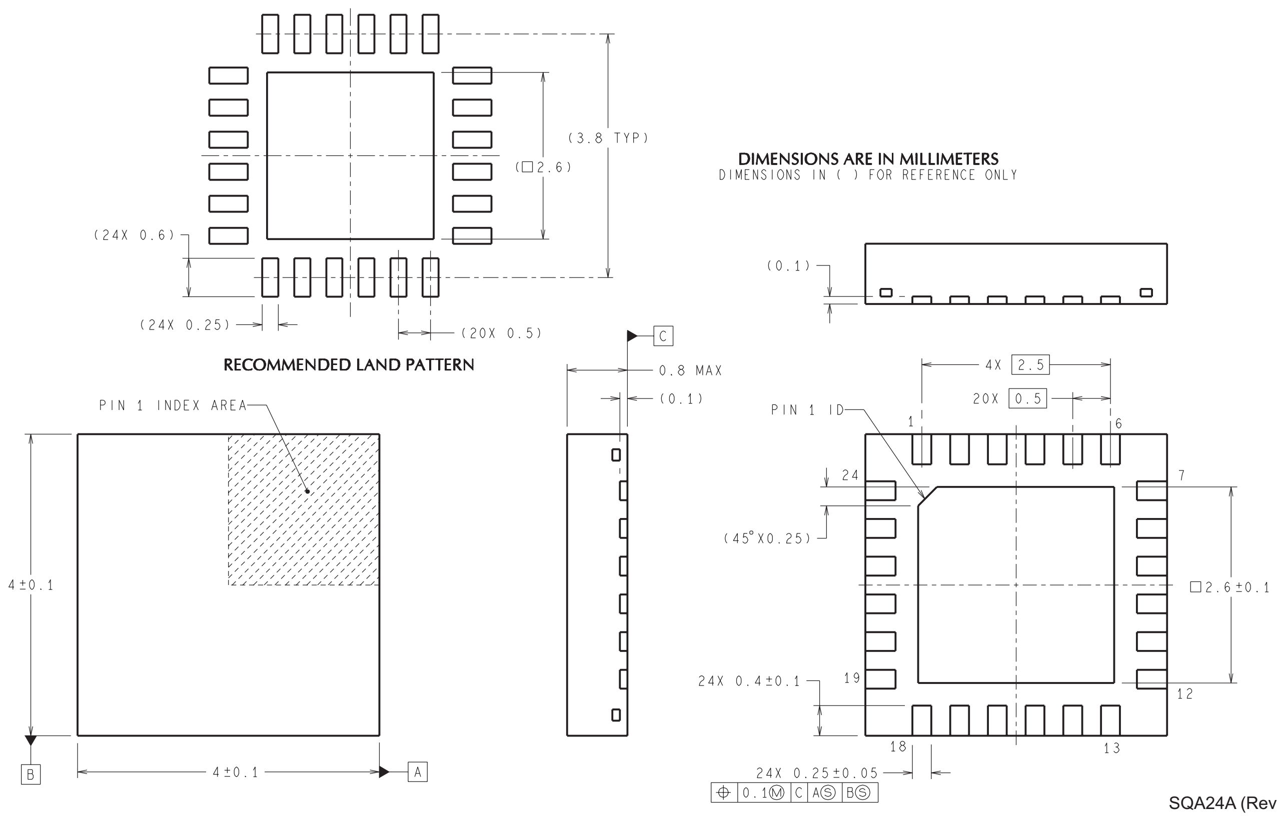
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6881SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LMH6881SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LMH6881SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

RTW0024A



SQA24A (Rev B)

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