High Common Mode, Gain of 14, Precision Voltage Difference Amplifier

Check for Samples: LMP8277

FEATURES

- **Typical Values, T_A = 25°C**
- **Input Offset Voltage ±2 mV Max**
- **TCVos ±30 µV/°C Max**
- **CMRR 80 dB Min**
- **Output Voltage Swing Rail-to-Rail**
- **Bandwidth 80 kHz**
- **Operating Temperature Range (Ambient) −40°C to 125°C**
- **Supply Voltage 4.75V to 5.5V**
- **Supply Current 1 mA**

APPLICATIONS

- **Fuel Injection Control**
- **High and Low Side Driver Configuration Current Sensing**
- **Power Management Systems**

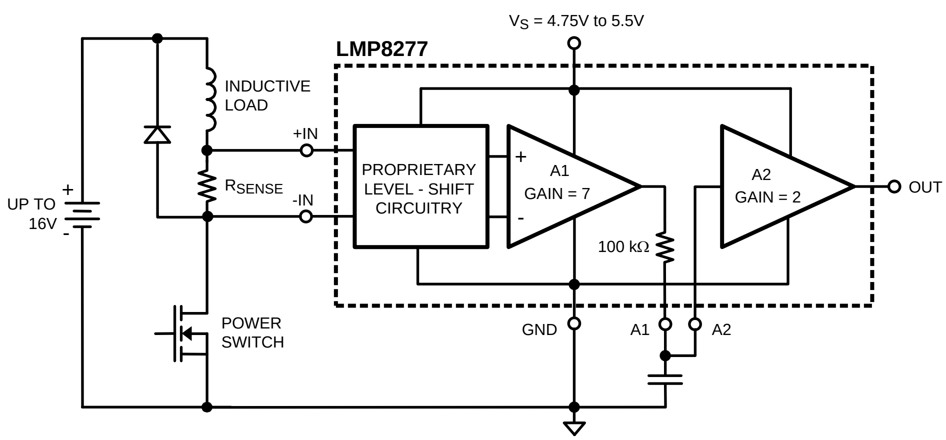
DESCRIPTION

The LMP8277 is a fixed gain differential amplifier with a −2V to 16V input common mode voltage range and a supply voltage range of 4.75V to 5.5V. The LMP8277 is part of the LMP™ precision amplifier family which will detect, amplify and filter small differential signals in the presence of high common mode voltages. The gain is fixed at 14 and is adequate to drive an ADC to full scale in most cases. This fixed gain is achieved in two separate stages, a preamplifier with gain of +7 and a second stage amplifier with a gain of +2. The internal signal path between these two stages is brought out on two pins that provide a connection for a filter network.

The LMP8277 will function over an extended common mode input voltage range making the device suitable for applications with load dump events such as automotive systems.

Typical Application

Figure 1. Low Side Current Sensing



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)]

ESD Tolerance[(2)]	Human Body Model	For input pins only	±4000V
		For All other pins	±2000V
	Machine Model		200V
Supply Voltage (V_S – GND)			5.75V
Common Mode Voltage on +IN and −IN		Transient (400 ms)	−7V to 45V
Storage Temperature Range			−65°C to +150°C
Junction Temperature[(3)]			+150°C max
Soldering Information		Infrared or Convection (20 sec)	235°C
		Wave Soldering Lead Temp. (10 sec)	260°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(2) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings[(1)]

Temperature Range		
Packaged Devices[(2)]		−40°C to +125°C
Supply Voltage (V_S – GND)		4.75V to 5.5V
Package Thermal Resistance (θ_{JA}[(2)])	8-Pin SOIC	190°C/W
	8-Pin VSSOP	235°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_S = 5V, GND = 0, −2V ≤ V_{CM} ≤ 16V, R_L = Open. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min	Typ (2)	Max	Units
V_{OS}	Input Offset Voltage	V_{CM} = V_S/2			±0.25	±2.0	mV
TC V_{OS}	Input Offset Voltage Drift	V_{CM} = V_S/2	25°C ≤ T_A ≤ 125°C		±20	**±30**	μV/°C
			−40°C ≤ T_A ≤ 25°C		±20	**±35**	
A2 I_B	Input Bias Current of A2	See (3)			−20		pA
						±20	nA
I_S	Supply Current				1.0	1.2 **1.4**	mA
R_{CM}	Input Impedance Common Mode			**160**	200	**240**	kΩ
R_{DM}	Input Impedance Differential Mode			**320**	400	**480**	kΩ
CMVR	Input Common-Mode Voltage Range			**–2**		**+16**	V
DC CMRR	DC Common Mode Rejection Ratio	0°C ≤ T_A ≤ 125°C	−2V ≤ V_{CM} ≤ 16V	**80**	97		dB
		−40°C ≤ T_A ≤ 0°C	−2V ≤ V_{CM} ≤ 16V	**77**			
AC CMRR	AC Common Mode Rejection Ratio (4)	−2V ≤ V_{CM} ≤ 16V	f = 1 kHz	80	95		dB
			f = 10 kHz		78		
PSRR	Power Supply Rejection Ratio	4.75V ≤ V_S ≤ 5.5V		**70**	80		dB
R_{F-INT}	Filter Resistor			**97**	100	**103**	kΩ
TCR_{F-INT}	Filter Resistor Drift				20		ppm/°C
A_V	Total Gain			13.86	14	14.14	V/V
	Gain Drift				±2	**±25**	ppm/°C
A_{V1}	A1 Gain			6.93	7	7.07	V/V
A_{V2}	A2 Gain			1.98	2	2.02	V/V
A1 V_{OUT}	A1 Output Voltage Swing		VOL		0.004	0.01	V
			VOH	4.80	4.95		
A2 V_{OUT}	A2 Output Voltage Swing (5) (6)	R_L = 100 kΩ on Output	VOL		0.007	0.02	V
			VOH	4.80	4.99		
		R_L = 10 kΩ on Output	VOL		0.03		V
			VOH		4.95		
SR	Slew Rate (7)				0.7		V/μs
BW	Bandwidth				80		kHz
Noise	0.1 Hz to 10 Hz				3.82		μV_{PP}
	Spectral Density	f = 1 kHz			486		nV/√Hz

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Typical values represent the parametric norm at the time of characterization.
(3) Positive current corresponds to current flowing into the device.
(4) AC Common Mode Signal is a 16 V_{PP} sine-wave (0V to 16V) at the given frequency
(5) For VOL, R_L is connected to V_S and for VOH, R_L is connected to GND.
(6) For this test input is driven from A1 stage.
(7) Slew rate is the average of the rising and falling slew rates.

Connection Diagram

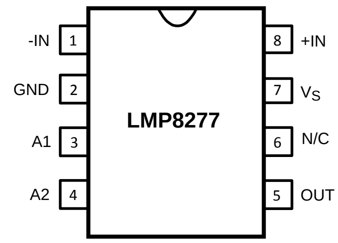


Figure 2. 8-Pin SOIC/VSSOP Top View

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2

V_{OS} vs. V_{CM} Over Temperature

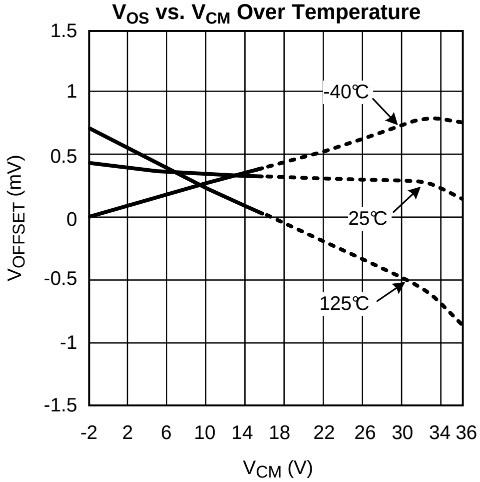


Figure 3.

Typical V_{OS} vs. Temperature

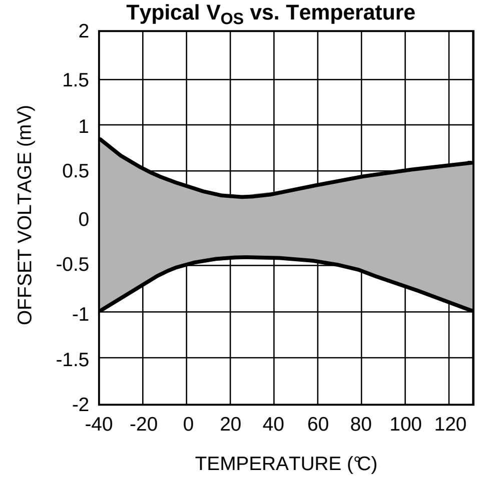


Figure 4.

Input Bias Current Over Temperature (A1 Inputs)

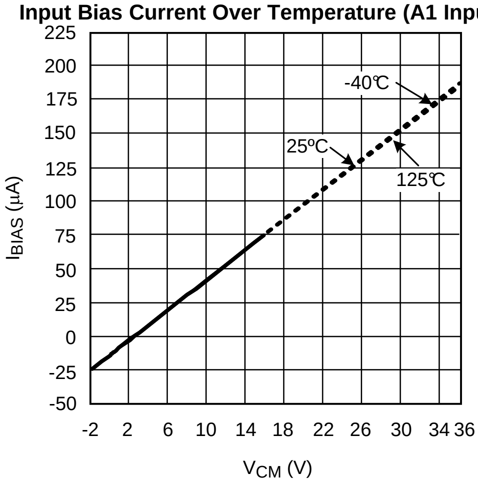


Figure 5.

Input Bias Current Over Temperature (A2 Inputs)

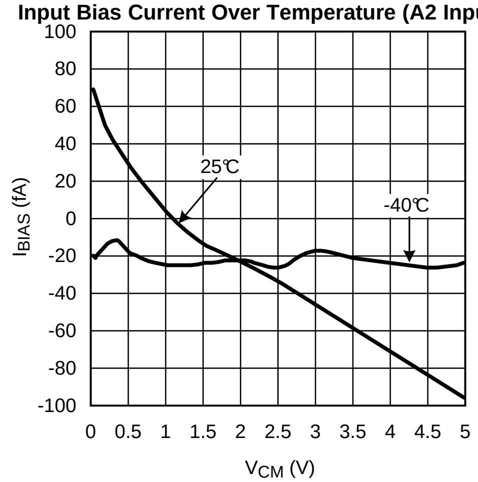


Figure 6.

Input Bias Current Over Temperature (A2 Inputs)

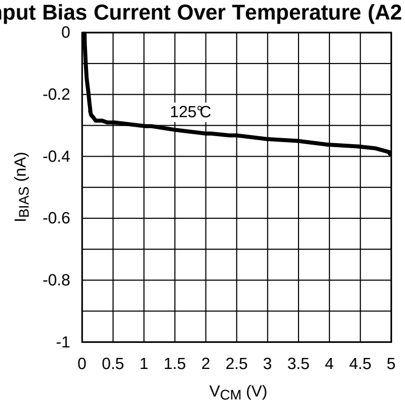


Figure 7.

Input Referred Voltage Noise vs. Frequency

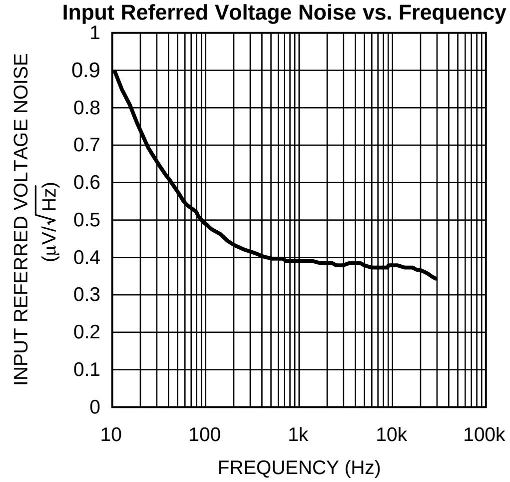


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2

PSRR vs. Frequency

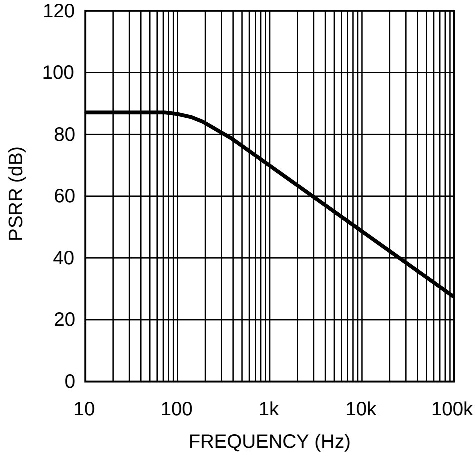


Figure 9.

V_{OS} vs. Supply Voltage

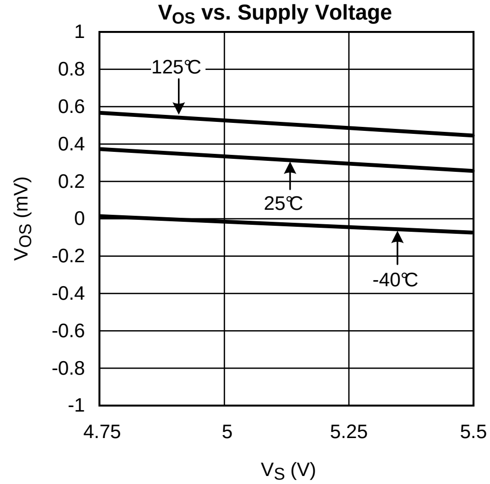


Figure 10.

Gain vs. Frequency Over Temperature

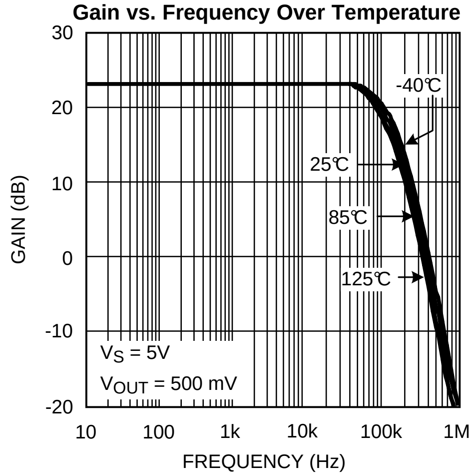


Figure 11.

Gain vs. Frequency Over Temperature

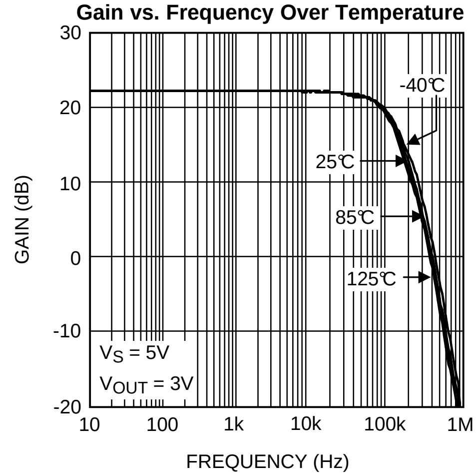


Figure 12.

Filter Resistor

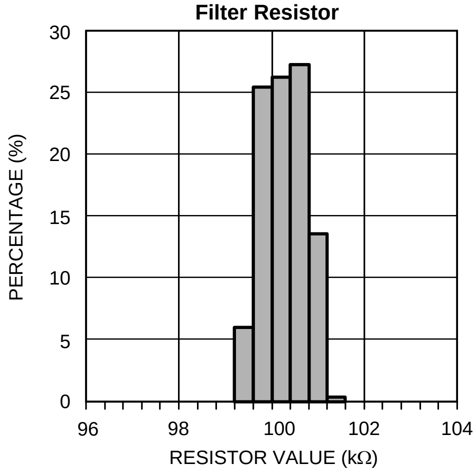


Figure 13.

CMRR vs. Frequency

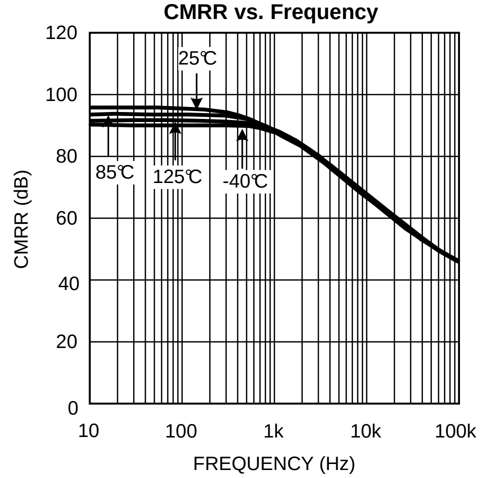


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S = 5V, V_{CM} = $V_S/2$

Settling Time (Rising Edge)

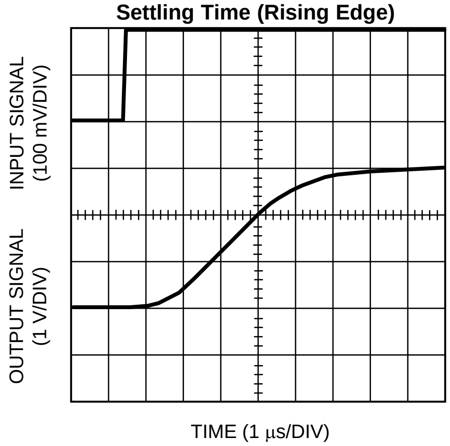


Figure 15.

Settling Time (Falling Edge

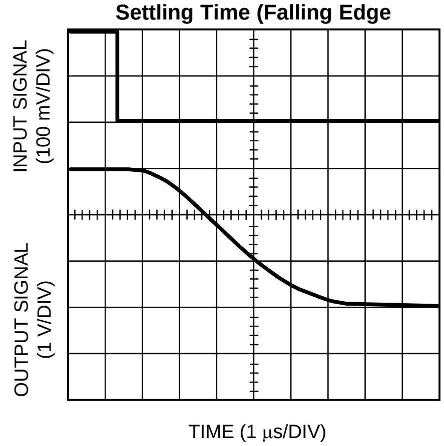


Figure 16.

Output Voltage vs. R_L to V_S

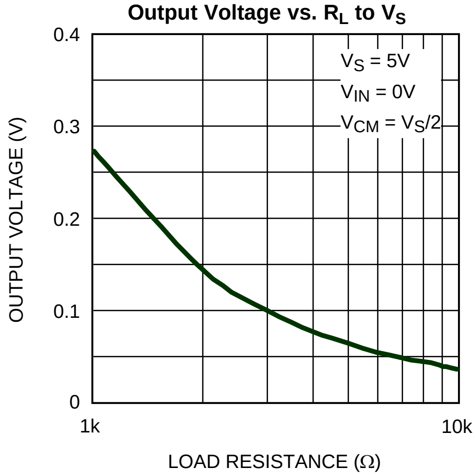


Figure 17.

Output Voltage vs. R_L to GND

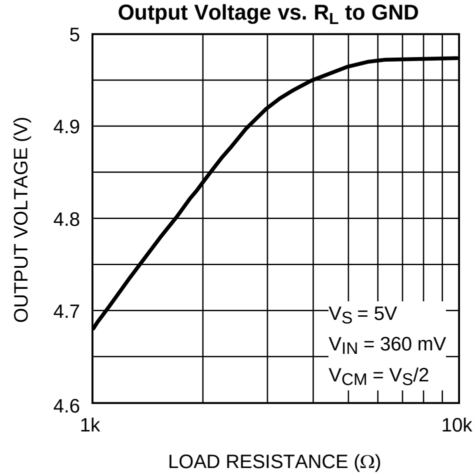


Figure 18.

Step Response

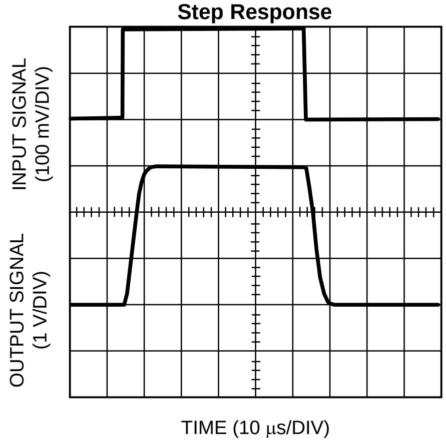


Figure 19.

APPLICATION NOTE

LMP8277

The LMP8277 is a single supply amplifier with a fixed gain of 14 and a common mode voltage range of −2V to 16V. The fixed gain is achieved in two separate stages, a preamplifier with gain of +7 and a second stage amplifier with gain of +2. A block diagram of the LMP8277 is shown in Figure 20.

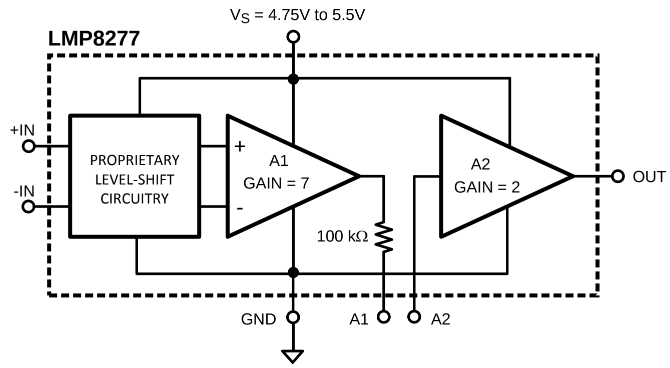


Figure 20. LMP8277

The overall offset of the LMP8277 is minimized by trimming amplifier A1. This is done so that the output referred offset of A1 cancels the input referred offset of A2 or $7V_{OS1} = -V_{OS2}$.

Because of this offset voltage relationship, the offset of each individual amplifier stage may be more than the limit specified for the overall system in the datasheet tables. Care must be given when pin 3 and 4, A1 and A2, are connected to each other. If the signal going from A1 to A2 is amplified or attenuated (by use of amplifiers and resistors), the overall LMP8277 offset will be affected as a result. Filtering the signal between A1 and A2 or simply connecting the two pins will not change the offset of the LMP8277.

Referencing the input referred offset voltages of each stage, the following relationship holds:

$$\frac{(7V_{OS1}) + (V_{OS2})}{7} = V_{OS}\,(\text{LMP8277}) \quad (1)$$

If the signal on pin 3 is scaled, attenuated or amplified, by a factor **X**, then the offset of the overall system will become:

$$\frac{(7V_{OS1}).(X) + (V_{OS2})}{7\,(X)} = V_{OS}\,(\text{LMP8277}) \quad (2)$$

POWER SUPPLY DECOUPLING

In order to decouple the LMP8277 from AC noise on the power supply, it is recommended to use a 0.1 µF on the supply pin. It is best to use a 0.1 µF capacitor in parallel with a 10 µF capacitor. This will generate an AC path to ground for most frequency ranges and will almost greatly reduce the noise introduced by the power supply.

SECOND ORDER LOW PASS FILTER

The LMP8277 can be effectively used to build a second order Sallen-Key low pass filter. The general filter is shown in Figure 21:

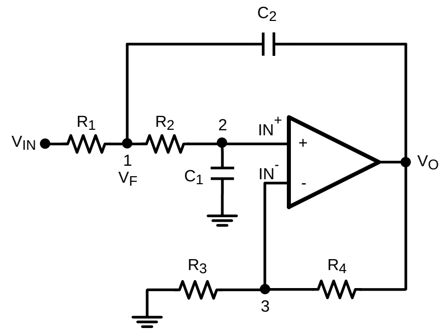


Figure 21. Second Order Low-Pass Filter

With the general transfer function:

$$\frac{V_O}{V_{IN}} = \frac{K}{M - KN} \quad (3)$$

Where:

$$M = s^2C_1C_2R_1R_2 + s(R_1C_1+R_1C_2+C_1R_2) + 1$$
$$N = sC_2R_1 \quad (4)$$

and

$$\frac{1}{K} = \frac{1}{A_{VOL}} + \frac{R_3}{R_3 + R_4} \quad (5)$$

K represents the sum of DC closed loop gain and the non-ideal behavior of the operational amplifier.

The LMP8277 can be used to realize this configuration as shown in Figure 22:

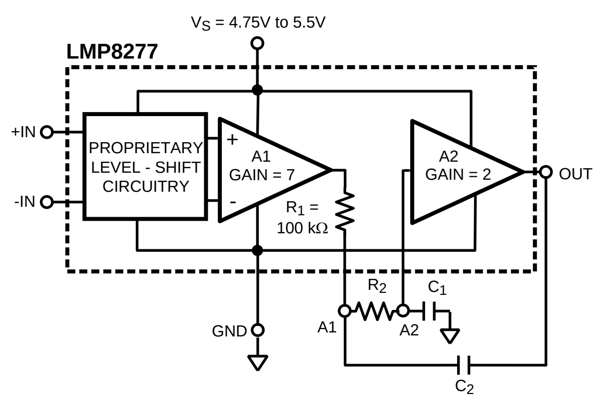


Figure 22. Low-Pass Filter With LMP8277

Assuming ideal behavior, the equation for K simply reduces to the DC gain, which is set to +2 for the LMP8277.

Using Equation 3, the filter parameters can be calculated as follows:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1+R_2C_1+(1-K)R_1C_2} \quad (6)$$

for the LMP8277, R_1 = 100 kΩ. Setting $R_1 = R_2$ and $C_1 = C_2$ results in a low pass filter with Q = 1. Since the values of resistors are predetermined, the corner frequency of this implementation of the filter depends on the capacitor values.

GAINS OTHER THAN 14

The LMP8277 has an internal gain of +14; however this gain can be modified. The signal path between the tow amplifiers is available as external pins.

GAINS LESS THAN 14

shows the configuration used to reduce the LMP8277 gain.

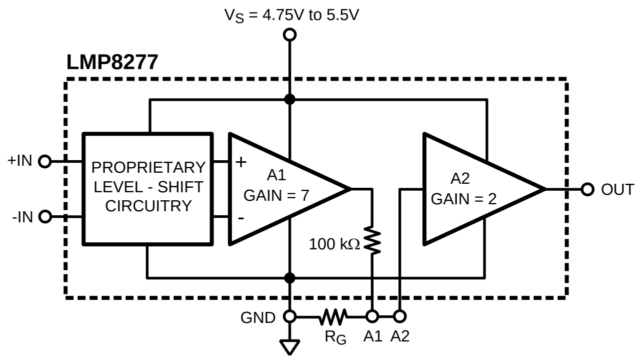


Figure 23. Gains Less than 14

Where:

$$GAIN\ (NEW) = \frac{14\ R_G}{R_G + 100\ k\Omega} \tag{7}$$

and

$$R_G = (100\ k\Omega)\ \frac{GAIN\ (NEW)}{14 - GAIN\ (NEW)} \tag{8}$$

GAINS GREATER THAN 14

A higher gain can be achieved by using positive feedback on the second stage amplifier, A2, of the LMP8277. Figure 24 shows the configuration:

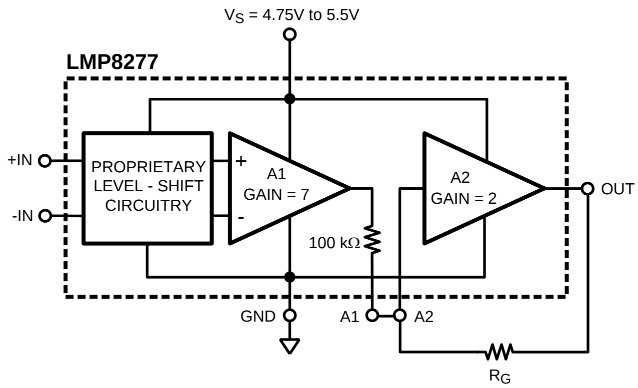


Figure 24. Gains Greater Than 14

The total gain is given by:

$$GAIN\ (NEW) = \frac{14\ R_G}{R_G - 100\ k\Omega} \tag{9}$$

Which can be rearranged to calculate R_G:

$$R_G = (100\ k\Omega)\ \frac{\text{GAIN (NEW)}}{\text{GAIN (NEW) - 14}} \quad (10)$$

The inverting gain of the second amplifier is set at 2, giving a total system gain of 14. The non-inverting gain which is achieved through positive feedback can be less than or equal to this gain without any issues. This implies a total system gain of 28 or less is easily achievable. Once the positive gain surpasses the negative gain, the system might oscillate.

As the value of gain resistor, R_G, approaches that of the internal 100 kΩ resistor, maintaining gain accuracy will become more challenging. This is because Gain(new) is inversely proportional to (R_G-100 kΩ), see Equation 9 . As $R_G \rightarrow$ 100 kΩ, the denominator of Equation 9 gets smaller. This smaller value will be comparable to the tolerance of the 100 kΩ resistor and R_G and hence the gain will be dominated by accuracy level of these resistors and the gain tolerance will be determined by the tolerance of the external resistor used for R_G and the 3% tolerance of the internal 100 kΩ resistor.

CURRENT LOOP RECEIVER

Many types of process control instrumentation use 4 to 20 mA transmitters to transmit the sensor's analog value to a central control room. The LMP8272 can be used as a current loop receiver as shown in Figure 25.

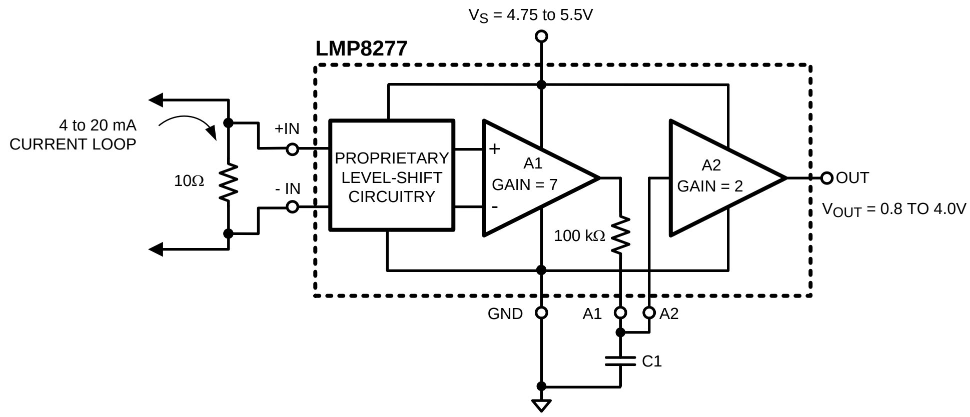


Figure 25. Current Loop Receiver

HIGH SIDE CURRENT SENSING

High side current measurement requires a differential amplifier with gain. Here the DC voltage source represent a common mode voltage with the +IN input at the supply voltage and the −IN input very close to the supply voltage. The LMP8277 can be used with a common mode voltage, V_{DC} in this case, of up to of 16V.

The LMP8277 can be used for high side current sensing. The large common mode voltage range of this device allows it to sense signals outside of its supply voltage range. Also, the LMP8277 has very high CMRR, which enables it to sense very small signals in presence of larger common mode signals. The system in Figure 26 couples these two characteristics of the LMP8277 in an automotive application. The signal through R_{S1} is detected and amplified by LMP8277 in the presence of a common mode signal of up to 16V with highest accuracy.

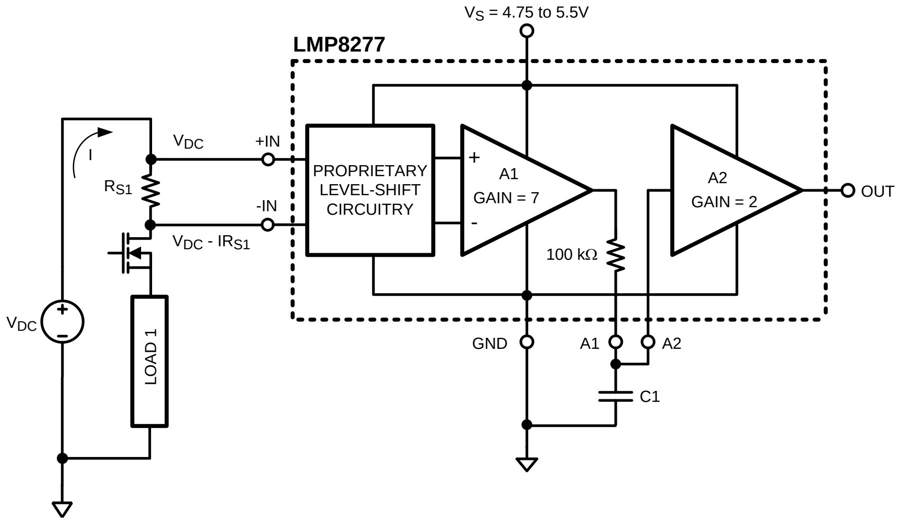


Figure 26. High Side Current Sensing

LOW SIDE CURRENT SENSING

Low side current measurements can cause a problem for operational amplifiers by exceeding the negative common mode voltage limit of the device. In Figure 27, the load current is returning to the power source through a common connection that has a parasitic resistance. The voltage drop across the parasitic resistances can cause the ground connection of the circuits being at a positive voltage with respect to the common side of the sense resistor. This will result in one or both of the inputs to be negative with respect to the measurement circuit's ground. The LMP8272 has a wide common mode voltage range of −2V to 16V and will function in this condition.

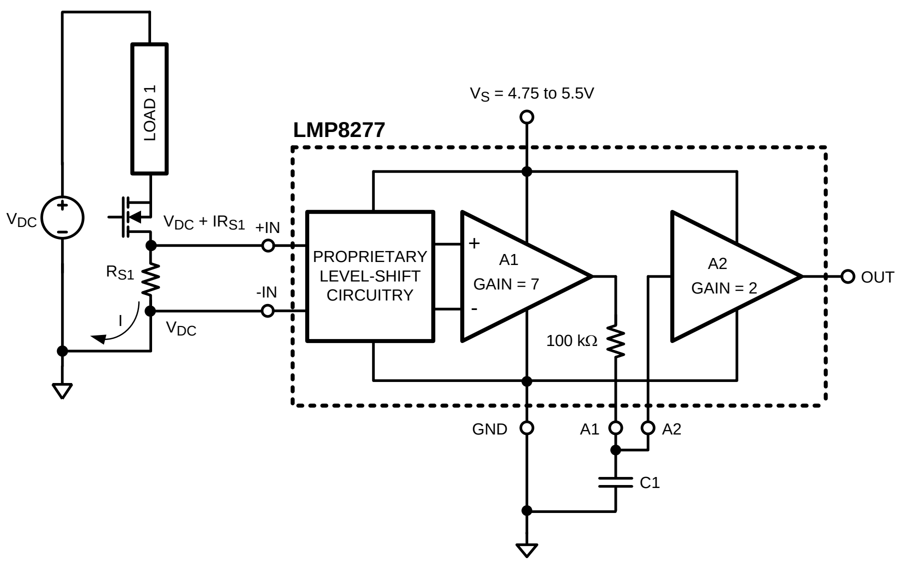


Figure 27. Low Side Current Sensing

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