LMP8480 / LMP8481 Precision 76V High-Side Current Sense Amplifiers with Voltage Output

Check for Samples: LMP8480, LMP8481

FEATURES

- **Typical values, T_A = 25°C**
- **Bi-Directional or Uni-Directional Sensing**
- **Common Mode Voltage Range 4.0V to 76V**
- **Supply Voltage Range 4.5V to 76V**
- **Fixed Gains 20, 50, 60 and 100 V/V**
- **Gain Accuracy ±0.1%**
- **Offset ±80µV**
- **Bandwidth (-3dB) 270KHz**
- **Quiescent Current <100µA**
- **Buffered High-Current Output >5mA**
- **Input Bias Current 7µA**
- **PSRR (DC) 122dB**
- **CMRR (DC) 124dB**
- **Temperature Range -40 to +125°C**
- **MSOP-8 or LLP-8 Packages**

APPLICATIONS

- **High-side current sense**
- **Vehicle current measurement**
- **Telecommunications**
- **Motor controls**
- **Laser or LED Drivers**
- **Energy Management**
- **Solar Panel Monitoring**

DESCRIPTION

The LMP8480 and LMP8481 are precision high-side current sense amplifiers that amplify a small differential voltage developed across a current sense resistor in the presence of high input common-mode voltages.

These amplifiers are designed for bidirectional (LMP8481) or unidirectional (LMP8480) current applications and will accept input signals with common-mode voltage range from 4V to 76V with a bandwidth of 270 kHz.

Since the operating power supply range overlaps the input common mode voltage range, the LMP848x can be powered by the same voltage that is being monitored. This benefit eliminates the need for an intermediate supply voltage to be routed to the point of load where the current is being monitored, resulting in reduced component count and board space.

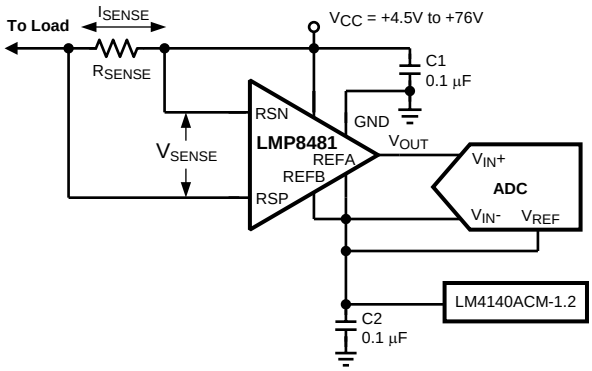
The LMP848x family consists of fixed gains of 20, 50, 60 and 100 for applications that demand high accuracy over temperature. The low input offset voltage allows the use of smaller sense resistors without sacrificing system error.

The wide operating temperature range of -40C to 125C makes the LMP848x an ideal choice for automotive, telecommunications, industrial, and consumer applications.

The LMP8480 and LMP8481 are pin for pin replacements for the MAX4080 and MAX4081, offering improved offset voltage, wider reference adjust range and higher output drive capabilities.

The LMP8480 and LMP8481 are available in a 8-pin MSOP package and the LMP8481 is also available in a 8–pad LLP.

Typical Application



Block Diagram

Figure 1. LMP8480 Block Diagram

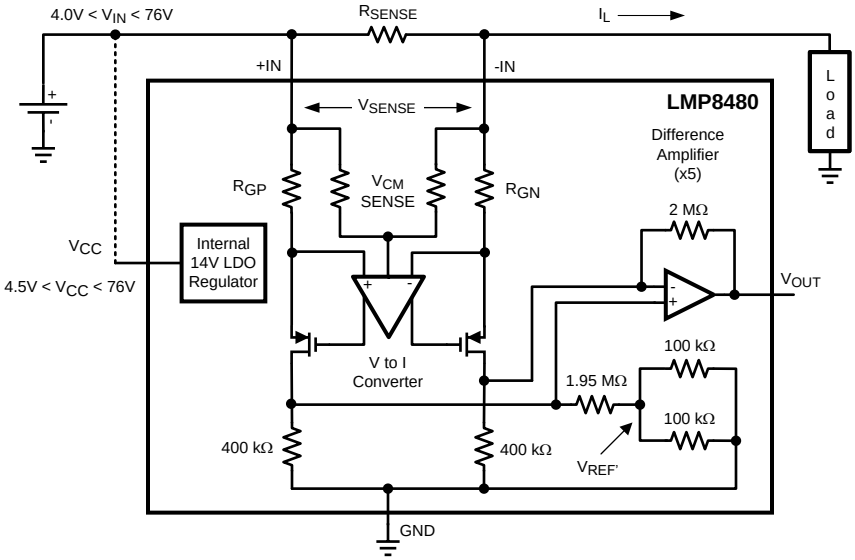
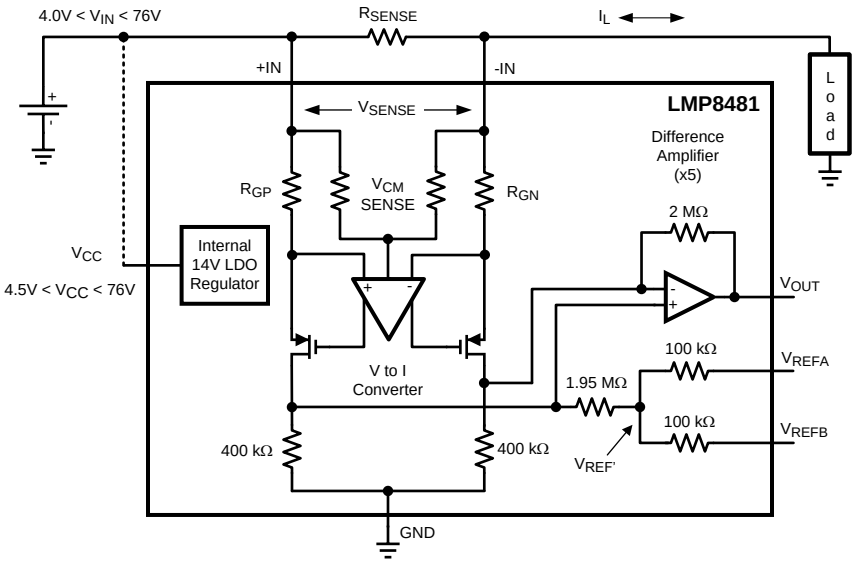


Figure 2. LMP8481 Block Diagram



Connection Diagram

LMP8480 8-Pin MSOP

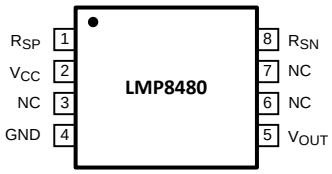


Figure 3. Top View

LMP8480 8-Pad LLP

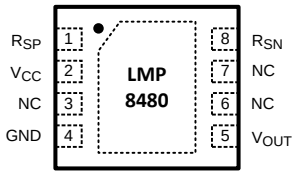


Figure 4. Top View

LMP8481 8-Pin MSOP

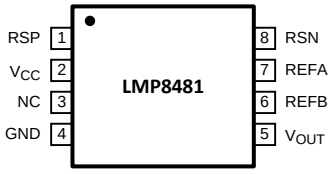


Figure 5. Top View

LMP8481 8-Pad LLP

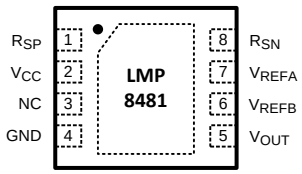


Figure 6. Top View

Table 1. Pin Descriptions

Pin	Name	Description	
1	R_{SP}	Positive current sense input	
2	V_{CC}	Positive supply voltage	
3	NC	No Connection – Not internally Connected.	
4	GND	Ground	
5	V_{OUT}	Output	
6	NC or R_{EFA}	LMP8480: No Connection	LMP8481: Reference Voltage “B” Input
7	NC or R_{EFB}	LMP8480: No Connection	LMP8481: Reference Voltage “A” Input
8	R_{SN}	Negative current sense input	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Over operating free-air temperature range (unless otherwise noted).

		LMP8480, LMP8481	UNIT
Supply Voltage (V_{CC} to GND)		-0.3 to +85	V
R_{SP} or R_{SN} to GND		-0.3 to +85	V
V_{OUT} to GND		-0.3 to the lesser of (V_{CC} + 0.3) or +20	V
V_{REF} Pins (LMP8481 Only)	Other V_{REF} pin tied to ground	-0.3 to +12	V
	Applied to both V_{REF} Pins tied together	-0.3 to +6	V
Differential Input Voltage		±85	V
Current into output pin		±20 (2)	mA
Current into any other pins		±5 (2)	mA
Operating Temperature		–40 to +125	°C
Storage Temperature		-65° to +150	°C
Junction Temperature		+150	°C
Package Thermal Resistance (θ_{JA})	MSOP-8	185	°C/W
	LLP-8	70	°C/W
ESD Ratings	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	750	V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

(2) When the input voltage (VIN) at any pin exceeds power supplies (VIN < GND or VIN > VS), the current at that pin must not exceed 5mA, and the voltage (VIN) has to be within the Absolute Maximum Rating for that pin. The 20mA package input current rating limits the number of pins that can safely exceed the power supplies with current flow to four pins.

Recommended Operating Ratings

Expected normal operating conditions over free-air temperature range (unless otherwise noted).

		LMP8480, LMP8481	UNIT
Supply Voltage (V_{CC})		+4.5V to +76	V
Common Mode Voltage		+4.0V to +76	V
Differential Input Voltage (V_{SENSE})		±667	mV
Reference Input (LMP8481 Only)	V_{REFA} and V_{REFB} tied together	-0.3 to the lesser of (V_{CC} - 1.5) or +6	V
	Single V_{REF} pin with other V_{REF} pin grounded	-0.3 to +12, or where the average of the two V_{REF} pins is less than the lesser of (V_{CC} - 1.5) or +6	V

Electrical Characteristics (1)

Unless otherwise specified, all limits guaranteed for at T_A = 25°C, V_{CC}= +4.5V to +76V, +4.5V < V_{CM} < +76V, R_L= 100k, V_{SENSE} = (V_{RSP} - V_{RSN}) = 0V. **Boldface** limits apply at the temperature extremes, $T_{MIN} \leqq T_A \leqq T_{MAX}$.

Parameter		Condition		Min (2)	Typ (3)	Max (2)	Units
Input Offset Voltage (RTI)	V_{OS}	V_{CC} = V_{RSP} = 48V, ΔV_{SENSE} = 100mV	T_a= +25°C		±80	±265	µV
			T_a= –40°C to +125°C			**±900**	
Input Offset Voltage Drift (4)	TCV_{OS}				6		µV/°C
Input Bias Current (5)	I_B	V_{CC} = V_{RSP} = 76V, Per Input			6.3	**12**	µA
Input Leakage Current	I_{LEAK}	V_{CC} = 0, V_{RSP} = 76V, Both Inputs Together			0.01	**2**	µA
Differential Input Voltage Across Sense Resistor (6)	$V_{SENSE(MAX)}$	V_{CC} = 16	-T Version			**667**	mV
			-F Version			**267**	
			-S Version			**222**	
			-H Version			**133**	
Gain	A_V	-T Version		**19.8**	20	**20.2**	V/V
		-F Version		**49.6**	50	**50.4**	
		-S Version		**59.5**	60	**60.5**	
		-H Version		**99.2**	100	**100.8**	
Gain Error		V_{CC} = V_{RSP} = 48V	T_a= +25°C			±0.6	%
			T_a= –40°C to +125°C			**±0.8**	%
DC Power Supply Rejection Ratio	DC PSRR	V_{RSP} = 48V, V_{CC} = 4.5 to 76V		**100**	122		dB
DC Common Mode Rejection Ratio	DC CMRR	V_{CC} = 48V, V_{RSP} = 4.5 to 76V		**100**	124		dB
		V_{CC} = 48V, V_{RSP} = 4 to 76V			124		dB
Input Common Mode Voltage Range	CMVR	CMRR > 100dB		**4**		**76**	V
Output Resistance / Load Regulation	R_{OUT}	V_{SENSE} = 100mV			0.1		
Maximum Output Voltage (Headroom) (V_{OMAX} = V_{CC} – V_{OUT})	V_{OMAX}	V_{CC} = 4.5V, V_{RSP} = 48V, V_{SENSE} = +1V I_{OUT} (sourcing) = 500µA			230	500	mV
Minimum Output Voltage	V_{OMIN}	V_{CC} = V_{RSP} = 48V, V_{SENSE} = -1V, I_{OUT} (sinking) = 10µA			3	**15**	mV
		V_{CC} = V_{RSP} = 4.5V, V_{SENSE} = -1V, I_{OUT} (sinking) = 10µA			3		
		V_{CC} = V_{RSP} = 48V, V_{SENSE} = -1V, I_{OUT} (sinking) = 100µA			18	**55**	
		V_{CC} = V_{RSP} = 4.5V, V_{SENSE} = -1V, I_{OUT} (sinking) = 100µA			18		
Output voltage with load	V_{OLOAD}	V_{CC}=28V, V_{RSP}=28V, V_{SENSE}=600mV, I_{OUT} (sourcing)=500uA			12		V
Output Load Regulation	V_{OLREG}	V_{CC} = 20, V_{RSP} = 16, V_{OUT} =12, ΔI_L= 200na to 8mA			0.001		%
Supply Current	I_{CC}	V_{OUT}=2V, R_L = 10M, V_{CC}= V_{RSP} = 76V			88	**155**	uA
−3 dB Bandwidth	BW	R_L= 10M, C_L = 20pF			270		kHz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) All limits are guaranteed by testing, design, or statistical analysis.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) Positive Bias Current corresponds to current flowing into the device.
(6) This parameter is guaranteed by design and/or characterization and is not tested in production.

Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits guaranteed for at T_A = 25°C, V_{CC}= +4.5V to +76V, +4.5V < V_{CM} < +76V, R_L= 100k, V_{SENSE} = (V_{RSP} - V_{RSN}) = 0V. **Boldface** limits apply at the temperature extremes, $T_{MIN} \leqq T_A \leqq T_{MAX}$.

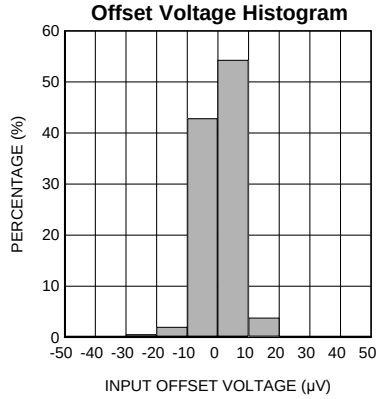
Parameter		Condition	Min (2)	Typ (3)	Max (2)	Units
Slew Rate (7)	SR	V_{SENSE} from 10mV to 80mV, RL=10M, C_L=20pF		1		V/µs
Input Referred Voltage Noise	e_{ni}	f = 1 kHz		95		nV/$\sqrt{Hz}$
Output Settling Time to 1% of Final Value	t_{SETTLE}	V_{SENSE} = 10mV to 100mV and 100mV to 10mV,		20		µs
Power-up Time	t_{PU}	V_{CC} = V_{RSP} = 48V, V_{SENSE} = 100mV, output to 1% of final value		50		µs
Saturation Recovery Time	$t_{RECOVERY}$	Output settles to 1% of final value, the device will not experience phase reversal when overdriven.		50		µs
Max Output Capacitance Load	C_{LOAD}	No sustained oscillations		500		pF

(7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

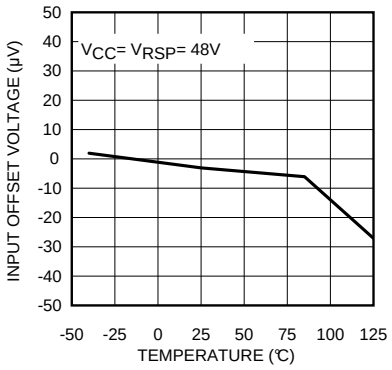
Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V_{CC}= 4.5V to 76V, 4.5V < V_{CM} < 76V, R_L= 100k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0V, for all gain options.

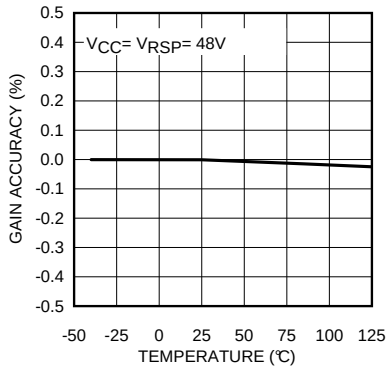
Offset Voltage Histogram



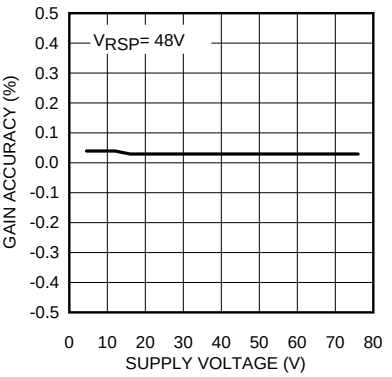
Typical Offset Voltage vs. Temperature



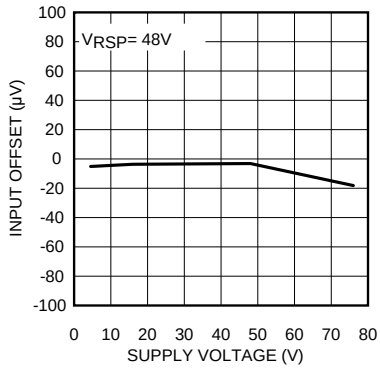
Typical Gain Accuracy vs. Temperature



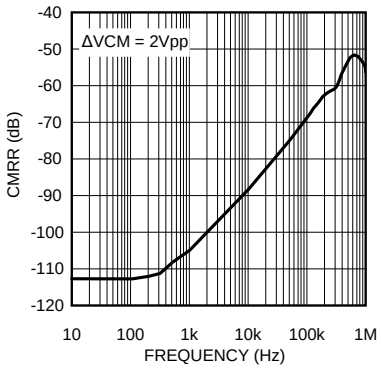
Typical Gain Accuracy vs. Supply Voltage



Typical Offset Voltage vs. Supply Voltage



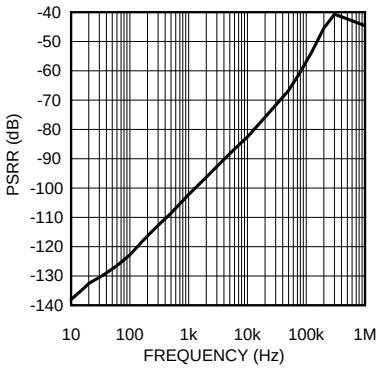
AC Common-Mode Rejection Ratio vs. Frequency



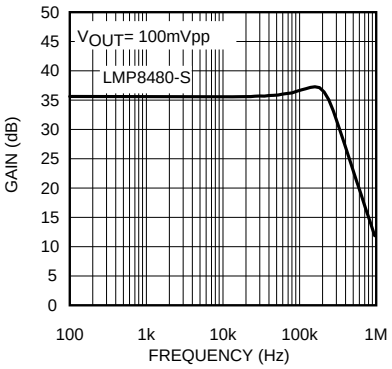
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{CC}= 4.5V to 76V, 4.5V < V_{CM} < 76V, R_L= 100k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0V, for all gain options.

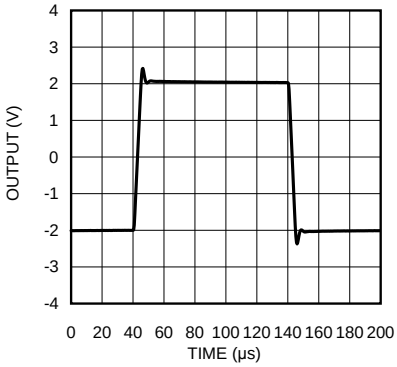
AC Power Supply Rejection Ratio vs. Frequency



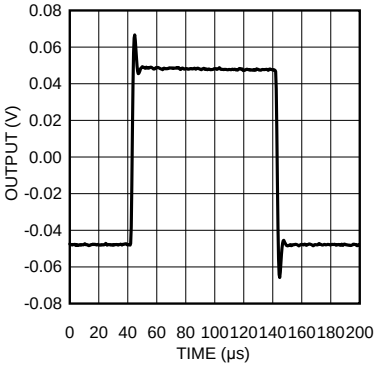
Small Signal Gain vs. Frequency



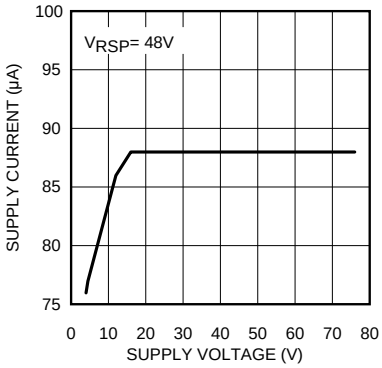
Large Signal Pulse Response



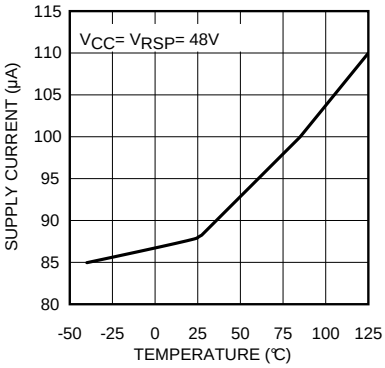
Small Signal Pulse Response



Supply Current vs. Supply Voltage



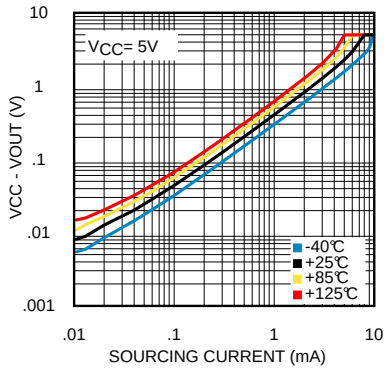
Supply Current vs. Temperature



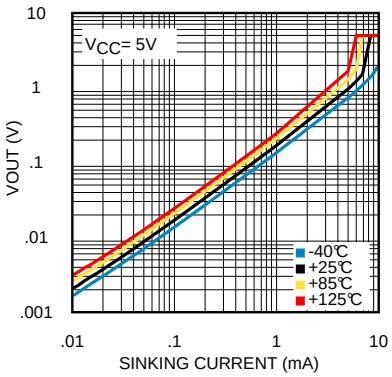
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{CC}= 4.5V to 76V, 4.5V < V_{CM} < 76V, R_L= 100k, V_{SENSE} = (V_{RSP} – V_{RSN}) = 0V, for all gain options.

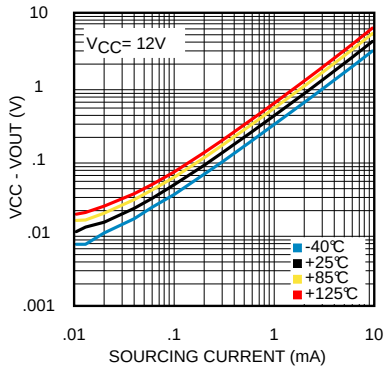
Saturated Output Sourcing Current at 4.5V



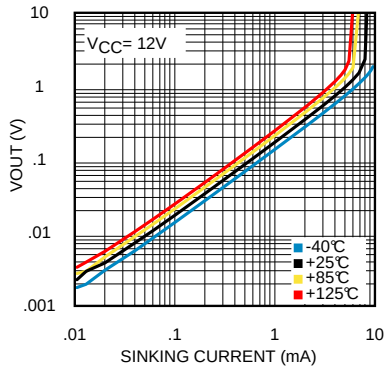
Saturated Output Sinking Current at 4.5V



Saturated Output Sourcing Current at 12V



Saturated Output Current Sinking at 12V



Application Information

LMP8480 AND LMP8481 INTRODUCTION

The LMP8480 and LMP8481 are single supply, high side current sense amplifiers with available fixed gains of x20, x50, x60 and x100. The power supply range is 4.5V to 76V, while the common mode input voltage range is capable of 4.0V to 76V operation. The supply voltage and common mode range are completely independent of each other. This makes the LMP848x supply voltage extremely flexible, as the LMP848x's supply voltage can be greater than, equal to, or less than the load source voltage, and allowing the device to be powered from the system supply or the load supply voltage.

The amplifier supply voltage does not have to be larger than the load source voltage. A 76V load source voltage with a 5V LMP8481 supply voltage is perfectly acceptable.

THEORY OF OPERATION

The LMP8480 and LMP8481 are comprised of two main stages. The first stage is a differential input current to voltage converter, followed by a differential voltage amplifier and level-shifting output stage. Also present is an internal 14 Volt Low Dropout Regulator (LDO) to power the amplifiers and output stage, as well as a reference divider resistor string to allow the setting of the reference level.

As seen in Figure 7, the current flowing through R_{SENSE} develops a voltage drop called V_{SENSE}. The voltage across the sense resistor, V_{SENSE}, is then applied to the input R_{SP} and R_{SN} pins of the amplifier.

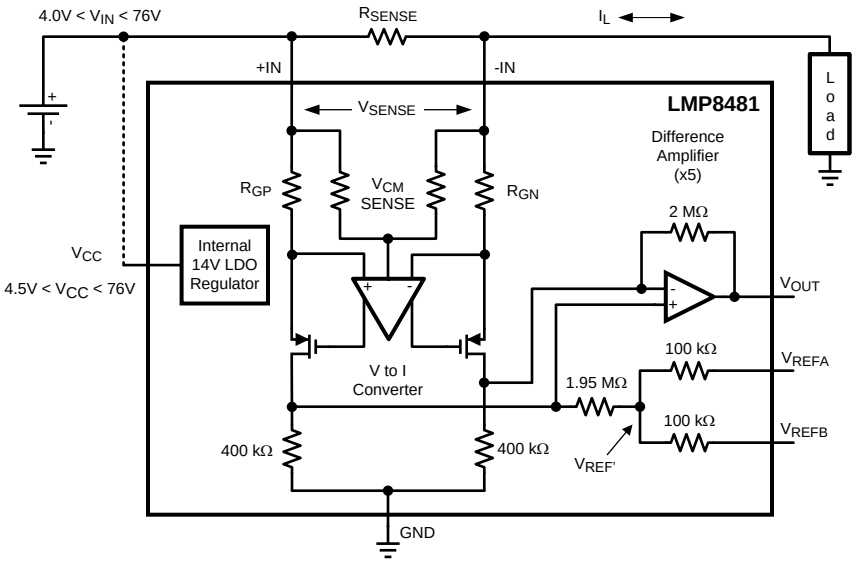


Figure 7. LMP8481 Functional Diagram

Internally, the voltage on each input pin is converted to a current by the internal precision thin-film input resistors R_{GP} and R_{GN} . A second set of much higher value V_{CM} sense resistors between the inputs provide a sample of the input common mode voltage for internal use by the differential amplifier.

V_{SENSE} is applied to the differential amplifier through R_{GP} and R_{GN}. These resistors change the input voltage to a differential current. The differential amplifier then servos the resistor currents through the MOSFETs to maintain a zero balance across the differential amplifier inputs.

With no input signal present, the currents in R_{GP} and R_{GN} are equal. When a signal is applied to V_{SENSE}, the current through R_{GP} and R_{GN} are imbalanced and are no longer equal. The amplifier then servos the MOSFETS to correct this current imbalance, and the extra current required to balance the input currents is then reflected down into the two lower 400kΩ “tail” resistors. The difference in the currents into the tail resistors is therefore proportional to the amplitude and polarity of V_{SENSE}. The tail resistors, being larger than the input resistors for the same current, then provide voltage gain by changing the current into a proportionally larger voltage. The gain of the first stage is then set by the tail resistor value divided by R_G value.

The differential amplifier stage then samples the voltage difference across the two 400K tail resistors and also applies a further gain-of-five and output level-shifting according to the applied reference voltage (V_{REF}).

The resulting output of the amplifier will be equal to the differential input voltage times the gain of the device, plus any voltage value applied to the two VREF pins.

The resistor values in the schematic are ideal values for clarity and understanding. The table below shows the actual values used that account for parallel combinations and loading. This table can be used for calculating the effects of any additional external resistance.

Table 2. Actual Internal Resistor Values

Gain Option	R_{GP} and R_{GN} (each)	$R_{VCMSENSE}$ (each)	R_{TAIL} (each)	Differential Amp FB (each)	V_{REFx} Resistors (each)
20x	98.38k	491.9k	393.52k	1967.6k	98.38k
50x	39.352k	196.76k	393.52k	1967.6k	98.38k
60x	32.793k	172.165k	393.52k	1967.6k	98.38k
100x	19.676k	98.38k	393.52k	1967.6k	98.38k

UNI-DIRECTIONAL VS. BI-DIRECTIONAL OPERATION

Uni-directional operation is where the load current only flows in one direction (V_{SENSE} is always positive). Application examples would be PA monitoring, non-inductive load monitoring and laser or LED drivers. This allows the output zero reference to be true zero volts on the output. The LMP8480 is designed for unidirectional applications where the setting of VREF is not required. See the UNI-DIRECTIONAL OPERATION for more details.

Bi-directional operation is where the load current can flow in both directions (V_{SENSE} can be positive or negative). Application examples would be battery charging or regenerative motor monitoring. The LMP8481 is designed for bidirectional applications and has a pair of VREF pins to allow the setting of the output zero reference level (V_{REF}). See the BI-DIRECTIONAL OPERATION (LMP8481 ONLY) section for more details.

UNI-DIRECTIONAL OPERATION

The LMP8480 is designed for unidirectional current sense applications. The output of the amplifier will be equal to the differential input voltage times the fixed device gain.

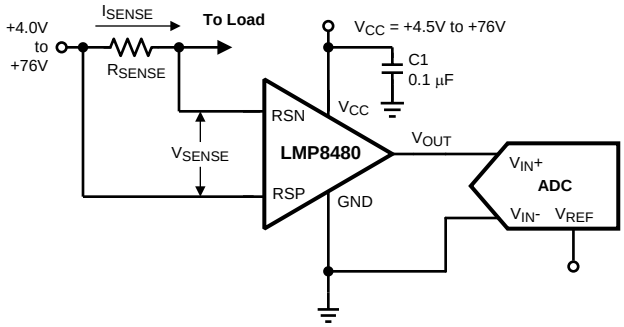


Figure 8. Uni-Directional Application with LMP8480

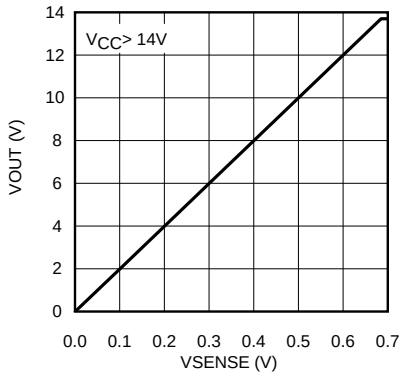


Figure 9. Uni-Directional Transfer Function for Gain-of-20 option

The output voltage can be calculated from:

$$VOUT = ((V_{RSP} – V_{RSN}) * Av) \quad (1)$$

It should be noted that the minimum “zero” reading will be limited by the lower output swing and input offset.

The LMP8480 is functionally identical to the LMP8481, but with the V_{REFA} and V_{REFB} nodes grounded internally. The LMP8481 can replace the LMP8480 if both the V_{REF} inputs (pins 6 & 7) are grounded.

BI-DIRECTIONAL OPERATION (LMP8481 ONLY)

Bi-directional operation is required where the measured load current can be positive or negative. Because V_{SENSE} can be positive or negative, and the output cannot swing negative, the “zero” output level must be level-shifted above ground to a known zero reference point. The LMP8481 allows for the setting this reference point.

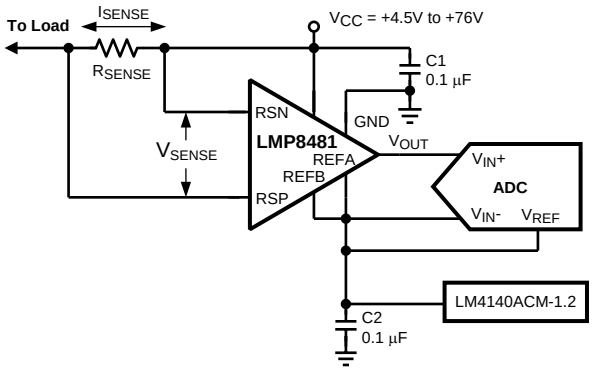


Figure 10. Bi-Directional current sensing using LMP8481

The V_{REFA} and V_{REFB} pins set the zero reference point. The output "zero" reference point is set by applying a voltage to the REFA and/or REFB pins. See the BI-DIRECTIONAL OPERATION (LMP8481 ONLY) section below. REFA AND REFB PINS (LMP8481 Only) below shows the output transfer function with a 1.2V reference applied to the Gain-of-20 option

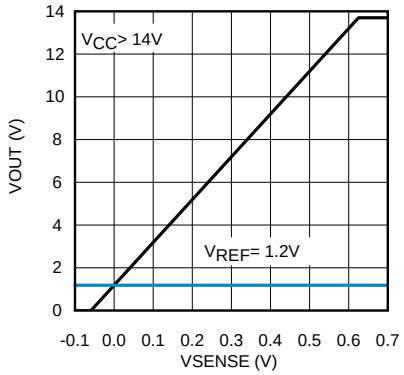


Figure 11. Bi-Directional Transfer Function using 1.2V Reference Voltage

REFA AND REFB PINS (LMP8481 Only)

The voltage applied to the V_{REFA} and V_{REFB} pins controls the output zero reference level.

The reference inputs consist of a pair of divider resistors with equal values to a common summing point, V_{REF}', as shown in Figure 16 below.

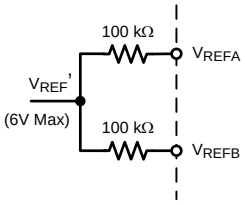


Figure 12. V_{REF} Input Resistor Network

V_{REF}' is the voltage at the resistor tap point that will be directly applied to the output as an offset.

$$V_{OUT} = ((V_{RSP} – V_{RSN}) * Av) + V_{REF}' \quad (2)$$

Where:

$$V_{REF}' = V_{REFA} = V_{REFB} \text{ (Equal Inputs)} \quad (3)$$

OR (4)

$$V_{REF}' = (V_{REFA} + V_{REFB}) / 2 \text{ (Separate inputs)} \quad (5)$$

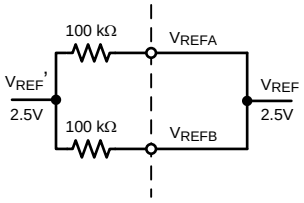


Figure 13. Applying 1:1 Direct Reference Voltage

For mid-range operation V_{REFB} should be tied to ground and V_{REFA} can be tied to VS or an external A/D reference voltage. The output will be set to one-half the reference voltage. For example, a 5V reference would result in a 2.5V output "zero" reference.

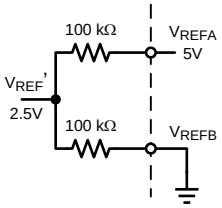


Figure 14. Applying A Divided Reference Voltage.

$$V_{REF}' = (V_{REFA} - V_{REFB}) / 2 \quad (6)$$

When the reference pins are biased at different voltages, the output will be referenced to the average of the two applied voltages.

The reference pins should always be driven from clean, stable sources, such as A/D reference lines or clean supply lines. Any noise or drifts on the reference inputs are directly reflected in the output. Care should be taken if the power supply is used as the reference source so as to not introduce supply noise, drift or sags into the measurement.

It is possible to set different resistor divider ratios by adding external resistors in series with the internal 100K resistors, though the temperature coefficient (tempco) of the external resistors may not tightly track the internal resistors and there will be slight errors over temperature.

REFERENCE INPUT VOLTAGE LIMITS

The maximum voltage on either reference input pin is limited to VCC or 12V, whichever is less.

The average voltage on the two V_{REF} pins, and thus the actual output reference voltage level, is limited to a maximum of 1.5V below VCC, or 6V, whichever is less. Beware that supply voltages of less than 7.5V will have a diminishing V_{REF} maximum.

Both V_{REFA} and V_{REFB} may both be grounded to provide a ground referenced output (thus functionally duplicating the LMP8480).

It should be noted that there can be a dynamic error in the V_{REF} to output level matching of up to 100µV/V. Normally this is not an issue for fixed references, but if the reference voltage is dynamically adjusted during operation, this error needs to be taken into account during calibration routines. This error will vary in both amplitude and polarity part-to-part, but the slope will generally be linear.

SELECTION OF THE SENSE RESISTOR

The accuracy of the current measurement depends heavily on the accuracy of the shunt resistor R_{SENSE}. Its value depends on the application and is a compromise between small-signal accuracy, maximum permissible voltage drop and allowable power dissipation in the current measurement circuit.

The use of a "4-terminal" or "Kelvin" sense resistor is highly recommended. See the ERROR SOURCES AND LAYOUT CONSIDERATIONS below.

For best results, the value of the resistor is calculated from the maximum expected load current I_{LMAX} and the expected maximum output swing V_{OUTMAX}, plus a few percent of headroom. See the MAXIMUM OUTPUT VOLTAGE section for details about the maximum output voltage limits.

High values of R_{SENSE} provide better accuracy at lower currents by minimizing the effects of amplifier offset. Low values of R_{SENSE} minimize load voltage loss, but at the expense of accuracy at low currents. A compromise between low current accuracy and load circuit losses must generally be made.

The maximum V_{SENSE} voltage that must be generated across the R_{SENSE} resistor will be:

$$V_{SENSE} = V_{OUTMAX} / A_V. \quad (7)$$

Note: The maximum V_{SENSE} voltage should be no more than 667mV.

From this maximum V_{SENSE} voltage, the R_{SENSE} value can be calculated from:

$$R_{SENSE} = V_{SENSE} / I_{LMAX} \quad (8)$$

Care must be taken to not exceed the maximum power dissipation of the resistor. The maximum sense resistor power dissipation will be:

$$P_{RSENSE} = V_{SENSE} * I_{LMAX} \quad (9)$$

It is recommended that a 2-3x minimum safety margin be used in selecting the power rating of the resistor.

USING PCB TRACES AS SENSE RESISTORS

While it may be tempting to use a known length of PCB trace resistance as a sense resistor, it is not recommended.

The tempco of copper is typically 3300-4000ppm/°K, which can vary over PCB process variations and require measurement correction (possibly requiring ambient temperature measurements).

A typical surface mount sense resistor tempco is in the 50ppm to 500ppm/°C range offering more measurement consistency and accuracy over the copper trace. Special low tempco resistors are available in the 0.1 to 50ppm range, but at a higher cost.

INPUT COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE

The input common mode range, where “common mode range” is defined as the voltage from ground to the voltage on R_{SP} input, should be in the range of +4.0V to +76V. Operation below 4.0V on either input pin will introduce severe gain error and nonlinearities.

The maximum differential voltage (defined as the voltage difference between R_{SP} and R_{SN}) should be 667mV or less. The theoretical maximum input is 700mV (14V / 20).

Taking the inputs below 4V will not damage the device, but the output conditions during this time are not predictable and are not guaranteed.

If the load voltage (Vcm) is expected to fall below 4V as part of normal operation, preparations must be made for invalid output levels during this time.

LOW SIDE CURRENT SENSING

The LMP8480 and LMP8481 are **not** recommended for low-side current sensing at ground level. The voltage on either input pin must be a minimum of 4.0V above the ground pin for proper operation.

INPUT SERIES RESISTANCE

Because the input stage uses precision resistors to convert the voltage on the input pin to a current, any resistance added in series with the input pins will change the gain. If a resistance is added in series with an input, the gain of that input will not track that of the other input, causing a constant gain error.

It is not recommended to use external resistances to alter the gain, as external resistors will not have the same thermal matching as the internal thin film resistors.

If resistors are purposely added for filtering, resistance should be added equally to both inputs and the user should be aware that the gain will change slightly. See end of the THEORY OF OPERATION section for the internal resistor values.

MINIMUM OUTPUT VOLTAGE

The amplifier output cannot swing to exactly zero volts. There will always be a minimum output voltage set by the output transistor saturation and input offset errors. This will create a minimum output swing around the zero current reading due to the output saturation. The user should be aware of this when designing any servo loops or data acquisition systems that may assume 0V = 0A. If a true zero is required, the LMP8481 should be used with a VREF set slightly above ground (>50mV). See the SWINGING OUTPUT BELOW GROUND section below for a possible solution to this issue.

SWINGING OUTPUT BELOW GROUND

If a negative supply is available, a pull-down resistor can be added from the output to the negative voltage to allow the output to swing a few millivolts below ground. This will now allow the ADC to resolve true zero and recover codes that would normally be lost to the negative output saturation limit.

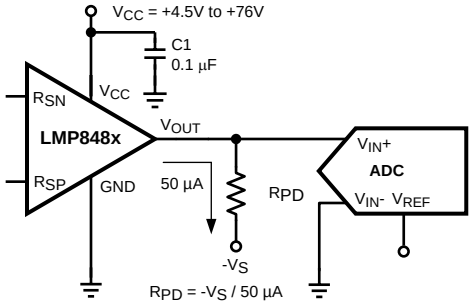


Figure 15. Output "Pull-Down" Resistor Example

A minimum of 50µA should be sourced ("pulled") from the output to a negative voltage. The pulldown resistor can be calculated from:

$$R_{PD} = -V_S/50\mu A \quad (10)$$

For example, if a -5V supply is available, a pull-down resistor of 5V/50uA = 100K should be used. This will allow the output to swing to about 10mV below ground.

This technique may also reduce the maximum positive swing voltage. Do not forget to include the parallel loading effects of the pulldown any output load. It is recommended not to exceed -100mV on the output. Source currents greater than 100uA should be avoided to prevent self-heating at high supply voltages. Pulldown resistor values should not be so low as to heavily load the output during positive output excursions. This mode of operation is not directly specified and is not guaranteed.

MAXIMUM OUTPUT VOLTAGE

The LMP8481 has an internal precision 14V low dropout regulator which limits the maximum amplifier output swing to about 250mV below V_{CC} or 13.7V (whichever is less). This effectively clamps the maximum output to slightly less than 13.7V even with a V_{CC} greater than 14V.

Care should be taken if the output is driving an A/D input with a maximum A/D maximum input voltage lower than the amplifier supply voltage, as the output can swing higher than the planned load maximum due to input transients or shorts on the load and overload or possibly damage the A/D input.

A resistive attenuator, as shown in Figure 16 below, can be used to match the maximum swing to the input range of the A/D.

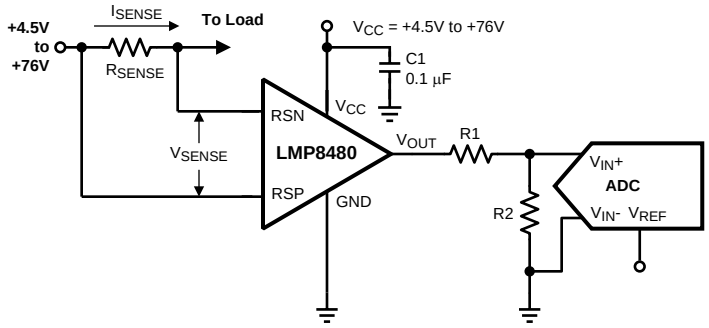


Figure 16. Typical Application with Resistive Divider

ERROR SOURCES AND LAYOUT CONSIDERATIONS

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (<100m), any trace resistance shared with the load current can cause significant errors.

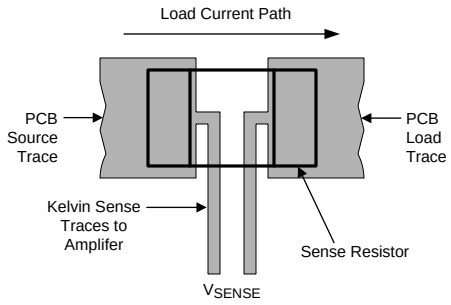


Figure 17. "Kelvin" or "4–wire" Connection to the Sense Resistor

The amplifier inputs should be directly connected to the sense resistor pads using "Kelvin" or "4-wire" connection techniques. The traces should be one continuous piece of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients.

To minimize noise pickup and thermal errors, the input traces should be treated as a differential signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these traces can contain high voltage, and should have the appropriate trace routing clearances.

Since the sense traces only carry the amplifier bias current (about 7µA at room temp), the connecting input traces can be thinner, signal level traces. Excessive Resistance in the trace should also be avoided.

The paths of the traces should be identical, including connectors and vias, so that these errors will be equal and cancel.

The sense resistor will heat up as the load increases. As the resistor heats up, the resistance generally goes up, which will cause a change in the readings The sense resistor should have as much heatsinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting over time after turn-on can usually be traced back to sense resistor heating.

POWER SUPPLY DECOUPLING

In order to decouple the LMP8480/81 from AC noise on the power supply, it is recommended to use a 0.1 µF bypass capacitor between the V_{CC} and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10 µF bypass capacitor may further reduce the supply noise.

Do not forget that these bypass capacitors must be rated for the full supply and/or load source voltage! It is recommended that the working voltage of the capacitor (WVDC) should be at least two times the maximum expected circuit voltage.

LLP DIE ATTACH PAD

The bottom thermal pad of the LLP package should be tied to the same ground as the ground pin. Be aware that noise on this pad can couple into the bottom of the die, so the ground should be as clean as possible.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8480MM-T/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV8A	Samples
LMP8480MME-S/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AY8A	Samples
LMP8480MME-T/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV8A	Samples
LMP8480MMX-S/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AY8A	Samples
LMP8480MMX-T/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV8A	Samples
LMP8481MM-H/NOPB	PREVIEW	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		
LMP8481MM-S/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA9A	Samples
LMP8481MM-T/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT9A	Samples
LMP8481MME-H/NOPB	PREVIEW	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		
LMP8481MME-S/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA9A	Samples
LMP8481MME-T/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT9A	Samples
LMP8481MMX-H/NOPB	PREVIEW	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125		
LMP8481MMX-S/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AA9A	Samples
LMP8481MMX-T/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT9A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

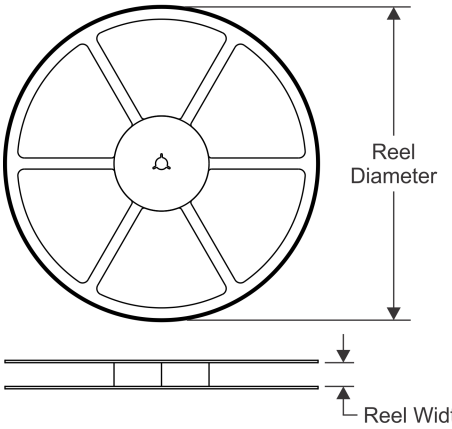
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

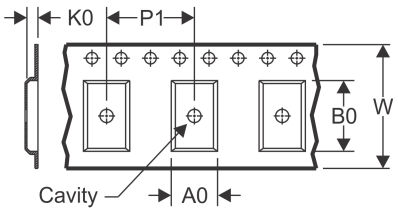
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

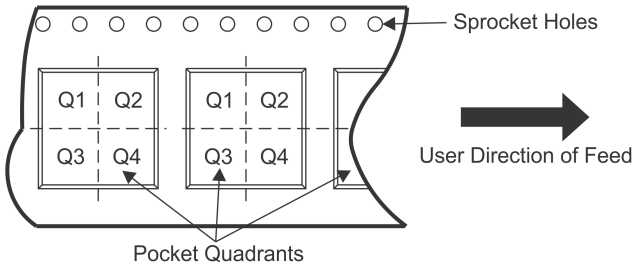


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

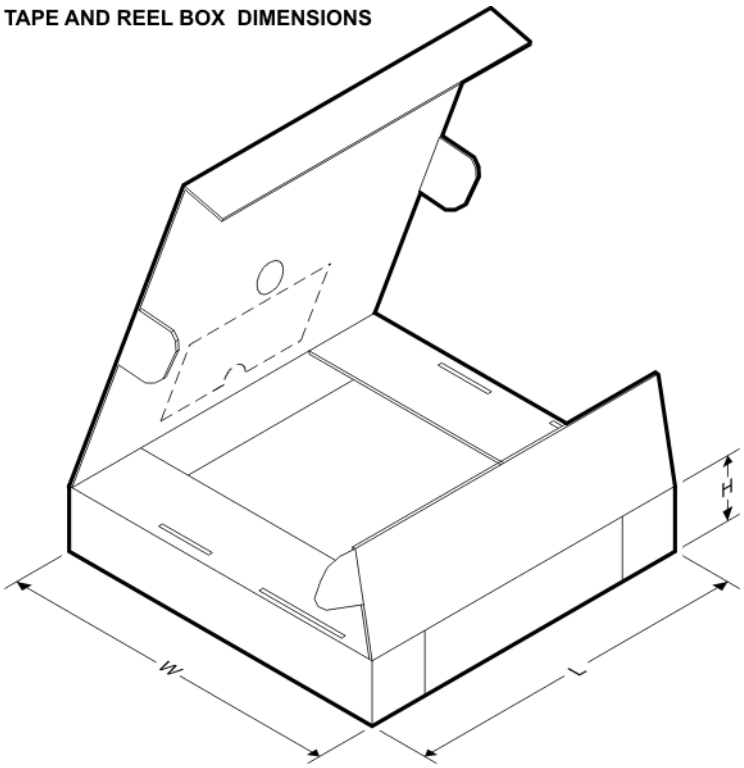
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8480MM-T/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MME-S/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MME-T/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MMX-S/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8480MMX-T/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MM-T/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MME-S/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MME-T/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8481MMX-T/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

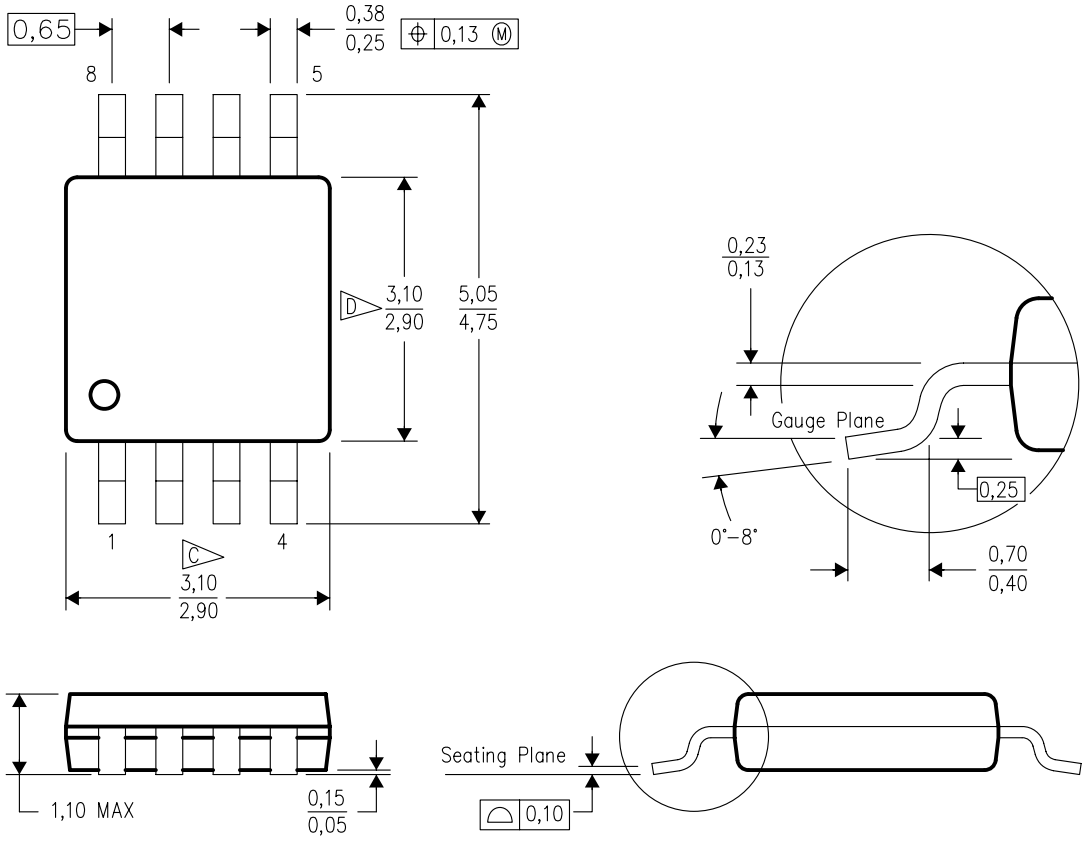
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8480MM-T/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8480MME-S/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8480MME-T/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8480MMX-S/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8480MMX-T/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8481MM-T/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8481MME-S/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8481MME-T/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8481MMX-T/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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