LMS202 5V Single Supply TIA/EIA-232 Dual Transceivers

Check for Samples: LMS202

FEATURES

- **Single +5V Power Supply**
- **230 kbps Data Rate**
- **On-Board DC-to-DC Converter**
- **0.1µF Charge Pump Capacitors**
- **Drop-In Replacement to Maxim's MAX202**

APPLICATIONS

- **POS Equipment (Bar Code Reader)**
- **Hand-Held Equipment**
- **General Purpose RS-232 Communication**

DESCRIPTION

The LMS202 features two transmitters and two receivers for RS-232 communication. It has a DC-to-DC converter that permits the device to operate with only a single +5V power supply. The on-chip DC-to-DC converter which utilizes four external 0.1µF capacitors to generate dual internal power supplies for RS-232 compatible output levels.

The device meet EIA/TIA-232E and CCITT V.28 specifications up to 230kbits/sec. The LMS202 is available in 16-pin narrow and wide SOIC packages.

Connection Diagram and Typical Circuit

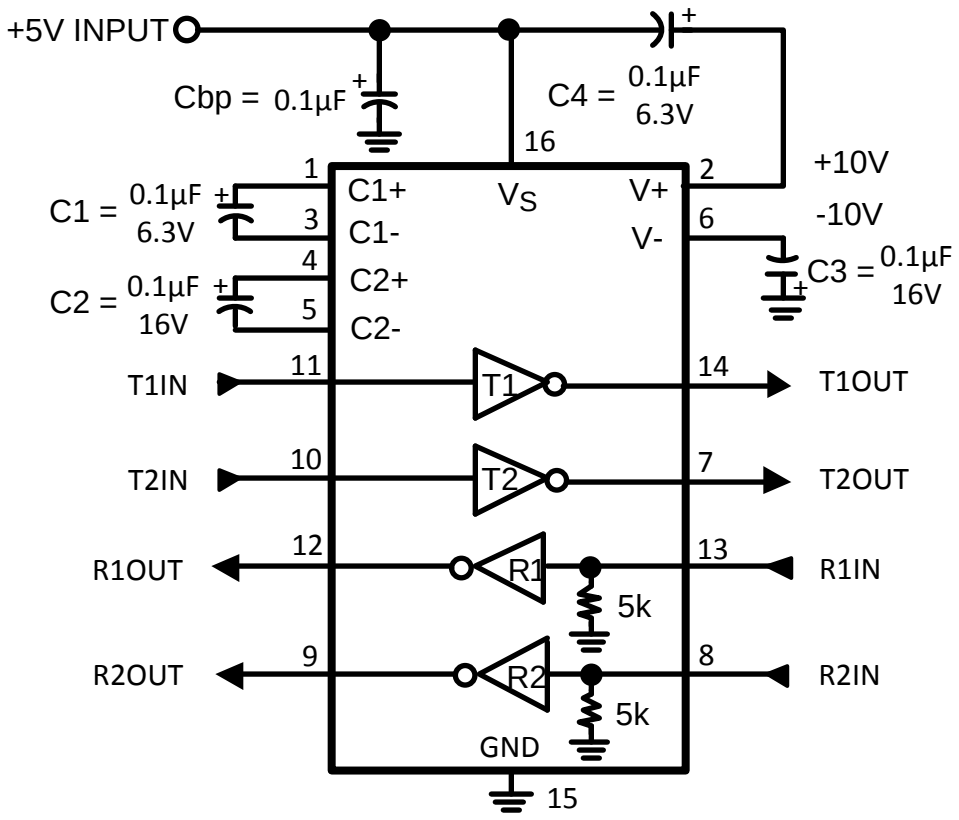

Figure 1. 16-Pin SOIC
See D or DW Package

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Function
1, 3	C1+, C1−	External capacitor connection pins. Recommended external capacitor C1 = 0.1µF (6.3V)
2	V+	Positive supply for TIA/EIA-232E drivers. Recommended external capacitor C4 = 0.1µF (6.3V)
4, 5	C2+, C2−	External capacitor connection pins. Recommended external capacitor C2 = 0.1µF (16V)
6	V−	Negative supply for TIA/EIA-232E drivers. Recommended external capacitor C3 = 0.1µF (16V)
7, 14	T1out, T2out	Transmitter output pins conform to TIA/EIA-232E levels. The typical transmitter output swing is ±8V when loaded 3kΩ load to ground. The open-circuit output voltage swings from (V+ − 0.6V) to V−
8,13	R1in, R2in	Receiver inputs accept TIA/EIA-232
9, 12	R1out and R2out	Receiver output pins are TTL/CMOS compatible
10, 11	Tin1, Tin2	Transmitter input pins are TTL/CMOS compatible. Inputs of transmitter do not have pull-up resistors. Connect all unused transmitter inputs to ground
15	GND	Ground pin
16	V_S	Power supply pin for the device, +5V (±10%)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_S		−0.3V to 6V
V+		(V_S − 0.3V) to +14V
V−		+0.3V to −14V
Driver Input Voltage, T_{IN}		−0.3V to (V+ +0.3V)
Receiver Input Voltage, R_{IN}		±30V
Driver Output Voltage T_O		(V− −0.3V) to (V+ +0.3V)
Receiver Output Voltage R_O		−0.3 to (V_S +0.3)
Short Circuit Duration, T_O		Continuous
ESD Rating	Human Body Model(3)	2kV
Machine Model(4)		200V
Soldering Information	Infrared or Convection (20sec.)	235°C
Junction Temperature		150°C
Storage Temperature Range		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, 1.5kΩ in series with 100pF
(4) Machine model, 0Ω in series with 200pF

Operating Ratings

Supply Voltage V_S		4.5V to 5.5V
Ambient Temperature Range, T_A	Commercial (C)	0°C to +70°C
	Industrial (I)	−40°C to +85°C
Package Thermal Resistance(1)	D Package	71°C/W
	DW Package	55°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified
C1 = C2 = C3 = C4 = Cbp = 0.1µF

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
DC Characteristics						
I_S	Supply Current	No Load, T_A = 25°C		1	7	mA
Logic						
I_{INPUT}	Input Leakage Current	T_{IN} = 0V to V_S			±10	µA
V_{THL}	Input Logic Theshold Low	T_{IN}			0.8	V
V_{THH}	Input Logic Theshold High	T_{IN}	2.0			V
V_{OL}	TTL/CMOS Output Voltage Low	R_{OUT}, I_{OUT} = 3.2mA			0.4	V
V_{OH}	TTL/CMOS Output Voltage High	R_{OUT}, I_{OUT} = −1.0mA	3.5	V_S −0.1		V
RS-232 Receiver Inputs						
V_{RI}	Receiver Input Voltage Range		−30		+30	V
V_{RTHL}	Receiver Input Theshold Low	V_S = 5V, T_A = 25°C	0.8	1.4		V
V_{RTHH}	Receiver Input Theshold High	V_S = 5V, T_A = 25°C		2	2.4	V
V_{HYST}	Receiver Input Hysteresis	V_S = 5V	0.2	0.6	1.0	V
R_I	Receiver Input Resistance	V_S = 5V, T_A = 25°C	3	5	7	kΩ
RS-232 Transmitter Outputs						
V_O	Transmitter Output Voltage Swing	All transmitters loaded with 3kΩ to GND	±5	±8		V
R_O	Output Resistance	V_S = V+ = V− = 0V, V_O = ± 2V	300			Ω
I_{OS}	Output Short Circuit Current			±11	±60	mA
Timing Characteristics						
DR	Maximum Data Rate	C_L = 50pF to 1000pF, R_L = 3kΩ to 7kΩ	230			kbps
T_{RPLH} T_{RPHL}	Receiver Propagation Delay	C_L = 150pF		0.08	1	µs
T_{DPLH} T_{DPHL}	Transmitter Propagation Delay	R_L = 3kΩ, C_L = 2500pF All transmitters loaded		2.4		µs
V_{SLEW}	Transition Region Slew Rate	T_A = 25°C, V_S = 5V C_L = 50pF to 1000pF, R_L = 3kΩ to 7kΩ Measured from +3V to −3V or vice versa	3	6	30	V/µs

(1) All limits are ensured by testing or statistical analysis
(2) Typical Values represent the most likely parametric norm.

Typical Characteristics

Transmitter Output High Voltage vs. Load Capacitance

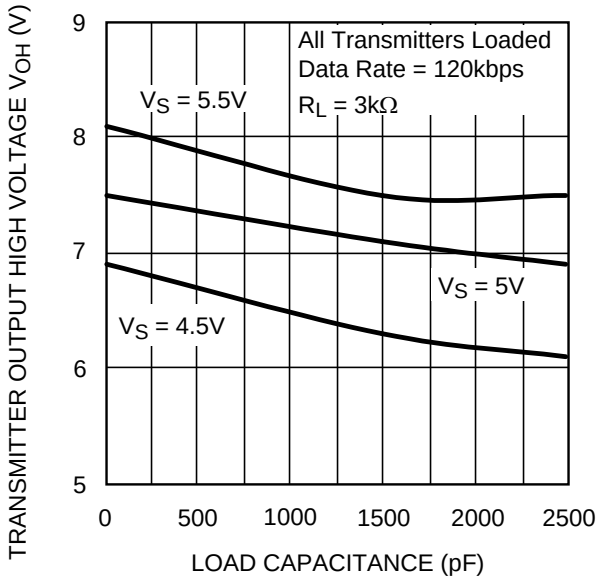

Figure 2.

Transmitter Slew Rate vs. Load Capacitance

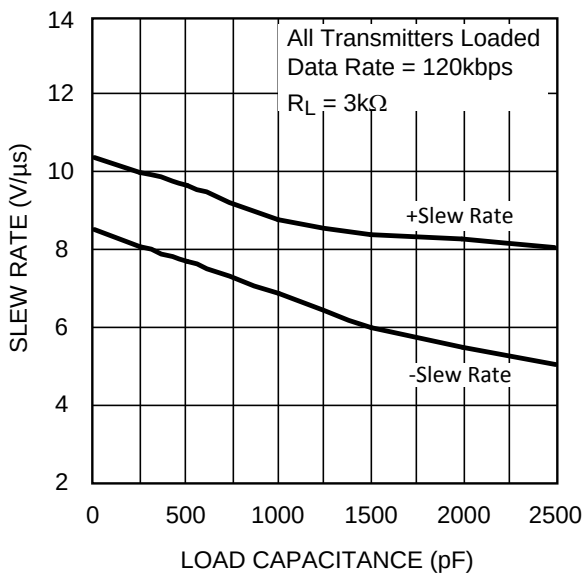

Figure 3.

APPLICATION INFORMATION

CAPACITOR SELECTION

The recommended capacitors are 0.1µF. However, larger capacitors for the charge pump may be used to minimized ripples on V+ and V− pins.

POWER SUPPLY DECOUPLING

In some applications that are sensitive to power supply noise from the charge pump, place a decoupling capacitor, Cbp, from V_S to GND. Use at least a 0.1µF capacitor or the same size as the charge pump capacitors (C1 − C4).

CHARGED PUMP

The dual internal charged-pump provides the ±10V to the to transmitters. Using capacitor C1, the charge pump converts +5V to +10V then stores the +10V in capacitor C3. The charge pump uses capacitor C2 to invert the +10V to −10V. The −10V is then stored in capacitor C4.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	5

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