LMS485 5V Low Power RS-485 / RS-422 Differential Bus Transceiver

Check for Samples: LMS485

FEATURES

- **Meet ANSI Standard RS-485-A and RS-422-B**
- **Data Rate 2.5 Mbps**
- **Single Supply Voltage Operation, 5V**
- **Thermal Shutdown Protection**
- **Short Circuit Protection**
- **Low Power BiCMOS**
- **Allows Up To 32 Transceivers on the Bus**
- **Open Circuit Fail-Safe for Receiver**
- **Extended Operating Temperature Range −40°C to 85°C**
- **Drop-In Replacement to MAX485**
- **Available in 8-pin SOIC and 8-Pin DIP Package**

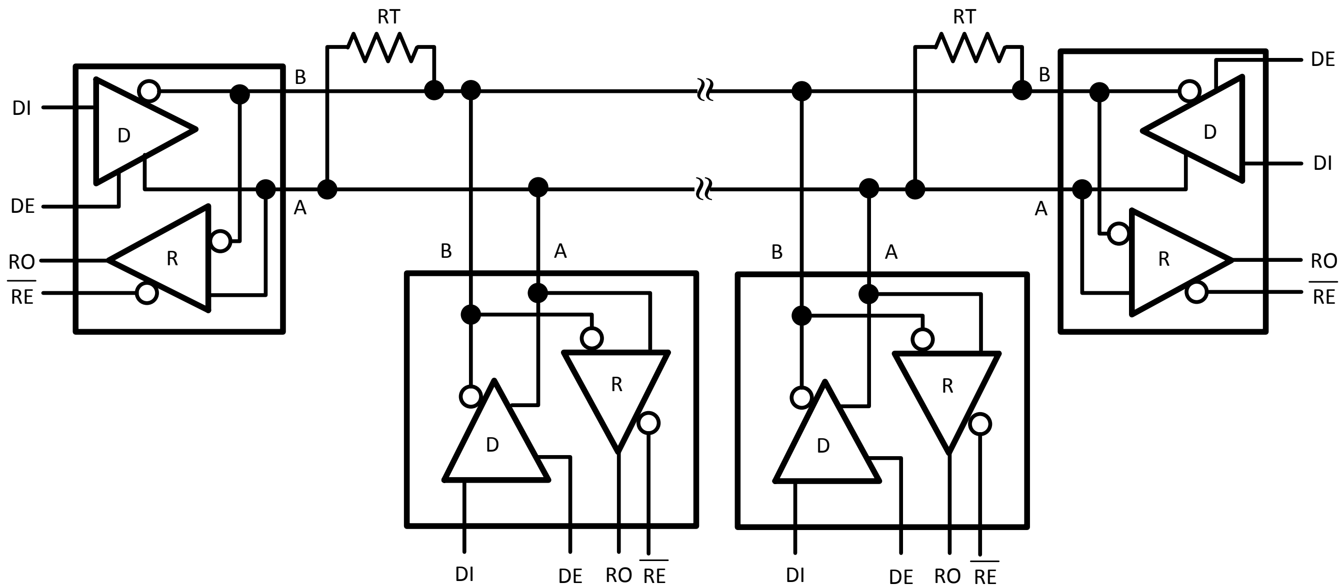
APPLICATIONS

- **Low Power RS-485 Systems**
- **Network Hubs, Bridges, and Routers**
- **Point of Sales Equipment (ATM, Barcode Scanners,…)**
- **Local Area Networks (LAN)**
- **Integrated Service Digital Network (ISDN)**
- **Industrial Programmable Logic Controllers**
- **High Speed Parallel and Serial Applications**
- **Multipoint Applications with Noisy Environment**

DESCRIPTION

The LMS485 is a low power differential bus/line transceiver designed for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines. It meets ANSI Standards TIA/EIA RS422-B, TIA/EIA RS485-A and ITU recommendation and V.11 and X.27. The LMS485 combines a TRI-STATE differential line driver and differential input receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active high and active low, respectively, that can be externally connected to function as a direction control. The driver and receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments. The LMS485 is available in a 8-Pin SOIC and 8-Pin DIP packages. It is a drop-in socket replacement to Maxim's MAX485

Typical Application



A Typical multipoint application is shown in the above figure. Terminating resistors, RT, are typically required but only located at the two ends of the cable. Pull up and pull down resistors maybe required at the end of the bus to provide failsafe biasing. The biasing resistors provide a bias to the cable when all drivers are in TRI-STATE, See TI Application Note, AN-847 for further information.

Connection Diagram

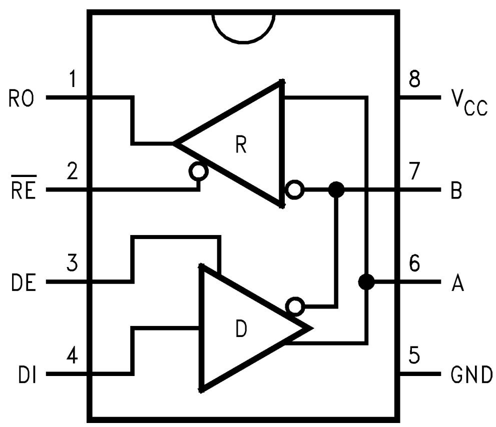


Figure 1. 8-Pin SOIC / DIP Top View

TRUTH TABLE

DRIVER SECTION				
$\overline{RE}$	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
$\overline{RE}$	**DE**	**A-B**		**RO**
L	L	≥ +0.2V		H
L	L	≤ −0.2V		L
H	X	X		Z
L	L	OPEN *[1]		H

(1) * = Non Terminated Open Input only
X = Irrelevant
Z = TRI-STATE
H = High level
L = Low level

Table 1. PIN DESCRIPTIONS

Pin #	I/O	Name	Function
1	O	RO	Receiver Output: If A > B by 200 mV, RO will be high; If A < B by 200mV, RO will be low. RO will be high also if the inputs (A and B) are open (non-terminated)
2	I	$\overline{RE}$	Receiver Output Enable: RO is enabled when $\overline{RE}$ is low; RO is in TRI-STATE when $\overline{RE}$ is high
3	I	DE	Driver Output Enable: The driver outputs (A and B) are enabled when DE is high; they are in TRI-STATE when DE is low. Pins A and B also function as the receiver input pins (see below)
4	I	DI	Driver Input: A low on DI forces A low and B high while a high on DI forces A high and B low when the driver is enabled
5	N/A	GND	Ground
6	I/O	A	Non-inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels
7	I/O	B	Inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels
8	N/A	V_{CC}	Power Supply: 4.75V ≤ V_{CC} ≤ 5.25V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage, V_{CC} (3)		7V
Input Voltage, V_{IN} (DI, DE, or $\overline{RE}$)		−0.3V to V_{CC} + 0.3V
Voltage Range at Any Bus Terminal (AB)		−7V to 12V
Receiver Outputs		−0.3V to V_{CC} + 0.3V
Package Thermal Impedance, θ_{JA}	SOIC	125°C/W
	DIP	88°C/W
Junction Temperature (4)		150°C
Operating Free-Air Temperature Range, T_A	Commercial	0°C to 70°C
	Industrial	−40°C to 85°C
Storage Temperature Range		−65°C to 150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Lead Temperature (4 sec.)	260°C
ESD Rating (5)		7kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the ELECTRICAL CHARACTERISTICS
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.
(5) ESD rating based upon human body model, 100pF discharged through 1.5kΩ.

OPERATING RATINGS

		Min	Nom	Max	
Supply Voltage, V_{CC}		4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode)		−7		12	V
V_{IN} or VIC					
High-Level Input Voltage, V_{IH} (1)		2			V
Low-Level Input Voltage, V_{IL} (1)				0.8	V
Differential Input Voltage, V_{ID} (2)				±12	V
High-Level Output	Driver, I_{OH}			−150	mA
	Receiver, I_{OH}			−42	mA
Low-Level Output	Driver, I_{OL}			80	mA
	Receiver, I_{OL}			26	mA

(1) Voltage limits apply to DI, DE, $\overline{RE}$ pins.
(2) Differential input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

ELECTRICAL CHARACTERISTICS

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver Section						
$\lvert V_{OD1} \rvert$	Differential Output Voltage	R = ∞ (See Figure 11)			5.25	V
$\lvert V_{OD2} \rvert$	Differential Output Voltage	R = 50Ω (See Figure 11) ,RS-422	2.0			V
		R = 27Ω (See Figure 11) ,RS-485	1.5		5.0	
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or 50Ω (See Figure 11)(1)			0.2	V
V_{OC}	Common-Mode Output Voltage	R = 27Ω or 50Ω (See Figure 11)			3.0	V
ΔV_{OC}	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	R = 27Ω or 50Ω (See Figure 11)(1)			0.2	V
V_{IH}	CMOS Inout Logic Threshold High	DE, DI, $\overline{RE}$	2.0			V
V_{IL}	CMOS Input Logic Threshold Low	DE, DI, $\overline{RE}$			0.8	V
I_{IN1}	Logic Input Current	DE, DI, $\overline{RE}$			±2	μA
Receiver Section						
I_{IN2}	Input Current (A, B)	DE = 0V, V_{CC} = 0V or 5.25V V_{IN} = 12V			1.0	mA
		V_{IN} = − 7V			−0.8	
V_{TH}	Differential Input Threshold Voltage	−7V ≤ V_{CM} ≤ + 12V	−0.2		+0.2	V
ΔV_{TH}	Input Hysteresis Voltage ($V_{TH+} - V_{TH-}$)	V_{CM} = 0		95		mV
V_{OH}	CMOS High-level Output Voltage	I_{OH} = −4mA, V_{ID} = 200mV	3.5			V
V_{OL}	CMOS Low-level	I_{OL} = 4mA, V_{ID} = −200mV			0.40	V
I_{OZR}	Tristate Output Leakage Current	0.4V ≤ V_O ≤ + 2.4V			±1	μA
R_{IN}	Input Resistance	− 7V ≤ V_{CM}≤+12V	12			kΩ
Power Supply Current						
I_{CC}	Supply Current	DE = $V_{CC,}$ $\overline{RE}$ = GND or V_{CC}		320	500	μA
		DE = 0V, $\overline{RE}$ = GND or V_{CC}		315	400	
I_{OSD1}	Driver Short-circuit Output Current	V_O = high, −7V ≤ V_{CM} ≤ + 12V(2)	35		250	mA
I_{OSD2}	Driver Short-circuit Output Current	V_O = low, − 7V ≤V_{CM} ≤ + 12V(2)	35		250	mA
I_{OSR}	Receiver Short-circuit Output Current	0 V ≤V_O ≤ V_{CC}	7		95	mA

(1) $\lvert\Delta V_{OD}\rvert$ and $\lvert\Delta V_{OC}\rvert$ are changes in magnitude of V_{OD} and V_{OC}, respectively when the input changes from high to low levels.
(2) Peak current

ELECTRICAL CHARACTERISTICS (continued)

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Switching Characteristics						
Driver						
T_{PLH}, T_{PHL}	Propagation Delay Input to Output	R_L = 54Ω, C_L = 100pF (See Figure 13 and Figure 17)	10	35	60	nS
T_{SKEW}	Driver Output Skew	R_L = 54Ω, C_L = 100 pF (See Figure 13 and Figure 17)		5	10	nS
T_R, T_F	Driver Rise and Fall Time	R_L = 54Ω, C_L = 100 pF (See Figure 13 and Figure 17)	3	8	40	nS
T_{ZH}, T_{ZL}	Driver Enable to Ouput Valid Time	C_L = 100 pF, R_L = 500Ω (See Figure 14 and Figure 18)		25	70	nS
T_{HZ}, T_{LZ}	Driver Output Disable Time	C_L = 15 pF, R_L = 500Ω (See Figure 14 and Figure 18)		30	70	nS
Receiver						
T_{PLH}, T_{PHL}	Propagation Delay Input to Output	R_L = 54Ω, C_L = 100 pF (See Figure 15 and Figure 17)	20	50	200	nS
T_{SKEW}	Receiver Output Skew	R_L = 54Ω, C_L = 100 pF (See Figure 15 and Figure 17)		5		nS
T_{ZH}, T_{ZL}	Receiver Enable Time	C_L = 15 pF, R_L = 1 kΩ (See Figure 16 and Figure 20)		20	50	nS
	Receiver Disable Time			20	50	nS
F_{MAX}	Maximum Data Rate		2.5			Mbps

TYPICAL PERFORMANCE CHARACTERISTICS

Output Current vs. Receiver Output Low Voltage

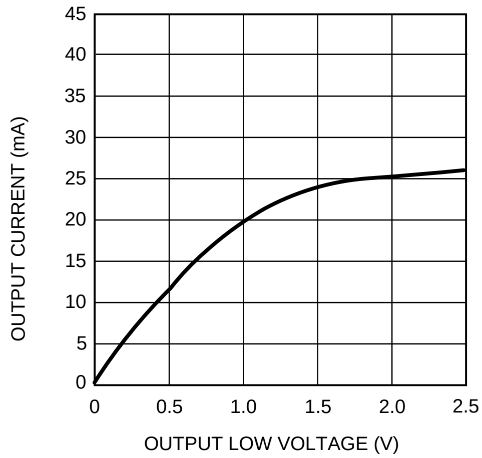


Figure 2.

Output Current vs. Receiver Output High Voltage

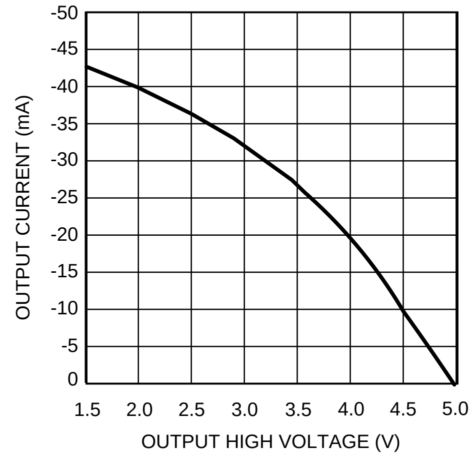


Figure 3.

Receiver Output High Voltage vs. Temperature

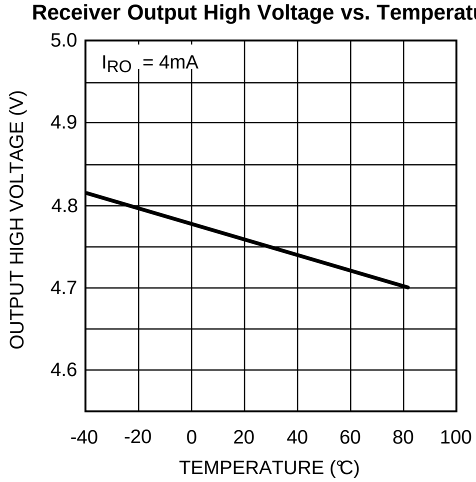


Figure 4.

Receiver Output Low-Voltage vs. Temperature

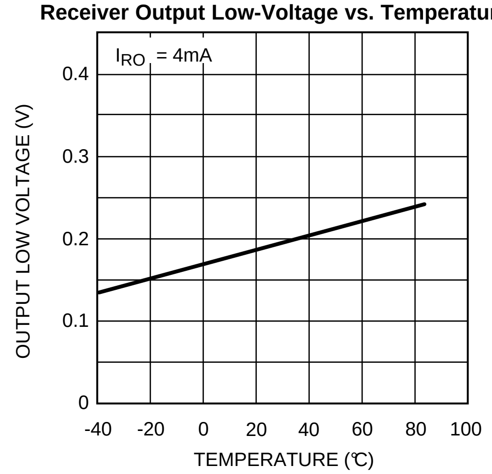


Figure 5.

Driver Output Current vs. Differential Output Voltage

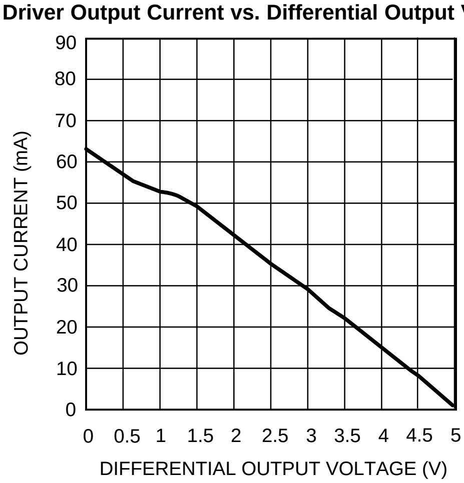


Figure 6.

Driver Differential Output Voltage vs. Temperature

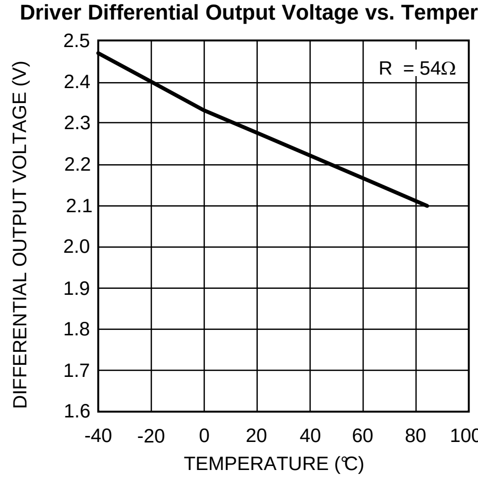


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Current vs. Driver Output Low Voltage

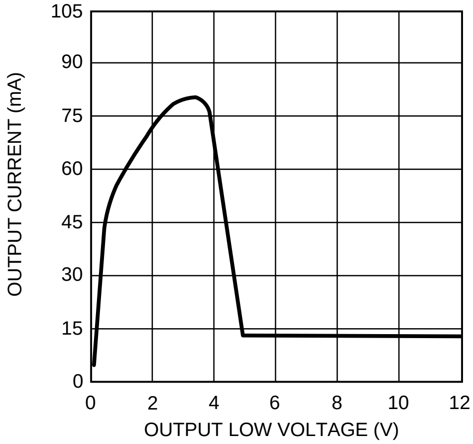


Figure 8.

Output Current vs. Driver Output High Voltage

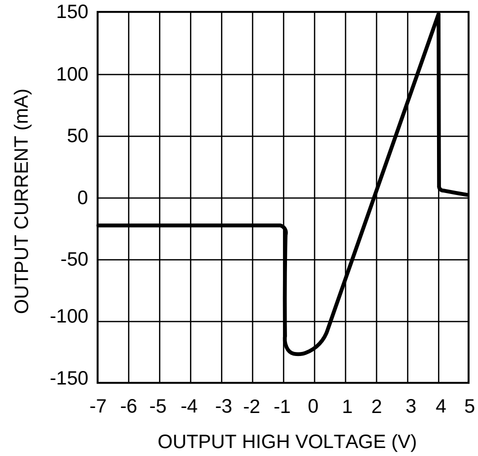


Figure 9.

Supply Current vs. Temperature

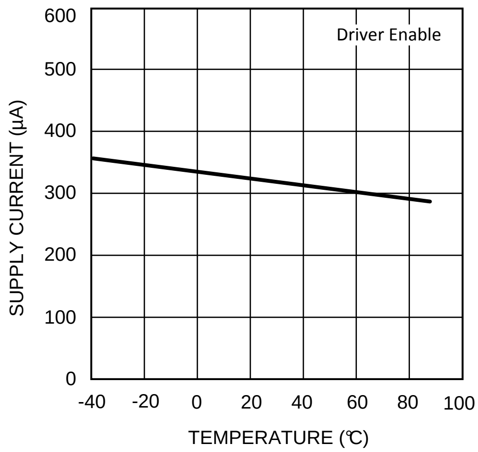


Figure 10.

PARAMETER MEASURING INFORMATION

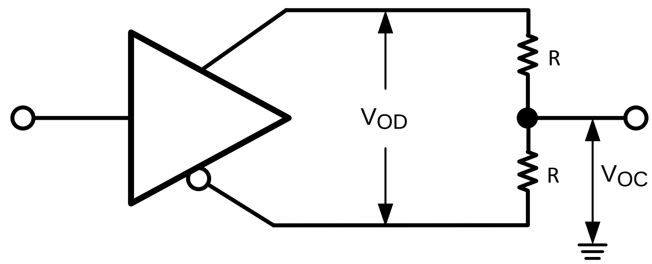


Figure 11. Test Circuit for V_{OD} and V_{OC}

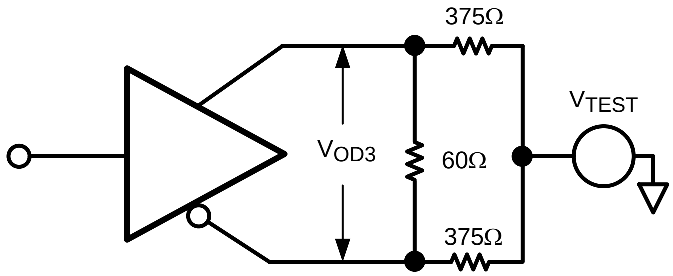


Figure 12. Test Circuit for V_{OD3}

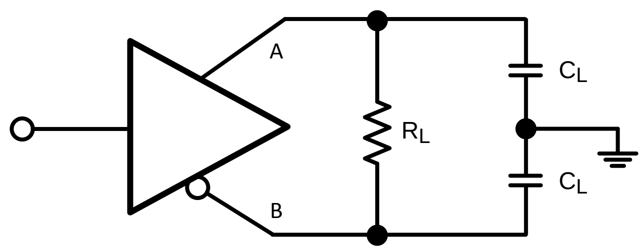


Figure 13. Test Circuit for Driver Propagation Delay

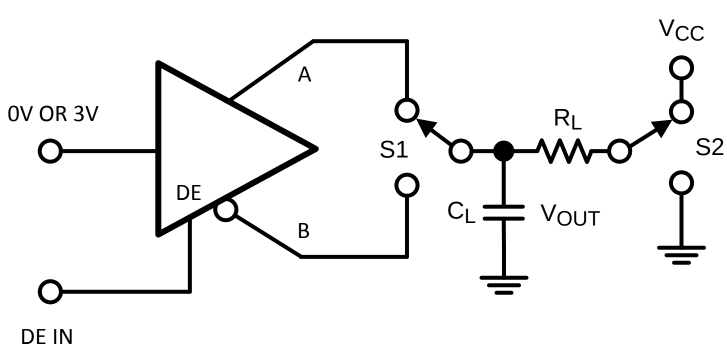


Figure 14. Test Circuit for Driver Enable / Disable

PARAMETER MEASURING INFORMATION (continued)

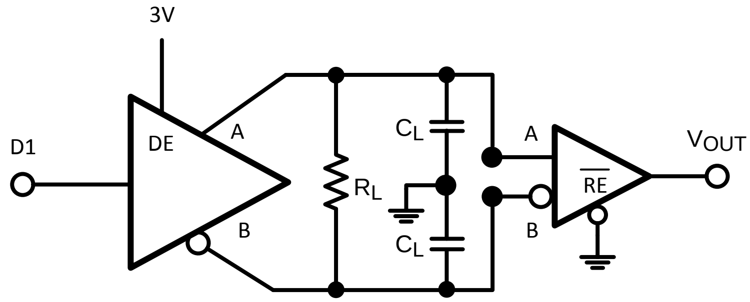


Figure 15. Test Circuit for Receiver Propagation Delay

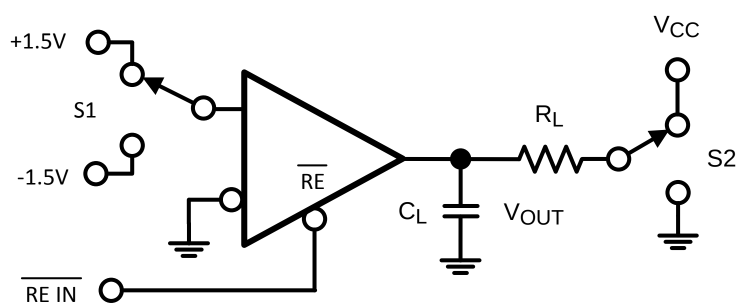


Figure 16. Test Circuit for Receiver Enable / Disable

Switching Characteristics

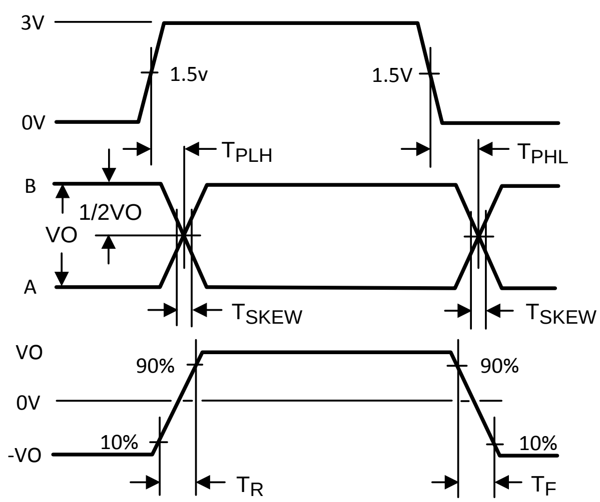


Figure 17. Driver Propagation Delay, Rise / Fall Time

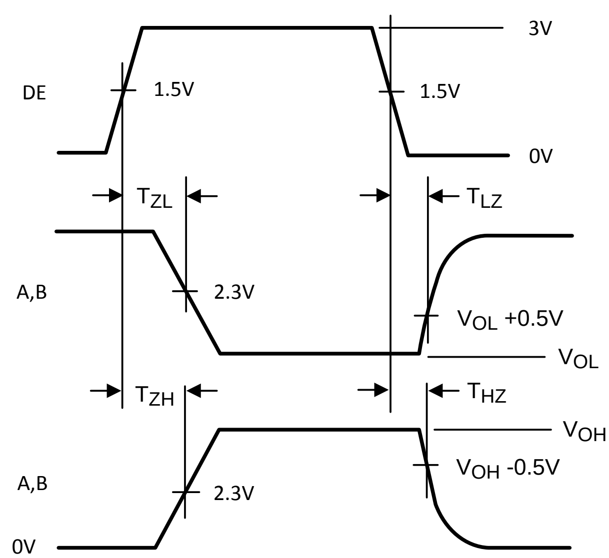


Figure 18. Driver Enable / Disable Time

PARAMETER MEASURING INFORMATION (continued)

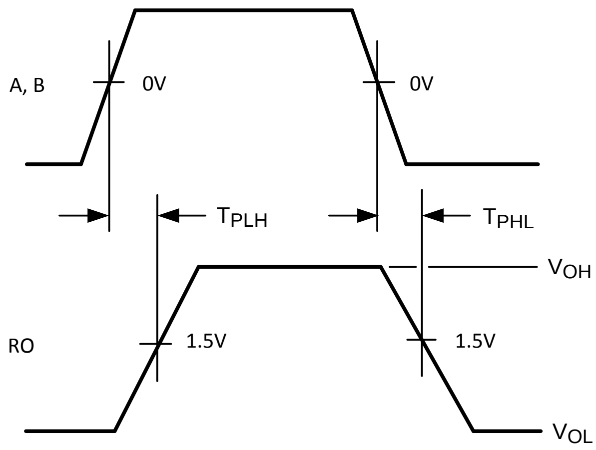


Figure 19. Receiver Propagation Delay

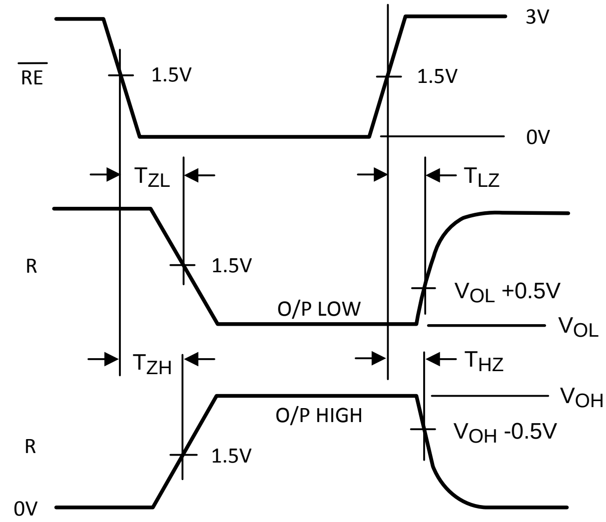


Figure 20. Receiver Enable / Disable Time

APPLICATION INFORMATION

Power Line Noise Filtering

A factor to consider in designing power and ground is noise filtering. A noise filtering circuit is designed to prevent noise generated by the integrated circuit (IC) as well as noise entering the IC from other devices. A common filtering method is to place by-pass capacitors (C_{bp}) between the power and ground lines.

Placing a by-pass capacitor (C_{bp}) with the correct value at the proper location solves many power supply noise problems. Choosing the correct capacitor value is based upon the desired noise filtering range. Since capacitors are not ideal, they may act more like inductors or resistors over a specific frequency range. Thus, many times two by-pass capacitors may be used to filter a wider bandwidth of noise. It is highly recommended to place a larger capacitor, such as 10µF, between the power supply pin and ground to filter out low frequencies and a 0.1µF to filter out high frequencies.

By-pass capacitors must be mounted as close as possible to the IC to be effective. Long leads produce higher impedance at higher frequencies due to stray inductance. Thus, this will reduce the by-pass capacitor's effectiveness. Surface mounted chip capacitors are the best solution because they have lower inductance.

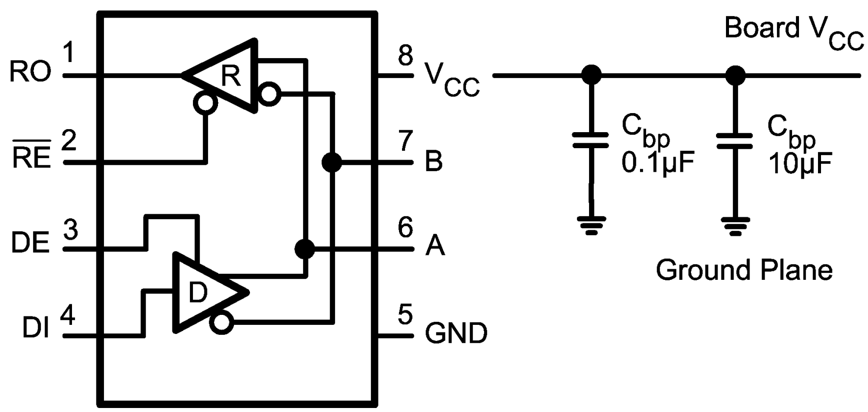


Figure 21. Placement of by-pass Capacitors, C_{bp}

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	**Page**
• Changed layout of National Data Sheet to TI format	12

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