LMV7231 Hex Window Comparator with 1.5% Precision and 400mV Reference

Check for Samples: LMV7231

FEATURES

- **(For V_S = 3.3V ±10%, Typical Unless Otherwise Noted)**
- **High Accuracy Voltage Reference: 400 mV**
- **Threshold Accuracy: ±1.5% (max)**
- **Wide Supply Voltage Range +2.2V to +5.5V**
- **Input/Output Voltage Range Above V+**
- **Internal Hysteresis: 6mV**
- **Propagation Delay: 2.6 µs to 5.6 µs**
- **Supply Current 7.7 µA Per Channel**
- **24 Lead WQFN Package**
- **Temperature Range: -40°C to 125°C**

APPLICATIONS

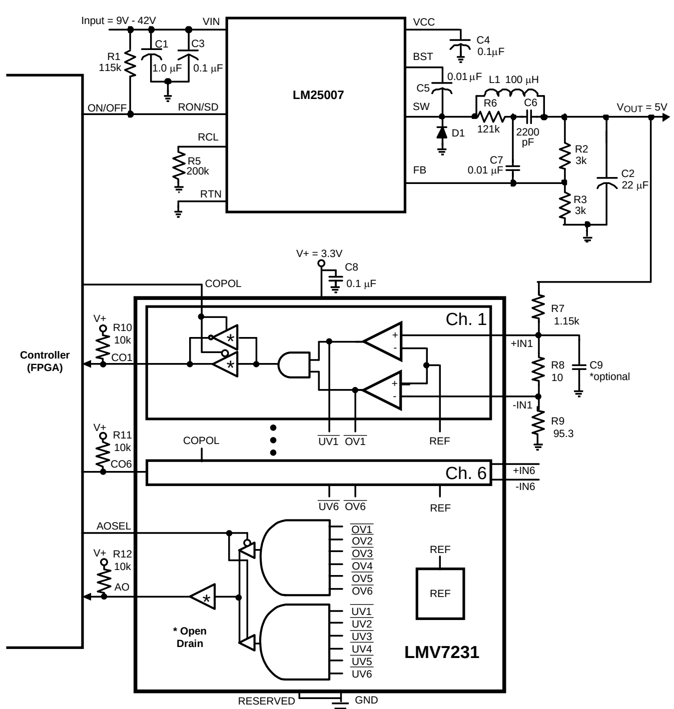
- **Power Supply Voltage Detection**
- **Battery Monitoring**
- **Handheld Instruments**
- **Relay Driving**
- **Industrial Control Systems**

DESCRIPTION

The LMV7231 is a 1.5% accurate Hex Window Comparator which can be used to monitor power supply voltages. The device uses an internal 400mV reference for the comparator trip value. The comparator set points can be set via external resistor dividers. The LMV7231 has 6 outputs (CO1-CO6) that signal an under-voltage or over-voltage event for each power supply input. An output (AO) is also provided to signal when any of the power supply inputs have an over-voltage or under-voltage event. This ability to signal an under-voltage or over-voltage event for the individual power supply inputs, in addition to an output to signal such an event on any of the power supply inputs adds unparalleled system protection capability.

The LMV7231's +2.2V to +5.5V power supply voltage range, low supply current, and input/output voltage range above V+ make it ideal for a wide range of power supply monitoring applications. Operation is ensured over the -40°C to +125°C temperature range. The device is available in a 24-pin WQFN package.

Typical Application Circuit



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

ESD Tolerance[(3)]	Human Body Model	2000V
	Machine Model	200V
Supply Voltage		6V
Voltage at Input/Output Pin		6V to (GND − 0.3V)
Output Current		10mA
Total Package Current		50mA
Storage Temp Range		−65°C to +150°C
Junction Temperature[(4)]		150°C
For soldering specifications: http://www.ti.com/lit/SNOA549		

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings[(1)]

Supply Voltage		2.2V to 5.5V
Junction Temperature Range[(2)]		−40°C to +125°C
Package Thermal Resistance, θ_{JA}	24 Lead WQFN	38°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

+3.3V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V+ = 3.3V ±10%, GND = 0V, and R_L > 1MΩ. **Boldface limits apply for T_A = –10°C to +70°C**.

Symbol	Parameter	Condition	Min[(1)]	Typ[(2)]	Max[(1)]ns	Units
V_{THR}	Threshold: Input Rising	R_L = 10kΩ	394 **391.4**	400	406 **408.6**	mV
V_{THF}	Threshold: Input Falling	R_L = 10kΩ	386 **383.8**	394	401 **403.2**	mV
V_{HYST}	Hysteresis ($V_{THR} - V_{THF}$)	R_L = 10kΩ	3.9	6.0	8.8	mV
I_{BIAS}	Input Bias Current	V_{IN} = V+, GND, and 5.5V	–5 **–15**	0.05	5 **15**	nA
V_{OL}	Output Low Voltage	I_L = 5mA		160	200 **250**	mV
I_{OFF}	Output Leakage Current	V_{OUT} = V+, 5.5V and 40mV of overdrive			0.4 **1**	µA
t_{PDHL1}	High-to-Low Propagation Delay (+IN falling)	10mV of overdrive		2.6	6	µs
t_{PDHL2}	High-to-Low Propagation Delay (-IN rising)	10mV of overdrive		5.4	10	µs

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

+3.3V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V+ = 3.3V ±10%, GND = 0V, and R_L > 1MΩ. **Boldface limits apply for T_A = –10°C to +70°C**.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)ns	Units
t_{PDLH1}	Low-to-High Propagation Delay (+IN rising)	10mV of overdrive		5.6	10	µs
t_{PDLH2}	Low-to-High Propagation Delay (-IN falling)	10mV of overdrive		2.8	6	µs
t_r	Output Rise Time	C_L= 10pF, R_L= 10kΩ		0.5		µs
t_f	Output Fall Time	C_L = 100pF, R_L = 10kΩ			0.25 **0.3**	µs
$I_{IN(1)}$	Digital Input Logic “1” Leakage Current				0.2 **1**	µA
$I_{IN(0)}$	Digital Input Logic “0” Leakage Current				0.2 **1**	µA
V_{IH}	Digital Input Logic “1” Voltage		**0.70 × V+**			V
V_{IL}	Digital Input Logic “0” Voltage				**0.30 × V+**	V
I_S	Power Supply Current	No loading (outputs high)		46	60 **84**	µA
$V_{TH}PSS$	V_{TH} Power Supply Sensitivity (3)	V+ Ramp Rate = 1.1ms V+ Step = 2.5V to 4.5V			+400	µV
		V+ Ramp Rate = 1.1ms V+ Step = 4.5V to 2.5V	–400			µV

(3) V_{TH} Power Supply Sensitivity is defined as the temporary shift in the internal voltage reference due to a step on the V+ pin.

CONNECTION DIAGRAM

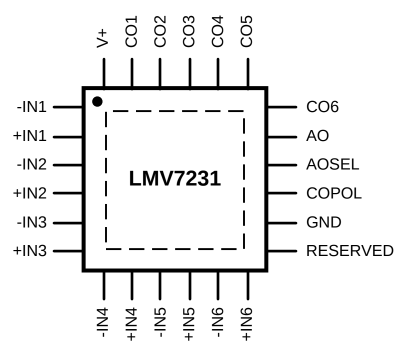
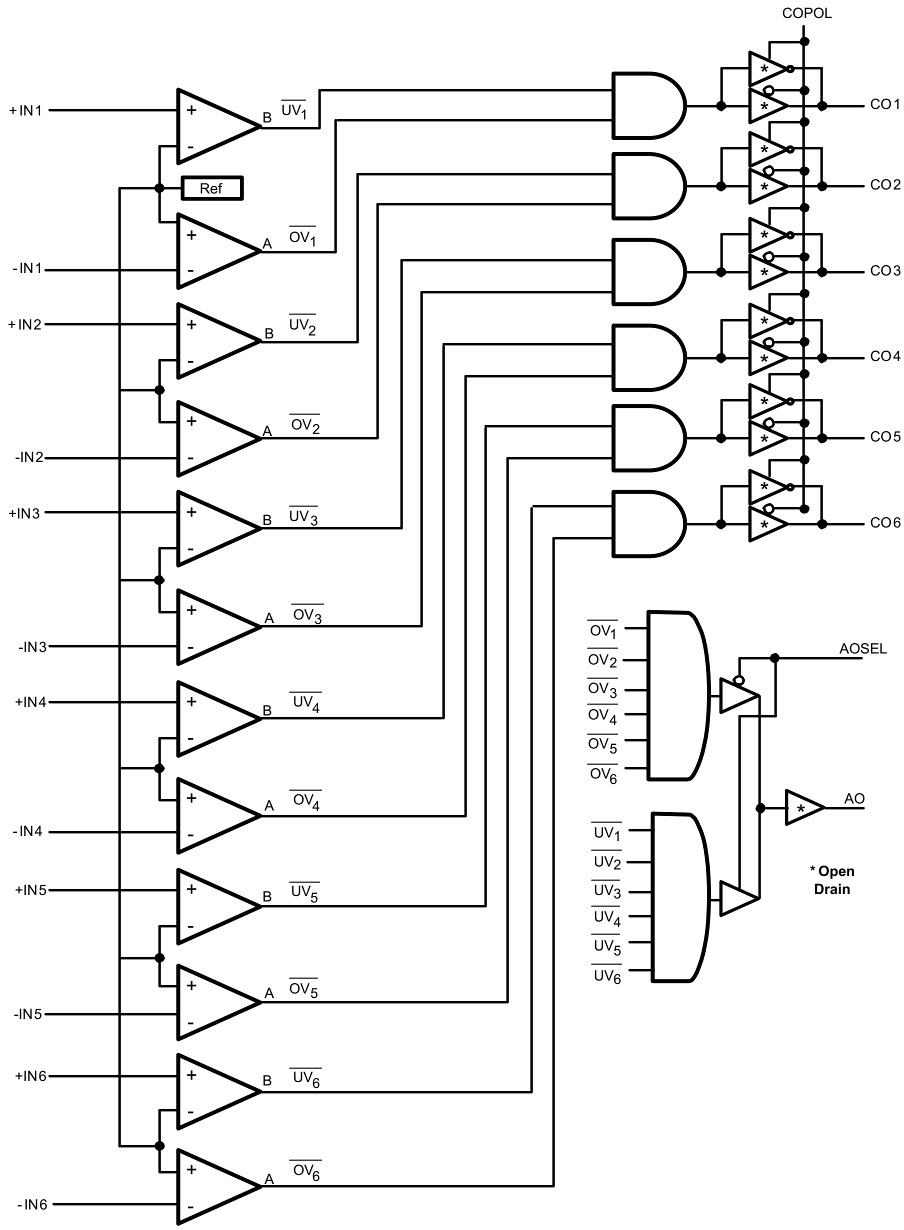


Figure 1. 24-Pin WQFN Package (Top View)
See Package RTW0024A

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	-IN1	Analog Input	Negative input for window comparator 1.
2	+IN1	Analog Input	Positive input for window comparator 1.
3	-IN2	Analog Input	Negative input for window comparator 2.
4	+IN2	Analog Input	Positive input for window comparator 2.
5	-IN3	Analog Input	Negative input for window comparator 3.
6	+IN3	Analog Input	Positive input for window comparator 3.
7	-IN4	Analog Input	Negative input for window comparator 4.
8	+IN4	Analog Input	Positive input for window comparator 4.
9	-IN5	Analog Input	Negative input for window comparator 5.
10	+IN5	Analog Input	Positive input for window comparator 5.
11	-IN6	Analog Input	Negative input for window comparator 6.
12	+IN6	Analog Input	Positive input for window comparator 6.
13	RESERVED	Digital Input	Connect to GND.
14	GND	Power	Ground reference pin for the power supply voltage.
15	COPOL	Digital Input	The state of this pin determines whether the CO1-CO6 pins are active “HIGH” or “LOW”. When tied LOW the CO1-CO6 outputs will go LOW to indicate an out of window comparison.
16	AOSEL	Digital Input	The state of this pin determines whether the AO pin is active on an over-voltage or under-voltage event. When tied LOW the AO output will be active upon an over-voltage event.
17	AO	Open-Drain NMOS Digital Output	This output is the ANDED combination of either the over-voltage comparator outputs or the under-voltage comparator outputs and is controlled by the state of the AOSEL. AO pin is active “LOW”.
18	CO6	Open-Drain NMOS Digital Output	Window comparator 6 NMOS open-drain output.
19	CO5	Open-Drain NMOS Digital Output	Window comparator 5 NMOS open-drain output.
20	CO4	Open-Drain NMOS Digital Output	Window comparator 4 NMOS open-drain output.
21	CO3	Open-Drain NMOS Digital Output	Window comparator 3 NMOS open-drain output.
22	CO2	Open-Drain NMOS Digital Output	Window comparator 2 NMOS open-drain output.
23	CO1	Open-Drain NMOS Digital Output	Window comparator 1 NMOS open-drain output.
24	V+	Power	Power supply pin.
DAP	DAP	Thermal Pad	Die Attach Paddle (DAP) connect to GND.

Block Diagram



Typical Performance Characteristics

V^+ = 3.3V and T_A =25°C unless otherwise noted.

+In Input Rising Threshold Distribution

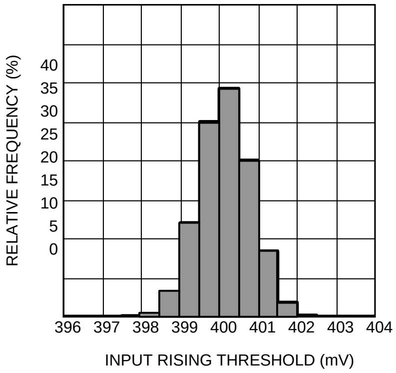


Figure 2.

−In Input Rising Threshold Distribution

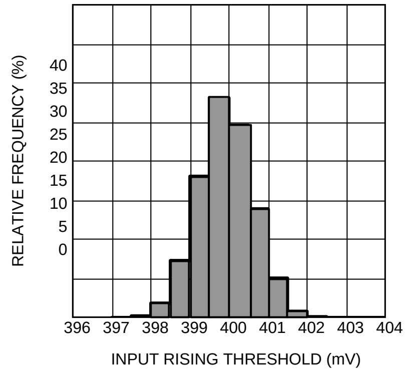


Figure 3.

+In Input Falling Threshold Distribution

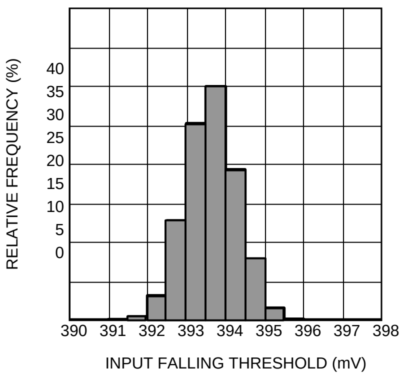


Figure 4.

−In Input Falling Threshold Distribution

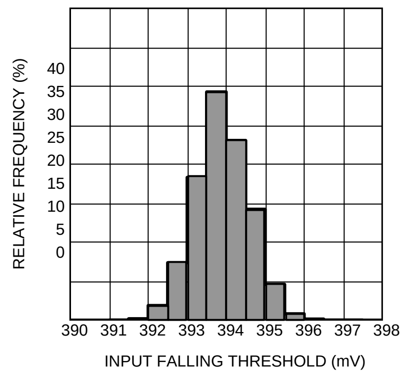


Figure 5.

+In Hysteresis Distribution

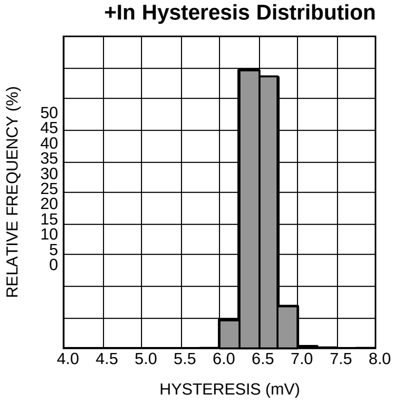


Figure 6.

−In Hysteresis Distribution

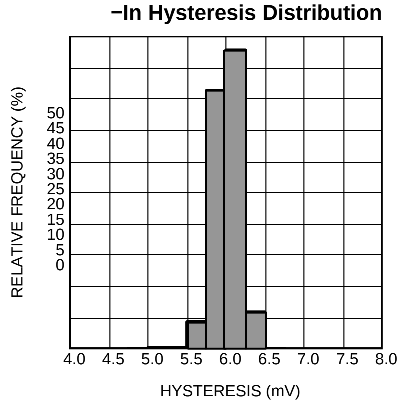


Figure 7.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A =25°C unless otherwise noted.

Input Rising Threshold Voltage vs. Temperature

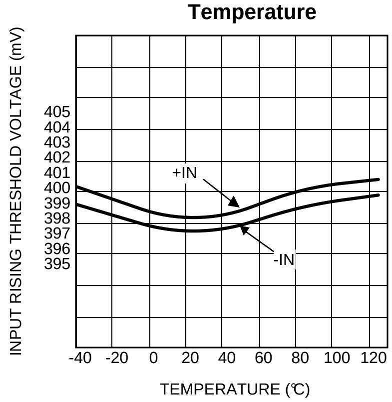


Figure 8.

Input Rising Threshold Voltage vs. Supply Voltage

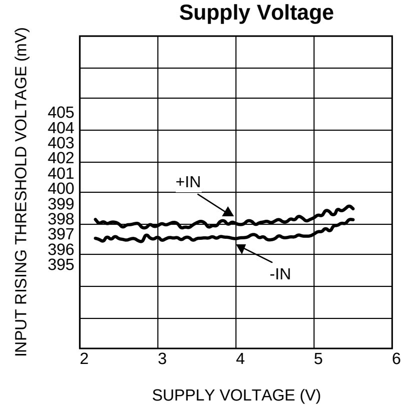


Figure 9.

Input Falling Threshold Voltage vs. Temperature

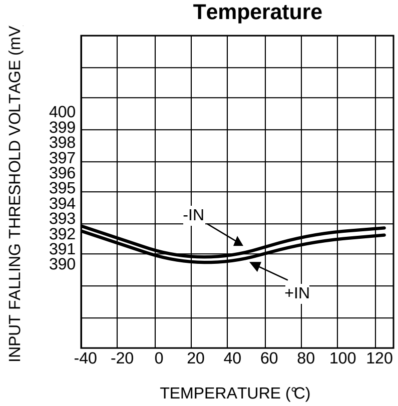


Figure 10.

Input Falling Threshold Voltage vs. Supply Voltage

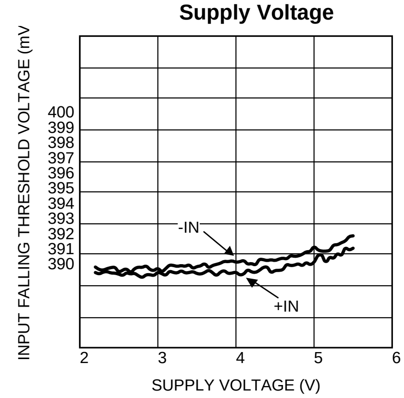


Figure 11.

Hysteresis vs. Temperature

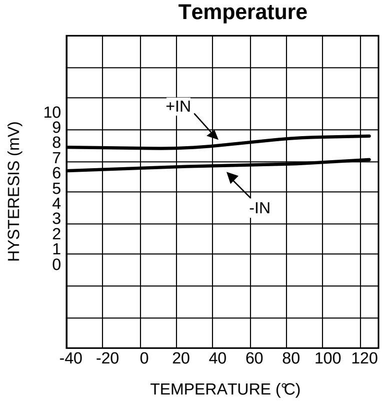


Figure 12.

Hysteresis vs. Supply Voltage

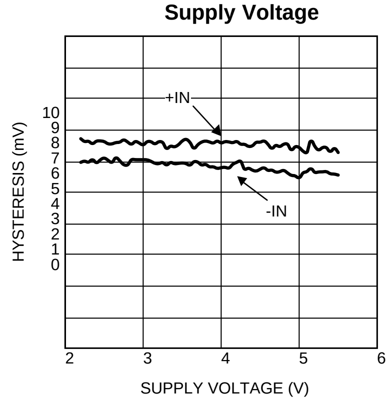


Figure 13.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A =25°C unless otherwise noted.

Supply Current vs. Supply Voltage and Temperature

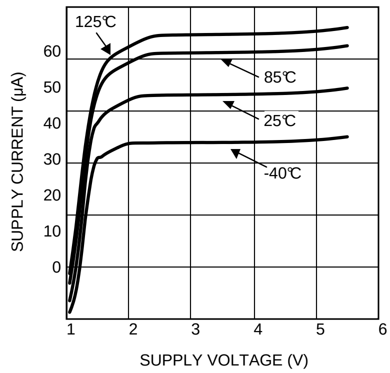


Figure 14.

Supply Current vs. Output Sink Current

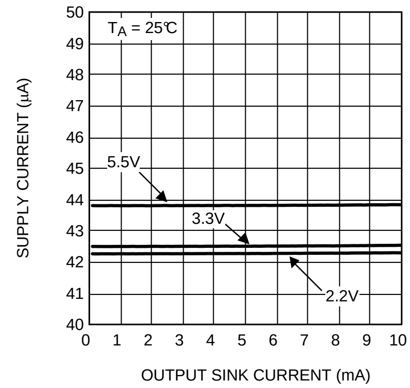


Figure 15.

Supply Current vs. Output Sink Current

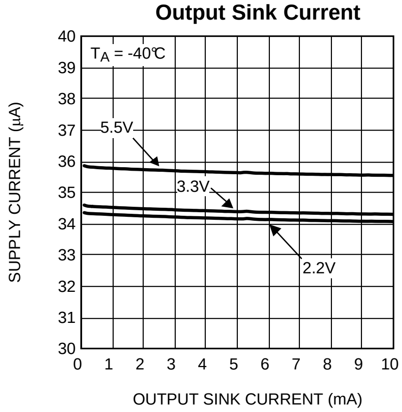


Figure 16.

Supply Current vs. Output Sink Current

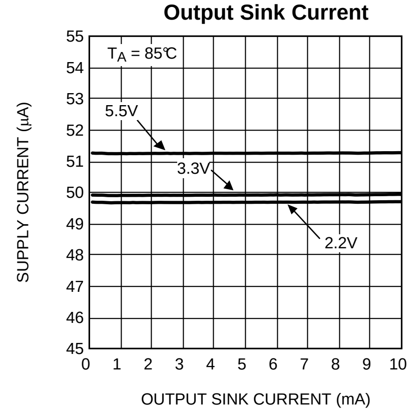


Figure 17.

Supply Current vs. Output Sink Current

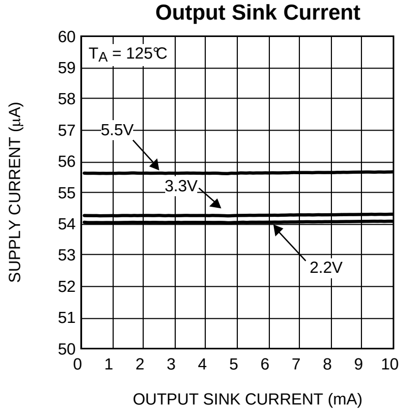


Figure 18.

Bias Current vs. Input Voltage

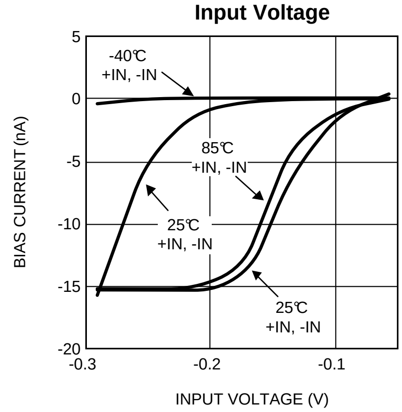


Figure 19.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A =25°C unless otherwise noted.

Bias Current vs. Input Voltage

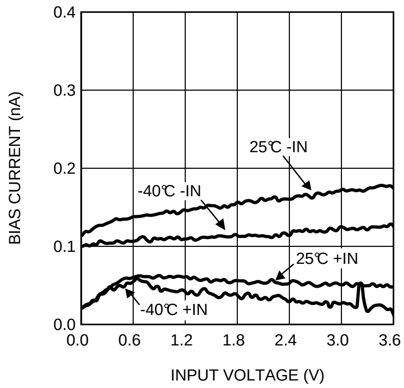


Figure 20.

Bias Current vs. Input Voltage

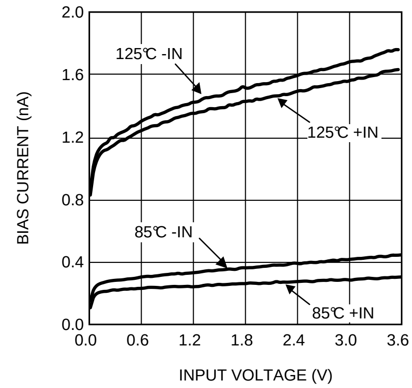


Figure 21.

Output Voltage Low vs. Output Sink Current

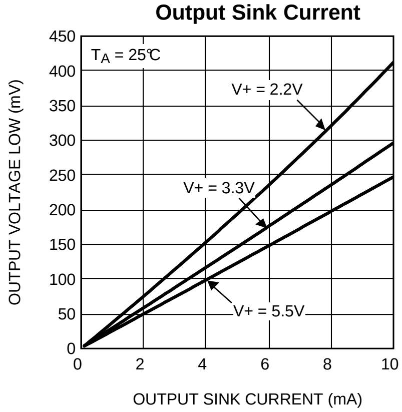


Figure 22.

Output Voltage Low vs. Output Sink Current

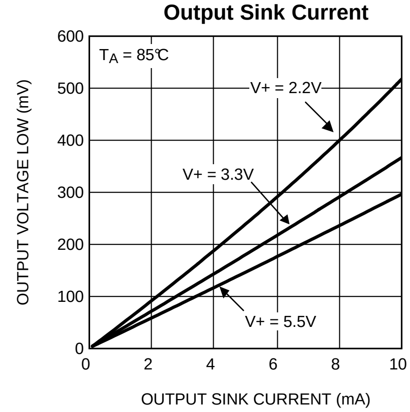


Figure 23.

Output Voltage Low vs. Output Sink Current

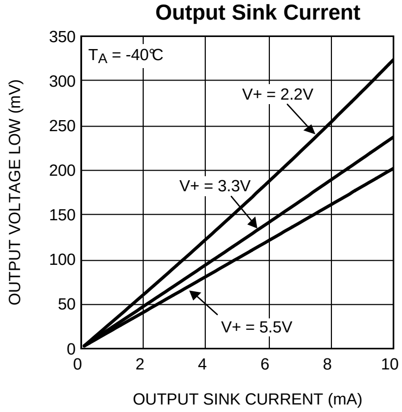


Figure 24.

Output Voltage Low vs. Output Sink Current

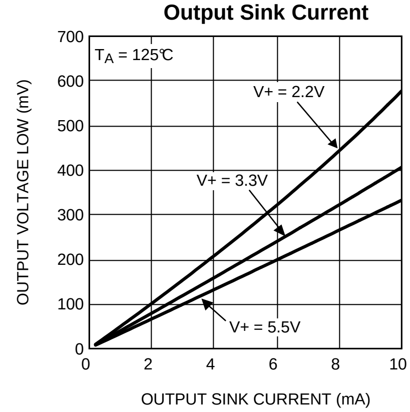


Figure 25.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A =25°C unless otherwise noted.

Output Short Circuit Current vs. Output Voltage

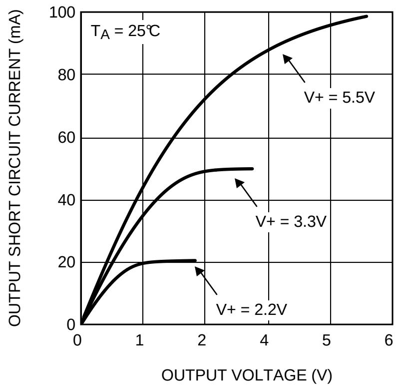


Figure 26.

Output Short Circuit Current vs. Output Voltage

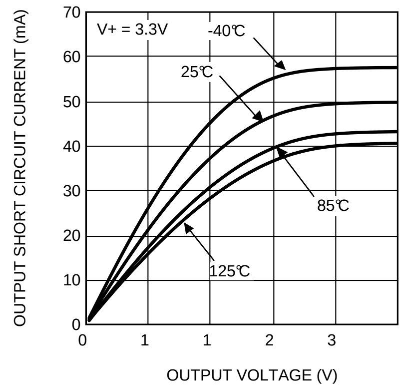


Figure 27.

Propagation Delay vs. Input Overdrive

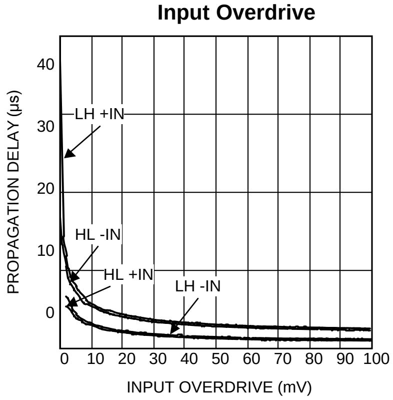


Figure 28.

Rise and Fall Times vs. Output Pull-Up Resistor

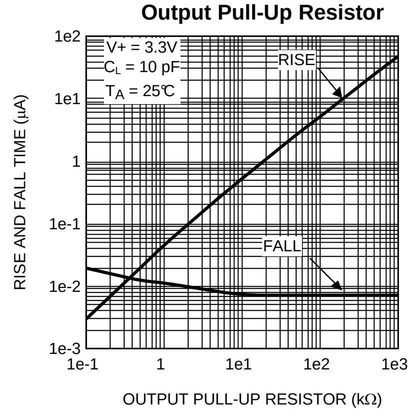


Figure 29.

Propagation Delay

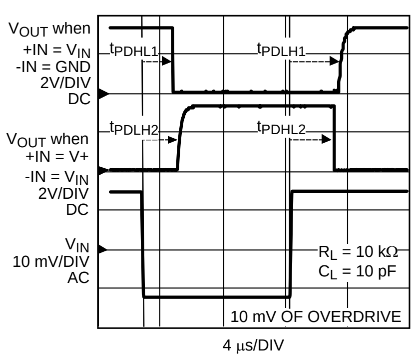


Figure 30.

Output Leakage Current vs. Output Voltage

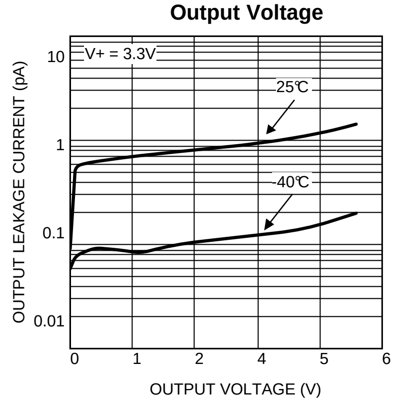


Figure 31.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A =25°C unless otherwise noted.

Output Leakage Current vs. Output Voltage

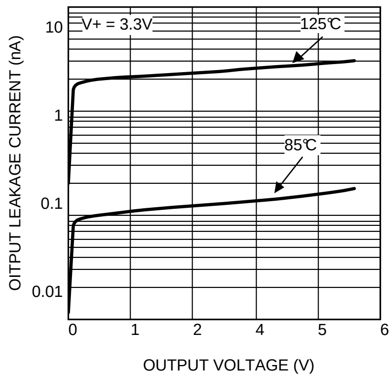


Figure 32.

APPLICATION INFORMATION

3 RESISTOR VOLTAGE DIVIDER SELECTION

The LMV7231 trip points can be set by external resistor dividers as shown in Figure 33

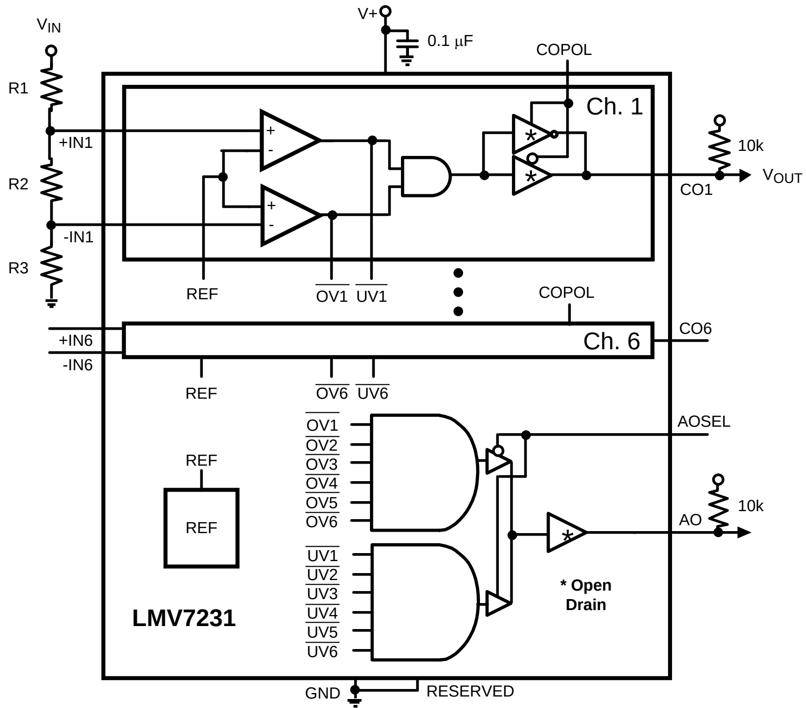
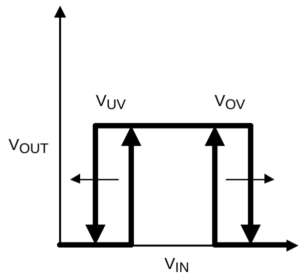


Figure 33. External Resistor Dividers

Each trip point, over-voltage, V_{OV}, and under-voltage, V_{UV}, can be optimized for a falling supply, V_{THF}, or a rising supply, V_{THR}. Therefore there are $2^2 = 4$ different optimization cases. Exiting the voltage detection window (Figure 34), rising into and out of the window (Figure 35), entering the window (Figure 36), falling into and out of the window (Figure 37). Note that for each case each trip point can be optimized for either a rising or falling signal, not both. The governing equations make it such that if the same resistor, R3, and over/under-voltage ratio, V_{OV}/V_{UV}, is used across the channels the same nominal current will travel through the resistor ladder. As a result R2 will also be the same across channels and only R1 needs to change to set voltage detection window maximizing reuse of resistor values and minimizing design complexity. Select the R3 resistor value to be below 100kΩ so the current through the divider ladder is much greater than the LMV7231 bias current. If the current traveling through the resistor divider is on the same magnitude of the LMV7231 I_{BIAS}, the I_{BIAS} current will create error in your circuit and cause trip voltage shifts. Keep in mind the greatest error due to I_{BIAS} will be caused when that current passes through the greatest equivalent resistance, REQ = R1ǁ(R2+R3), which will be seen by the positive input of the window comparator, +IN.



R3 set

$R2 = R3((V_{THF}/V_{THR})V_{OV}/V_{UV} – 1)$

$R1 = R3((1/V_{THR})V_{OV} - (V_{THF}/V_{THR})V_{OV}/V_{UV})$

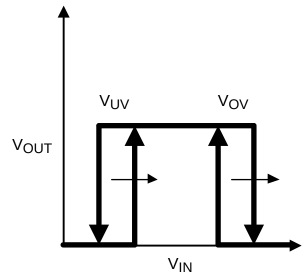
Ex. V_{OV} = 3.465V, V_{UV} = 3.135V, i.e. V_{RANGE} = 3.3V +/- 5%

R3 set to 10 kΩ

R2 = 10k((0.394/0.4)3.465/3.135 – 1) ≈ 887Ω

R1 = 10k((1/0.4)3.465 - (0.394/0.4)3.465/3.135) ≈ 75 kΩ

Figure 34. Exiting the Voltage Detection Window



R3 set

$R2 = R3(V_{OV}/V_{UV} – 1)$

$R1 = R3((1/V_{THR})V_{OV} - V_{OV}/V_{UV})$

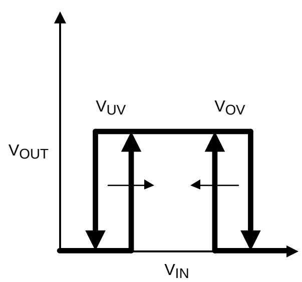
Ex. V_{OV} = 3.465V, V_{UV} = 3.135V, i.e. V_{RANGE} = 3.3V +/- 5%

R3 set to 10 kΩ

R2 = 10k((3.465/3.135) – 1) ≈ 1.05 kΩ

R1 = 10k((1/0.4)3.465 – 3.465/3.135) ≈ 75 kΩ

Figure 35. Rising Into and Out Of the Voltage Detection Window



R3 set

$R2 = R3((V_{THR}/V_{THF})V_{OV}/V_{UV} – 1)$

$R1 = R3((1/V_{THF})V_{OV} - (V_{THR}/V_{THF})V_{OV}/V_{UV})$

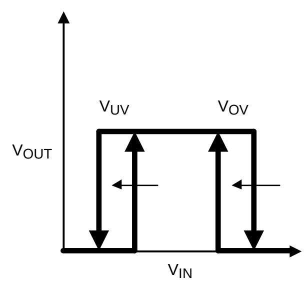
Ex. V_{OV} = 3.465V, V_{UV} = 3.135V, i.e. V_{RANGE} = 3.3V +/- 5%

R3 set to 10 kΩ

R2 = 10k((0.4/0.394)3.465/3.135 – 1) ≈ 1.21 kΩ

R1 = 10k((1/0.394)3.465 - (0.4/0.394)3.465/3.135) ≈ 76.8 kΩ

Figure 36. Entering the Voltage Detection Window



R3 set

$R2 = R3(V_{OV}/V_{UV} – 1)$

$R1 = R3((1/V_{THF})V_{OV} - V_{OV}/V_{UV})$

Ex. V_{OV} = 3.465V, V_{UV} = 3.135V, i.e. V_{RANGE} = 3.3V +/- 5%

R3 set to 10 kΩ

R2 = 10k((3.465/3.135) – 1) ≈ 1.05 kΩ

R1 = 10k((1/0.394)3.465 – 3.465/3.135) ≈ 76.8 kΩ

Figure 37. Falling Into and Out Of the Voltage Detection Window

INPUT/OUTPUT VOLTAGE RANGE ABOVE V+

The LMV7231 Hex Window Comparator with 1.5% precision can accurately monitor up to 6 power rails or batteries at one time. The input and output voltages of the device can exceed the supply voltage, V+, of the comparator, and can be up to the absolute maximum ratings without causing damage or performance degradation. The typical µC input pin with crowbar diode ESD protection circuitry will not allow the input to go above V+, and thus its usefulness is limited in power supply supervision applications.

The supply independent inputs of the window comparator blocks allow the LMV7231 to be tolerant of system faults. For example if the power is suddenly removed from the LMV7231 due to a system malfunction yet there still exists a voltage on the input, this will not be an issue as long as the monitored input voltage does not exceed absolute maximum ratings. Another example where this feature comes in handy is a battery sense application such as the one in Figure 38. The boards may be sitting on the shelf unbiased with V+ grounded, and yet have a fully charged battery on board. If the comparator measuring the battery had crowbar diodes, the diode from –IN to V+ would turn on, sourcing current from the battery eventually draining the battery. However, when using the LMV7231 no current, except the low input bias current of the device, will flow into the chip, and the battery charge will be preserved.

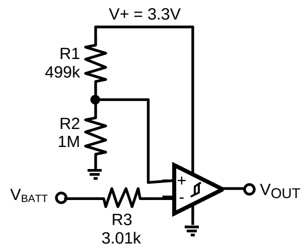


Figure 38. Battery Sense Application

The output pin voltages of the device can also exceed the supply voltage, V+, of the comparator. This provides extra flexibility and enables designs which pull up the outputs to higher voltage levels to meet system requirements. For example it's possible to run the LMV7231 at its minimum operating voltage, V+ = +2.2V, but pull up the output up to the absolute maximum ratings to bias a blue LED, with a forward voltage of V_F = +4V.

In a power supply supervision application the hardwired LMV7231 is a sound solution compared to the uC with software alternative for several reasons. First, startup is faster. During startup you don't need to account for code loading time, oscillator ramp time, and reset time. Second, operation is quick. The LMV7231 has a maximum propagation delay in the µs and isn't affected by sampling and conversion delays related to reading data, calculating data, and setting flags. Third, less overhead. The LMV7231 doesn't require an expensive power consuming microcontroller nor is it dependent on controller code which could get damaged or crash.

POWER SUPPLY BYPASSING

Bypass the supply pin, V+, with a 0.1 µF ceramic capacitor placed close to the V+ pin. If transients with rise/fall times of 100's µs and magnitudes of 100's mV are expected on the power supply line a RC low pass filter network as shown in Figure 39 is recommended for additional bypassing. If no such bypass network is used power supply transients can cause the internal voltage reference of the comparator to temporarily shift potentially resulting in a brief incorrect comparator output. For example if an RC network with 100Ω resistance and 10µF capacitance (1.1ms rise time) is used the voltage reference will shift temporarily the amount, V_{TH} Power Supply Sensitivity (V_{TH}PSS), specified in the Electrical Characteristics table.

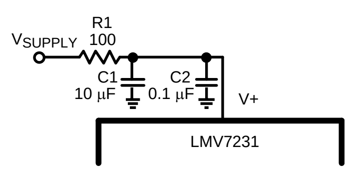


Figure 39. Power Supply Bypassing

POWER SUPPLY SUPERVISION

Figure 40 shows a power supply supervision circuit utilizing the LMV7231. This application uses the efficient, easy to use LM25007 step-down switching regulator. This switching regulator can handle a 9V – 42V input voltage range and it's regulated output voltage is set to 5V with R2 = R3 = 3kΩ.

$$V_{OUT} = 2.5 \times (R2 + R3)/R3$$

$$= 2.5 \times (3k + 3k)/3k = 5V \quad (1)$$

Resistor R6 and capacitors C6, C7 are utilized to minimize output ripple voltage per the LM25007 evaluation board application note.

The comparator voltage window is set to 5V +/- 5% by R7=1.15kΩ , R8=10Ω, R9=95.3Ω. See 3 RESISTOR VOLTAGE DIVIDER SELECTION section in the Application Information section of the datasheet for details on how to set the comparator voltage window.

With components selected the output ripple voltage seen on the LM25007 is approximately 30 - 35mV and is reduced to about 4mV at the comparator input, +IN1, by the resistor divider. This ripple voltage can be reduced multiple ways. First, user can operate the device in continuous conduction mode rather than discontinuous conduction mode. To do this increase the load current of the device (see LM25007 datasheet for more details). However, make sure not to exceed the power rating of the resistors in the resistor ladder. Second, ripple can be reduced further with a bypass cap, C9, at the resistor divider. If desired a user can select a 1uF capacitor to achieve less than 3mV ripple at +IN1. However, there is a tradeoff and adding capacitance at this node will lower the system response time.

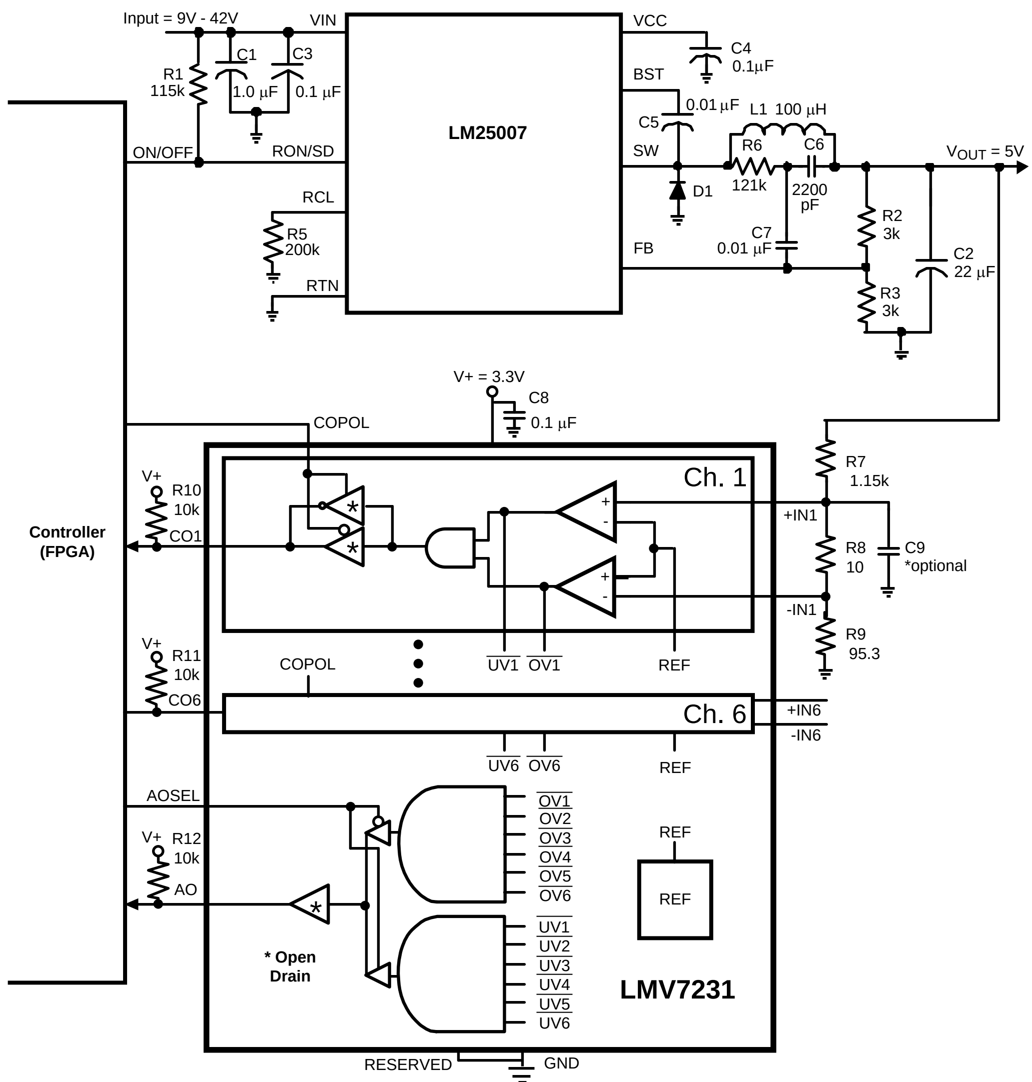


Figure 40. Power Supply Supervision

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV7231SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L7231SQ	Samples
LMV7231SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L7231SQ	Samples
LMV7231SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L7231SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION

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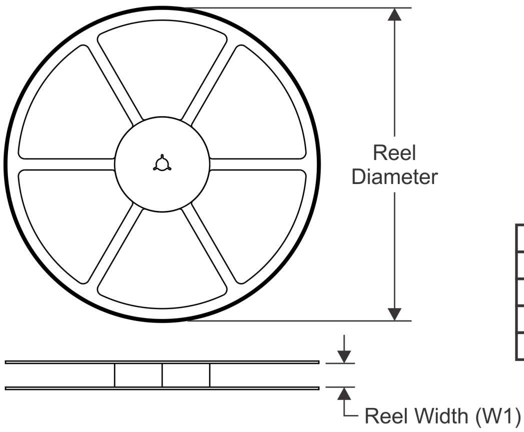
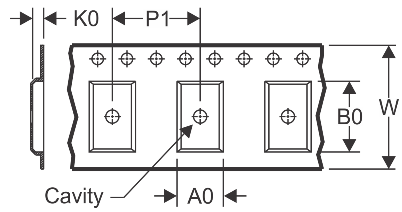
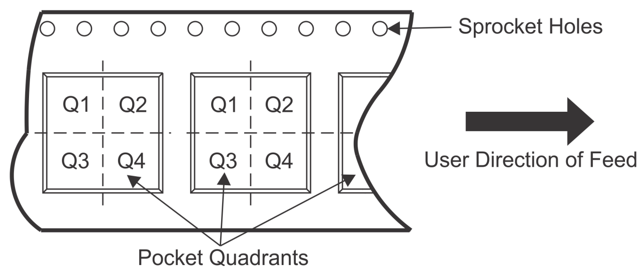


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

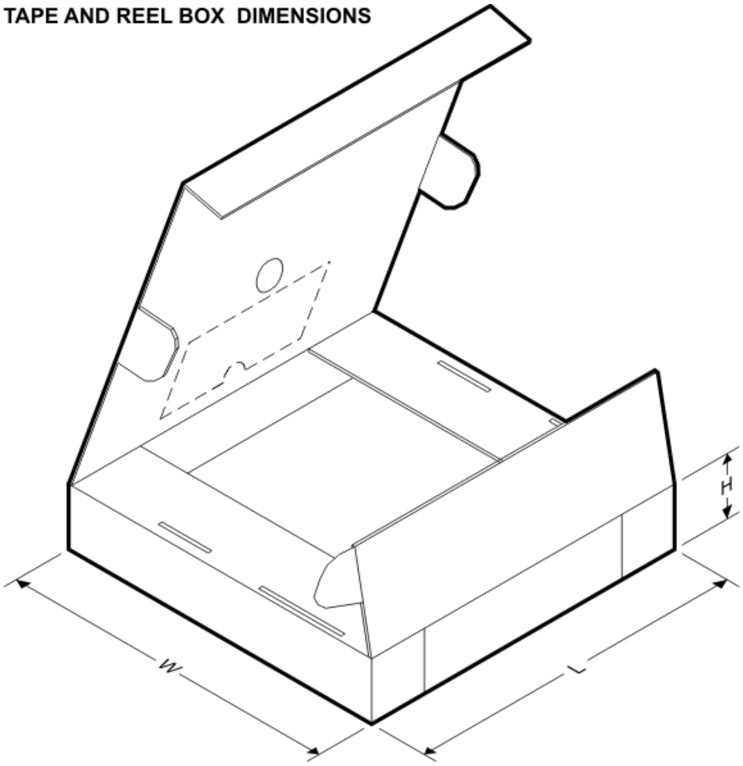
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7231SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMV7231SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMV7231SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

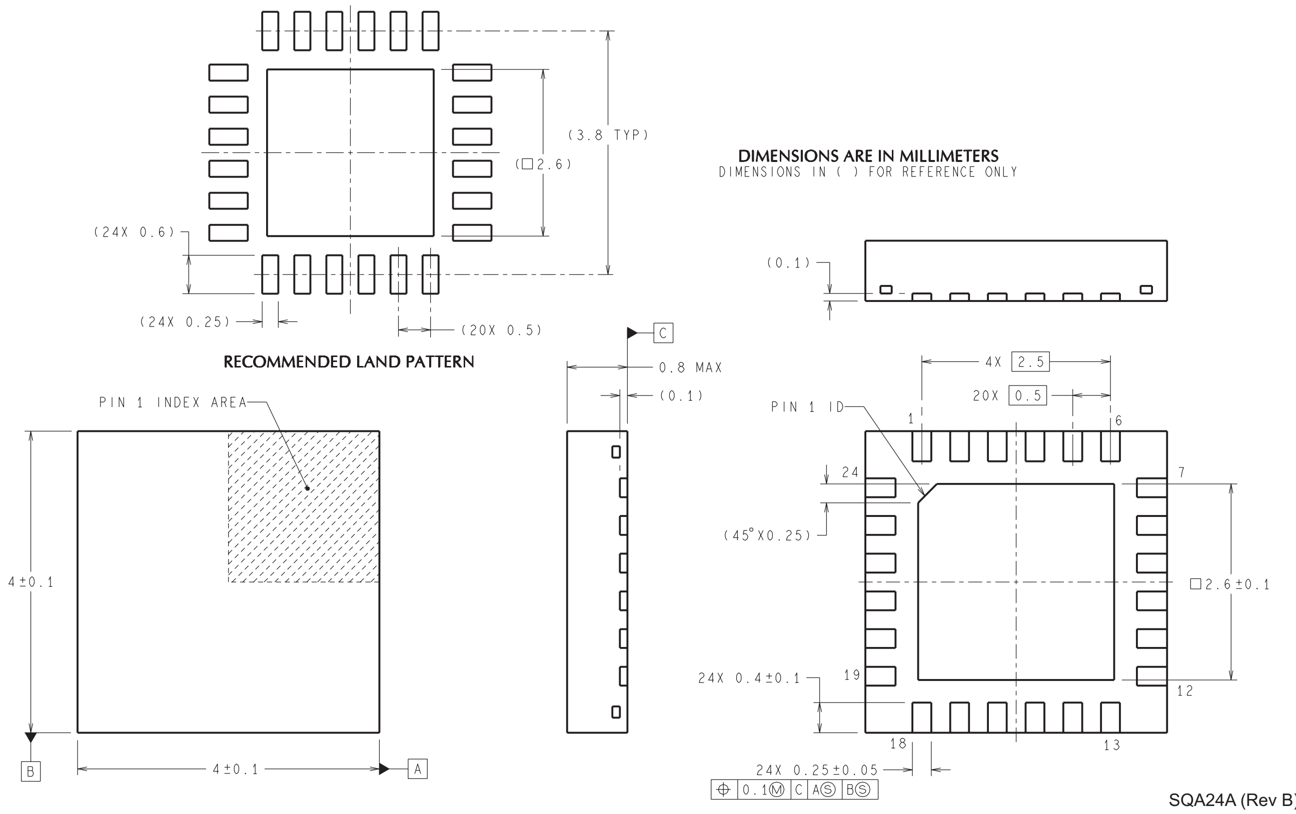
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7231SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LMV7231SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LMV7231SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

RTW0024A



SQA24A (Rev B)

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