LMZ22003 3A SIMPLE SWITCHER® Power Module with 20V Maximum Input Voltage

Check for Samples: LMZ22003

FEATURES

- **Integrated Shielded Inductor**
- **Simple PCB Layout**
- **Frequency Synchronization Input (650 kHz to 950 kHz)**
- **Flexible Startup Sequencing Using External Soft-start, Tracking and Precision Enable**
- **Protection Against Inrush Currents and Faults such as Input UVLO and Output Short Circuit**
- **– 40°C to 125°C Junction Temperature Range**
- **Single Exposed Pad and Standard Pinout for Easy Mounting and Manufacturing**
- **Fast Transient Response for Powering FPGAs and ASICs**
- **Fully Enabled for Webench® Power Designer**
- **Pin Compatible with LMZ23605/LMZ23603/LMZ22005**

APPLICATIONS

- **Point of Load Conversions from 12V Input Rail**
- **Time Critical Projects**
- **Space Constrained / High Thermal Requirement Applications**
- **Negative Output Voltage Applications See AN-2027 SNVA425**

Top View Bottom View

Figure 1. Easy To Use 7 Pin Package
10.16 x 13.77 x 4.57 mm (0.4 x 0.542 x 0.18 in)
θ_{JA} = 12°C/W, θ_{JC} = 1.9°C/W (1)
RoHS Compliant
Peak Reflow Case Temp = 245°C
Power Module SMT Guidelines

DESCRIPTION

The LMZ22003 SIMPLE SWITCHER© power module is an easy-to-use step-down DC-DC solution capable of driving up to 3A load. The LMZ22003 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ22003 can accept an input voltage rail between 6V and 20V and deliver an adjustable and highly accurate output voltage as low as 0.8V. The LMZ22003 only requires two external resistors and three external capacitors to complete the power solution. The LMZ22003 is a reliable and robust design with the following protection features: thermal shutdown, programmable input under-voltage lockout, output over-voltage protection, short-circuit protection, output current limit, and allows startup into a pre-biased output. The sync input allows synchronization over the 650 to 950 kHz switching frequency range.

ELECTRICAL SPECIFICATIONS

- **18W Maximum Total Output Power**
- **Up to 3A Output Current**
- **Input Voltage Range 6V to 20V**
- **Output Voltage Range 0.8V to 6V**
- **Efficiency up to 92%**

PERFORMANCE BENEFITS

- **High Efficiency Reduces System Heat Generation**
- **Complies with EN55022 Class B** (2)
- **Low Component Count, Only 5 External Components**
- **Low Output Voltage Ripple**
- **Uses PCB as Heat Sink, no Airflow Required**

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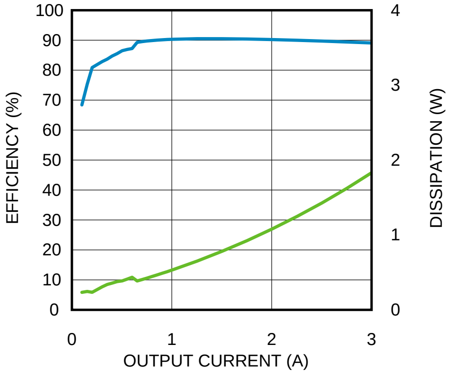
(1) Theta JA measured on a 3.5" x 3.5" four layer board, with three ounce copper on outer layers and two ounce copper on inner layers, sixty thermal vias, no air flow, and 1W power dissipation. Refer to application note layout diagrams.

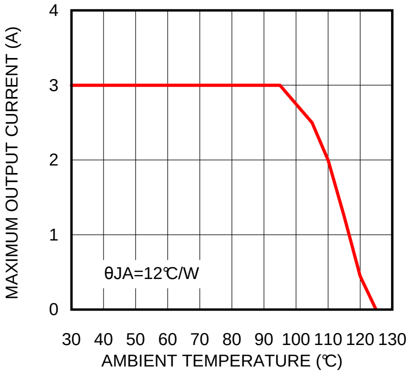
(2) EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See AN-2125 SNVA473 and layout for information on device under test. Vin = 12V, Vo = 3.3V, Io = 3A

System Performance

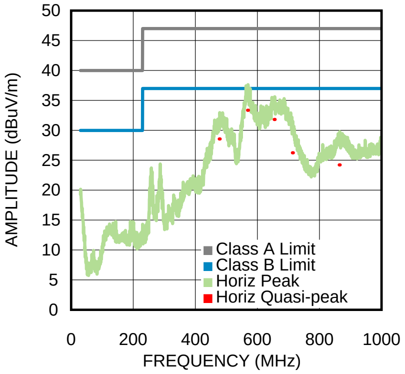
Efficiency V_{IN} = 12V V_{OUT} = 5.0V



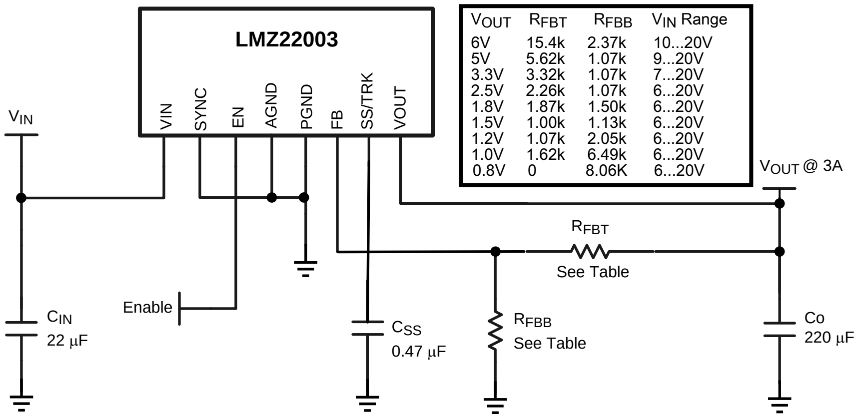
Thermal Derating Curve
V_{IN} = 12V V_{OUT} = 5.0V



Radiated EMI (EN 55022)
of Demo Board (See AN-2125)



Simplified Application Schematic



V_{OUT}	R_{FBT}	R_{FBB}	V_{IN} Range
6V	15.4k	2.37k	10...20V
5V	5.62k	1.07k	9...20V
3.3V	3.32k	1.07k	7...20V
2.5V	2.26k	1.07k	6...20V
1.8V	1.87k	1.50k	6...20V
1.5V	1.00k	1.13k	6...20V
1.2V	1.07k	2.05k	6...20V
1.0V	1.62k	6.49k	6...20V
0.8V	0	8.06K	6...20V

Connection Diagram

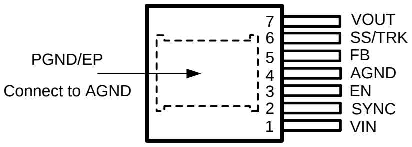


Figure 2. 7-Lead PFM
Top View

Pin Descriptions

Pin	Name	Description
1	VIN	Supply input — Nominal operating range is 6V to 20V . A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and exposed pad (PGND).
2	SYNC	Sync Input — Apply a CMOS logic level square wave whose frequency is between 650 kHz and 950 kHz to synchronize the PWM operating frequency to an external frequency source. When not using synchronization connect to ground. The module free running PWM frequency is 812 kHz (Typ).
3	EN	Enable — Input to the precision enable comparator. Rising threshold is 1.279V typical. Once the module is enabled, a 21 uA source current is internally activated to facilitate programmable hysteresis.
4	AGND	Analog Ground — Reference point for all stated voltages. Must be externally connected to PGND (EP).
5	FB	Feedback — Internally connected to the regulation amplifier, over-voltage comparators. The regulation reference point is 0.796V at this input pin. Connect the feedback resistor divider between the output and AGND to set the output voltage.
6	SS/TRK	Soft-Start/Track — To extend the 1.6 mSec internal soft-start connect an external soft start capacitor. For tracking connect to an external resistive divider connected to a higher priority supply rail. See Design Steps for the LMZ22003 Application section
7	VOUT	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and exposed pad.
EP	PGND	Exposed Pad / Power Ground Electrical path for the power circuits within the module. — NOT Internally connected to AGND / pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

VIN to PGND	-0.3V to 24V
EN, SYNC to AGND	-0.3V to 5.5V
SS/TRK, FB to AGND	-0.3V to 2.5V
AGND to PGND	-0.3V to 0.3V
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility (3)	± 2 kV
Peak Reflow Case Temperature (30 sec)	245°C
For soldering specifications, refer to the following document: www.ti.com/lit/snoa549c	

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

Operating Ratings (1)

VIN	6V to 20V
EN, SYNC	0V to 5.0V
Operation Junction Temperature	−40°C to 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, Vout = 3.3V

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
SYSTEM PARAMETERS						
Enable Control						
V_{EN}	EN threshold trip point	V_{EN} rising	**1.10**	1.279	**1.458**	V
V_{EN-HYS}	EN input hysteresis current	V_{EN} > 1.279V		–21		µA
Soft-Start						
I_{SS}	SS source current	V_{SS} = 0V	**40**	50	**60**	µA
t_{SS}	Internal soft-start interval			1.6		msec
Current Limit						
I_{CL}	Current limit threshold	d.c. average	**3.4**			A
Internal Switching Oscillator						
f_{osc}	Free-running oscillator frequency	Sync input connected to ground.	711	812	914	kHz
f_{sync}	Synchronization range		650		950	kHz
$V_{IL-sync}$	Synchronization logic zero amplitude	Relative to AGND			**0.4**	V
$V_{IH-sync}$	Synchronization logic one amplitude	Relative to AGND.	**1.5**			V
$Sync_{d.c.}$	Synchronization duty cycle range		15	50	85	%
D_{max}	Maximum Duty Factor			83		%

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V, Vout = 3.3V

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Regulation and Over-Voltage Comparator						
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8V I_O = 3A	**0.776**	0.796	**0.816**	V
V_{FB-OV}	Feedback over-voltage protection threshold			0.86		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non Switching Input Current	V_{FB}= 0.86V		2.6		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0V		70		µA
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis	Falling		15		°C
θ_{JA}	Junction to Ambient(3)	4 layer Evaluation Printed Circuit Board, 60 vias, No air flow		12.0		°C/W
		2 layer JEDEC Printed Circuit Board, No air flow		21.5		°C/W
θ_{JC}	Junction to Case	No air flow		1.9		°C/W
PERFORMANCE PARAMETERS(4)						
ΔV_O	Output voltage ripple	Cout = 220uF w/ 7 milliohm ESR + 100uF X7R + 2 x 0.047uF BW@ 20 MHz		9		mV $_{PP}$
$\Delta V_O/\Delta V_{IN}$	Line regulation	V_{IN} = 12V to 20V, I_O= .001A		±0.02		%
$\Delta V_O/\Delta I_{OUT}$	Load regulation	V_{IN} = 12V, I_O= 0.001A to 3A		1		mV/A
η	Peak efficiency	V_{IN} = 12V V_O = 3.3V I_O = 1A		86		%
η	Full load efficiency	V_{IN} = 12V V_O = 3.3V I_O = 3A		85		%

(3) Theta JA measured on a 3.5” x 3.5” four layer board, with three ounce copper on outer layers and two ounce copper on inner layers, sixty thermal vias, no air flow, and 1W power dissipation. Refer to application note layout diagrams.
(4) Refer to BOM in Table 1.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10µF + 1µF X7R Ceramic; C_O = 220µF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

Efficiency 6.0V Output @ 25°C Ambient

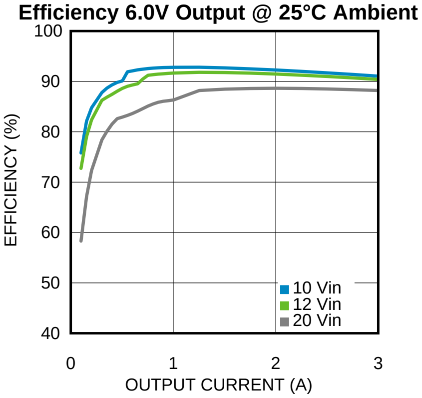


Figure 3.

Dissipation 6.0V Output @ 25°C Ambient

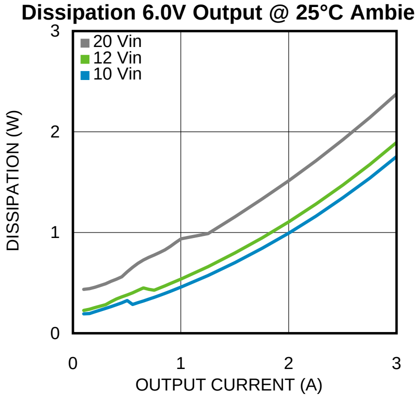


Figure 4.

Efficiency 5.0V Output @ 25°C Ambient

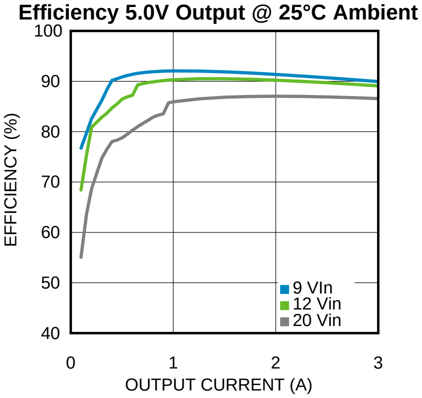


Figure 5.

Dissipation 5.0V Output @ 25°C Ambient

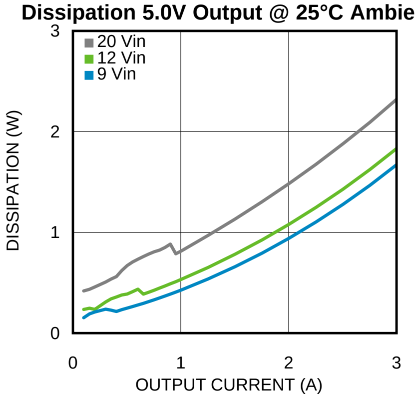


Figure 6.

Efficiency 3.3V Output @ 25°C Ambient

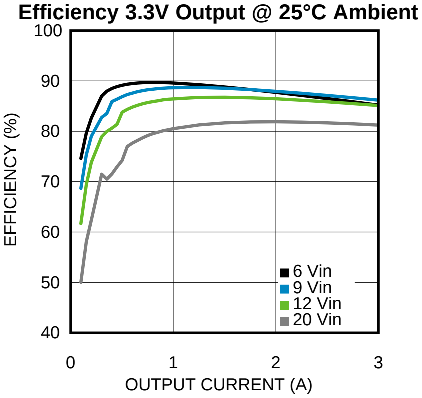


Figure 7.

Dissipation 3.3V Output @ 25°C Ambient

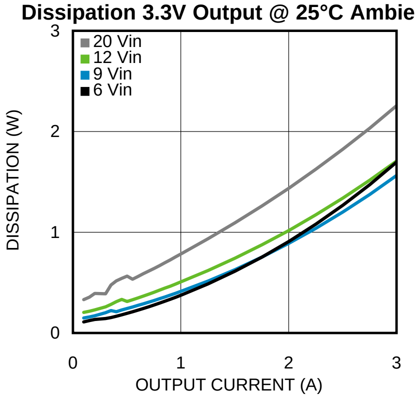


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10µF + 1µF X7R Ceramic; C_O = 220µF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

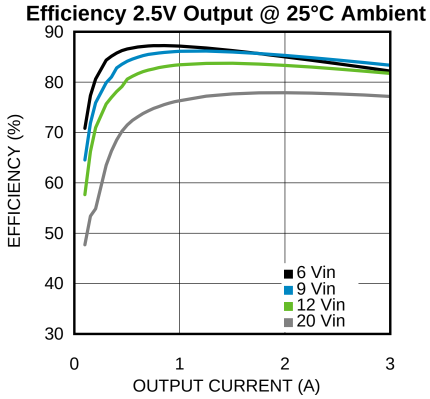

Efficiency 2.5V Output @ 25°C Ambient

Figure 9.

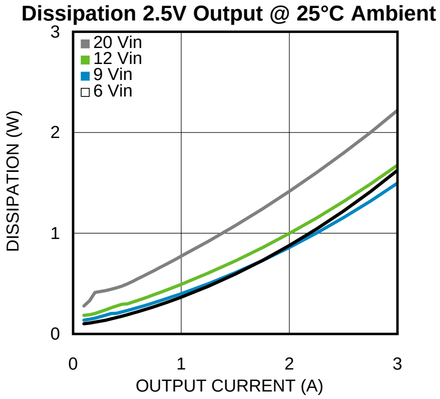

Dissipation 2.5V Output @ 25°C Ambient

Figure 10.

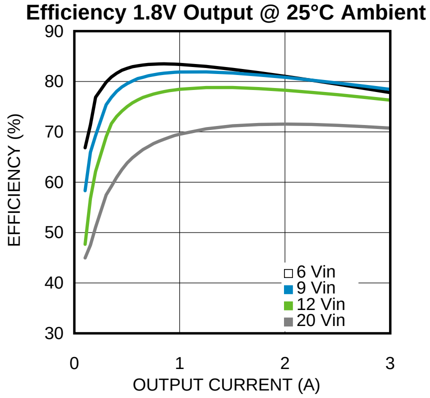

Efficiency 1.8V Output @ 25°C Ambient

Figure 11.

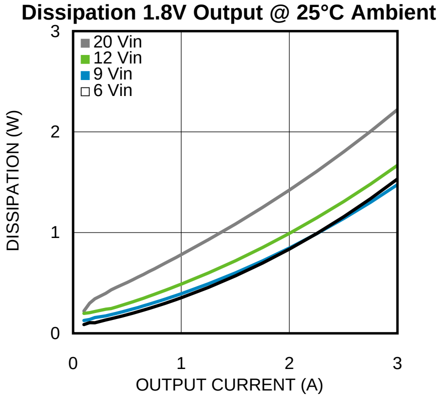

Dissipation 1.8V Output @ 25°C Ambient

Figure 12.

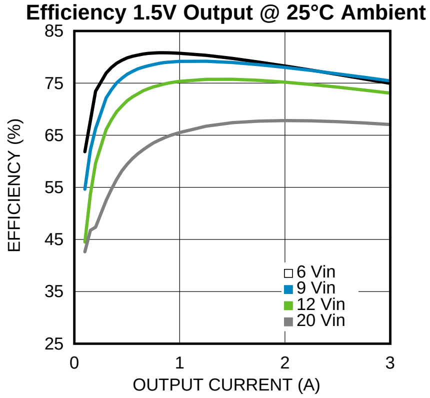

Efficiency 1.5V Output @ 25°C Ambient

Figure 13.

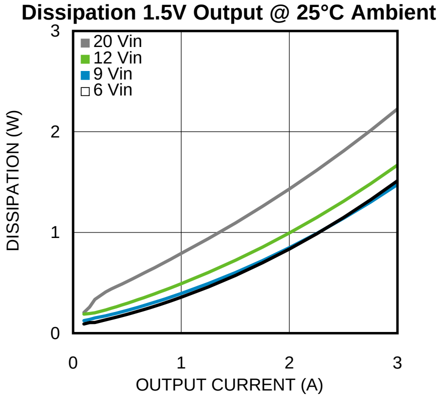

Dissipation 1.5V Output @ 25°C Ambient

Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10μF + 1μF X7R Ceramic; C_O = 220μF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

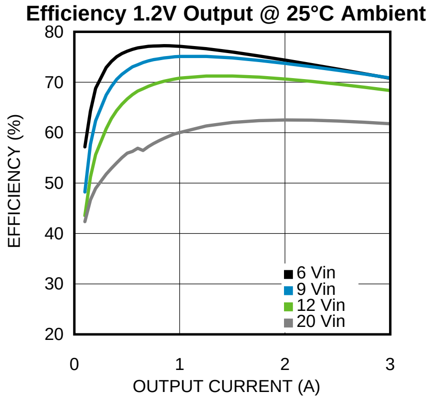


Figure 15.

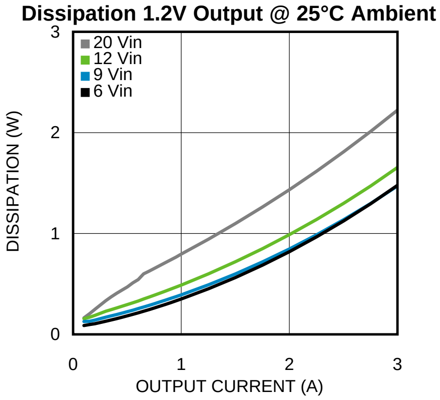


Figure 16.

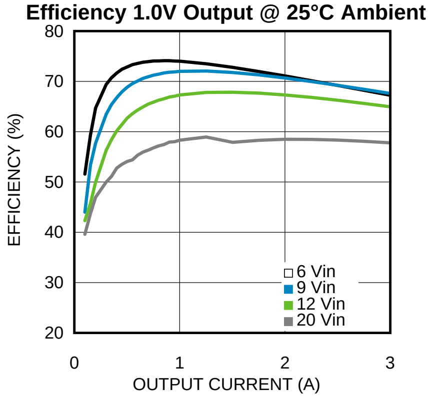


Figure 17.

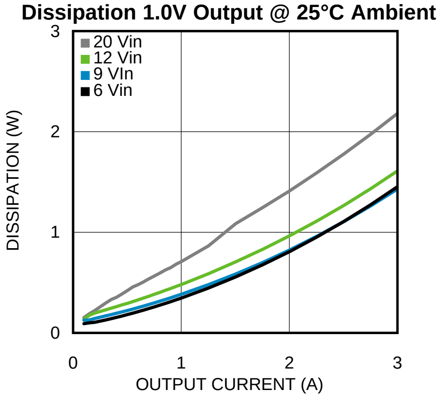


Figure 18.

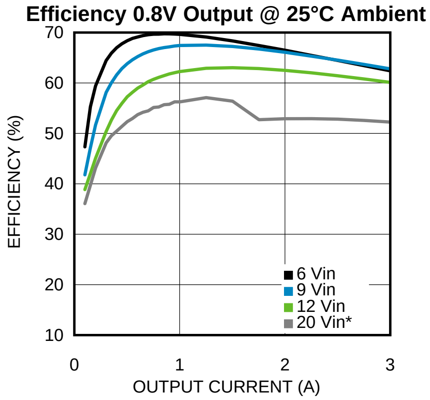


Figure 19.

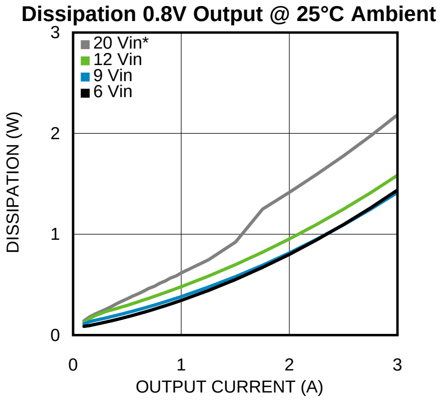


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10µF + 1µF X7R Ceramic; C_O = 220µF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

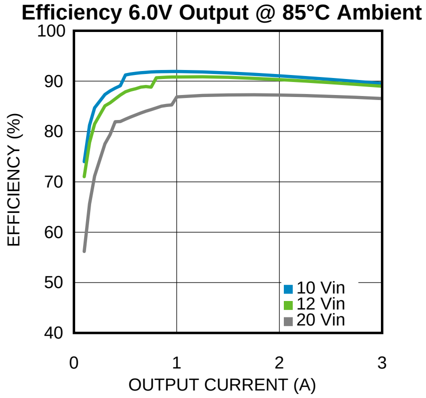


Figure 21.

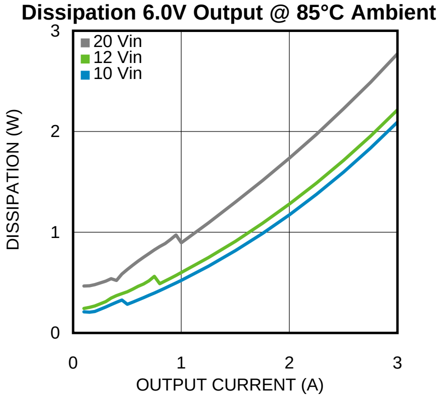
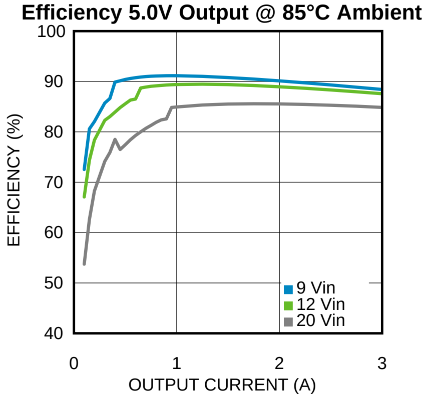


Figure 22.



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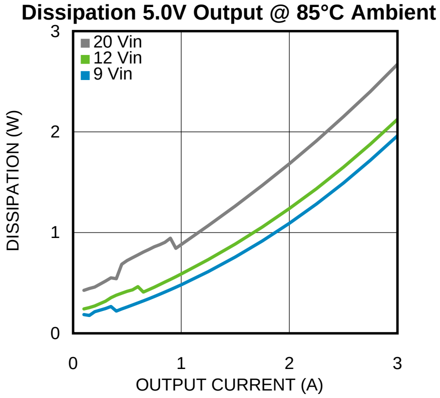

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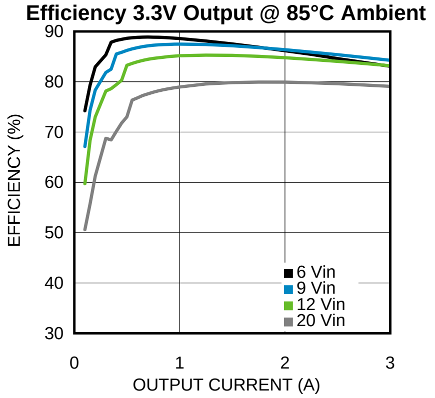


Figure 25.

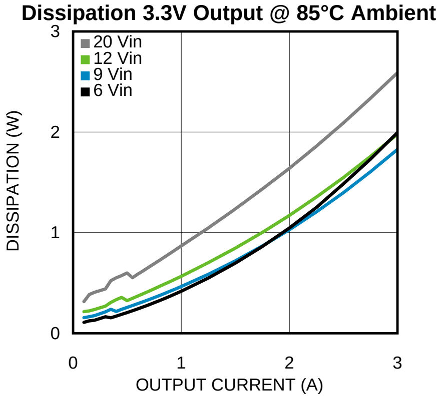


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10µF + 1µF X7R Ceramic; C_O = 220µF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

Efficiency 2.5V Output @ 85°C Ambient

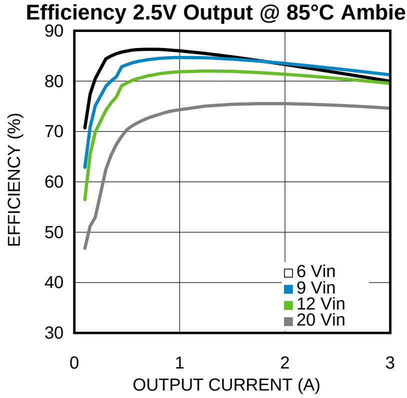


Figure 27.

Dissipation 2.5V Output @ 85°C Ambient

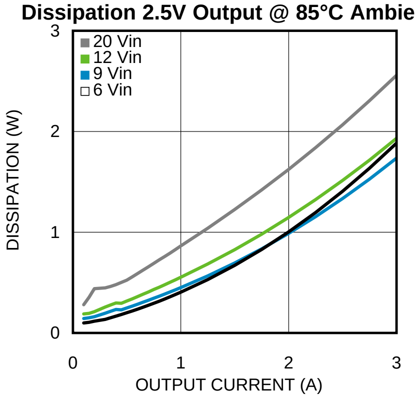


Figure 28.

Efficiency 1.8V Output @ 85°C Ambient

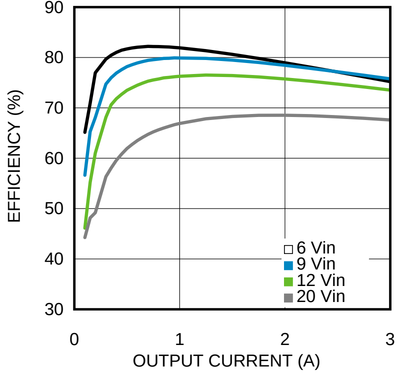


Figure 29.

Dissipation 1.8V Output @ 85°C Ambient

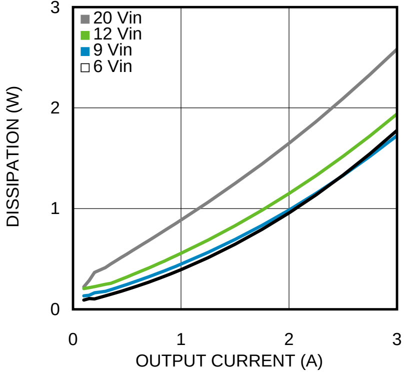


Figure 30.

Efficiency 1.5V Output @ 85°C Ambient

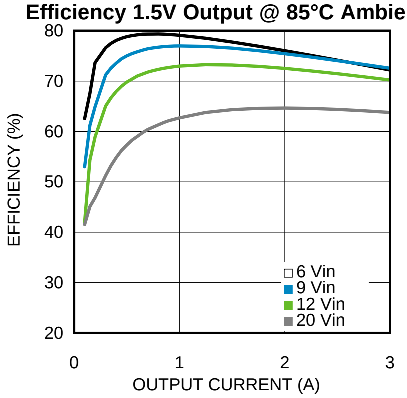


Figure 31.

Dissipation 1.5V Output @ 85°C Ambient

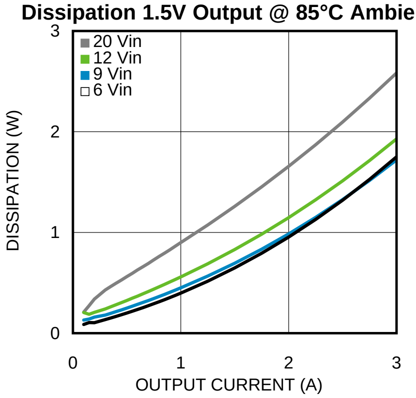


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10µF + 1µF X7R Ceramic; C_O = 220µF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

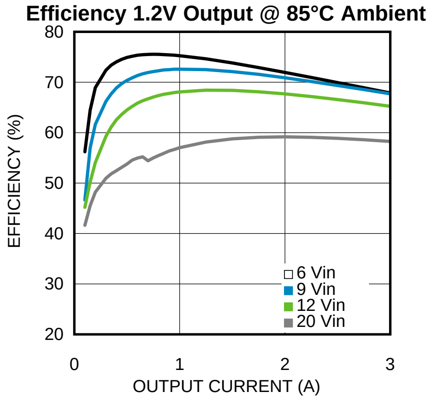

Efficiency 1.2V Output @ 85°C Ambient

Figure 33.

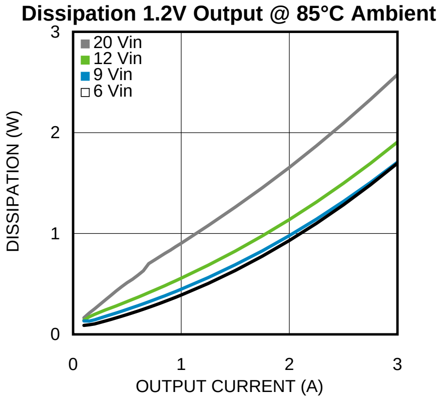

Dissipation 1.2V Output @ 85°C Ambient

Figure 34.

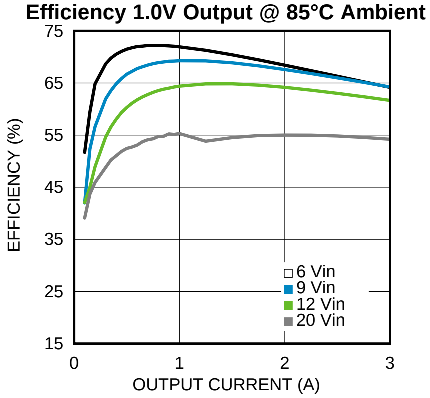

Efficiency 1.0V Output @ 85°C Ambient

Figure 35.

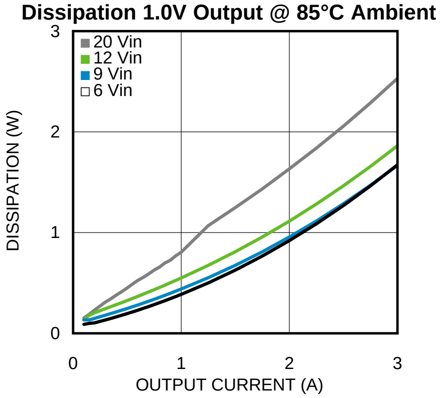

Dissipation 1.0V Output @ 85°C Ambient

Figure 36.

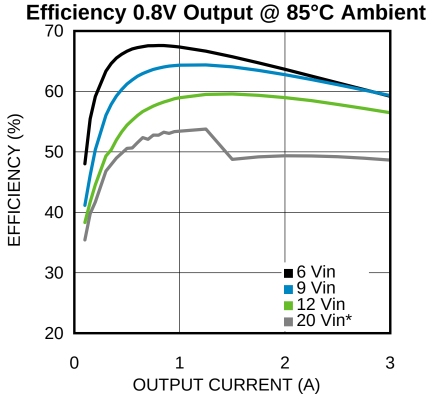

Efficiency 0.8V Output @ 85°C Ambient

Figure 37.

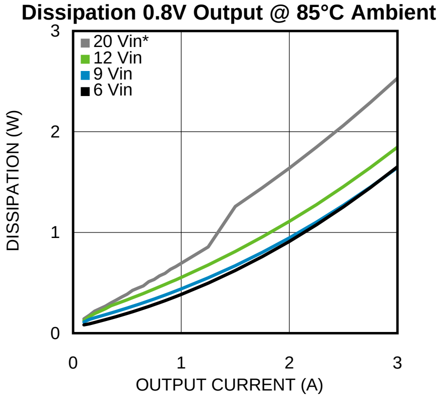

Dissipation 0.8V Output @ 85°C Ambient

Figure 38.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10µF + 1µF X7R Ceramic; C_O = 220µF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

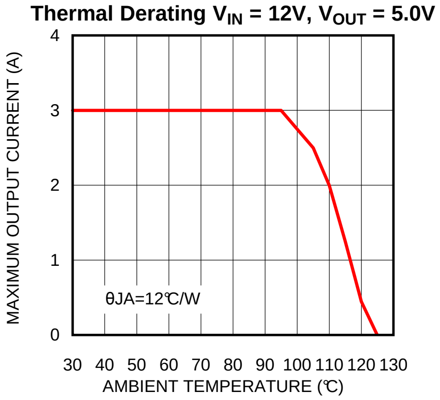

Thermal Derating V_{IN} = 12V, V_{OUT} = 5.0V

Figure 39.

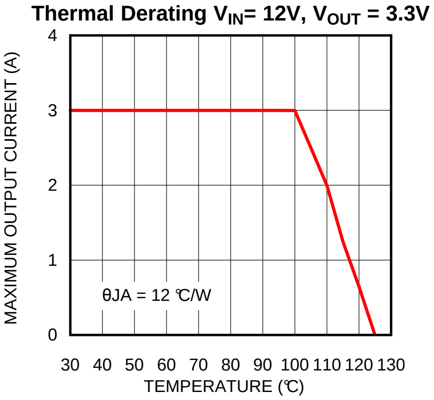

Thermal Derating V_{IN}= 12V, V_{OUT} = 3.3V

Figure 40.

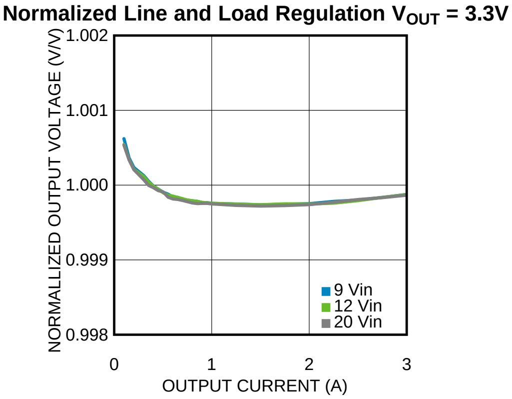

Normalized Line and Load Regulation V_{OUT} = 3.3V

Figure 41.

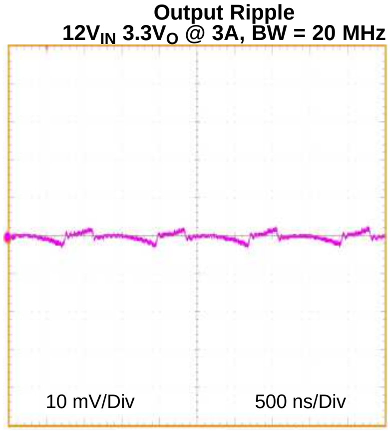

Output Ripple
$12V_{IN}$ $3.3V_O$ @ 3A, BW = 20 MHz

Figure 42.

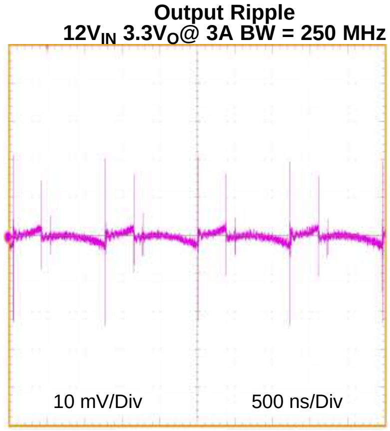

Output Ripple
$12V_{IN}$ $3.3V_O$@ 3A BW = 250 MHz

Figure 43.

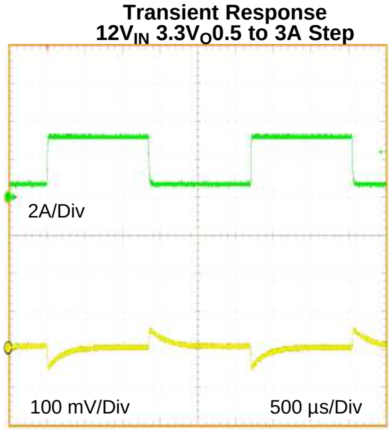

Transient Response
$12V_{IN}$ $3.3V_O$0.5 to 3A Step

Figure 44.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12V; Cin = 2 x 10µF + 1µF X7R Ceramic; C_O = 220µF Specialty Polymer + 10 uF Ceramic; TAmbient = 25° C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher Output ripple – See Design Steps for the LMZ22003 Application section.

Short Circuit Current vs Input Voltage

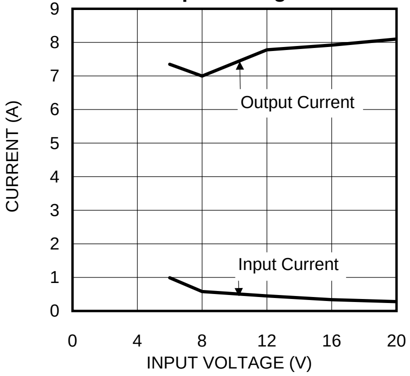
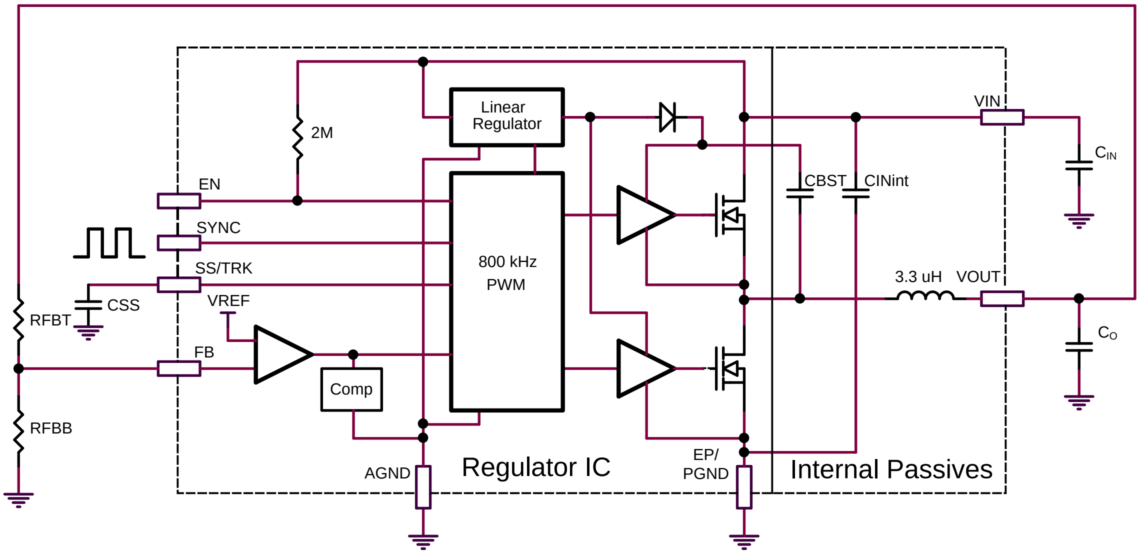


Figure 45.

BLOCK DIAGRAM



DESIGN STEPS FOR THE LMZ22003 APPLICATION

The LMZ22003 is fully supported by Webench® which offers: component selection, electrical and thermal simulations. Additionally there are both evaluation and demonstration boards that may be used as a starting point for design. The following list of steps can be used to manually design the LMZ22003 application.

All references to values refer to the typical applications schematic Figure 51.

- Select minimum operating V_{IN} with enable divider resistors
- Program V_O with resistor divider selection
- Select C_O
- Select C_{IN}
- Determine module power dissipation
- Layout PCB for required thermal performance

ENABLE DIVIDER, R_{ENT}, R_{ENB} AND R_{ENH}SELECTION

Internal to the module is a 2 mega ohm pull-up resistor connected from V_{IN} to Enable. For applications not requiring precision under voltage lock out (UVLO), the Enable input may be left open circuit and the internal resistor will always enable the module. In such case, the internal UVLO occurs typically at 4.3V (V_{IN}rising).

In applications with separate supervisory circuits Enable can be directly interfaced to a logic source. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ22003 output rail.

Enable provides a precise 1.279V threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. Additionally there is 21 µA(typ) of switched offset current allowing programmable hysteresis. See Figure 46.

The function of the enable divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable UVLO. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.279V) – 1 \quad (1)$$

The LMZ22003 typical application shows 12.7kΩ for R_{ENB} and 42.2kΩ for R_{ENT} resulting in a rising UVLO of 5.46V. Note that this divider presents 8.33V to the input when the divider is raised to 20V which would exceed the recommended 5.5V limit for Enable. A midpoint 5.1V Zener clamp is applied to allow the application to cover the full 6V to 20V range of operation. The zener clamp is not required if the target application prohibits the maximum Enable input voltage from being exceeded.

Additional enable voltage hysteresis can be added with the inclusion of R_{ENH}. It is possible to select values for R_{ENT} and R_{ENB} such that R_{ENH} is a value of zero allowing it to be omitted from the design.

Rising threshold can be calculated as follows:

$$V_{EN}(rising) = 1.279 (1 + (R_{ENT}|| 2 meg)/ R_{ENB})$$

Whereas the falling threshold level can be calculated using:

$$V_{EN}(falling) = V_{EN}(rising) – 21 µA (R_{ENT}|| 2 meg || R_{ENTB} + R_{ENH})$$

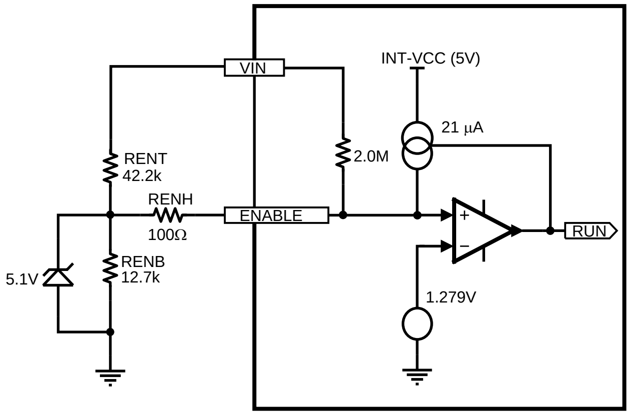


Figure 46. Enable Input Detail

OUTPUT VOLTAGE SELECTION

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.796V * (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.796V) - 1 \quad (3)$$

These resistors should generally be chosen from values in the range of 1.0 kΩ to 10.0 kΩ.

For V_O = 0.8V the FB pin can be connected to the output directly and R_{FBB} can be set to 8.06kΩ to provide minimum output load.

A table of values for R_{FBT} , and R_{FBB}, is included in the Simplified Applications Schematic.

SOFT-START CAPACITOR SELECTION

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time.

Upon turn-on, after all UVLO conditions have been passed, an internal 1.6mSec circuit slowly ramps the SS/TRK input to implement internal soft start. If 2 mSec is an adequate turn–on time then the Css capacitor can be left unpopulated. Longer soft-start periods are achieved by adding an external capacitor to this input.

Soft start duration is given by the formula:

$$t_{SS} = V_{REF} * C_{SS} / Iss = 0.796V * C_{SS} / 50uA \quad (4)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} * 50\mu A / 0.796V \quad (5)$$

Using a 0.22µF capacitor results in 3.5 msec typical soft-start duration; and 0.47µF results in 7.5 msec typical. 0.47 µF is a recommended initial value.

As the soft-start input exceeds 0.796V the output of the power stage will be in regulation and the 50 µA current is deactivated. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal current sink.

- The Enable input being pulled low
- Thermal shutdown condition
- Internal Vcc UVLO (Approx 4.3V input to V_{IN})

TRACKING SUPPLY DIVIDER OPTION

The tracking function allows the module to be connected as a slave supply to a primary voltage rail (often the 3.3V system rail) where the slave module output voltage is lower than that of the master. Proper configuration allows the slave rail to power up coincident with the master rail such that the voltage difference between the rails during ramp-up is small (i.e. <0.15V typ). The values for the tracking resistive divider should be selected such that the effect of the internal 50uA current source is minimized. In most cases the ratio of the tracking divider resistors is the same as the ratio of the output voltage setting divider. Proper operation in tracking mode dictates the soft-start time of the slave rail be shorter than the master rail; a condition that is easy satisfy since the C_{SS} cap is replaced by R_{TKB}. The tracking function is only supported for the power up interval of the master supply; once the SS/TRK rises past 0.8V the input is no longer enabled and the 50 uA internal current source is switched off.

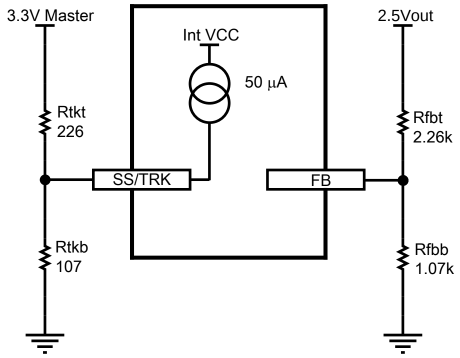


Figure 47. Tracking Option Input Detail

C_O SELECTION

None of the required C_O output capacitance is contained within the module. A minimum value of 200 μF is required based on the values of internal compensation in the error amplifier. Low ESR tantalum, organic semiconductor or specialty polymer capacitor types are recommended for obtaining lowest ripple. The output capacitor C_O may consist of several capacitors in parallel placed in close proximity to the module. The output capacitor assembly must also meet the worst case minimum ripple current rating of 0.5 * $I_{LR\ P\text{-}P}$, as calculated in Equation 14 below. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. Loop response verification is also valuable to confirm closed loop behavior.

For applications with dynamic load steps; the following equation provides a good first pass approximation of C_O for load transient requirements. Where $V_{O\text{-}Tran}$ is 100 mV on a 3.3V output design.

$$C_O \geq I_{O\text{-}Tran}/((*V_{O\text{-}Tran} - ESR * I_{O\text{-}Tran}) * (F*_{SW}/V_O)) \tag{6}$$

Solving:

$$C_O \geq 2.5A / ((0.1V - .007*2.5A) * (800000\ Hz/ 3.3V) \geq 125\mu F \tag{7}$$

Note that the stability requirement for 200 µF minimum output capacitance will take precedence.

One recommended output capacitor combination is a 220uF, 7 milliohm ESR specialty polymer cap in parallel with a 100 uF 6.3V X5R ceramic. This combination provides excellent performance that may exceed the requirements of certain applications. Additionally some small ceramic capacitors can be used for high frequency EMI suppression.

C_{IN} SELECTION

The LMZ22003 module contains a small amount of internal ceramic input capacitance. Additional input capacitance is required external to the module to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. This input capacitance should be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I(C_{IN(RMS)}) \cong 1/2 * I_O * SQRT(D / 1\text{-}D) \tag{8}$$

where $D \cong V_O / V_{IN}$

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 * V_O$).

Recommended minimum input capacitance is 22uF X7R (or X5R) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature derating of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this parameter.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) be maintained then the following equation may be used.

$$C_{IN} \geq I_O * D * (1–D) / f_{SW\text{-}CCM} * \Delta V_{IN} \quad (9)$$

If ΔV_{IN} is 1% of V_{IN} for a 12V input to 3.3V output application this equals 120 mV and f_{SW} = 812 kHz.

$C_{IN} \geq$ 3A * 3.3V/12V * (1– 3.3V/12V) / (812000 * 0.120 V)

≥ 6.14µF

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines. The LMZ22003 typical applications schematic and evaluation board include a 150 µF 50V aluminum capacitor for this function. There are many situations where this capacitor is not necessary.

POWER DISSIPATION AND BOARD THERMAL REQUIREMENTS

When calculating module dissipation use the maximum input voltage and the average output current for the application. Many common operating conditions are provided in the characteristic curves such that less common applications can be derived through interpolation. In all designs, the junction temperature must be kept below the rated maximum of 125°C.

For the design case of V_{IN} = 12V, V_O = 3.3V, I_O = 3A, and $T_{AMB(MAX)}$ = 85°C, the module must see a thermal resistance from case to ambient of less than:

$$\theta_{CA} < (T_{J\text{-}MAX} – T_{A\text{-}MAX}) / P_{IC\text{-}LOSS} - \theta_{JC} \quad (10)$$

Given the typical thermal resistance from junction to case to be 1.9 °C/W. Use the 85°C power dissipation curves in the Typical Performance Characteristics section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 2W.

$$\theta_{CA} = (125 – 85) / 2W – 1.9 = 18.1 \quad (11)$$

To reach θ_{CA} = 18.1, the PCB is required to dissipate heat effectively. With no airflow and no external heat-sink, a good estimate of the required board area covered by 2 oz. copper on both the top and bottom metal layers is:

$$\text{Board\_Area\_cm}^2 = 500°C \times cm^2/W / \theta_{CA} \quad (12)$$

As a result, approximately 28 square cm of 2 oz copper on top and bottom layers is required for the PCB design. The PCB copper heat sink must be connected to the exposed pad. Approximately sixty, 8mil thermal vias spaced 39 mils (1.0 mm) apart connect the top copper to the bottom copper. For an example of a high thermal performance PCB layout for SIMPLE SWITCHER© power modules, refer to AN-2085, AN-2125, AN-2020 and AN-2026.

PC BOARD LAYOUT GUIDELINES

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules. A good example layout is shown in Figure 52.

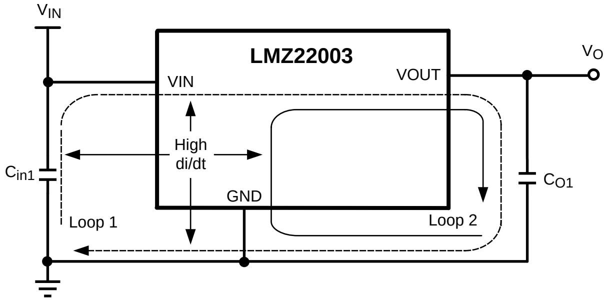


Figure 48. PC Board Layout

1. Minimize area of switched current loops.

From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout as shown in Figure 48. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ22003. Therefore place C_{IN1} as close as possible to the LMZ22003 VIN and PGND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad (EP).

2. Have a single point ground.

The ground connections for the feedback, soft-start, and enable components should be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Additionally provide the single point ground connection from pin 4 (AGND) to EP/PGND.

3. Minimize trace length to the FB pin.

Both feedback resistors, R_{FBT} and R_{FBB} should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB} should be routed away from the body of the LMZ22003 to minimize possible noise pickup.

4. Make input and output bus connections as wide as possible.

This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 10 via array with minimum via diameter of 8mils thermal vias spaced 39mils (1.0 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

Additional Features

SYNCHRONIZATION INPUT

The PWM switching frequency can be synchronized to an external frequency source. If this feature is not used, connect this input either directly to ground, or connect to ground through a resistor of 1.5 kΩ ohm or less. The allowed synchronization frequency range is 650kHz to 950 kHz. The typical input threshold is 1.4V transition level. Ideally the input clock should overdrive the threshold by a factor of 2, so direct drive from 3.3V logic via a 1.5kΩ Thevenin source resistance is recommended. Note that applying a sustained “logic 1” corresponds to zero Hz PWM frequency and will cause the module to stop switching.

OUTPUT OVER-VOLTAGE PROTECTION

If the voltage at FB is greater than a 0.86V internal reference, the output of the error amplifier is pulled toward ground, causing V_O to fall.

CURRENT LIMIT

The LMZ22003 is protected by both low side (LS) and high side (HS) current limit circuitry. The LS current limit detection is carried out during the off-time by monitoring the current through the LS synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds the low side current limit value, the current limit comparator disables the start of the next switching period. Switching cycles are prohibited until current drops below the limit. It should also be noted that d.c. current limit is dependent on both duty cycle as illustrated in the graph in the typical performance section. The HS current limit monitors the current of top side MOSFET. Once HS current limit is detected, the HS MOSFET is shutoff immediately, until the next cycle. Exceeding HS current limit causes V_O to fall. Typical behavior of exceeding LS current limit is that f_{SW} drops to 1/2 of the operating frequency.

THERMAL PROTECTION

The junction temperature of the LMZ22003 should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 150 °C (typ Hyst = 15°C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures.

PRE-BIASED STARTUP

The LMZ22003 will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The following scope capture shows proper behavior in this mode. Trace one is Enable going high. Trace two is 1.5V pre-bias rising to 3.3V. Rise-time determined by C_{SS}, trace three.

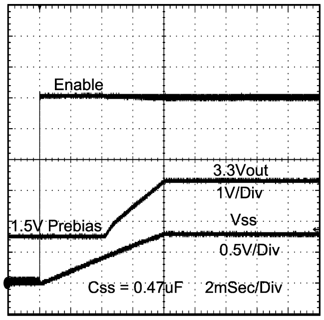


Figure 49. Pre-Biased Startup

DISCONTINUOUS CONDUCTION AND CONTINUOUS CONDUCTION MODES

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time. When operating in DCM, inductor current is maintained to an average value equaling Iout. Inductor current exhibits normal behavior for the emulated current mode control method used. Output voltage ripple typically increases during this mode of operation.

Following is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.

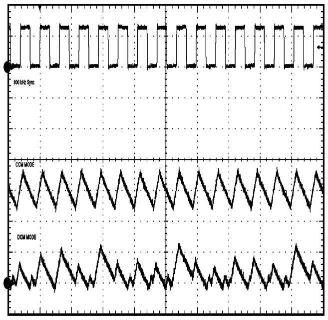


Figure 50. CCM and DCM Operating Modes
V_{IN} = 12V, V_O = 3.3V, I_O = 3A/0.3A 2 µsec/div

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O*(V_{IN}–V_O)/(2*3.3\ \mu H*f_{SW(CCM)}*V_{IN}) \tag{13}$$

The inductor internal to the module is 3.3 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P}=V_O*(V_{IN}\text{- } V_O)/(3.3\mu H*f_{SW}*V_{IN}) \tag{14}$$

Where V_{IN} is the maximum input voltage and f_{SW} is typically 812 kHz.

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined.

Typical Application Schematic Diagram

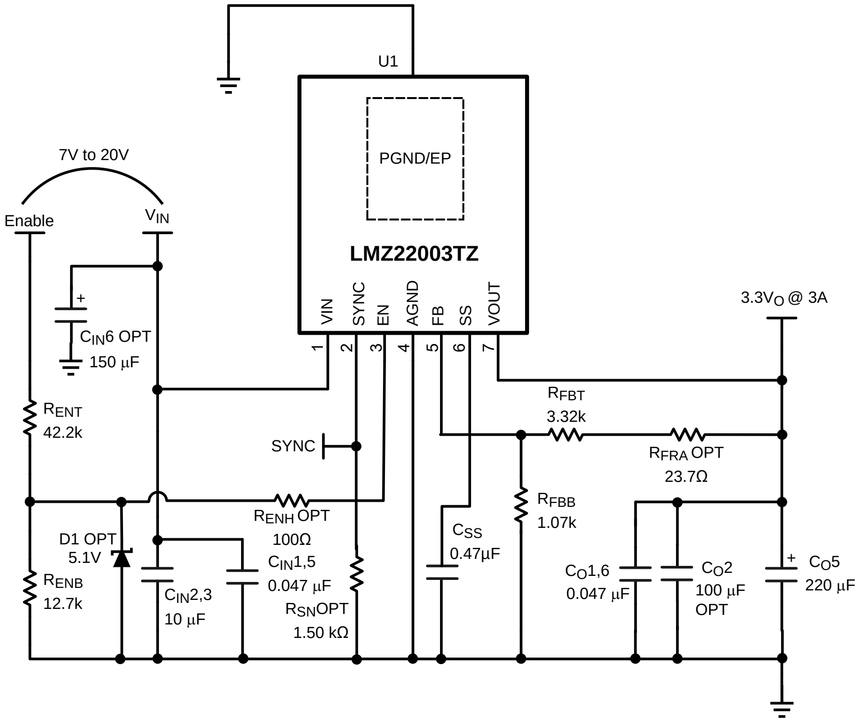


Figure 51. Typical Application Schematic

Table 1. Typical Application Bill of Materials

Ref Des	Description	Case Size	Manufacturer	Manufacturer P/N
U1	SIMPLE SWITCHER ®	PFM-7	Texas Instruments	LMZ22003TZ
C_{in}1,5	0.047 µF, 50V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_{in}2,3	10 µF, 50V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{in}6 (OPT)	CAP, AL, 150µF, 50V	Radial G	Panasonic	EEE-FK1H151P
C_O1,6	0.047 µF, 50V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_O2 (OPT)	100 µF, 6.3V, X7R	1210	TDK	C3225X5R0J107M
C_O5	220 µF, 6.3V, SP-Cap	(7343)	Panasonic	EEF-UE0J221LR
R_{FBT}	3.32 kΩ	0805	Panasonic	ERJ-6ENF3321V
R_{FBB}	1.07 kΩ	0805	Panasonic	ERJ-6ENF1071V
R_{SN}(OPT)	1.50 kΩ	0805	Vishay Dale	CRCW08051K50FKEA
R_{ENT}	42.2 kΩ	0805	Panasonic	ERJ-6ENF4222V
R_{ENB}	12.7 kΩ	0805	Panasonic	ERJ-6ENF1272V
R_{FRA}(OPT)	23.7Ω	0805	Vishay Dale	CRCW080523R7FKEA
R_{ENH}	100 Ω	0805	Vishay Dale	CRCW0805100RFKEA
C_{SS}	0.47 µF, ±10%, X7R, 16V	0805	AVX	0805YC474KAT2A
D1(OPT)	5.1V, 0.5W	SOD-123	Diodes Inc.	MMSZ5231BS-7-F

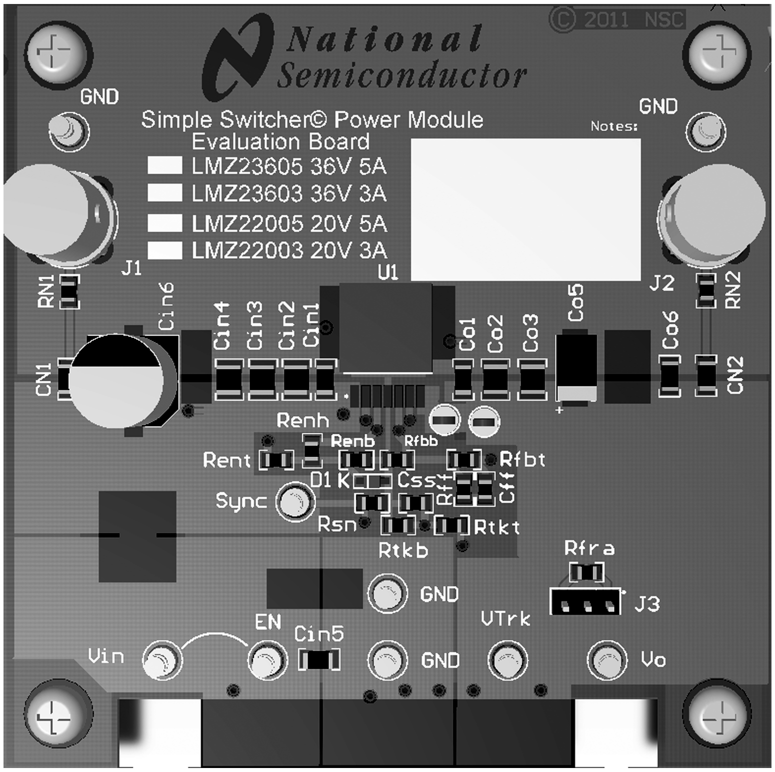


Figure 52. Top View Evaluation Board – See AN–2085

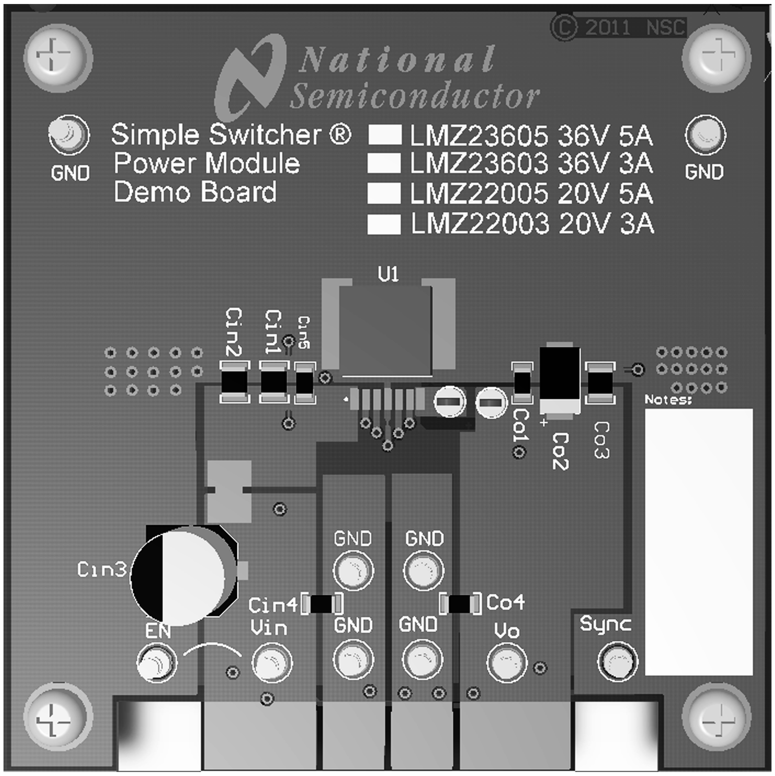


Figure 53. Top View Demonstration Board – See AN–2125 SNVA473

Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness – 0.125 to 0.15mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Maximum number of reflows allowed is one

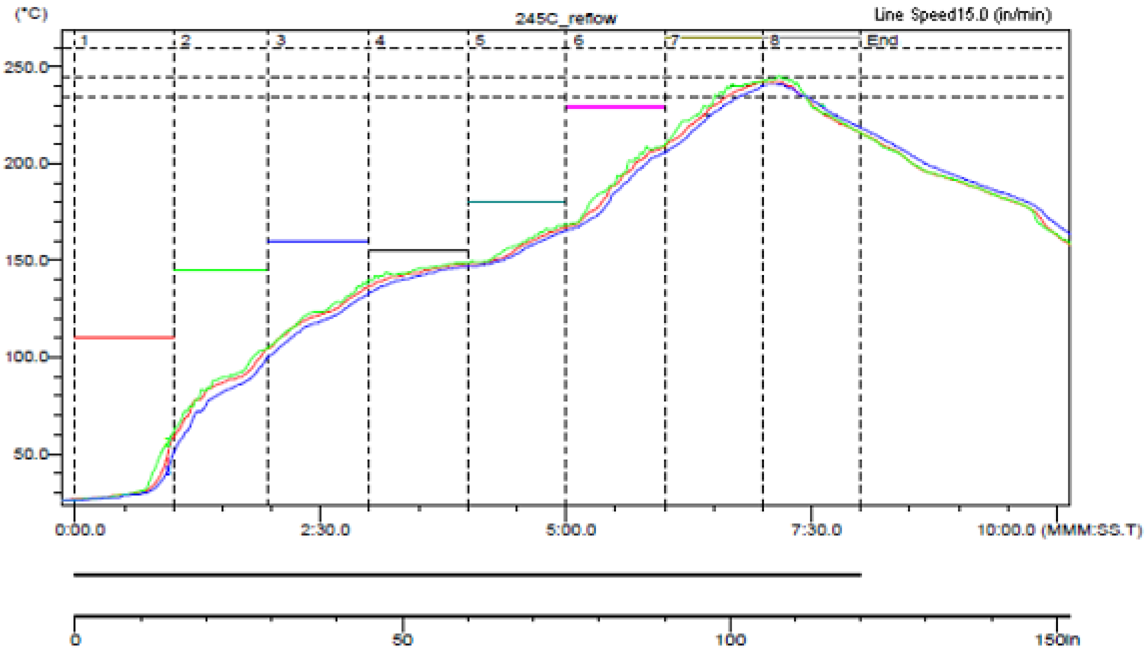


Figure 54. Sample Reflow Profile

Table 2.

Probe	Max Temp (°C)	Reached Max Temp	Time Above 235°C	Reached 235°C	Time Above 245°C	Reached 245°C	Time Above 260°C	Reached 260°C
#1	242.5	6.58	0.49	6.39	0.00	–	0.00	–
#2	242.5	7.10	0.55	6.31	0.00	7.10	0.00	–
#3	241.0	7.09	0.42	6.44	0.00	–	0.00	–

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
• Added Peak Reflow Case Temp = 245°C	1
• Deleted 10mil	1
• Deleted 10mil	5
• Changed 10mil	18
• Changed 10mils	19
• Added Power Module SMT Guidelines	23

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ22003TZ/NOPB	ACTIVE	TO-PMOD	NDW	7	45	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	LMZ22003	Samples
LMZ22003TZE/NOPB	ACTIVE	TO-PMOD	NDW	7	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	LMZ22003	Samples
LMZ22003TZX/NOPB	ACTIVE	TO-PMOD	NDW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	LMZ22003	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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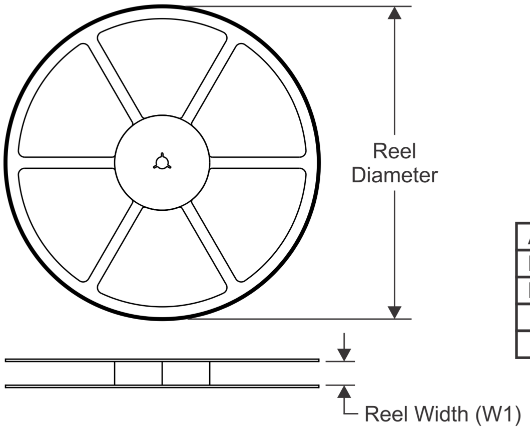
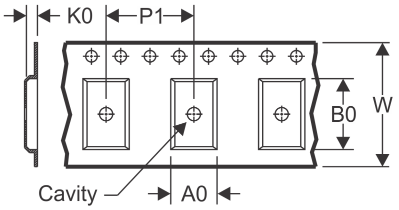
TAPE AND REEL INFORMATION

REEL DIMENSIONS

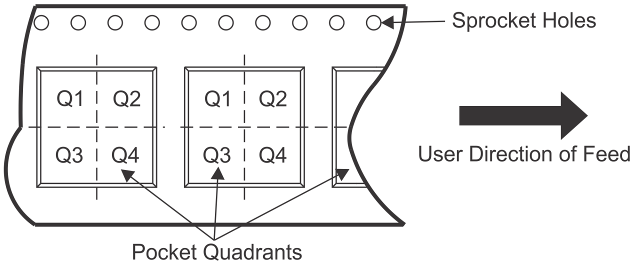


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

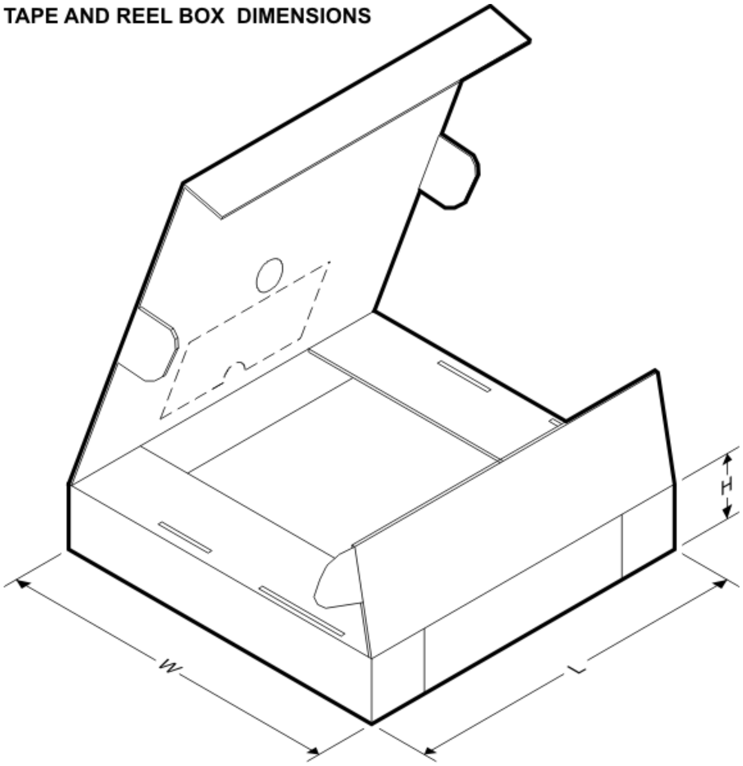
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ22003TZE/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ22003TZX/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

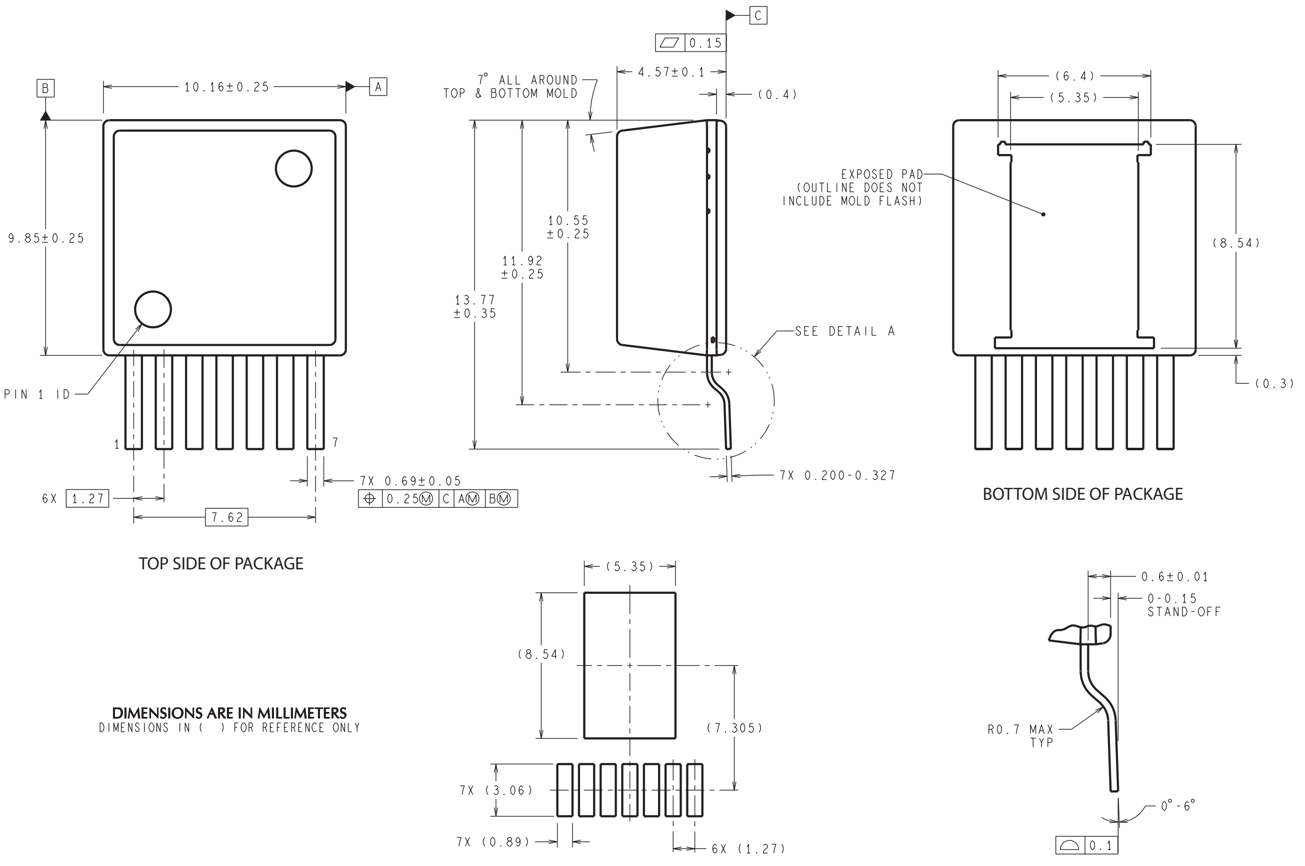
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ22003TZE/NOPB	TO-PMOD	NDW	7	250	367.0	367.0	45.0
LMZ22003TZX/NOPB	TO-PMOD	NDW	7	500	367.0	367.0	45.0

NDW0007A



TOP SIDE OF PACKAGE

BOTTOM SIDE OF PACKAGE

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN

DETAIL A

TZA07A (Rev D)

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