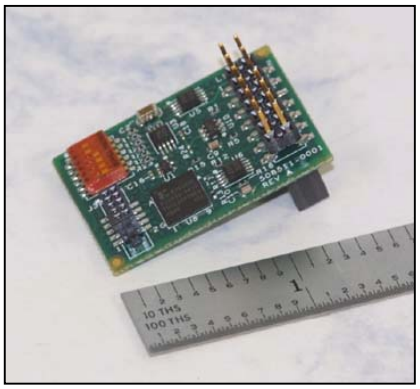
Low Voltage Adapter with Adaptive Clocking for JTAG Emulators

Quick Start Installation Guide

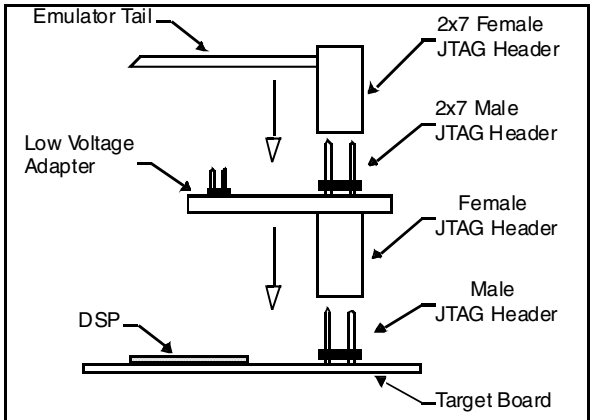


The Spectrum Digital Low Voltage Adapter with Adaptive Clocking provides the following:

- Voltage translation between 3.3-volt emulator interfaces and JTAG targets that require down to 1.8-volt interfaces
- Adaptive clocking for TI ARM based processors

The adapter is designed primarily to support the XDS510USB emulator but may be used with most any emulator that supports the standard TI 14-pin JTAG header.

To get started simply plug the Low Voltage adapter into your emulator's 14-pin cable connector. Then plug the other end into your target. Both the male header and female connector on the Low Voltage adapter are keyed to prevent incorrect insertion. The diagram below shows a side view of the connection to the board.



Connecting the Emulator to the LV Adapter and DSP Target Board

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1.1 SWITCH SW1

Switch SW1 allows the user to select the various Adaptive Clocking modes required for the specific processor they have in the circuit. The signals associated with each switch position are shown in the table below. When a switch is in the ON position then it is low, when it is in the OFF position then it is high. Default mode is all switches OFF.

Switch SW1	
Position	**Signal**
1	TCK MODE-0
2	TCK MODE-1
3	CNT0
4	CNT1
5	CNT2
6	ISSPROG

1.1.1 TCK MODE-01 (Switch 1, Positions 1,2)

The TCK mode switches (positions 1 and 2) determine how TCK and RTCK are generated. The four combinations of the switch positions are shown in the table below.

SW1-1	SW1-2	Mode
OFF	OFF	SD Default: Adaptive clocking with clock delay.
OFF	ON	SD OMAP: Adaptive clocking no clock delay, optimal OMAP.
ON	OFF	TI XDS560: Adaptive clocking no clock delay.
ON	ON	BYPASS: No adaptive clocking adapter.

1.1.1.1 SD Default

When SW1-1 and SW1-2 are both in the off position then the value of CNT0-2 determines the number of high-speed sync clock delays between RTCK and the next TCK edge inverted. The default high-speed sync clock is 71.59MHz which provides a 13.96 ns. delay per count. This allows the user to set a minimum amount of RTCK to TCK delay when required. When an emulator cable is not plugged in, the adapter will be in low power mode.

1.1.1.2 SD OMAP

When SW1-1 is OFF, and SW1-2 is ON then the adapter is configured for optimal OMAP mode. This mode has been predefined based on operation of processors in the TI OMAP15xx, OMAP16xx, OMAP17xx, OMAP59xx, and OMAP242x families. In this mode there is one high-speed sync clock delay between RTCK and the next TCK edge inverted. When an emulator cable is not plugged in the adapter will be in low power mode.

1.1.1.3 TI XDS560

When SW1-1 is ON, and SW1-2 is OFF then the adapter is configured for TI XDS560 mode. This mode is same as “SD OMAP” mode except that emulator cable detection and low power mode are disabled. The XDS560 emulator does target cable detection on the same JTAG header pin as the adapter which creates a conflict. If an XDS560 is connected and not in the TI XDS560 mode then CCS will report that there is a cable break at the far end.

1.1.1.4 BYPASS

When SW1-1 is ON, and SW1-2 is ON then the adapter is configured for BYPASS mode. In BYPASS mode the adapter simply becomes a low voltage adapter with no adaptive clocking support.

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1.1.2 CNT0-CNT2 (Switch 1, Positions 3,4,5)

The delay count switches (positions 3, 4, 5) determine the amount of delay between RTCK and the next TCK edge inverted. The delay time may be defined as (CNT + 2) * 13.96 ns. The table below shows the switch settings and the delays.

SW1-3	SW1-4	SW1-5	Delay Counts	Delay Time (ns)
ON	ON	ON	0	27.92
OFF	ON	ON	1	41.88
ON	OFF	ON	2	55.84
OFF	OFF	ON	3	69.80
ON	ON	OFF	4	83.76
OFF	ON	OFF	5	97.72
ON	OFF	OFF	6	111.68
OFF	OFF	OFF	7	125.64

1.1.3 ISSPROG (Switch 1, Position 6)

Switch 1, position 6, enables and disables the programming of the CPLD. When set to the ON position the on-board CLPD can be programmed. When set to the OFF position the on-board CPLD programming is disabled.

1.2 ADAPTER POWER

The adapter requires between 1.8v and 3.6v on pin 5 of the target side JTAG header, the PD pin. An on-board buck-boost regulator will generate 3.3v to drive the adapter logic. The I/O voltage levels between the target and the adapter track the target I/O voltage as defined on pin 5 (PD) of the target JTAG header. The typical adapter power requirements are 48mA at 1.8v and 25mA at 3.3v. When adapter is in low power mode the power consumption will drop 25%-50% depending on the mode. The power consumption mode of the adapter from lowest to highest is BYPASS, SD OMAP, TI XDS560, SD Default.

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1.3 JTAG HEADER PINOUTS

The two figures below show the pin outs of the 14 and 20 pin female connectors on the adapter.

TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD	5	6	**no pin (key)**	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

14 Pin Header Signals and Dimensions

TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD	5	6	**no pin (key)**	Pin-to-Pin spacing, 0.100 in. (X)
TDO	7	8	GND	Pin-to-Pin spacing, 0.050 in. (Y)
TCK-RET	9	10	GND	Female connector on adapter:
TCK	11	12	GND	SAMTEC: RSM-110-02-S-D
EMU0	13	14	EMU1	
NC	15	16	GND	
NC	17	18	NC	
NC	19	20	GND	

20 Pin Header Signals and Dimensions

1.4 ORDERING INFORMATION

Part Number	Description
701210-0001	Low Voltage Adapter with Adaptive Clocking, 14 pin-14 pin
701212-0001	Low Voltage Adapter with Adaptive Clocking, 14 pin-CTI-20 pin

Call today for pricing and delivery information:

SPECTRUM DIGITAL, INC.

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